

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
6 March 2003 (06.03.2003)

PCT

(10) International Publication Number
WO 03/01994 A1

(51) International Patent Classification⁷: H05B 41/392,
G01R 19/02

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(21) International Application Number: PCT/IB02/02965

(22) International Filing Date: 12 July 2002 (12.07.2002)

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(25) Filing Language: English

(26) Publication Language: English

(81) Designated States (national): CN, JP.

(30) Priority Data:
01203231.4 27 August 2001 (27.08.2001) EP

(84) Designated States (regional): European patent (AT, BE,
BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, IE, IT,
LU, MC, NL, PT, SE, SK, TR).

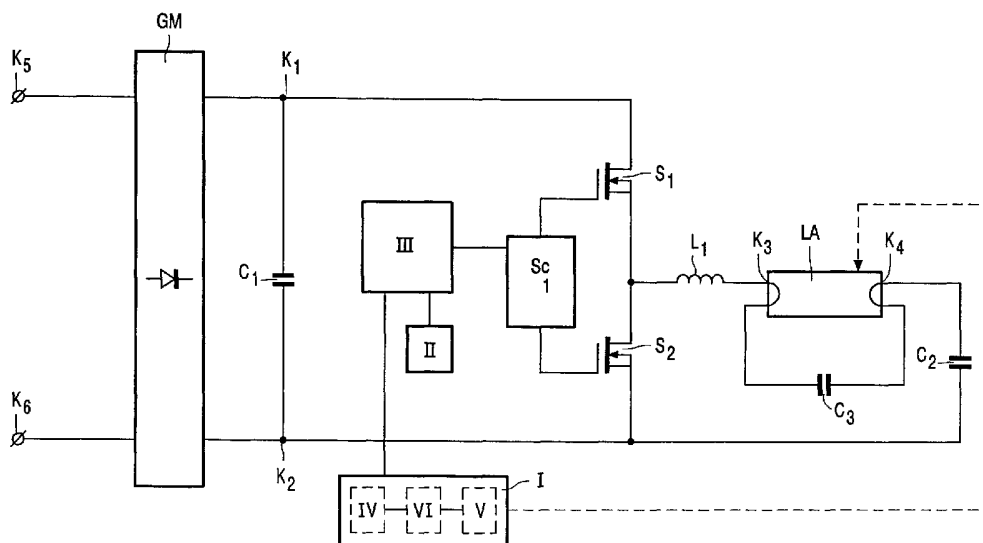
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Published:
— with international search report

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For two-letter codes and other abbreviations, refer to the "Guid-
ance Notes on Codes and Abbreviations" appearing at the begin-
ning of each regular issue of the PCT Gazette.

(54) Title: CIRCUIT ARRANGEMENT



(57) Abstract: An electronic ballast for supplying a lamp comprises a control loop for controlling the rms value of an operational parameter so as to be constant. In the control loop, the actual rms value of the parameter is generated as a linear combination of its average value and its peak value.

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Circuit arrangement

The invention relates to a circuit arrangement for feeding a load, which is equipped with

- input terminals which are to be connected to a supply voltage source,
- a power converter for generating a current through the load from a supply voltage
5 supplied by the supply voltage source,
- a control circuit for controlling the rms value of an operating parameter, comprising
- a first circuit for generating a first signal that is a measure of the actual rms value of the operating parameter,
- 10 – a second circuit for generating a second signal that is a measure of the desired rms value of the operating parameter,
- a third circuit that is coupled to the first and the second circuit for generating a third signal that is dependent on the first and the second signal, and for
influencing the operating state of the circuit arrangement in dependence on the
15 third signal.

Such a circuit arrangement is known. The first signal is frequently generated by successively rectifying and averaging the signal that represents the operating parameter.
20 As regards sinusoidal signals, it applies that $V_{rms} = 1.111 * V_{avg}$, where V_{rms} is the rms value of the signal and V_{avg} is the average value, so that said operation yields a reliable rms value for sinusoidal signals. However, if said operation is applied to a signal that deviates substantially from a sine-shaped signal, the result of the operation may also deviate substantially from the actual rms value of the signal. To determine the rms value of such a
25 non-sinusoidal signal use can be made of a "true rms sensor". Such a "true rms sensor" however is a complicated circuit comprising many (active) components, as a result of which said circuit is also comparatively expensive.

It is an object of the invention to provide a circuit arrangement wherein the rms value of an operating parameter can be determined by means of comparatively simple means and regulated so as to obtain a desired level.

To achieve this, a circuit arrangement as mentioned in the opening paragraph is characterized in accordance with the invention in that the first circuit is equipped with

- a fourth circuit for generating a fourth signal that is a measure of the actual average value of the operating parameter,
- a fifth circuit for generating a fifth signal that is a measure of the actual maximum amplitude of the operating parameter,
- a sixth circuit for generating a signal that is a linear combination of the third signal and the fourth signal.

It has been found that the rms value generated by the first circuit of a circuit arrangement in accordance with the invention is substantially equal to the actual rms value of the operating parameter, even if the form of the operating parameter as a function of time deviates substantially from the sine shape. By virtue thereof, also the rms value of the operating parameter is accurately regulated so as to obtain the desired value. The fourth circuit and the fifth circuit can be obtained using comparatively simple electronics, so that these circuits are also comparatively inexpensive. The same applies to the sixth circuit.

Good results were achieved using embodiments of a circuit arrangement in accordance with the invention wherein the load is a lamp, and the operating parameter is selected among the group consisting of the lamp current, the lamp voltage and the power consumed by the lamp.

Good results were also achieved using embodiments of a circuit arrangement in accordance with the invention wherein the sixth circuit generates a signal of the general formula

$$A * OP_{avg} + B * OP_{max},$$

wherein OP_{avg} and OP_{max} are the value of the fourth signal and the value of the fifth signal, respectively, and wherein

$$0 < A < 1 \quad \text{and} \quad 0 < B < 1.$$

More particularly, good results were achieved for embodiments wherein

$$0.76 < A < 0.93 \quad \text{and} \quad 0.12 < B < 0.19.$$

These and other aspects of the invention are apparent from and will be elucidated with reference to the embodiment(s) described hereinafter.

In the drawings:

Fig. 1 shows an example of a circuit arrangement in accordance with the invention to which a lamp is connected, and

5 Fig. 2 shows different embodiments of a part of the circuit arrangement shown in Fig. 1.

In Fig. 1, K5 and K6 are input terminals that are to be connected to the poles
10 of a supply voltage source. Input terminals K5 and K6 are connected to respective inputs of the circuit part GM that forms a rectifier in the form of a diode bridge. A first output K1 of circuit part GM is connected to a second output K2 by means of a capacitor C1 and by means of a series arrangement of switching element S1 and switching element S2. A control electrode of switching element S1 is connected to a first output of circuit part Sc1. A control
15 electrode of switching element S2 is connected to a second output of circuit part Sc1. Circuit part Sc1 is a control circuit for generating a control signal for rendering the switching elements S1 and S2 alternately conducting and non-conducting at a frequency f . Switching element S1 is shunted by a series arrangement of coil L1, lamp terminal K3, lamp LA, lamp terminal K4 and capacitor C2. The lamp LA is shunted by capacitor C3. Circuit parts GM
20 and Sc1, switching elements S1 and S2, coil L1, lamp terminals K3 and K4 and capacitors C2 and C3 jointly form a power converter for generating a current from a supply voltage supplied by the supply voltage source, which current flows through the load formed by the lamp LA. An input of circuit part Sc1 is coupled to an output of circuit part III. A first input of circuit part III is connected to an output of circuit part II. A further input of circuit part III
25 is connected to an output of circuit part I. An input of circuit part I is coupled to the lamp LA. In Fig. 1, this coupling is indicated by means of a dashed line. Circuit part I forms a first circuit for generating a first signal that is a measure of the rms value of an operating parameter which, in this example, is a lamp quantity. Circuit part I comprises circuit parts IV, V and VI which are coupled with each other. Circuit part IV forms a fourth circuit for
30 generating a fourth signal that is a measure of the actual average value of the operating parameter. Circuit part V forms a fifth circuit for generating a fifth signal that is a measure of the actual maximum amplitude of the operating parameter. Circuit part VI forms a sixth circuit for generating a signal that is a linear combination of the third signal and the fourth signal. For this reason, respective inputs of circuit part VI are coupled to an output of circuit

part IV and an output of circuit part V. Circuit part II forms a second circuit for generating a second signal that is a measure of the desired rms value of the operating parameter. Circuit part III forms a third circuit for generating a third signal that depends on the first signal and the second signal, and for influencing the operating state of the circuit arrangement in
5 dependence upon the third signal. Circuit part I, II and III jointly form a control circuit for controlling the rms value of the operating parameter.

Next, a description is given of the operation of the circuit arrangement shown in Fig. 1.

If the input terminals K5 and K6 are connected to a supply voltage source such
10 as the electric power mains supplying a low-frequency AC voltage, this low-frequency AC voltage is rectified by the circuit part GM and a substantially constant DC voltage is present across capacitor C1. The circuit part Sc1 renders the switching elements S1 and S2 alternately conducting and non-conducting at a frequency f. As a result, a substantially square-wave voltage of frequency f is present at a junction point of the two switching
15 elements, and an alternating current of frequency f flows through the lamp. The circuit part I generates the first signal that is a measure of the rms value of a lamp quantity such as the lamp current, lamp voltage or lamp power. The first signal is formed via the circuit part VI as a linear combination of the fourth signal generated by circuit part IV and the fifth signal generated by circuit part V. More particularly, the first signal is equal to $0.845 \cdot OP_{avg} +$
20 $0.155 \cdot OP_{pk}$, where OP_{avg} and OP_{pk} form, respectively, the fourth signal and the fifth signal. The circuit part II generates a second signal that is a measure of the desired rms value of the lamp quantity. The circuit part III generates a third signal from the first and the second signal. This third signal is used to influence the operating state of the circuit arrangement via the frequency and/or the duty cycle of the control signal in such a manner that the rms value
25 of the lamp quantity at any moment in time is substantially equal to the desired value. This can be achieved, for example, via the frequency and/or duty cycle of the control signal. It is also possible to regulate the conduction time of the switching elements or the voltage across capacitor C1 by means of means that are not shown in Fig. 1.

Fig. 2A shows an embodiment of the circuit part I of the circuit arrangement
30 shown in Fig. 1 wherein the lamp quantity forming the operating parameter is the lamp voltage. K2 and K7 are terminals between which a signal is present during operation of the circuit arrangement shown in Fig. 1, which signal is a measure of the actual value of the lamp voltage. This can be achieved, for example, by arranging the primary winding of a transformer equipped with a primary winding and a secondary winding over the lamp and

connecting the terminals K2 and K7 to respective ends of the secondary winding. Terminals K7 and K2 are interconnected by means of a series arrangement of diode D1, ohmic resistor R1 and capacitor C5. The series arrangement of diode D1 and ohmic resistor R1 is shunted by a series arrangement of diode D2 and ohmic resistor R4. A junction point of diode D1 and ohmic resistor R1 is connected to terminal K2 by means of ohmic resistor R3. Ohmic resistor R3 is shunted by capacitor C4. A junction point of diode D2 and ohmic resistor R4 is connected to terminal K2 by means of ohmic resistor R2. A junction point of ohmic resistor R1, ohmic resistor R4 and capacitor C5 forms terminal K8. During operation of the circuit arrangement shown in Fig. 1, the first signal is present between terminal K8 and terminal K2. Diode D2, ohmic resistors R2 and R4, and capacitor C5 jointly form the circuit part IV. Diode D1, capacitors C4 and C5 and ohmic resistors R3 and R1 jointly form the circuit part V. The circuit VI is formed by the junction point of ohmic resistor R1, ohmic resistor R4 and capacitor C5.

Next, a description is given of the operation of the example shown in Fig. 2A.

If a signal that is a measure of the actual lamp voltage is present between the terminals K7 and K2, then the circuit part IV generates a fourth signal that is a measure of the actual average value of the lamp voltage. Circuit part V generates a signal that is a measure of the actual maximum value of the amplitude of the lamp voltage. Circuit part VI generates the first signal that is a linear combination of the first and the second signal: $A \cdot OP_{avg} + B \cdot OP_{pk}$, where OP_{avg} forms the fourth signal and OP_{pk} forms the fifth signal. The values of the constants A and B are determined by the resistance values of the ohmic resistors R1, R2, R3 and R4. The first signal is formed by the voltage across capacitor C5.

Fig. 2B shows an example of circuit part I, wherein the operating parameter whose rms value is controlled is the lamp current. K9 and K10 are terminals forming the ends of the primary winding of a transformer T1. During operation of the circuit arrangement shown in Fig. 1, a signal that is a measure of the actual value of the lamp current is present between the terminals K9 and K10. This can be achieved, for example, by arranging the transformer and the lamp so as to be in series. Respective ends of a secondary winding of the transformer T1 are connected to respective inputs of a diode bridge formed by diodes D1-D4. A first output of the diode bridge is connected to a second output by means of ohmic resistor R2 and by means of a series arrangement of diode D5 and capacitor C4. Capacitor C4 is shunted by ohmic resistor R3 and by a series arrangement of ohmic resistor R1 and capacitor C5. Ohmic resistor R2 is shunted by a series arrangement of ohmic resistor R4 and capacitor C5. A junction point of ohmic resistor R4 and capacitor C5 forms a terminal K8. During

operation of the circuit arrangement, the first signal is present between terminal K8 and terminal K2 in the form of the voltage across capacitor C5. Circuit part IV is formed by transformer T1, the diode bridge, ohmic resistors R4 and R2 and capacitor C5. Circuit part V is formed by transformer T1, the diode bridge, diode D5, ohmic resistors R3 and R1 and
5 capacitors C4 and C5. Circuit part VI is formed by the junction point of ohmic resistor R1, ohmic resistor R4 and capacitor C5.

The operation of the example shown in Fig. 2 corresponds to the operation of the example shown in Fig. 2A and will not be separately described herein. Also in this example, the values of the constants A and B are determined by the resistance values of the
10 ohmic resistors R1, R2, R3 and R4.

Fig. 2C shows a further embodiment of the circuit part I, in which the operating parameter whose rms value is controlled is the lamp voltage. K2 and K7 are terminals between which, during operation of the circuit arrangement shown in Fig. 1, a signal is present that is a measure of the actual value of the lamp voltage. This can be
15 achieved, for example, by arranging the primary winding of a transformer equipped with a primary and a secondary winding over the lamp and connecting terminals K2 and K7 to respective ends of the secondary winding. Terminals K7 and K2 are connected together by means of a series arrangement of capacitor C3, ohmic resistor R6 and diode D1. Diode D1 is shunted by a series arrangement of diode D2 and ohmic resistor R2. A junction point of diode
20 D2 and ohmic resistor R2 is connected to terminal K2 by means of a series arrangement of diode D5 and capacitor C4. Diode D5 is shunted by a series arrangement of ohmic resistor R4 and ohmic resistor R1. Capacitor C4 is shunted by ohmic resistor R3. A junction point of ohmic resistor R4 and ohmic resistor R1 forms a terminal K8. Terminal K8 is connected to terminal K2 by means of a capacitor C5. During operation of the circuit arrangement, the first
25 signal is present between terminals K8 and K2 in the form of the voltage across capacitor C5. Capacitor C3, ohmic resistors R6 and R2, and diodes D1 and D2 form a single-phase rectifier that, during operation, rectifies the signal present between terminals K7 and K2. This rectifier and ohmic resistors R4, R1 and R3, and capacitor C5 jointly form the circuit part IV. The circuit part V is formed by the rectifier in combination with diode D5, capacitors C4 and C5
30 and ohmic resistors R1 and R3. Circuit part VI is formed by the junction point of ohmic resistor R4, ohmic resistor R1 and capacitor C5.

The operation of the example shown in Fig. 2C corresponds to the operation of the examples shown in Fig. 2A and Fig. 2B and will not be separately described herein. Also

in this example, the values of the constants A and B are determined by the resistance values of the ohmic resistors R1, R2, R3 and R4.

Fig. 2D forms a fourth example of circuit part I, which corresponds substantially to the example shown in Fig. 2C. In the example shown in Fig. 2D, ohmic resistor R6 is arranged in series with diode D1. The series arrangement of diode D1 and ohmic resistor R6 is shunted by a capacitor C6. For the rest, the structure of the example shown in Fig. 2D corresponds to that of the example shown in Fig. 2C. Capacitor C4 and capacitor C3 jointly form a capacitive divider. The resistance value of ohmic resistor R6 is chosen to be substantially equal to that of ohmic resistor R2. As a result, diode D1 and diode D2 carry substantially equal currents and a DC offset due to a difference in diode threshold voltages does not develop.

The operation of the example shown in Fig. 2D corresponds to the operation of the examples shown in Fig. 2A, Fig. 2B and Fig. 2C and will not be separately described herein.

CLAIMS:

1. A circuit arrangement for feeding a load, which is equipped with
- input terminals which are to be connected to a supply voltage source,
 - a power converter for generating a current through the load from a supply voltage supplied by the supply voltage source,
 - 5 – a control circuit for controlling the rms value of an operating parameter, comprising
 - a first circuit for generating a first signal that is a measure of the actual rms value of the operating parameter,
 - a second circuit for generating a second signal that is a measure of the desired rms
 - 10 value of the operating parameter,
 - a third circuit that is coupled to the first and the second circuit for generating a third signal that is dependent on the first and the second signal, and for influencing the operating state of the circuit arrangement in dependence on the third signal,
- 15 characterized in that the first circuit is equipped with
- a fourth circuit for generating a fourth signal that is a measure of the actual average value of the operating parameter,
 - a fifth circuit for generating a fifth signal that is a measure of the actual maximum amplitude of the operating parameter,
 - 20 – a sixth circuit for generating a signal that is a linear combination of the third signal and the fourth signal.
2. A circuit arrangement as claimed in claim 1, wherein the load is a lamp, and the operating parameter is selected among the group consisting of the lamp current and the
- 25 lamp voltage.
3. A circuit arrangement as claimed in claim 1, wherein the sixth circuit generates a signal of the general formula

$$A * OP_{avg} + B * OP_{max},$$

wherein OPavg and OPmax are the value of the fourth signal and the value of the fifth signal, respectively, and wherein

$$0 < A < 1 \quad \text{and} \quad 0 < B < 1.$$

5 4. A circuit arrangement as claimed in claim 3, wherein

$$0.76 < A < 0.93 \quad \text{and} \quad 0.12 < B < 0.19.$$

5. A first circuit for use in a circuit arrangement as claimed in any one of the preceding claims.

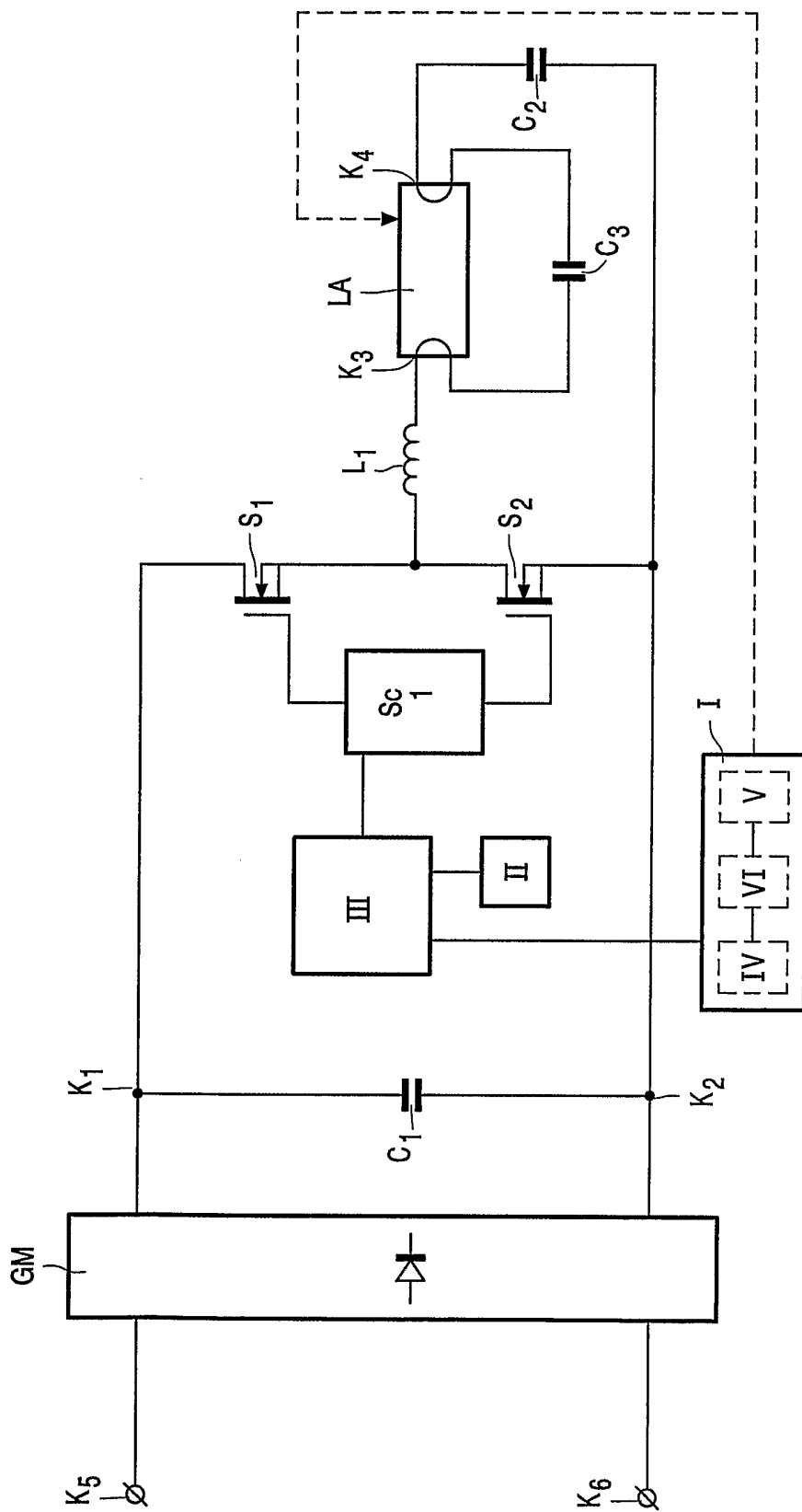


FIG. 1

2/2

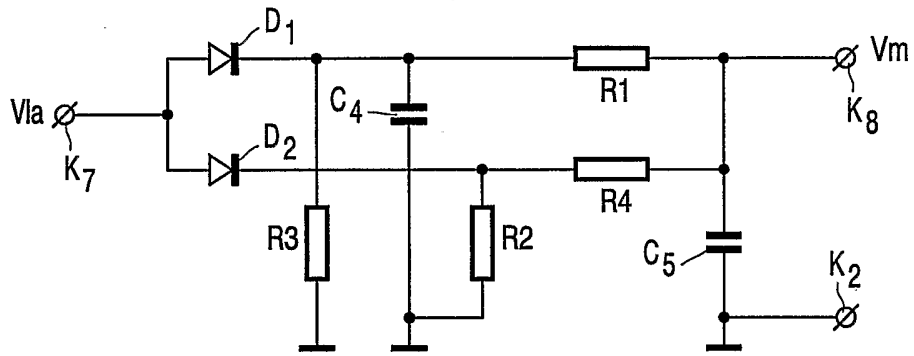


FIG. 2A

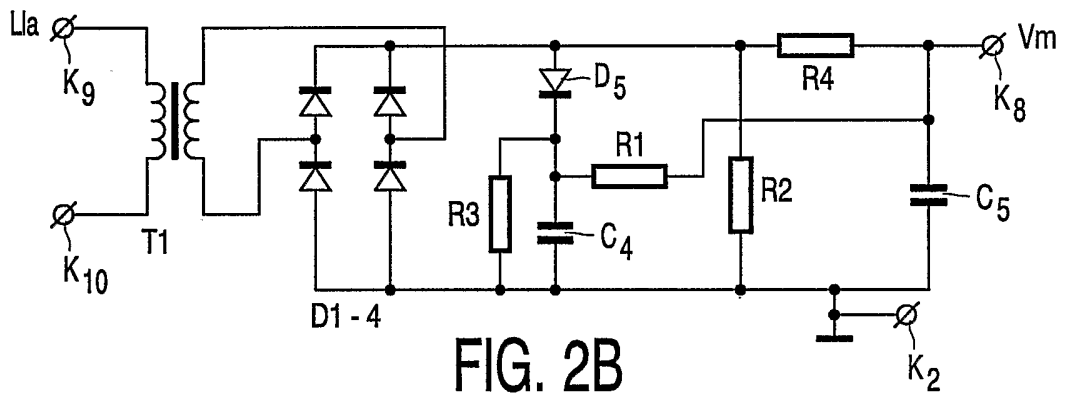


FIG. 2B

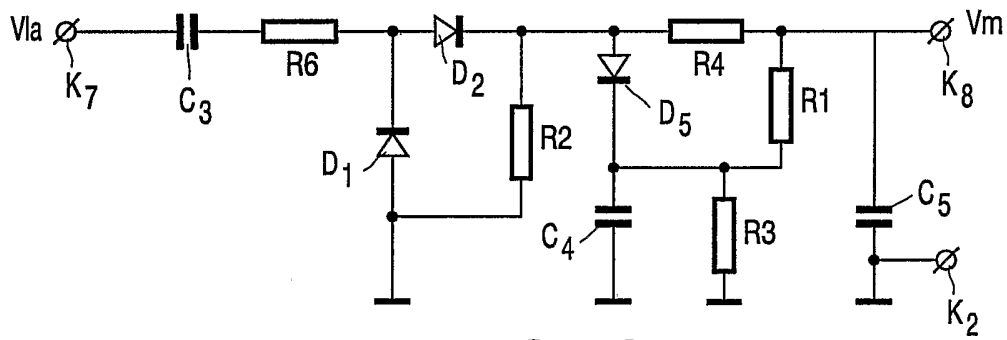


FIG. 2C

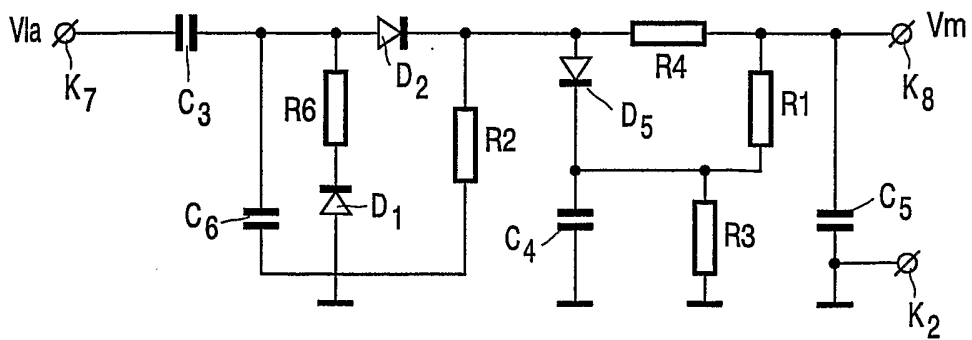


FIG. 2D

INTERNATIONAL SEARCH REPORT

International Application No
PCT/IB 02/02965

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H05B41/392 G01R19/02

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED
Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H05B G01R

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 450 268 A (PHILLIPS TIMOTHY B ET AL) 12 September 1995 (1995-09-12) column 3, line 63 -column 4, line 56	1,3-5
Y	column 4, line 65 -column 5, line 44; figure 3	2
X	US 3 434 053 A (MCKEE DONALD A) 18 March 1969 (1969-03-18) column 1, line 14 -column 3, line 41; figures 1,3-5	1,3-5
Y	EP 0 605 052 A (PHILIPS ELECTRONICS NV) 6 July 1994 (1994-07-06) figures 1,4	2

Further documents are listed in the continuation of box C. Patent family members are listed in annex.

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Date of the actual completion of the international search 22 October 2002	Date of mailing of the international search report 29/10/2002
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INTERNATIONAL SEARCH REPORT

national Application No

PCT/IB 02/02965

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