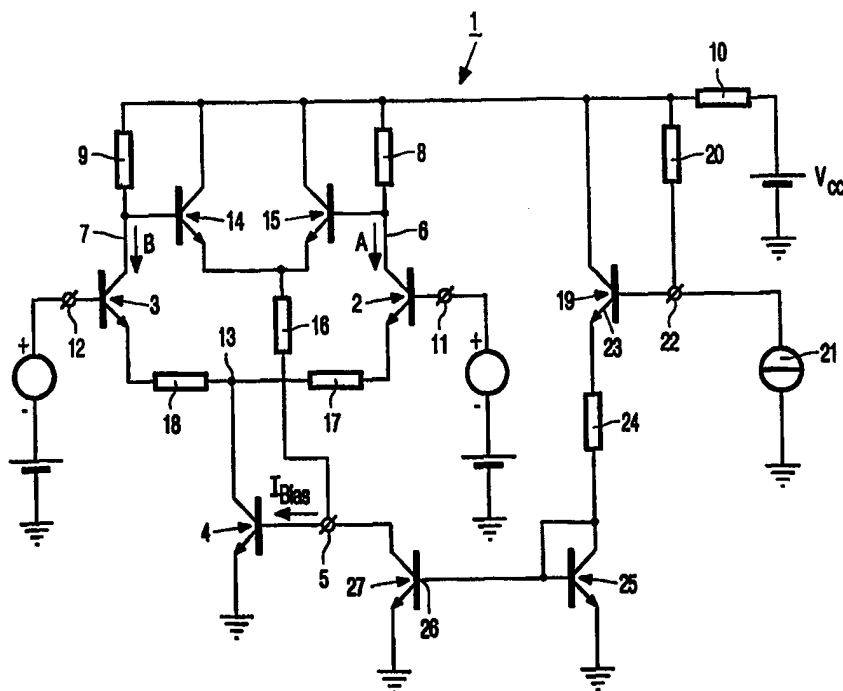




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(21) International Application Number: PCT/IB98/00572 (22) International Filing Date: 16 April 1998 (16.04.98) (30) Priority Data: 97201944.2 25 June 1997 (25.06.97) EP (34) Countries for which the regional or international application was filed: NL et al. (71) Applicant: KONINKLIJKE PHILIPS ELECTRONICS N.V. [NL/NL]; Groenewoudseweg 1, NL-5621 BA Eindhoven (NL). (71) Applicant (for SE only): PHILIPS AB [SE/SE]; Kottbygatan 7, Kista, S-164 85 Stockholm (SE). (72) Inventor: BALTUS, Petrus, Gerardus, Maria; Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL). (74) Agent: MAK, Theodorus, N.; Internationaal Octrooibureau B.V., P.O. Box 220, NL-5600 AE Eindhoven (NL).		(81) Designated States: CN, JP, European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE). Published <i>With international search report.</i> <i>Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.</i>

(54) Title: A DIFFERENTIAL AMPLIFIER, AN INTEGRATED CIRCUIT, AND A TELEPHONE



(57) Abstract

A differential amplifier comprises differential main current streams, a controlled current source means to feed the main current streams, the controlled current source means having a control input for controlling the main current streams, and a saturation sensing circuit coupled between the main current streams and the control input for generating a control input signal in dependence of saturation sensed in at least one of the main current streams. The differential amplifier has an improved large signal behaviour at low power dissipation and increased efficiency.

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"A differential amplifier, an integrated circuit, and a telephone"

The present invention relates to a differential amplifier outlined in the first part of claim 1.

The present invention also relates to an integrated circuit provided with such a differential amplifier and to a telephone provided with such an integrated circuit.

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Such a differential amplifier is known from US patent 3,440,554. The known differential amplifier comprises differential main current (ways, paths) hereafter called streams having a two-stage differential transistor pair fed by a controlled current source transistor means having a control input for controlling the main current streams, and comprises a loop circuit embodied as a common mode negative feedback loop coupled between the main current streams and the control input of the controlled current source transistor means. The common mode negative feedback acts to improve the discrimination factor (defined as the ratio of differential mode to common mode gain) and to improve the common mode rejection factor (defined as the common mode voltage input to the differential mode voltage input to produce the same output voltage). In addition a negative feedback bias loop is implemented in the differential main current streams to permit elimination of the collector resistances in said streams. The operation of the known differential amplifier is such that the combination of the common mode negative feedback loop and the negative feedback bias loop results in a cooperative effort to maintain the collector bias voltage constant. It is an disadvantage of the known differential amplifier that the large AC signal behaviour is poor and that only a limited range of input amplitudes can be amplified effectively.

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Therefore it is an object of the present invention to provide a differential amplifier having improved large AC signal behaviour and being suitable for being applied in a wider variety of applications.

Thereto the differential amplifier according to the invention has the

characterising features outlined in claim 1. The present invention makes use of the notion that the poor large AC signal behaviour of the known differential amplifiers is due to saturation effects originating from large AC output signals whose top amplitude approach the supply voltage, and that this disadvantageous behaviour improves if the controlled current source means is controlled such that during saturation the differential main current provided by said means is temporarily increased to compensate for the saturation effects. The differential circuit according to the invention can now be used in applications where low power dissipation and/or high efficiency are/is required. Apart from low frequencies the differential amplifier according to the invention can, depending on the bandwidth of the applied semiconductors, also be used in RF applications. Special attention deserves application in processes offering excess bandwidth at currents lower than currents required for achieving dynamic range requirements. The excess bandwidth can then be used through the differential amplifier according to the invention to reduce power dissipation and increase efficiency, but also to make the power dissipation adaptive to signal levels that are being processed. This opens further possibilities of the differential amplifier according to the invention for being applied in front-end circuits for mobile radio and mobile telephone applications, viz. GSM and AMPS front-ends. In addition easy integration is possible which will result in improved characteristics because integration leads to better matched applicable semiconductor components in the respective differential main current streams and to small sized appliances.

One embodiment of the differential circuit according to the invention has the characterising features outlined in claim 2. In this embodiment of the differential amplifier according to the invention such a detecting circuit senses saturation in the main current streams by detecting the maximum voltage which is allowable for a saturation free functioning.

An embodiment which has the advantage of being easily implementable by means of only one type of semiconductors, that is to say either PNP or the more easily to integrate NPN semiconductors, has the characterising features outlined in claim 3.

A further embodiment of the differential amplifier according to the invention has the characterising features outlined in claim 4. Such a bias element which can either be resistive or reactive serves effective gain control purposes for controlling the tail current -which is the combined current in both main current streams- provided by the controlled current source means.

A still further embodiment of the differential amplifier according to the

invention has the characterising features outlined in claim 5. The advantage of applying degeneration elements, such as for example resistors in the differential main current stream is that these elements improve linearity around the cross-over point, which otherwise would introduce troublesome third order distortion.

5 A next embodiment of the differential amplifier according to the invention has the characterising features outlined in claim 6. This embodiment of the differential amplifier according to the invention has the advantage of mainly containing semiconductor elements as bias controlling elements, thus forming an alternative to such bias controlling elements embodied with a bias resistor means.

10 Still a next embodiment of the differential amplifier according to the invention has the characterising features outlined in claim 7 for providing the advantage of a reduced supply voltage dependency of the functioning of said differential amplifier.

15 The present invention will now be described, by way of example, with reference to the accompanying drawings, wherein

In the drawing:

Fig. 1 schematically shows combined embodiments of the differential amplifier according to the invention,

20 Fig. 2 shows graphs of V_{ce} , I_{bias} and V_{out} ($=V_7-V_6$) as functions of time (t) respectively appearing in the amplifier of fig. 1,

Fig. 3 shows a further embodiment of the differential amplifier according to the invention,

25 Fig. 4 shows a still further embodiment of the differential amplifier according to the invention,

Fig. 5 shows a telecommunication system provided with telephones having integrated circuits including a differential amplifier according to the invention and

Fig. 6 shows an embodiment of the differential amplifier according to the invention.

30 Throughout the figures the same reference numerals are used for the same features.

Fig. 1 shows a differential amplifier 1 comprising differential main

current paths or streams, designated A and B, formed by the collector-emitter chains of two controllable semiconductor transistors 2 and 3. A controlled current source means 4 included in the amplifier 1 feeds the main current streams A and B. The controlled current source means 4 showing one current source transistor has a control input 5 for controlling current in the main current streams. The collectors 6 and 7 respectively of transistor 2 and 3 are connected to a supply voltage V_{cc} , through resistors 8 and 9 and possible common resistor 10. V_{cc} is also connected to earth as shown. Bases 11 and 12 of the respective transistors 2 and 3 form input terminals for an input signal to be amplified, whereas the amplified signal can be taken from collectors 6 and 7. As shown the main stream currents A, B are being combined at collector 13 of current source transistor 4, whose emitter is also grounded. The functioning of such a differential amplifier is generally known.

The differential amplifier 1 further comprises a saturation sensing circuit which in the shown embodiment has two semiconductors 14 and 15 whose emitters are mutually connected to a bias element 16, which saturation sensing circuit 14, 15, 16 is coupled between the main current streams A, B and the control input 5 of the controlled current source means 4. The respective bases of the transistors 14, 15 are connected to the collectors 6 and 7, whereas its collectors are mutually coupled to V_{cc} . The functioning of the saturation sensing circuit 14-16 is such that it senses saturation in at least one of the main current streams A and B. The sensing circuit 14-16 is shown to be embodied as a main current stream maximum voltage detection circuit such that saturation is detected by detecting the maximum voltage on either one of the collectors 6 and 7, which maximum voltage V_{ce} approaches V_{cc} , thus showing saturation symptoms, elucidated in fig. 2.

The functioning of the sensing circuit 14-16 is such that it generates a increased biasing current I_{bias} -see fig. 2- which is controlled by the maximum of the two output voltages on collectors 6, 7. This maximum voltage will occur in the stream containing the lowest current, and therefore the lowest input voltage. The increased biasing current is injected at the control input 5 of current source 4, thus increasing the tail current through current source 4 which increase will essentially only increase the current in that stream A or B, were through the highest current flows. The current in the other stream stays at a more or less constant value higher than zero. The thus further increased higher current stream pulls the corresponding collector output temporarily down during saturation. The result is an amplified differential voltage V_{out} , shown in fig. 2, which does not show saturation effects.

Bias element 16, shown to comprise a resistor can simply be used for gain control by controlling the tail current through current source 4. Degeneration elements 17

and 18, comprising resistors, are used to improve linearity around the cross-over point, where conduction of one of the transistors 2, 3 is taken over by the other. This reduces third order harmonic distortion.

The differential amplifier 1 further comprises a ripple supply voltage
5 detecting means having a ripple control output coupled to the control input 5 of the controlled current source means 4. The ripple supply voltage detecting means comprises a transistor 19 connected as an emitter follower with a resistor 20 and a current source 21 connected in series to earth, whose connecting point is connected to the base 22 of transistor 19. Its emitter 23 is connected to earth through a series arrangement of resistor 24 and
10 junction 25. The connecting point of 24 and 25 is connected to the base 26 of transistor 27, whose mirrored main current stream is connected to control input 5.

The functioning of the ripple supply voltage detecting means 19-27 is such that it reduces the bias current dependence on the power supply voltage V_{cc} , since any change in the supply voltage across the differential amplifier 1 results in a corresponding
15 change in base current to transistor 4, leaving uninfluenced the biasing current through resistor 16.

Fig. 3 shows a further embodiment of the differential amplifier according to the invention, wherein the controlled current source means comprises two separate current source semiconductors 4-1 and 4-2, whose respective biasing currents are now voltage
20 controlled by at wish only one V_{bias} on the interconnected respective bases 28 and 29 of the semiconductors 4-1 and 4-2.

Fig. 4 shows a further worked out embodiment of the differential amplifier 1. Extra circuitry is added therein to lower the third harmonic distortion with 3 dB. The circuitry essentially comprises two current sources 30 and 31 controlled by parallel input
25 transistors 32 and 33 thus providing additional control to current source 4 for improving linearity at the cross over point mentioned earlier. Bias element 16 now comprises a parallel arrangement of a resistor 41 and a capacitor 34 for improving speed control characteristics.

The differential amplifier 1 can be implemented in an IC for application in a telecommunication device such as a telephone 35 as shown in fig. 5. Such a telephone can
30 be a mobile telephone or a fixed telephone or the like and can be implemented in a telecommunication system 36. It contains a microprocessor 37, an associated memory 38, display screen 39, and a keyboard 40. Of course the telephone 35 will comprise all further features properly implemented and necessary for the required functioning thereof, together with additional features such as hands free capabilities, listening in features, loudspeaker

facilities, dialling features, charging facilities etcetera.

Fig. 6 shows an embodiment of the differential amplifier 1 according to the invention, comprising transistors 40, 41, 42, 43, 44 and 45, and resistors 46, 47, 48, 49, 50, 51, 52, 53, 54 and 55, and further capacitors 56 and 57, and a resistor 58 between
5 emitters of the transistors 40 and 41. This embodiment has similar properties as the other described embodiment, but provides a higher efficiency because of the larger output voltage OUT if sufficient bandwidth is available from the active devices. The resistor 58 sets the gain. The bias voltage V_{Bias} sets the limits for the class A region of operation. The output
10 voltage OUT is the largest possible in an NPN-only circuit, a CMOS implementation also being applicable. The capacitors 56 and 57 may be replaced by level shift circuits, well known in the art.

In view of the foregoing it will be evident to a person skilled in the art that various modifications may be made within the spirit and the scope of the present invention as hereinafter defined by the appended claims and the present invention is thus not
15 limited to the examples provided.

CLAIMS:

1. A differential amplifier comprising:
 - differential main current streams,
 - a controlled current source means to feed the main current streams, the controlled current source means having a control input for controlling the main
 - 5 current streams, and
 - a loop circuit coupled between the main current streams and the control input, characterised in that the loop circuit is a saturation sensing circuit for generating a control input signal in dependence of saturation sensed in at least one of the main current streams.
2. A differential amplifier according to claim 1, characterised in that the
- 10 saturation sensing circuit is a main current stream maximum voltage detection circuit.
3. A differential amplifier according to claim 2, characterised in that the main current stream maximum voltage detection circuit comprises common collector connected semiconductors.
4. A differential amplifier according to one of the claims 1-3, characterised
- 15 in that the differential amplifier comprises a bias element coupled between the main current streams and the control input of the controlled current source means.
5. A differential amplifier according to one of the claims 1-4, characterised in that the differential amplifier comprises degeneration elements included in the differential main current streams.
- 20 6. A differential amplifier according to one of the claims 1-5, characterised in that the controlled current source means comprises separately controlled current sources each coupled to a respective differential main current stream.
7. A differential amplifier according to one of the claims 1-6, characterised in that the differential amplifier comprises ripple supply voltage detecting means having a
- 25 ripple control output coupled to the control input of the controlled current source means.
8. An integrated circuit provided with a differential amplifier according to one of the claims 1-7, comprising:
 - differential main current streams,
 - a controlled current source means to feed the main current streams, the

controlled current source means having a control input for controlling the main current streams, and

- a loop circuit coupled between the main current streams and the control input, characterised in that the loop circuit is a saturation sensing circuit for generating a control input signal in dependence of saturation sensed in at least one of the main current streams.

9. A telephone provided with an integrated circuit according to claim 8, having a differential amplifier according to one of the claims 1-7, comprising:

- differential main current streams,
- a controlled current source means to feed the main current streams, the controlled current source means having a control input for controlling the main current streams, and
- a loop circuit coupled between the main current streams and the control input, characterised in that the loop circuit is a saturation sensing circuit for generating a control input signal in dependence of saturation sensed in at least one of the main current streams.

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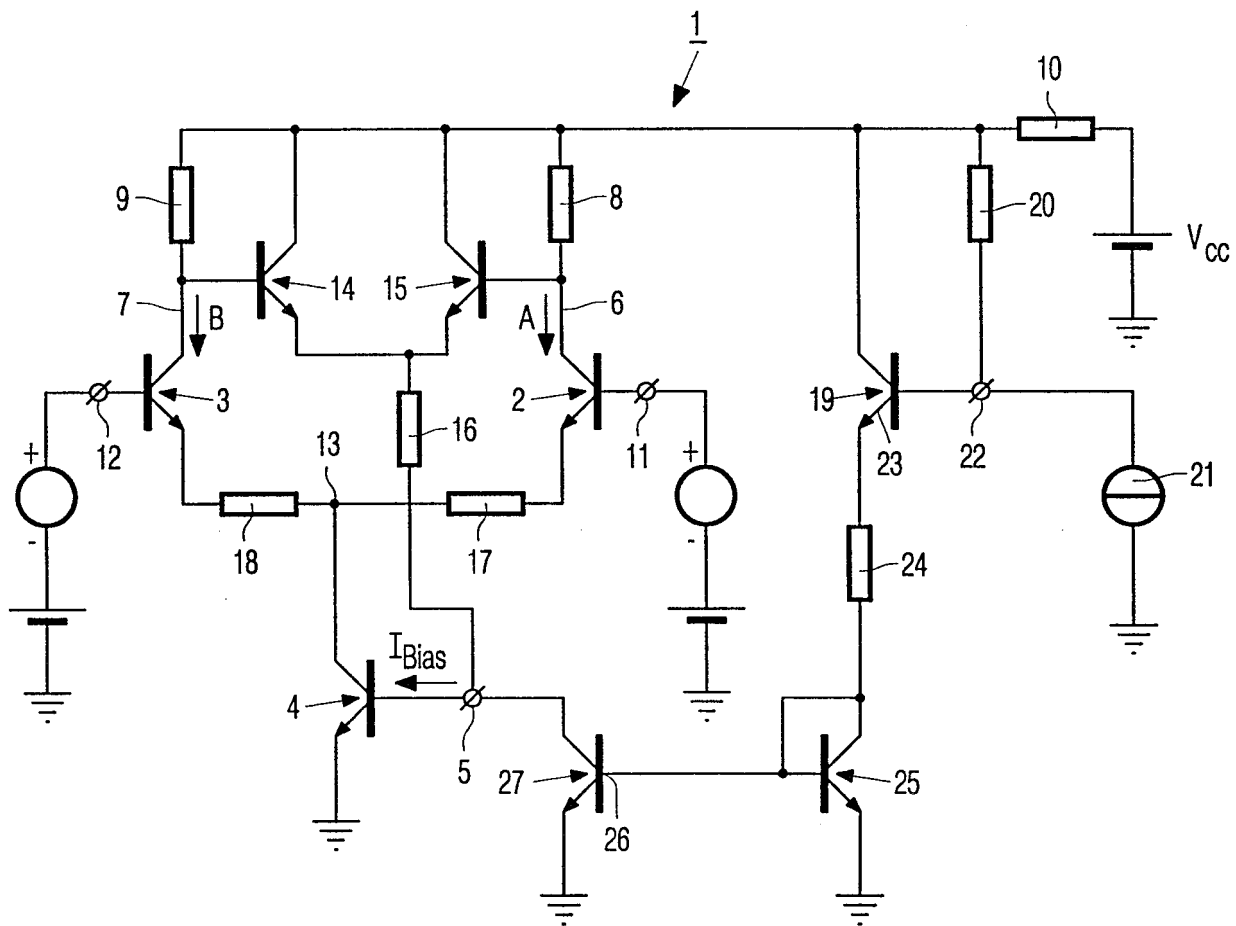


FIG. 1

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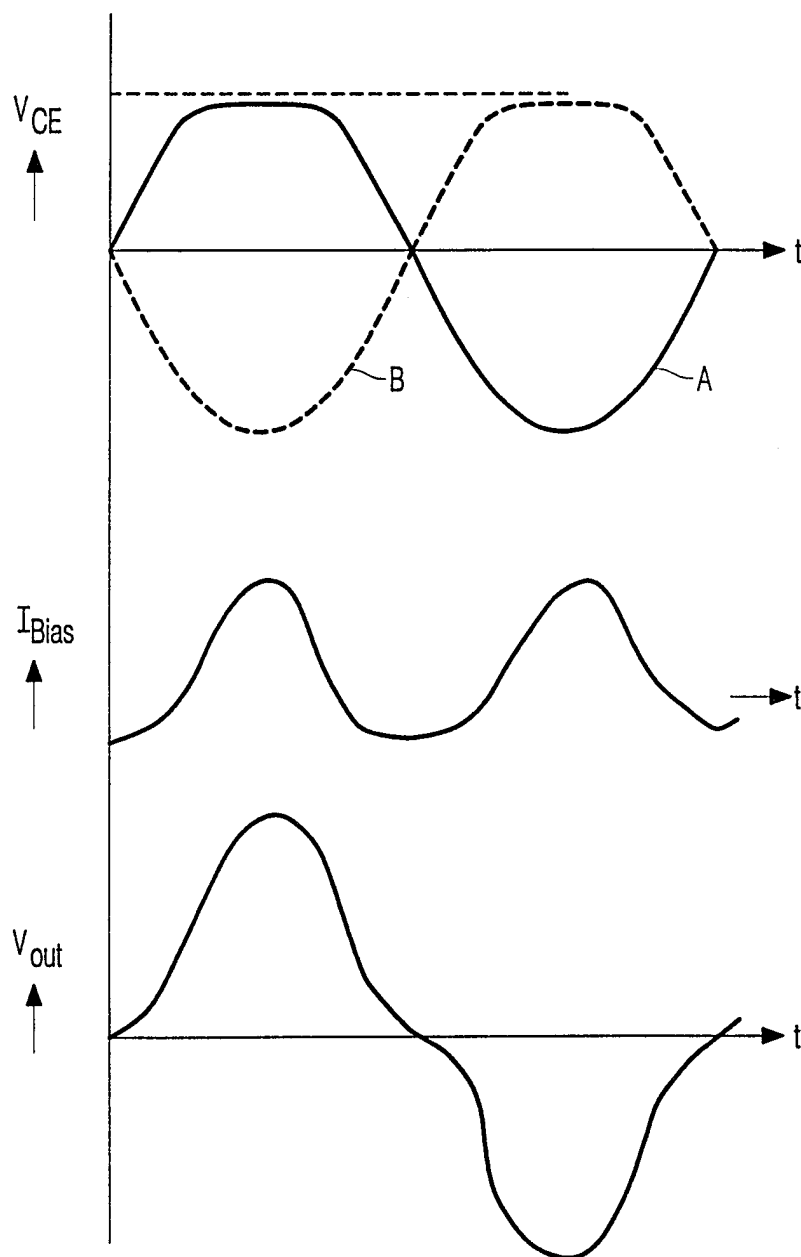


FIG. 2

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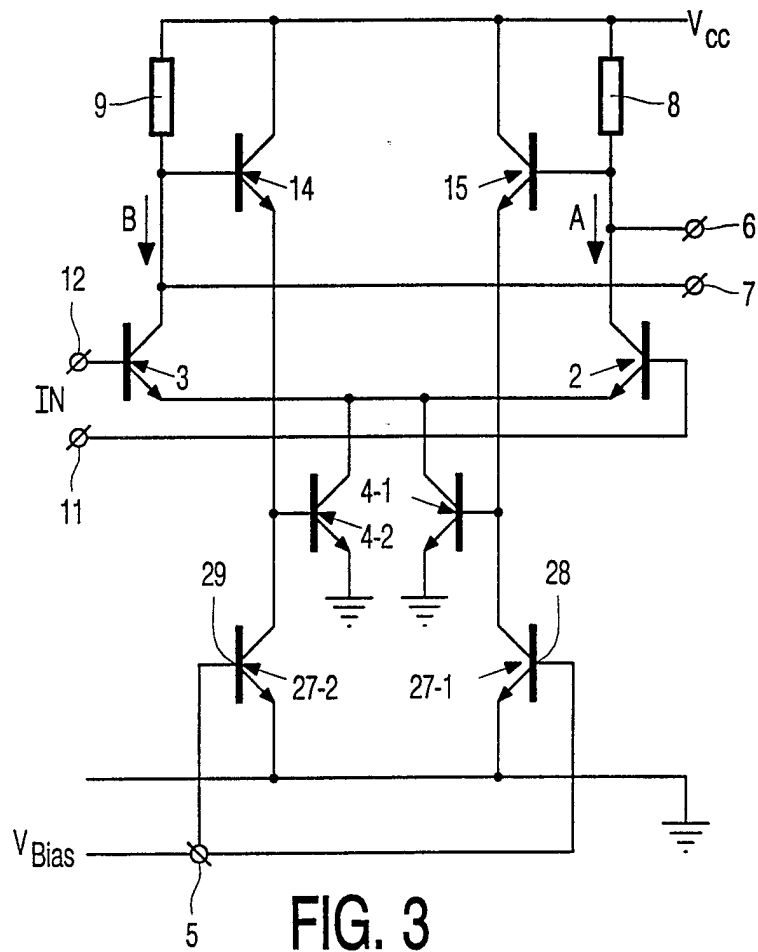


FIG. 3

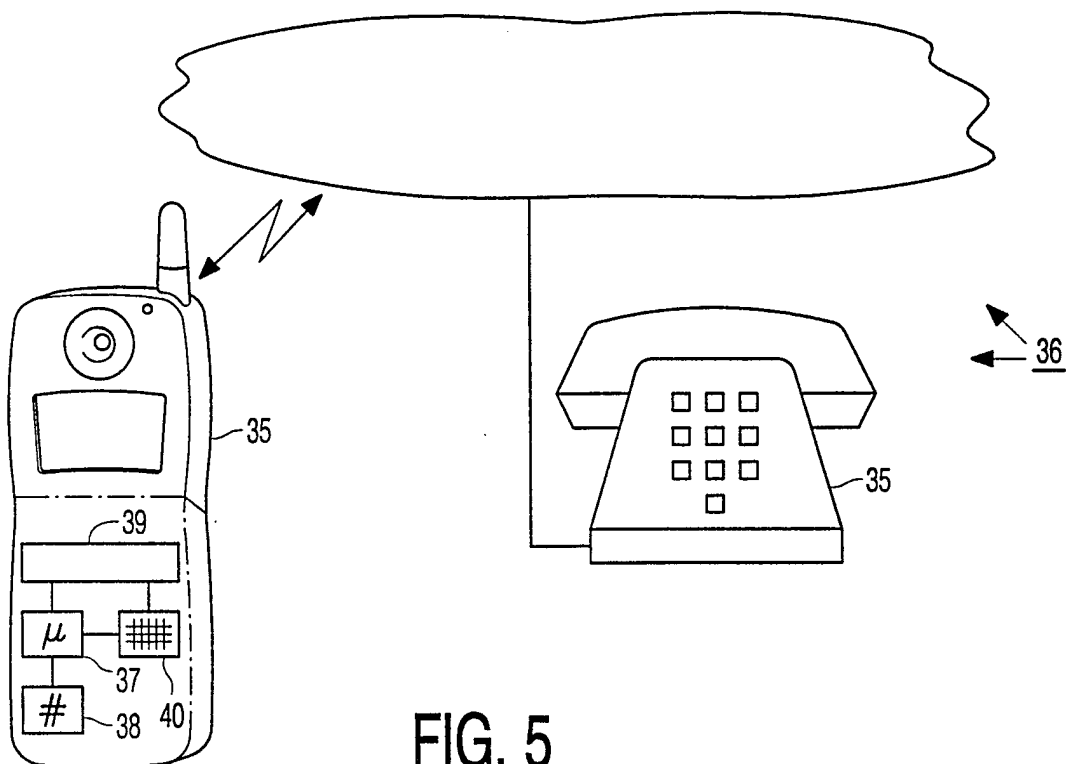


FIG. 5

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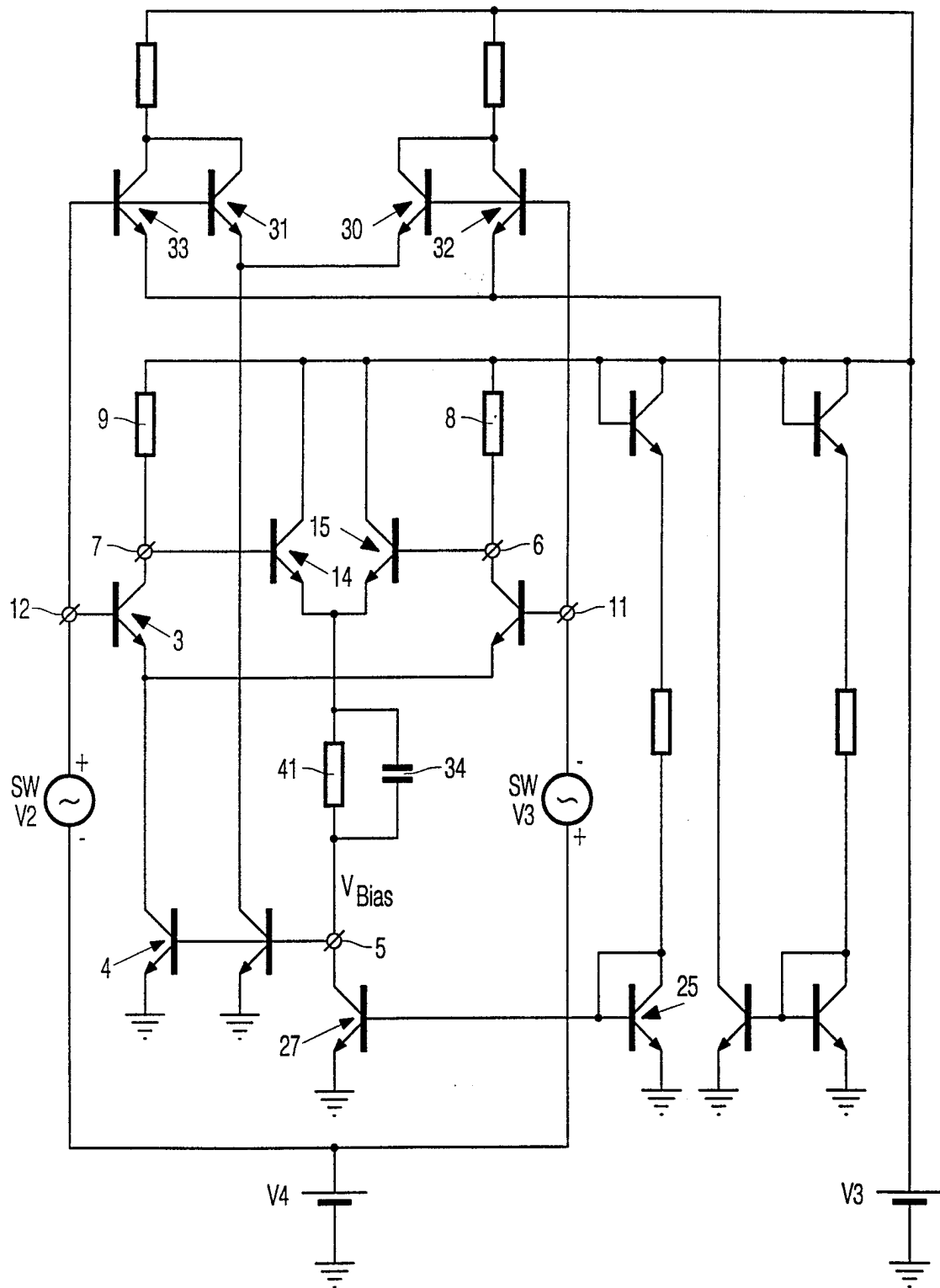


FIG. 4

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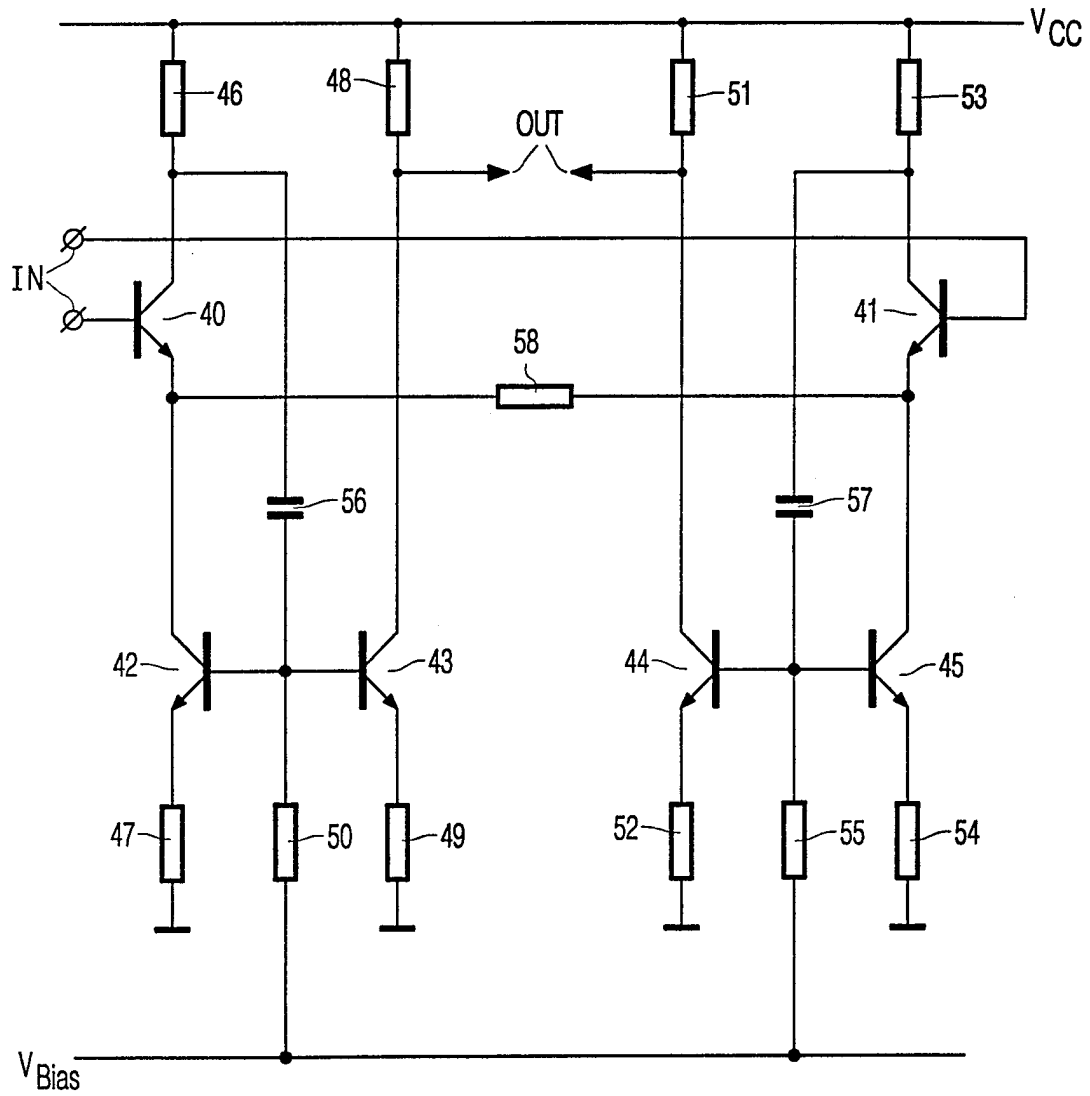


FIG. 6

INTERNATIONAL SEARCH REPORT

International application No.

PCT/IB 98/00572

A. CLASSIFICATION OF SUBJECT MATTER

IPC6: H03F 3/45

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC6: H03F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

SE,DK,FI,NO classes as above

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EDOC, WPIL, JAPIO, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 4442408 A (TRUNG LE), 10 April 1984 (10.04.84), column 2, line 45 - line 65; column 3, line 10 - line 20; column 3, line 55, figure 1 --	1-9
A	US 3440554 A (D.R. MCGRAW ET AL), 22 April 1969 (22.04.69), See the whole document. Cited in the application. --	1,8-9
A	US 4272728 A (HAROLD A. WITTLINGER), 9 June 1981 (09.06.81), See the whole document -- -----	1,8-9



Further documents are listed in the continuation of Box C.



See patent family annex.

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INTERNATIONAL SEARCH REPORT

Information on patent family members

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Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 4442408 A	10/04/84	CA 1187144 A	14/05/85
		EP 0094485 A,B	23/11/83
		SE 0094485 T3	
		JP 1047048 B	12/10/89
		JP 1562169 C	31/05/90
		JP 58206211 A	01/12/83

US 3440554 A	22/04/69	NONE	

US 4272728 A	09/06/81	NONE	
