Title: SIGNAL DROP COMPENSATION AT EXTERNAL TERMINAL OF INTEGRATED CIRCUIT PACKAGE

Abstract: Compensation is provided for signal drop in bond wires of an integrated circuit (integrated circuit) (110) while minimizing the number of external terminals in the integrated circuit package (120). A functional circuit provides an output signal (e.g., voltage) on a pad of the integrated circuit, which is connected to an external terminal (130) on the package via a bond wire (170). A second circuit contained in the integrated circuit determines the signal drop in the bond wire by examining a parameter (e.g., current) proportional to a strength of the output signal at or before the pad in a transmission path of the signal. Thus, additional external terminals to sense the signal strength at a point external to the integrated circuit to provide compensation for the drop may not be required.
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SIGNAL DROP COMPENSATION AT EXTERNAL TERMINAL OF INTEGRATED CIRCUIT PACKAGE

The invention relates generally to integrated circuits, and more specifically to signal drop compensation in a wire conductor of a packaged integrated circuit.

BACKGROUND

An integrated circuit (integrated circuit, sometimes also referred to variously as microcircuit, microchip, silicon chip, chip, etc.,) generally is a miniaturized circuit, often containing semiconductor devices (as well as passive components such as resistors etc) that have been manufactured on a substrate, usually of a semiconductor or ceramic material.

An integrated circuit may be constructed/fabricated as a monolithic integrated circuit or hybrid integrated circuit. In a monolithic integrated circuit, the entire circuit is built into a single piece of semiconductor (chip), whereas a hybrid integrated circuit may contain multiple monolithic integrated circuits, and/or discrete semiconductor device circuits (typically fabricated on a ceramic substrate) interconnected in a desired manner.

Integrated circuits may be packaged in a housing (integrated circuit package, chip package), which is generally suitable for plugging into or soldering onto a printed circuit board. Dual-in-line package (DIP), Small-outline-integrated circuit (SOIC), plastic leaded chip carrier (PLCC), flat-pack, etc., are some examples of the various packages, as is well-known in the relevant arts. Each package contains external terminals (such as a pin or ball), which may operate as input, output and/or power pins.

An integrated circuit may contain one or more pads on which corresponding signals of interest such as input signals, output signals, power supply voltages, etc., are provided/received to/from external components. A pad generally refers to a contact on the substrate to provide/receive such signals, and is often implemented as a metal.

Generally, each pad of the integrated circuit is connected by a bond wire (often made of gold) to a corresponding external terminal on the integrated circuit package. A bond wire may be associated with an impedance and often causes a reduction in signal strength (signal drop). For example, the voltage drop (IR drop) caused by a bond wire, may cause an output voltage generated in the integrated circuit (e.g., at a pad of the integrated circuit) to be below a desired level (strength) at the external terminals.
Therefore, it is desirable to compensate for such signal drops due to bond wires. It is further generally desirable that the compensation be provided while reducing (or using as few pins as possible) the pin-count (i.e., number of external terminals) requirements.

SUMMARY

Several aspects of the invention enable minimizing the number of external terminals required when compensation is to be provided for signal drop in bond wire of a package in which an integrated circuit is provided.

An integrated circuit implemented according to an aspect of the invention contains a functional circuit to generate an output signal. The functional circuit provides the output signal on a pad of the integrated circuit, which is connected to an external terminal on the integrated circuit package via a bond wire. The integrated circuit contains a second circuit to determine the difference between the strengths of the output signal at the pad and at the external terminal by examining a parameter proportional to a strength of the signal at or before the pad in a transmission path of the signal in the integrated circuit. The strength of the signal is adjusted by the difference (for example, by generating a corresponding correction voltage) to ensure that the signal has a desired strength at the external terminal, thereby compensating for signal drop in the bond wire.

Since the difference is determined by examining a parameter at or before the pad, additional external terminals may not be required to provide compensation.

According to another aspect of the invention, an integrated circuit contains a scaling block to amplify the difference of the strengths noted above. As a result, components such as resistors used in the circuit to generate a correction voltage may be implemented as small value resistors occupying a small area on the integrated circuit.

Several aspects of the invention are described below with reference to examples for illustration. It should be understood that numerous specific details, relationships, and methods are set forth to provide a full understanding of the invention. One skilled in the relevant art, however, will readily recognize that the invention can be practiced without one or more of the specific details, or with other methods, etc. In other instances, well-known structures or operations are not shown in detail to avoid obscuring the features of the invention.
BRIEF DESCRIPTION OF THE DRAWINGS

Example embodiments are described below with reference to accompanying drawings, wherein:

FIG. 1 is a diagram illustrating an integrated circuit housed in an integrated circuit package in one embodiment.

FIG. 2 is a block diagram illustrating example interconnections between integrated circuits on a printed circuit board.

FIG. 3 is a diagram illustrating the manner in which compensation for signal drop in the bond wire of an integrated circuit package is provided according to a prior approach.

FIG. 4 is a diagram of an integrated circuit in an embodiment of the invention providing compensation for signal drop in bond wires.

FIG. 5 is a diagram of an integrated circuit in an alternative embodiment of the invention providing compensation for signal drop in bond wires, while minimizing the area on the integrated circuit.

FIG. 6 is a diagram of a scaling block used in an embodiment of the invention.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

FIG. 1 illustrates an integrated circuit housed in a package, integrated circuit 110 is shown housed in package 120. Pad 175 is shown connected through bond wire 170 to an external terminal 130, which is a pin in this example. Pad 185 is shown connected to an external terminal via bond wire 180, with the external terminal shown implemented as ball 160. Typically, an integrated circuit is packaged with either balls or pins, though the diagram is shown containing both merely for illustration. Integrated circuit 110 in packaged form (i.e., package 120) is typically mounted or soldered on printed circuit board 150 to enable interconnections with other integrated circuits/devices in printed circuit board 150 to achieve a desired operation, as illustrated in FIG. 2.

FIG. 2 is a block diagram illustrating the interconnections between integrated circuit 110 (housed in package 120) and integrated circuits 220 and 230 (which may also be in packaged form), integrated circuit 110 is shown with a logical view (removing some of the components not needed) with only those components needed for understanding IR drop being included.
The voltage output on pad 175 is provided to external terminal 130 via bond wire 170. External pin 130 is shown connected to pins 240 and 250 of integrated circuits 220 and 230 respectively via printed circuit board trace 222. Pins 240 and 250 may correspond to power supply pins of integrated circuits 220 and 230 respectively.

During operation, corresponding internal circuitry connected to pins 240 and 250 (of integrated circuits 220 and 230 respectively) draws current from the voltage output on pad 175. Due to the impedance (e.g., resistance) of bond wire 170, a voltage (IR) drop in bond wire 170 causes the voltage (strength) on external terminal 130 (and hence pins 240 and 250) to be less than the voltage provided on pad 175 (by integrated circuit 110), thereby resulting in poor load regulation.

For example, assuming that it is required to supply a voltage of 1.75 V (volts) on pins 240 and 250, integrated circuit 110 may be designed to generate 1.75V (available/provided on pad 175). However, due to the voltage drop in bond wire 170 noted above, the voltage at external terminal 130 (and hence pins 240 and 250) may be less than 1.75V. Consequently, techniques to compensate for the voltage drop are typically employed, as noted below with respect to a prior technique.

FIG. 3 is a diagram illustrating the manner in which compensation for signal drop in the bond wire of an integrated circuit package is provided according to a prior approach.

Integrated circuit 310 packaged in integrated circuit package 320 is shown containing voltage regulator 330. Voltage regulator 330 provides a desired voltage on pad 340, which is available to external devices via external terminal 360 and bond wire 350.

Resistor 395 represents a load presented by external components (for example, integrated circuits 220 and 230 of FIG. 2) to the voltage provided by voltage regulator 330. As noted above, the voltage drop due to bond wire 350 may cause the voltage at external terminal 360 (and hence across load resistor 395) to be less than a desired value (such as the value provided by voltage regulator 330 at pad 340).

In the prior technique of FIG. 3, integrated circuit package 320 contains an input terminal 390 (connected to pad 370 via bond wire 380) for sensing (measuring) the voltage at a point external to integrated circuit 310 (and also integrated circuit package 320). As shown in FIG. 3, voltage regulator 330 receives the voltages at pad 340 (via path 343) and load...
resistor 395 (via path formed by 369, 390, 380, 370 and 373). Voltage regulator 330 may then adjust (e.g., by increasing) the output voltage so that the voltage at terminal 360 and hence across load resistor 395 is at a desired level.

In general, one input terminal each for the positive signal path and a return (e.g., ground) signal path may be required to provide compensation according to the technique of FIG. 3, generally known in the relevant arts as 4-wire Kelvin sensing.

The prior technique noted above, however, requires at least one additional external pin (e.g. 390 in FIG. 3) and pad (370) for each output for which compensation is to be provided, thereby increasing the pin count of package 320. This is often undesirable.

Several aspects of the invention provide compensation for signal drop due to bond wire while minimizing the number of external terminals of an integrated circuit package, as described next with respect to an example embodiment.

FIG. 4 is a diagram of an integrated circuit in an embodiment of the invention, integrated circuit 401 is shown packaged in package 402, and contains a low drop-out (LDO) voltage regulator 403 providing a voltage output on pad 470, in turn connected to an external terminal 490 via bond wire 480. Resistor 495 represents a load presented to the output voltage on external terminal 490.

In FIG. 4, it is assumed that all voltages are provided with respect to ground terminal 499. It is also assumed (but not shown) that the respective components shown in the FIG. are connected to appropriate power supply terminals (which may, for example, be connected to an external power supply via an external terminal, not shown). Further the components of FIG. 4 are provided merely by way of illustration, and various features of the invention can be implemented in other environments and other components. The various sub-components/blocks of FIG. 4 are described in detail below.

LDO Voltage regulator 403 represents an example functional circuit which generates an output signal provided on pad 470, and is shown containing voltage generator 410, summing blocks 420 and 440 and gain block 430. The details of an example implementation of voltage regulator 403 as a low-drop out (LDO) regulator is illustrated and described in product description of part number REG102-25 (Single Output LDO, 250mA, Fixed(2.5V), Low Noise, Fast Transient Response), designed by Texas Instruments. An LDO regulator
generally refers to a linear voltage regulator that provides a regulated voltage output when
the input voltage (e.g., on path 412) is only very slightly larger than the voltage (pad 470).

Voltage generator 410 represents a stable power source providing a voltage on path
412, and may correspond, for example, to a battery, or a voltage reference generating a
voltage from an external source (not shown).

Summing block 440 receives as input a voltage signal each on paths 454 (connected
to path 425 or pad 470) and 464, and provides a difference of the voltages on path 443. Gain
block 430 amplifies the voltage difference on path 443 and provides an amplified voltage on
path 432. Summing block 440 and gain block 430 may together be referred to as an error
amplifier. In an embodiment the error amplifier is implemented as an Operational Amplifier
(OPAMP).

Summing block 420 provides a difference of voltages on paths 412 and 432 and
provides a voltage on path 425. Voltage signal on path 425 is also available on pad 470 and
external terminal 490, although at different strengths. In an embodiment, summing block 420
is implemented as a single-stage Operational Amplifier (OPAMP) having a single-pole roll-
off (low-pass filter characteristics).

During operation, load resistor 495 draws a current, resulting in a voltage drop across
bond wire 480, which in turn causes the voltage strength on external terminal 490 to be less
than that at pad 470. Path 425, pad 470, bond wire 480, external terminal 490, load resistor
495 and return path 499 (ground) may be referred to as a transmission path of the output
voltage generated/provided by voltage regulator 403.

According to an aspect of the invention, integrated circuit 401 contains circuit 404
(also referred to as a second circuit in this document) formed by sense element 450 and
"compensation" resistor 460. Sense element 450 senses the output current IL (on the
transmission path noted above) and provides a fraction "α" of the output current IL to flow
across "compensation" metal resistor 460 (RCOMP). Node 455 may be connected to a
voltage generated internally in integrated circuit 401. Sense element 450 may be
implemented using techniques, well known in the relevant arts.

The fraction α is selected (usually much less than 1) such that voltage drop across
metal resistor 460 (RCOMP) is substantially the same as the voltage drop across bond wire
480. The value of resistor 460 may be chosen based on the value of the impedance (resistance) of bond wire 480, which is usually known at the time of packaging integrated circuit 401.

The "compensation" (or correction) voltage generated on path 464 is given by the following equation:

\[ V_{COMP} = (\alpha \times I_L \times R_{COMP}) \]

\[ = (R_{BW} \times I_L) \]

Equation 1

Equation 2

wherein, \( V_{COMP} \) is the compensation voltage generated on path 464, \( R_{COMP} \) is the value of resistor 460, and \( R_{BW} \) is the value of resistance of bond wire 480.

From equations 1 and 2:

\[ R_{COMP} = \frac{R_{BW}}{\alpha} \]

Equation 3

\( R_{BW} \) may be known a priori (before fabrication of integrated circuit 401) and thus \( R_{COMP} \) may be selected accordingly. Designating the voltage on paths 412 as \( V_{ref} \), and on pad 470 (or path 425) as \( V_{OUT} \), the feedback loop formed by path 454-440-43-432-420 will ensure that in the stable condition \( V_{ref} \) is given by the following equation:

\[ V_{ref} = K(V_{OUT} - V_{COMP}) \]

Equation 4

Wherein \( K \) represents the gain provided by gain block 430.

From equation 4:

\[ V_{OUT} = \frac{[V_{ref} + (K \times V_{COMP})]}{K} = \left(\frac{V_{ref}}{K}\right) + V_{COMP} \]

Equation 5

Assuming \( V_{COMP} \) substantially equals the voltage drop \((R_{BW} \times I_L)\) across bond wire 480, equation 5 may be written as:

\[ V_{OUT} = \left(\frac{V_{ref}}{K}\right) + (R_{BW} \times I_L) \]

Equation 6

It may be noted from equation 6 that \( V_{OUT} \) has been boosted up (compensated) to the extent of the bond-wire drop represented by \((R_{BW} \times I_L)\). That is the output voltage on pad 470 and consequently on external terminal 490 has been compensated for the voltage drop in the bond-wire 490. The compensation is provided across variations in load current \( I_L \).

It may be observed also that the circuit of FIG. 4 determines the magnitude of voltage drop in bond wire 480 by sensing (examining) the load current at or before pad 470, thereby not requiring an additional input terminal (such as 390 in FIG. 3). As a result, compensation
is provided without requiring additional pins, thereby minimizing pin count of package 402.

It is usually desirable that compensation be effective across a wide range of temperatures (example, over a range 125 degrees centigrade), thereby requiring that both RCOMP (resistor 460) and RBW (bond wire 480) have the same (or very nearly the same) temperature coefficient of resistivity. RBW usually being a metal (such as gold having a temperature coefficient of resistivity of 4 parts per million per degree centigrade), RCOMP may be implemented as a metal resistor (copper or aluminum having temperature coefficients of resistivity of 4.3 and 4.2 parts per million per degree centigrade respectively) on-chip so that RCOMP substantially tracks the changes of bond-wire resistance RBW over wide temperature ranges.

As noted above, the value of $\alpha$ is generally selected to have a value much less than 1 to minimize power dissipation in RCOMP. However, a value of $\alpha$ much less than 1 requires that RCOMP have a value much larger than RBW, as may be observed on inspection of Equation 3. Such a large value for RCOMP generally requires resistor 460 to have a large area, thus occupying a large die area on integrated circuit 401. This may not be desirable for reasons such as size, cost of fabricating integrated circuit 401 etc.

An alternative embodiment of the invention overcomes the drawback noted above, and is described next.

FIG. 5 is a diagram of integrated circuit 401 in an alternative embodiment. All components/blocks in FIG. 5 are similar to corresponding components/blocks in FIG. 4. In addition, in the alternative embodiment of FIG. 5, integrated circuit 401 contains a scaling block 510 to amplify the correction voltage generated on path 464 by a suitable factor Kl, and provide the scaled correction voltage to summing block 440 via path 514.

The value of correction voltage VCOMP in the circuit of FIG. 5 may be expressed as:

$$VCOMP = (Kl \ast \alpha \ast IL \ast RCOMP)$$

Equation 7

For the compensation to be effective, the value of VCOMP as expressed in equation 7 may need to also equal (Kl* RBW * IL), i.e.,

$$VCOMP = (RBW \ast IL)$$

Equation 8

From equations 7 and 8 the expression of RCOMP may be obtained as:

$$RCOMP = RBW / (Kl \ast \alpha)$$

Equation 9
Thus, by selecting $K_1$ to be suitably large, the value of $R_{COMP}$ (and hence area on integrated circuit 401) may be made small. As an example, assuming $\alpha$ is chosen to be 0.01 so that power dissipation in $R_{COMP}$ is minimized, value of $R_{COMP}$ is chosen sufficiently small so that area on the die (as well as power dissipation) is minimized. The value of $K_1$ may then be chosen to be: $K_1 = 100^* RBW / R_{COMP}$.

In an embodiment scaling block 510 is implemented as an OPAMP connected in a non-inverting configuration, as shown in FIG. 6. In FIG. 6, OPAMP 630 is shown connected in a non-inverting configuration. The gain of OPAMP 630 is given by $(1 + R_f/R)$, wherein $R_f$ is the value of resistor 620, and $R$ is the value of resistor 610. Resistors 610 and 620 are implemented using a same material.

Therefore, resistors 610 and 620 have the same temperature coefficient of resistivity, thereby resulting in the value of gain $K_1$ being substantially constant over a wide temperature range. Further, resistors 610 and 620 may be placed in integrated circuit 401 such that variations in their resistance values are minimized over process variations also.

Integrated circuit 401 implemented as described above may contain several functional circuit blocks (in addition to functional circuit 403). Integrated circuit 401 may, for example be a system-on-a-chip (SOC) incorporating multiple operational/functional blocks to provide features of a large system (for example, telecommunications system) and may contain microprocessor(s), digital signal processor (DSP), RAM and ROM, graphics processors etc. Functional block 403 (operating in conjunction with sensing block 404 as described above may provide a regulated voltage to several on-chip as well as off-chip (via external terminal 490) components with compensation provided for voltage drop in bond wires as described above.

Those skilled in the art will appreciate that many other embodiments and variations are also possible within the scope of the claimed invention. Embodiments having different combinations of one or more of the features or steps described in the context of example embodiments having all or just some of such features or steps are also intended to be covered hereby.
CLAIMS

What is claimed is:

1. A method of providing a signal at a desired strength on an external terminal of a package in which an integrated circuit is packaged, the integrated circuit comprising a pad, wherein said pad is coupled to said external terminal via a wire conductor, said conductor being characterized by an impedance, said method comprising:
   - generating said signal;
   - determining a magnitude of a signal drop in said conductor by examining a parameter proportional to a strength of said signal at or before said pad in a transmission path of said signal; and
   - adjusting a strength of said signal by said magnitude to cause said signal to have a desired strength on said external terminal.

2. The method of claim 1, wherein said signal is an output voltage, said parameter is a current, and said determining step comprises:
   - generating a second current proportional to said current parameter; and
   - generating a correction voltage substantially equaling the voltage drop in said conductor, wherein said adjusting adds said correction voltage to said output voltage, thereby compensating for said voltage drop.

3. The method of claim 1, wherein said signal is an output voltage, said parameter is a current, and said determining step comprises:
   - generating a second current proportional to said current parameter;
   - generating a first voltage proportional to said second current by passing said second current through a compensation resistor; and
   - amplifying said first voltage to generate a correction voltage substantially equaling the voltage drop in said conductor, wherein said adjusting adds said correction voltage to said output voltage, thereby compensating for said voltage drop.

4. The method of claim 1, 2 or 3, wherein said conductor is a bond wire.

5. An integrated circuit designed to provide a signal from a packaged integrated circuit to an external terminal via a wire conductor, said conductor being characterized by an impedance, and said integrated circuit comprising:
a pad coupled to said external terminal through said conductor;

a functional circuit to provide said signal at said pad, wherein said signal has a first strength at said pad and a second strength at said external terminal, wherein said second strength is less than said first strength due to impedance of said conductor; and

a second circuit to determine a difference of said first strength and said second strength by examining a parameter proportional to a strength of said signal at or before said pad in a transmission path of said signal, wherein the strength of said signal is adjusted by said difference to ensure that said signal has a desired strength at said external terminal.

6. The integrated circuit of claim 1, wherein said conductor is a bond wire; signal is an output voltage; wherein said second circuit comprises a current sensing element, said parameter being a current flowing on said transmission path; and wherein said current sensing element generates a second current proportional to said current.

7. The integrated circuit of claim 6, wherein said second circuit further comprises a compensation resistor; said functional circuit comprises a summing block; said current sensing element is designed to provide said second current to said compensation resistor to generate a corresponding correction voltage substantially equaling the voltage drop in said bond wire; and said summing block receives said correction voltage and adds said correction voltage to said output voltage, thereby compensating for said voltage drop.

8. The integrated circuit of claim 6, wherein said second circuit further comprises a compensation resistor; said functional circuit comprises a summing block and a scaling block; said scaling block is designed to amplify a voltage across said compensation resistor to generate a correction voltage substantially equaling the voltage drop in said bond wire; and said summing block receives said correction voltage and adds said correction voltage to said output voltage, thereby compensating for said voltage drop.

9. A device for providing a signal at a desired strength on an external terminal of an integrated circuit package, said integrated circuit comprising a pad, wherein said pad is coupled to said external terminal via a bond wire, said bond wire being characterized by an impedance, said article comprising:

means for generating said signal;

means for determining a magnitude of a signal drop in said bond wire by
examining a parameter proportional to a strength of said signal at or before said pad in a
transmission path of said signal; and
means for adjusting a strength of said signal by said magnitude to cause said signal to have a desired strength on said external terminal.

10. The article of claim 9, wherein said signal is an output voltage, said parameter being a current, wherein said means for determining is operable to:
   generate a second current proportional to said current; and
   generate a correction voltage substantially equaling the voltage drop in said bond wire, wherein said adjusting adds said correction voltage to said output voltage, thereby compensating for said voltage drop.

11. The article of claim 9, wherein said signal is an output voltage, said parameter being a current, wherein said means for determining is operable to:
   generate a second current proportional to said current;
   generate a first voltage proportional to said second current by passing said second current through a compensation resistor; and
   amplify said first voltage to generate a correction voltage substantially equaling the voltage drop in said bond wire,
   wherein said adjusting adds said correction voltage to said output voltage, thereby compensating for said voltage drop.