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Powell

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[54] **MOS VOLTAGE REFERENCE CIRCUIT**

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[51] **Int. Cl.** **H03k 3/26**

[58] **Field of Search**..... 307/297, 205, 221 C, 251, 307/279, 304, 227

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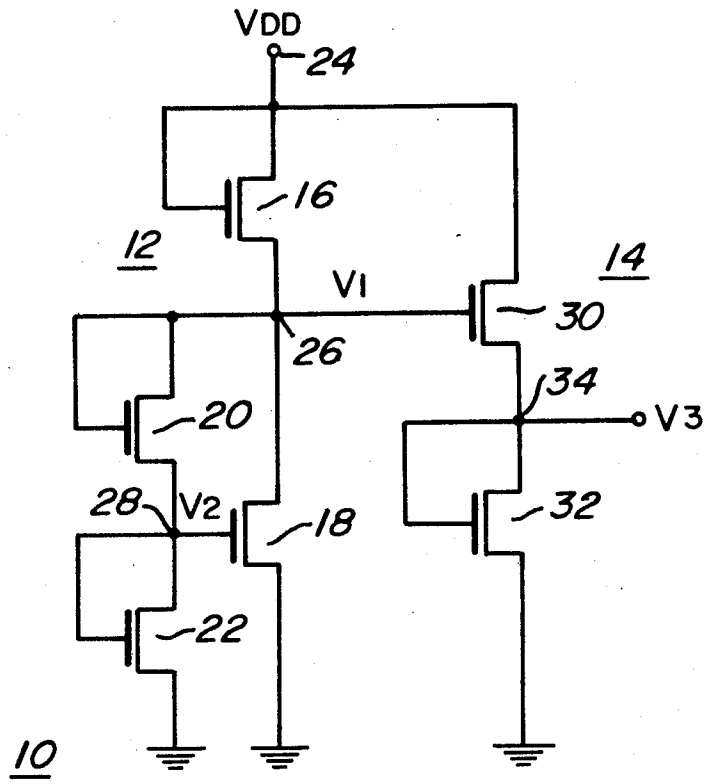
[57] **ABSTRACT**

A MOS voltage regulator circuit produces a regulated voltage at an output node. A reference circuit including first and second MOSFETs connected in series between ground and a power supply produces an internal reference voltage. The internal reference voltage is sensed by a feedback circuit including a diode-connected MOSFET and is regulated thereby. The internal reference voltage is applied to an output circuit including a pullup MOSFET and a pulldown diode-connected MOSFET which produce a regulated output voltage.

15 Claims, 2 Drawing Figures



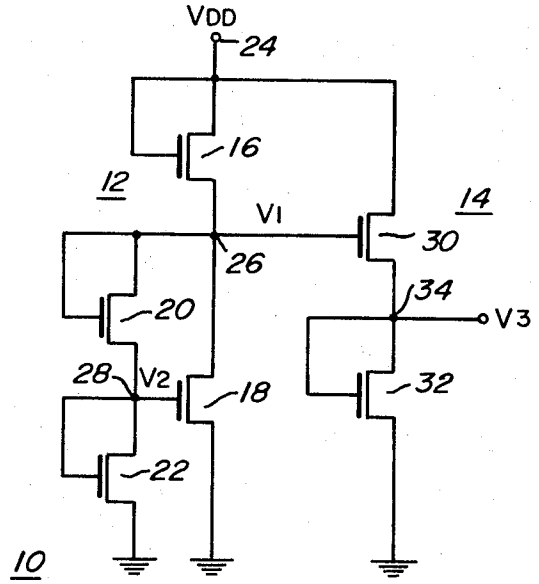
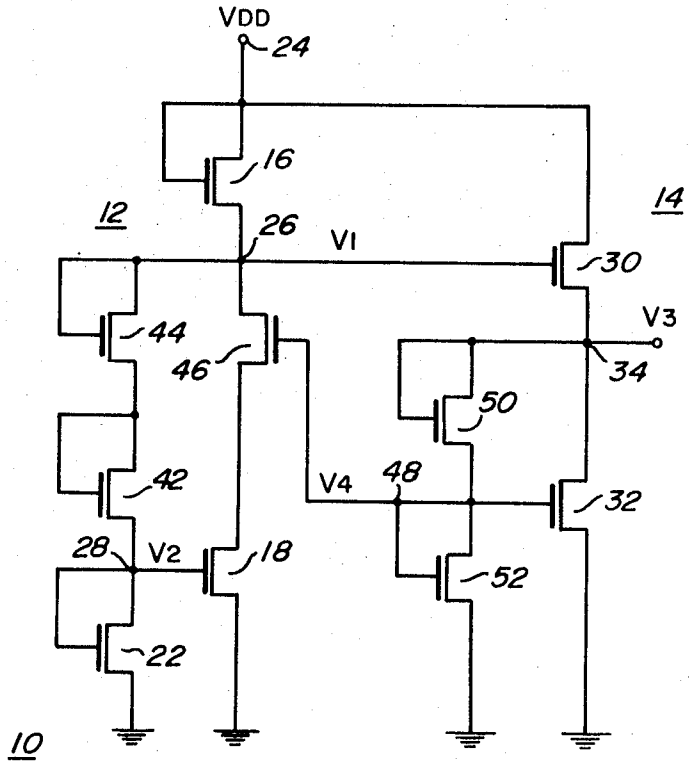

VDD
24
16
12
V1
14
30
26
34
V3
20
28
V2
18
32
22
10

Fig. 1


VDD
24
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26
V1
14
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V3
44
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42
V4
48
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V2
18
52
22
10

Fig. 2

MOS VOLTAGE REFERENCE CIRCUIT

BACKGROUND OF THE INVENTION

This invention relates to voltage regulator circuits, and particularly to MOS voltage regulator circuits suitable for application in integrated circuits.

Exact uniformity in the manufacture of MOS integrated circuits is not practically achievable. The threshold voltage (V_{TH}) necessary to cause the finished MOS devices to operate may vary widely from one integrated circuit chip to another. It therefore is frequently required in such circuits to have an internal circuit which provides a reference voltage dependent mainly on V_{TH}. Further, in MOS integrated circuits it is frequently useful to have a bias voltage supply which may be required to supply only a very small current. Usually, an extra lead is required on the package for connection to an external bias voltage supply, which prevents that lead from being used for some other function. Further, it is frequently desirable that the voltage provided by such a bias voltage supply tracks with the MOS threshold voltage V_{TH}. HOwever, since V_{TH} may be different for each However, chip, it is normally unfeasible to provide such a variation, except by providing a voltage regulator circuit on each MOS chip. Circuits are known which are capable of generating a reference voltage which varies directly with V_{TH}, but they are capable of responding only very slowly to an excursion of the reference voltage if a capacitive load is connected to the voltage reference circuit. Further, such prior art voltage reference circuits tend to dissipate an unacceptably large amount of power in order to provide a sufficiently low impedance voltage source. Further, such prior art voltage reference circuits provide output voltages which vary strongly with variations in the power supply, by a factor approximately equal to the ratios of the pullup and pulldown MOSFETS therein. Some prior art circuits are capable of rapidly discharging a capacitive load to the desired reference voltage and other prior art circuits have been capable of rapidly charging a capacitive load to the desired reference voltage, but none provide the capability of rapid adjustment of any perturbation of the voltage on a capacitive load while drawing negligible current and having negligible dependence upon variations in the power supply voltage. The present invention solves the aforementioned shortcomings of the prior art by providing a MOS voltage regulator circuit which produces a reference voltage which varies directly with the MOS threshold voltage, and responds rapidly to changes in the reference voltage even when connected to a capacitive load. The MOS voltage regulator circuit according to the present invention further is sufficiently small in an integrated circuit implementation thereof to permit it to be economically incorporated on each chip, and yet dissipates negligible power.

SUMMARY OF THE INVENTION

Briefly described, the invention is a MOS voltage regulator circuit. The regulator circuit includes a threshold reference circuit and an output circuit. The threshold reference circuit includes a first MOSFET having a low width-to-length geometry ratio connected in series with a second MOSFET having a relatively large width-to-length geometry ratio. The first MOSFET and the second MOSFET are connected between ground and the power supply voltage. A feedback circuit from the threshold reference circuit output node consists of a third MOSFET having its gate connected to its drain. The drain of the third MOSFET is connected to the threshold reference circuit output node. The source of the third MOSFET is connected to the gate of the second MOSFET, thereby limiting the quiescent voltage on the threshold reference stage output node to two MOS threshold voltage drops. The output circuit includes a fourth MOSFET and a fifth MOSFET connected in a series between ground and the power supply, both having relatively large width-to-length geometry ratios. The fifth MOSFET is a pulldown device having its gate connected to its drain and the fourth MOSFET is a pullup device having its gate connected to the threshold reference stage output node. The voltage regulator output node is connected to the source of the fourth MOSFET, and is held at a MOS threshold voltage drop from ground by the fourth and fifth MOSFETs. A sixth MOSFET having its gate connected to its drain and its source connected to ground has its drain also connected to the gate of the second MOSFET, thereby tending to limit the voltage thereon to one MOS threshold voltage from ground.

In a second embodiment of the present invention, the sixth MOSFET described hereinbefore is replaced by a diode. The leakage current of the diode performs the same function as the current through the above-described sixth MOSFET.

In a third embodiment of the present invention, the third MOSFET is replaced by two MOSFETs connected in series, each having its gate connected to its drain, so that the voltage reference circuit output node is held at three MOS threshold voltage drops from ground. Also, the gate-to-drain connection of the fifth MOSFET is broken and a diode-connected MOSFET is connected therein so that the voltage regulator output is held at two MOS threshold voltage drops from ground.

In a fourth embodiment of the present invention, a voltage from the output circuit is fed back to the threshold reference stage to amplify the threshold reference circuit output voltage to compensate for any deviation in the voltage regulator output voltage.

In view of the foregoing, it is an object of this invention to provide a MOS voltage regulator circuit capable of providing a reference voltage in an integrated circuit which is independent of power supply voltage variations.

Another object of this invention is to provide an MOS voltage regulator circuit which presents a relatively low output impedance to a capacitive load, and responds within a specified time to a positive or negative change of the voltage on the capacitive load.

Yet another object of the invention is to provide an MOS voltage regulator circuit of the type described which dissipates low power.

BRIEF DESCRIPTION OF THE FIGURES

FIG. 1 is a schematic diagram of the preferred embodiment of the invention.

FIG. 2 is a schematic diagram of another embodiment of the invention.

DETAILED DESCRIPTION OF THE INVENTION

FIG. 1 is a schematic diagram of a field-effect transistor voltage regulator circuit **10**. Voltage regulator **10** includes a reference circuit **12** and an output circuit **14**.

The reference circuit **12** includes MOSFETs **16, 18, 20** and **22.** (It should be noted that in the art the acronym MOSFET is widely understood to include within the scope of its meaning all insulated gate field-effect transistors, and this is the intended meaning in the description herein of this invention. It should be recognized by those skilled in the art that a MOSFET may be of the P-channel type or the N-channel type. For the description of the operation of the circuits presented herein, it is assumed that N-channel MOSFETs are used. However, P-channel MOSFETs may also be used. It is also well known that a MOSFET is a bilateral device having two main electrodes which may interchangeably function as source or drain electrodes, depending on which is at the more positive voltage. The convention adopted for the description herein is that the main electrodes will each be identified as either a source or a drain, although it is understood that during circuit operation an electrode identified as a source may function as a drain part of the time). MOSFET **16** has its drain and gate connected to power supply terminal **24,** designated V_{DD}. The source of MOSFET **16** is connected to node **26,** designated V_1. MOSFET **18** has its drain connected to node **26,** and its source connected to ground and its gate connected to node **28.** MOSFET **20** has its gate and drain connected to node **26,** and its source connected to node **28,** designated V_2. MOSFET **22** has its gate and drain connected to node **28** and its source connected to ground. The output circuit **14** includes MOSFET **30** and MOSFET **32.** MOSFET **30** has its drain connected to power supply terminal **24** and its gate connected to node **26** and its source connected to output node **34,** which is designated V_3. MOSFET **32** has its gate and drain connected to output node **34** and its source connected to ground. Thus, the regulated voltage output of the voltage regulator **10** is V_3.

MOSFET **16** has a relatively small width-to-length geometry ratio. MOSFET **18** has a large width-to-length geometry ratio, which is normally many times that of MOSFET **16.** (A MOSFET having its gate connected to its drain, may be referred to as a diode-connected MOSFET, since current can flow only in one direction therethrough and is blocked from flowing in the other direction). The operation of the reference circuit **12** is such that the voltage V_1 increases due to current supplied through MOSFET **16** if MOSFET **18** is off. (The threshold voltage at which a MOSFET begins to turn on is designated hereafter as V_{TH}; it is well known that the threshold voltage V_{TH} for a MOSFET increases as the reverse bias of the diode formed by the source of the MOSFET and the substrate is increased). Once V_1 has increased to approximately $2V_{TH}$ volts, V_2 tends to follow a threshold voltage drop below V_1, impeded by current flowing to ground through MOSFET **22.** It should be appreciated that the width-to-length ratio of MOSFET **22** should normally be designed to be very small, so that the impedance thereof is very high compared to that of MOSFET **20,** which may be a minimum geometry device. Then, assuming that MOSFET **18** has a much larger width-to-length geometry ratio than MOSFET **16,** when V_1 reaches approximately $2V_{TH}$ volts, MOSFET **18** begins to turn on, sinking the current flowing from MOSFET **16** into node **26** thereby limiting V_1 to approximately $2V_{TH}$ volts. It should be recognized that the equilibrium value of V_1 may be increased by merely reducing the width-to-length geometry ratio of MOSFET **18.** It should be appreciated by those skilled in the art that due to the very high impedances of MOSFET gate electrodes, voltages may be capacitively stored on the gates of MOSFETs for appreciable periods of time. Thus, if V_2 is caused to increase to a value substantially more than V_{TH} volts, MOSFET **22** will be turned on more strongly, and V_1 will decrease to less than $2V_{TH}$. Since MOSFET **20** is diode-connected, it will be turned off. If there is no discharge path provided for charge stored on the gate of MOSFET **18,** V_1 will remain at less than $2V_{TH}$ volts, which is obviously undesirable. MOSFET **22** prevents such a condition from occurring. Its width-to-length geometry ratio is chosen to be sufficiently high that it will adequately discharge excess charge from the gate of MOSFET **18** without appreciably impeding V_2 from following a V_{TH} voltage drop below V_1. It should be appreciated, however, that in some cases MOSFET **22** may be omitted, if the leakage current of the reverse-biased diode formed by the source of MOSFET **20** and the substrate is sufficiently large to discharge excess charge from the gate of MOSFET **18** in an acceptable amount of time. It should also be recognized that the amount variation of V_1 caused by a variation in V_{DD} is approximately proportional to the ratio of the impedance of MOSFET **16** to that of MOSFET **18.** Thus, the geometry ratios of MOSFET **16** and MOSFET **18** may be chosen so that V_1 depends almost solely on V_{TH}, (which is a MOS processing parameter) and is nearly exactly equal to $2V_{TH}$.

Assuming a completely capacitive load (not shown) is connected to node **34,** the regulated output voltage V_3 will attain an equilibrium value of V_{TH} volts, since diode-connected MOSFET **32,** which normally has a relatively large geometry ratio, will discharge the current from the load capacitance, thereby tending to decrease V_3 to V_{TH} volts. Also, if V_3 is less than V_{TH} volts, MOSFET **32** is off, and MOSFET **30** is on, since its gate-to-source voltage will be more than V_{TH} volts, and therefore supplies current which charges the load capacitance, and increases V_3 up to V_{TH} volts. However the geometry ratio of MOSFETs **30** and **32** may be chosen to provide recovery of V_3 from excursions about V_{TH} volts as rapidly as desired, for a completely capacitive load. If the load is also resistive, the MOSFET geometry ratios may be chosen sufficiently large to provide the desired degree of regulation of V_3.

FIG. **2** is a schematic diagram of another embodiment of the present invention. A feature illustrated in the embodiment shown in FIG. **2** is use of series connections of diode-connected MOSFETs to obtain an internal reference voltage V_1 equal to $3V_{TH}$, and an output voltage V_3 equal to $2V_{TH}$. The circuit illustrated in FIG. **1** is modified, as shown in FIG. **2,** to include diode-connected MOSFETs **42** and **44,** which are connected in series between nodes **26** and **28** in place of MOSFET **20.** Thus, V_2 follows an increase in V_1 by a $2V_{TH}$ volt drop, so V_1 attains an equilibrium value close to $3V_{TH}$ volts. Also, diode-connected MOSFET **50** is connected between node **34** and node **48,** designated V_4. If V_3 is greater than $2V_{TH}$, then V_4 will be greater than V_{TH}, and MOSFET **32** will begin to turn on, causing V_3 to return to $2V_{TH}$ volts. Diode-connected MOSFET **52** serves a purpose similar to that of MOSFET **22,** previously described, and is connected between ground and node **48** to prevent V_4 from being capacitively held at voltage greater than V_{TH} volts. Of course, the impedance of MOSFET **52** must be sufficiently large that V_4

efficiently follows positive excursions of V_3 above $2V_{TH}$ volts. Another feature illustrated in FIG. **2** is the utilization of feedback from output circuit **14** to reference circuit **12** so that an excursion of V_3 about $2V_{TH}$ volts causes an amplified corrective response by V_1. MOSFET **46** is connected between the drain of MOSFET **18** and the source of MOSFET **16,** and has its gate electrode connected to the gate of MOSFET **32,** which is at V_4 volts. If MOSFET **46** is on, and has a sufficiently large geometry ratio, then as V_1 increases toward V_{DD}, V_2 follows 2 V_{TH} voltage drops below V_1, until MOSFET **18** starts to turn on. V_3 then follows one V_{TH} drop below V_1, and attains equilibrium at $2V_{TH}$ volts. Note that in the embodiment shown in FIG. **1** the voltage V_1 is independent of output voltage V_3. Referring to FIG. **3,** if V_3 increases to a value greater than $2V_{TH}$ volts, then V_4 increases above V_{TH} volts, thereby turning MOSFET **32** on harder and then MOSFET **30** turns off, and V_3 is discharged back toward $2V_{TH}$ volts through MOSFET **32.** This too reduces V_1 negligibly, and therefore negligibly affects V_3. However, if V_3 is lower than $2V_{TH}$ volts, then MOSFET **52** causes MOSFET **46** to turn off, and V_1 increases, thereby turning MOSFET **30** on much more strongly, which results in increased current through MOSFET **30,** which increases V_3 to approximately $2V_{TH}$ volts.

It should be appreciated that variations of the above-described embodiments of the present invention to obtain different equilibrium values of the regulated output voltage V_3 are possible and are within the scope of the present invention. For example, additional diode-connected MOSFETs may be added in series with MOSFETs **42** and **44,** and, correspondingly, with MOSFET **50** (as in FIG. **2**) to obtain a regulated output voltage V_3 which is equal to the sum of a higher number of V_{TH} voltage drops. In any case, MOSFET **46** and the feedback connection from the gate thereof to the gate of MOSFET **32** may be included or excluded, depending on the desired characteristics of V_3. Also, various geometry ratios may be chosen for the MOSFETs, depending on the desired characteristics of V_3.

In summary, the present invention provides a MOS voltage regulator circuit which produces a regulated voltage which tracks with the MOS threshold voltage V_{TH}, and is much less dependent on power supply variations than prior art MOS regulator circuits. The power dissipation of the regulator circuit is very low compared to prior art MOS voltage regulator circuits, and the flexibility of designing the geometry ratios to obtain various characteristics of the regulated voltage is much greater than for prior art MOS voltage regulators.

Thus, while this invention has been shown in connection with several specific examples, it should be apparent to persons skilled in the art that various changes in form and arrangement of parts may be made to suit various requirements without departing from the spirit and scope of the present invention.

What is claimed is:

1. A field-effect transistor circuit connected to first and second power supply conductors for producing a regulated voltage at an output node comprising:

a reference circuit connected to an internal reference node for producing an internal reference voltage thereon;

an output circuit connected to said reference circuit and the output node for producing the regulated voltage at the output node;

said first reference circuit including the first circuit means responsive to the internal reference voltage connected to the internal reference node, second circuit means connected to the internal reference node for controlling the internal reference voltage thereon, and a first field-effect transistor having its gate connected to said first circuit means and its source connected to said second power supply conductor and its drain connected to said second circuit means, said output circuit including pull-up circuit means connected to the first power supply, the internal reference node of the reference circuit, and the output node for tending to increase the magnitude of the regulated output voltage, and pull-down circuit means connected to the output node and the second power supply conductor for tending to reduce the magnitude of the regulated output voltage.

2. The field-effect transistor circuit as recited in claim **1** wherein said first circuit means include a second field-effect transistor having its gate and drain connected to the internal reference node and its source connected to the gate of said first field-effect transistor.

3. The field-effect transistor circuit as recited in claim **1** wherein said second circuit means includes a third field-effect transistor having its gate and drain connected to the first power supply conductor and its source connected to the internal reference node.

4. The field-effect transistor circuit as recited in claim **1** further including third circuit means connected to the gate of said first field-effect transistor and the second power supply for discharging excess charge capacitively stored on the gate of said first field-effect transistor.

5. The field-effect transistor circuit as recited in claim **4** wherein said third circuit means include a fourth field-effect transistor having its gate and drain connected to the gate of said first field-effect transistor and its source connected to the second power supply.

6. The field-effect transistor circuit as recited in claim **1** wherein said second circuit means include a conductor connected between the internal reference node and the drain of said first field-effect transistor.

7. The field-effect transistor circuit as recited in claim **4** wherein said third circuit means comprise a reverse-biased diode connected between the gate of said first field-effect transistor and the second power supply.

8. A field-effect transistor circuit as recited in claim **1** wherein said pull-up circuit means comprise a fifth field-effect transistor having its source connected to the output node and its gate connected to the internal reference node, and its drain coupled to said first power supply conductor.

9. The field-effect transistor circuit as recited in claim **7** wherein said pulldown circuit means comprise a sixth field-effect transistor having its source connected to the second power supply conductor and its gate and drain connected to the output node.

10. The field-effect transistor circuit as recited in claim **1** wherein said first circuit means include at least two diode-connected field-effect transistors coupled in series, one having its gate and drain-connected to the internal reference node, and another having its source connected to the gate of said first field-effect transistor.

11. The field-effect transistor circuit as recited in claim 1 wherein said second circuit means include a seventh field-effect transistor having its drain connected to the internal reference node, its source connected to the drain of said first field-effect transistor, and its gate connected to said output circuit.

12. The field-effect transistor circuit as recited in claim 9 wherein said second circuit means include a seventh field-effect transistor having its drain connected to the internal reference node, its source connected to the drain of said first field-effect transistor, and its gate connected to the gate of said sixth field-effect transistor.

13. The field-effect transistor circuit as recited in claim 1 wherein said pull-down circuit means comprise a sixth field-effect transistor having its source connected to the second power supply conductor and its drain connected to the output node, and at least two diode-connected field-effect transistors connected in series, for biasing the gate electrode of said sixth field-effect transistor one having its source connected to the gate of said sixth field-effect transistor and another having its gate and drain connected to the output node.

14. A field-effect transistor regulator circuit coupled to first and second power supplies for producing a regulated voltage at an output node including a reference circuit connected to an internal reference node for producing an internal reference voltage thereon, an output circuit coupled to said reference circuit and to the output node for producing the regulated voltage at the output node, the output circuit including a pull-up field-effect transistor coupled to the first power supply, the internal reference node of the reference circuit, and the output node for tending to increase the regulated output voltage to one field-effect transistor threshold voltage drop from the second power supply voltage, and a pull-down field-effect transistor coupled to the output node and the second power supply for tending to reduce the regulated output voltage to one field-effect transistor threshold voltage drop from a second power supply voltage, the improvement comprising:

first, second and third electron control devices, respectively, in said reference circuit, said first electron control device being coupled between said internal reference node and said second power supply conductor, said second electron control device being coupled between said first power supply conductor and said internal reference node, and said third electron control device being coupled between said internal reference node and a control electrode of said first electron control device.

15. A field-effect transistor regulator circuit connected to first and second power supply conductors for producing a regulated voltage at an output node including a reference circuit connected to an internal reference node for producing an internal reference voltage thereon, an output circuit connected to said reference circuit and to the output node for producing the regulated voltage at the output node, the output circuit including a pull-up field-effect transistor coupled to the first power supply conductor, the internal reference node of the reference circuit, and the output node for tending to increase the regulated output voltage to one field-effect transistor threshold voltage drop from the second power supply conductor, and a pull-down field-effect transistor coupled to the output node and to the second power supply conductor for tending to reduce the regulated output voltage to one field-effect transistor threshold voltage drop from the second power supply conductor, the improvement comprising:

first, second, third and fourth insulated gate field-effect transistors, respectively, said first insulated gate field-effect transistor being connected between the internal reference node and the second power supply conductor, the second insulated gate field-effect transistor being connected between the first power supply conductor and the internal reference node, the gate electrode of the second insulated gate field-effect transistor being connected to the first power supply conductor, the third insulated gate field-effect transistor having its gate and drain electrodes connected to the internal reference node and having its source electrode connected to the gate of first insulated gate field-effect transistor, the fourth insulated gate field-effect transistor having its gate and drain electrodes connected to the gate electrode of first insulated gate field-effect transistor and its source electrode connected to the second power supply conductor.

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