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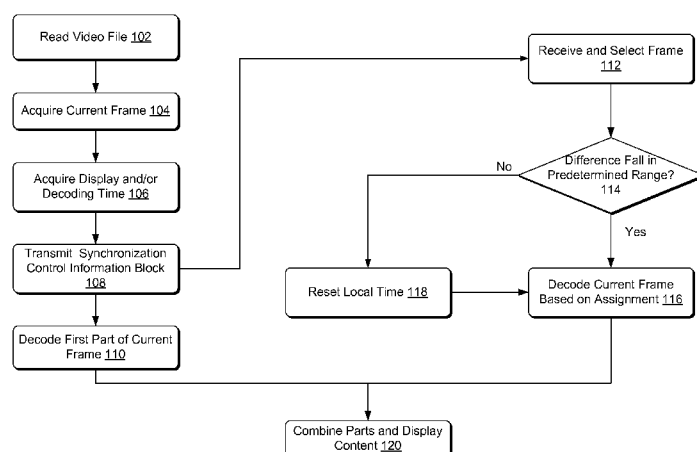
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[US/—]; Fourth Floor, One Capital Place, P.O. Box 847,
Grand Cayman (KY).(72) Inventor: **WANG, Guonai**; C/o Alibaba Group Holding
Limited, 5/f, Building 3, No.969 West Wen Yi Road, Yu
Hang District, Hangzhou, 311121 (CN).(74) Agents: **LEE, Lewis, C.** et al.; Lee & Hayes, PLLC, 601
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(54) Title: VIDEO CHANNEL DISPLAY METHOD AND APPARATUS

**FIG. 1**(57) **Abstract:** Methods for video display using a computing system. The computing system includes a main computing module and an ancillary computing module. The main computing module may transmit a synchronization control information block to the ancillary computing module. The synchronization control information block includes a frame number of a current frame and the reference time associated with the main computing module. The ancillary computing module receives the synchronization control information block and selects a frame pack having the same frame number contained in the synchronization control information block as the current frame. The ancillary computing module may obtain the reference time of the current frame based on a local time of the ancillary computing module. The main computing module and the ancillary computing module may decode one or more parts of the frame, respectively. Further, the decoded parts of the frame may be combined and displayed.

Video Channel Display Method and Apparatus

CROSS REFERENCE TO RELATED PATENT APPLICATIONS

This disclosure claims priority to Chinese Patent Application No.
5 201410302686.X, filed on June 27, 2014, entitled "Video Channel Display Method
And Apparatus," which is hereby incorporated by reference in its entirety.

TECHNICAL FIELD

The present disclosure relates to computer video display technology, and
10 more specifically to methods and systems for video display.

BACKGROUND

Current high definition (HD) display devices may display video contents in a
resolution of 1920 * 1080 pixels (2K * 1K or full HD). With the development of
15 information technology, various higher resolutions, such as 6K or 8K, are available for
video contents.

Existing displaying devices may not be able to play video contents in
resolutions higher (6K or 8K) than 2K * 1K. Under conventional techniques, such
video contents in higher resolutions may be converted to lower resolutions (e.g.,
20 1920 * 1080 pixels). However, not only is the conversion process too computationally
expensive but also may cause converted videos to become distorted and blur.

Accordingly, problems for displaying video contents in resolutions higher than
full HD need to be addressed.

25

SUMMARY

Implementations of the present disclosure solve problems associated with
conventional techniques, such as failures for displaying videos in higher resolutions
than full HD, distorted images, and/or blur images. This Summary is not intended to

identify all key features or essential features of the claimed subject matter, nor is it intended to be used alone as an aid in determining the scope of the claimed subject matter.

5 The implementations of the present disclosure relate to methods for video display. In implementations, a main computing module and one or more ancillary computing module read a video file, for example at substantially the same time. The main computing module may retrieve a current frame of a frame stream of the video file and read a display time and/or a decoding time of the current frame based on a frame number of the current frame and a local time of the main computing module.

10 The main computing module may transmit to the one or more ancillary computing module a synchronization control information block containing the frame number of the current frame and the display time and/or the decoding time associated with the main computing module. The main computing module decodes a first part of the current frame. The ancillary computing module receives the synchronization control

15 information block and selects a frame pack having the same frame number contained in the synchronization control information block as the current frame. Further, the ancillary computing module reads the display time and/or decoding time of the current frame on the ancillary computing module based on a local time of the ancillary computing module, and decodes a Nth part of the current frame based on a

20 predetermined assignment. The decoded parts of the current frame from the ancillary computing module and decoded parts of the current frame from the main computing module may be combined to form a decoded content of the current frame. A displaying device may then display the decoded content.

In implementations, the one or more ancillary computing modules may

25 include an ancillary computing module. The main computing module may decode an upper half or lower half of the current frame. Accordingly, the ancillary computing module may decode a lower half or upper half of the current frame. In some instances, the main computing module may decode a right half or left half of the

current frame, while the ancillary computing module may decode a left half or right half of the current frame.

5 In implementations, the ancillary computing module reads the display time and/or decoding time of the current frame on the ancillary computing module based on a local time of the ancillary computing module. The ancillary computing module may calculate a difference between the display time and/or decoding time of the ancillary computing module and the display time and/or decoding time of the synchronization control information block, and further determine whether the difference falls in a predetermined threshold range. If the difference falls in a
10 predetermined threshold range, the ancillary computing module decodes a N^{th} part of the current frame based on a predetermined assignment. If the difference does not fall in a predetermined threshold range, the ancillary computing module resets the local time of the ancillary computing module based on the display time and/or decoding time contained in the synchronization control information block. Further
15 the ancillary computing module decodes the N^{th} part of the current frame based on a predetermined assignment.

In implementations, the ancillary computing module may reset the local time of the ancillary computing module based on the display time and/or decoding time contained in the synchronization control information block. The ancillary computing
20 module may designate the display time contained in the synchronization control information block as a display time of the ancillary computing module, and may designate the decoding time contained in the synchronization control information block as the decoding time of the ancillary computing module.

In implementations, the predetermined threshold range is a time period of
25 persistence of vision of a human eye. The decoding may be implemented by calling ffmpeg decoding and display functions. In some implementations, the main computing module and the ancillary computing module communicates using local

area network (LAN), Internet or data bus, Wi-Fi, or Bluetooth to transmit the synchronization control information block.

In implementations, the synchronization control information block is implemented using a data block defined by a function. The data block includes the
5 frame number, and the display time and/or deciding time.

The implementations of the present disclosure relate to systems for video display. A system for video display may include a main computing module and one or more ancillary computing module. The main computing module may include an acquiring module configured to retrieve a current frame of a frame stream of the
10 video file, and a reading module configured to read the display time and/or decoding time of the current frame on the ancillary computing module based on a local time of the ancillary computing module. The main computing module may further include a transmitting module configured to transmit to the one or more ancillary computing module a synchronization control information block containing the frame number
15 and the display time and/or the decoding time, and a first decoding module configured to decode a first part of the current frame.

The ancillary computing module may include a receiving module configured to receive the synchronization control information block and select a frame pack having the same frame number contained in the synchronization control information block
20 as the current frame, and a reading module configured to obtain the display time and/or decoding time of the current frame on the ancillary computing module based on a local time of the ancillary computing module. The ancillary computing module may further include a N^{th} decoding module configured to the ancillary computing module that decodes a Nth part of the current frame based on a predetermined
25 assignment, and a displaying module configured to combine decoded parts of the current frame from the ancillary computing module and decoded parts of the current frame from the main computing module to form a decoded content of the current frame, and to display the decoded content.

In implementations, the first decoding module may decode an upper half or lower half of the current frame. Accordingly, a N^{th} decoding module may decode a lower half or upper half of the current frame. In implementations, the first decoding module may decode a right half or left half of the current frame. Accordingly, the N^{th} decoding module may decode a left half or right half of the current frame.

In implementations, the ancillary computing module may include a determining module configured to obtain the display time and/or decoding time of the current frame on the ancillary computing module based on a local time of the ancillary computing module. The determining module may further calculate a difference between the display time and/or decoding time of the ancillary computing module and the display time and/or decoding time of the synchronization control information block, and determine whether the difference falls in a predetermined threshold range.

If the difference falls in the predetermined threshold range, the ancillary computing module may transmit a decoding signal to the N^{th} decoding module. If the difference does not fall in the predetermined threshold range, the ancillary computing module may transmit a resetting signal to a resetting module. The resetting module may be configured to reset the local time of the ancillary computing module based on the display time and/or decoding time contained in the synchronization control information block. The N^{th} decoding module decodes the N^{th} part of the current frame based on a predetermined assignment.

In implementations, the resetting module may be configured to designate the display time contained in the synchronization control information block as a display time of the ancillary computing module, and to designate the decoding time contained in the synchronization control information block as the decoding time of the ancillary computing module.

In implementations, the predetermined threshold range is a time period of persistence of vision of a human eye. The decoding between the first decoding

module and the Nth decoding module may be implemented by calling ffmpeg decoding and display functions.

Compared with conventional techniques, one aspect of the present disclosure has the following advantages. The main computing module and the ancillary
5 computing module read the same video frame stream, and the main computing module decodes the first part of the current frame. The main computing module transmits to the one or more ancillary computing module a synchronization control information block containing the frame number of the current frame and the display time and/or the decoding time associated with the main computing module. The
10 ancillary computing module receives the synchronization control information block and selects a frame pack having the same frame number contained in the synchronization control information block as the current frame. The ancillary computing module decodes a Nth part of the current frame based on a predetermined assignment. The decoded parts of the current frame from the
15 ancillary computing module and decoded parts of the current frame from the main computing module may be combined to form a decoded content of the current frame, which is displayed. This enables the display video files in higher resolution than full HD.

The implementations herein also generate a predetermined assignment to
20 assign the decoding of the video frame stream to the main computing module and the ancillary computing module. Based on the assignment, the main computing module and the ancillary computing module decode various parts of the video frame stream accordingly. The decoded parts of the current frame from the ancillary computing module and decoded parts of the current frame from the main computing
25 module may be combined to form a decoded content of the current frame, which is displayed. After using this method, when a video file is a high resolution video file, a decoding process will not be restricted to the computing power of decoding devices.

Therefore, this avoids distorted images or blurred images for displaying high resolution video files due to limited computing power.

BRIEF DESCRIPTION OF THE DRAWINGS

5 The Detailed Description is described with reference to the accompanying figures. The use of the same reference numbers in different figures indicates similar or identical items.

FIG. 1 is a flow chart of an illustrative process for displaying a video file.

10 FIG. 2 is schematic diagram of an illustrative computing architecture that enables displaying a video file.

DETAILED DESCRIPTION

15 The present disclosure may be implemented in many ways other than those described herein, and those skilled in the art may make similar promotion without departing from the present disclosure. Therefore, the present disclosure is not limited to the particular implementation described below.

FIG. 1 is a flow chart of an illustrative process for displaying a video file. FIG. 1 illustrates operations of a main computing module and one or more ancillary computing modules.

20 At 102, a main computing module and an ancillary computing module read and process a video file. The main computing module and the ancillary computing module read a video file, which may be obtained from a local hard drive associated with the main computing module or the ancillary computing module. In implementations, the video file may be obtained via a connection node of a network,
25 from an Internet server, or directly from a device that captures information and generates the video file.

In implementations, the main computing module may be a local computing device, and the ancillary computing module may be at least one computing unit of a

distributed computing network associated with the main computing module. In implementations, the ancillary computing module may a local computing device, and the main computing module may be at least one computing unit of a distributed computing network associated with the main unit. In implementations, the main
5 computing module and ancillary computing module may be computing units of a distributed computing network. The number of the ancillary computing modules may change based on demands. Accordingly, the ancillary computing module is not limited to completing corresponding calculation process on the local computing device. The ancillary computing modules may include multiple ancillary computing
10 modules.

In implementations, two computing units: the main computing module and the ancillary computing module, may have a dynamic relationship. For example, when there are multiple computing units, one computing unit may be determined as the main computing module and the rest of the multiple computing units may be
15 considered as ancillary computing modules. The main computing module and the ancillary computing module may communicate using LAN, Internet or data bus, Wi-Fi, Bluetooth to transmit the synchronization control information block.

At 104, the main computing module may retrieve and acquire a current frame of a frame stream of the video file. For example, this operation may be
20 implementation by calling an opencv function. The main computing module may adopt a cvQueryFrame function to retrieve the current frame of the video frame stream of the video file. It is appreciated that retrieving the current frame of the video stream can be implemented using other methods.

At 106, the main computing module may read and acquire a display time
25 and/or a decoding time of the current frame based on a frame number of the current frame and a local time of the main computing module. In implementations, the main computing module may obtain a display time and/or a decoding time of the current

frame based on a frame number of the current frame and a local time of the main computing module.

5 The main computing module reads a display time (e.g., presentation time stamp (PTS)) and/or a decoding time (e.g., decoding time stamp (DTS)) of the current frame based on a local time of the main computing module. The display time indicates a time when a frame pack is transmitted to a displaying device for display. The decoding time indicates a time when a frame pack is transmitted to a computing unit for decoding. A display order may be determined based on the display time and the decoding time. The display time and decoding time are generally consistent
10 while being different in certain conditions.

In implementations, the main computing module and the ancillary computing module may be synchronized based on the decoding time and/or the display time. In implementations, the decoding time and display time may be used to avoid a situation that the main computing module and the ancillary computing module are
15 not synchronized.

At 108, the main computing module transmits to the one or more ancillary computing module a synchronization control information block containing the frame number and the display time and/or the decoding time. The main computing module may define a data structure type, which may be in the form of data blocks. In
20 implementations, the main computing module transmit to the ancillary computing module the frame number and the display time and/or the decoding time, which may be defined as a synchronization control information block. Such a definition may be implemented using a struct function. The main computing module may transmit the synchronization control information block to the ancillary computing module for
25 storage.

For example, the synchronization control information block may be defined as follow:

```
struct syncMsg {
```

```
        Long PTS; // display time
        Long DTS; // decoding time
        Int FrameNo; // frame number
    }
```

5 wherein, the data block includes the frame number, and the display time and/or decoding time.

At 110, the main computing module may decode the first part of the current frame to decode an upper half or lower half of the current frame or decode a right half or left half of the current frame. For example, this operation may be
10 implemented by calling ffmpeg decoding and display functions.

At 112, the ancillary computing module may receive the synchronization control information block and may select a frame pack having the same frame number contained in the synchronization control information block as the current frame. In implementations, the ancillary computing module and the main computing
15 module may obtain the same video frame stream, and may receive the synchronization control information block from the main computing module. For example, the ancillary computing module receives the synchronization control information block and selects a frame pack having the same frame number contained in the synchronization control information block as the current frame. The main
20 computing module and the ancillary computing module may decode the content of the same frame.

In implementations, the ancillary computing module may read the display time and/or decoding time of the current frame on the ancillary computing module based on a local time of the ancillary computing module. The ancillary computing
25 module may calculate a difference between the display time and/or decoding time of the ancillary computing module and the display time and/or decoding time of the synchronization control information block, and determine whether the difference falls in a predetermined threshold range. In some implementations, local times of

the main computing module and the ancillary computing module are the same since the local times may be synchronized over the network, and therefore errors between the local times can be ignored.

5 In implementations, the ancillary computing module reads a display time (e.g., presentation time stamp (PTS)) and/or a decoding time (e.g., decoding time stamp (DTS)) of the current frame based on a local time of the ancillary computing module.

10 The ancillary computing module may calculate a difference between the display time and/or decoding time of the ancillary computing module and the display time and/or decoding time of the synchronization control information block, and determine whether the difference falls in a predetermined threshold range at 114.

If the difference falls in the predetermined threshold range, the ancillary computing module may decode the current frame based on the assignment at 116. For example, the predetermined threshold range may be a time period of persistence of vision of a human eye (e.g., 100 to 400 milliseconds) such as 200 milliseconds.

15 In implementations, the ancillary computing module decodes a N^{th} part of the current frame based on a predetermined assignment. The N^{th} part of the current frame corresponds to the first part of the current frame decoded by the main computing module.

20 In implementations, if the first part of the current frame decoded by the main computing module is the upper half of the current frame, then the N^{th} part of the current frame decoded by the ancillary computing module is the lower half of the current frame, and vice versa. If the first part of the current frame decoded by the main computing module is the left half of the current frame, then the N^{th} part of the current frame decoded by the ancillary computing module is the right half of the
25 current frame, and vice versa.

It should be noted that, when there are multiple computing units, one or more main computing modules and one or more ancillary computing modules are

correlated. For example, the decoding between the first decoding module and the N^{th} decoding module may be implemented by calling a ffmpeg decoding function.

If the difference of the display times and/or decoding times of the main computing module and the ancillary computing module is greater than a predetermined threshold range (e.g., human visual persistence value within 200 milliseconds), the ancillary computing module may reset the local time of the ancillary computing module based on the display time and/or decoding time contained in the synchronization control information block at 118. The resetting process may enable the ancillary computing module to decode the current frame based on a local time of the ancillary computing module without frequently changing a pace of the ancillary computing module. Also, the resetting process may correct the local time of the ancillary computing module when the difference of video content is beyond the scope that human eyes can perceive with respect to a normal view.

In implementations, the ancillary computing module may decode a N^{th} part of the current frame based on a predetermined assignment. The ancillary computing module may designate the display time contained in the synchronization control information block as a display time of the ancillary computing module, and designate the decoding time contained in the synchronization control information block as the decoding time of the ancillary computing module. This will make consistent between the display time and/or decoding time of the ancillary computing module and the display time and decoding time contained in the synchronization control information block. Further, the decoding of the N^{th} part of the current frame may be implemented by calling a ffmpeg decoding function.

At 120 a displaying module may combine decoded parts of the current frame from the ancillary computing module and decoded parts of the current frame from the main computing module to form a decoded content of the current frame, which may be displayed. For example, the main computing module may transmit the first

part of decoded content to a buffer zone of the displaying module, and the ancillary computing module may also transmit the N^{th} part of the decoded content to the buffer zone. The displaying module may combine the decoded content in the buffer zone and display the combined decoded content.

5 In implementations, the main computing module may decode the first part of the current frame and then the displaying module may display the decoded first part. The ancillary computing module may decode the N^{th} part of the current frame and then the displaying module may display the decoded N^{th} part.

10 The implementations of the present disclosure relate to methods for video display. The main computing module and the ancillary computing module read the same video frame stream. Based on the assignment, the main computing module and the ancillary computing module decode various parts of the video frame stream respectively. The decoded parts of the current frame from the ancillary computing module and decoded parts of the current frame from the main computing module
15 may be combined to form a decoded content of the current frame, and to display the decoded content. The implementations herein can avoid image distortion and image blurring due to excessive decoding computation that is beyond computing capacities.

20 In above described implementations, the main computing module and the ancillary computing module may correspond to two network nodes that are in long distance. Therefore, implementations can call on the network to achieve full computing power, in particular the use of cloud computing approach for high definition video display. The implementations may determine a difference between the display time and/or decoding time of the ancillary computing module and the display time and/or decoding time of the synchronization control information block,
25 and determine whether the difference falls in a predetermined threshold range. The decoding time and the display time may be reset if the difference is greater than the predetermined threshold range. The above determination may avoid a long interval due to different display times generated by the main computing module and the

ancillary computing module when the ancillary computing module and the ancillary computing module decode different parts of the same frame respectively. In some implementations, the resetting process may be removed.

FIG. 2 is a schematic diagram of an illustrative computing architecture that enables displaying a video file. FIG. 2 is a diagram of a computing system 200. The computing system 200 may be one or more user devices or one or more servers for video display, a combination thereof. In one exemplary configuration, the computing system 200 includes one or more processors 202, input/output interfaces 204, network interface 206, and memory 208.

The memory 208 may include computer-readable media in the form of volatile memory, such as random-access memory (RAM) and/or non-volatile memory, such as read only memory (ROM) or flash RAM. The memory 208 is an example of computer-readable media.

Computer-readable media includes volatile and non-volatile, removable and non-removable media implemented in any method or technology for storage of information such as computer readable instructions, data structures, program modules, or other data. Examples of computer storage media include, but are not limited to, phase change memory (PRAM), static random-access memory (SRAM), dynamic random-access memory (DRAM), other types of random-access memory (RAM), read-only memory (ROM), electrically erasable programmable read-only memory (EEPROM), flash memory or other memory technology, compact disk read-only memory (CD-ROM), digital versatile disks (DVD) or other optical storage, magnetic cassettes, magnetic tape, magnetic disk storage or other magnetic storage devices, or any other non-transmission medium that may be used to store information for access by a computing device. As defined herein, computer-readable media does not include transitory media such as modulated data signals and carrier waves.

Turning to the memory 208 in more detail, the memory 208 may include a main computing module 210, an ancillary computing module 220, and a displaying module 230. The main computing module 210 may include various components such as an acquiring module 212, a reading module 214, a transmitting module 216, and a first part decoding module 218. The ancillary computing module 220 may include various components such as a receiving module 222, a determining module 224, a resetting module 226, and a Nth part decoding module 228.

The main computing module 210 and the ancillary computing module 220 may read the same video file. The acquiring module 212 may retrieve a current frame of a frame stream of the video file, and the reading module 214 may reads the display time and/or decoding time of the current frame on the ancillary computing module based on a local time of the main computing module. The transmitting module 216 may transmit to the ancillary computing module 218 a synchronization control information block containing the frame number and the display time and/or the decoding time, and the first part decoding module 218 may decode the first part of the current frame.

In implementations, the first part decoding module 218 decodes the first part of the current frame to decode an upper half or lower half of the current frame, or decode a right half or left half of the current frame.

The receiving module 222 may receive the synchronization control information block and select a frame pack having the same frame number contained in the synchronization control information block as the current frame. The determining module 224 may obtain the display time and/or decoding time of the current frame on the ancillary computing module based on a local time of the ancillary computing module, and calculate a difference between the display time and/or decoding time of the ancillary computing module and the display time and/or decoding time of the synchronization control information block. The determining module 224 may further determine whether the difference falls in a predetermined threshold range.

If the difference does not fall in a predetermined threshold range, the determining module 224 may transmit a resetting signal to the resetting module 226. If the difference falls in a predetermined threshold range, the determining module 224 may transmit a decoding signal to the N^{th} part decoding module 228.

5 The resetting module 226 may reset the local time of the ancillary computing module based on the display time and/or decoding time contained in the synchronization control information block, and then transmit a decode signal to the N^{th} part decoding module 228. The N^{th} part decoding module 228 may decode a N^{th} part of the current frame based on a predetermined assignment. The resetting
10 module 226 may designate the display time contained in the synchronization control information block as a display time of the ancillary computing module 220, and designate the decoding time contained in the synchronization control information block as the decoding time of the ancillary computing module 220.

 The N^{th} part decoding module 228 may decode a N^{th} part of the current frame
15 based on a predetermined assignment to decode a N^{th} part of the current frame based on a predetermined assignment. The decoding of the N^{th} part decoding module 228 may correspond to the lower part or the upper part of the current frame decoded by the first part decoding module 218. In implementations, the N^{th} part decoding module 228 may decode a left half or right half of the current frame.

20 The displaying module 230 may combine decoded parts of the current frame from the ancillary computing module and decoded parts of the current frame from the main computing module to form a decoded content of the current frame, which may be displayed on a displaying device.

 The embodiments are merely for illustrating the present disclosure and are
25 not intended to limit the scope of the present disclosure. It should be understood for persons in the technical field that certain modifications and improvements may be made and should be considered under the protection of the present disclosure without departing from the principles of the present disclosure.

CLAIMS

What is claimed is:

1. A computer-implemented method for video display, the method comprising:
reading, by one or more processors associated with a computing system
5 including a main computing module and an ancillary computing module, a video file;
retrieving, by the one or more processors, a current frame of the video file on
the main computing module;
obtaining, by the one or more processors, a reference time of the current
frame based on a frame number of the current frame and a local time of the main
10 computing module, the reference time including a display time or a decoding time
associated with the main computing module, or a combination thereof;
transmitting, by the one or more processors and from the main computing
module to the ancillary computing module, a synchronization control information
block containing the frame number of the current frame and the reference time
15 associated with the main computing module;
decoding, by the one or more processors, a first part of the current frame on
the main computing module;
selecting, by the one or more processors, a frame pack having the frame
number contained in the synchronization control information block as the current
20 frame that is processed on the ancillary computing module;
obtaining, by the one or more processors, the reference time of the current
frame based on a local time of the ancillary computing module;
decoding, by the one or more processors, a Nth part of the current frame on
the ancillary computing module based on a predetermined assignment, N being
25 integer and greater than one;
combining, by the one or more processors, decoded parts of the current
frame from the ancillary computing module and decoded parts of the current frame

from the main computing module to form a decoded content of the current frame;
and

displaying, by the one or more processors, the decoded content.

5 2. The method of claim 1, wherein the decoding the first part of the current frame comprises decoding an upper half of the current frame, and the decoding the N^{th} part of the current frame comprises decoding a lower half of the current frame, or wherein the decoding the first part of the current frame comprises decoding a right half of the current frame, and the decoding the N^{th} part of the current frame
10 comprises decoding a left half of the current frame.

3. The method of claim 1, wherein the obtaining the reference time from the current frame based on the local time of the ancillary computing module and the decoding the N^{th} part of the frame comprise:

15 calculating a difference between a reference time of the ancillary computing module and the reference time contained in the synchronization control information block;

 determining whether the difference falls in a predetermined threshold range;

 in response to a determination that the difference falls in the predetermined
20 threshold range, decoding the N^{th} part of the current frame based on the predetermined assignment; and

 in response to a determination that the difference does not fall in the predetermined threshold range:

 resetting the local time of the ancillary computing module based on the
25 reference time contained in the synchronization control information block,
and

 decoding the N^{th} part of the current frame.

4. The method of claim 3, wherein the resetting the local time of the ancillary computing module based on the reference time contained in the synchronization control information block comprises:

- designating the display time contained in the synchronization control
5 information block as a display time of the ancillary computing module; and
designating the decoding time contained in the synchronization control
information block as the decoding time of the ancillary computing module.

5. The method of claim 3, wherein the predetermined threshold range is a
10 time period of persistence of vision of a human eye.

6. The method of claim 1, further comprising:
calling a ffmpeg decoding and display function.

15 7. The method of claim 1, wherein the main computing module and the
ancillary computing module communicates using local area network (LAN), Internet
or data bus, Wi-Fi, or Bluetooth to transmit the synchronization control information
block.

20 8. The method of claim 1, wherein the synchronization control information
block is implemented using a data block defined by a function, and wherein the data
block includes the frame number of the current frame and the reference time
associated with the main computing module.

25 9. A system comprising:
one or more processors; and
memory to maintain a plurality of components executable by the one or more
processors, the plurality of components comprising:

a main computing module configured to read a video file, and
an ancillary computing module configured to read the video file, wherein the
main computing module comprises:

an acquiring module configured to retrieve a current frame of the video
5 file,

a reading module configured to obtain a reference time of the current
frame based on a local time of the main computing module, the reference
time including a display time or a decoding time associated with the main
computing module, or a combination thereof,

10 a transmitting module configured to transmit from the main computing
module to the ancillary computing module a synchronization control
information block containing a frame number of the current frame and the
reference time associated with the main computing module, and

a first decoding module configured to decode a first part of the current
15 frame, and

the ancillary computing module comprises:

a receiving module configured to:

receive the synchronization control information block, and

select a frame pack having the frame number contained in the
20 synchronization control information block as the current frame for the
ancillary computing module,

a reading module configured to read the reference time of the current
frame based on a local time of the ancillary computing module,

25 a N^{th} decoding module configured to decode a N^{th} part of the current
frame based on a predetermined assignment, N being integer and greater
than one, and

a displaying module configured to:

combine decoded parts of the current frame from the ancillary computing module and decoded parts of the current frame from the main computing module to form a decoded content of the current frame, and

5 display the decoded content.

10. The system of claim 9, wherein the decoding the first part of the current frame comprises decoding an upper half of the current frame, and the decoding the Nth part of the current frame comprises decoding a lower half of the current frame,
10 or wherein the decoding the first part of the current frame comprises decoding a right half of the current frame, and the decoding the Nth part of the current frame comprises decoding a left half of the current frame.

11. The system of claim 9, wherein the obtaining the reference time from the
15 current frame based on the local time of the ancillary computing module and the decoding the Nth part of the frame comprise:

calculating a difference between a reference time of the ancillary computing module and the reference time contained the synchronization control information block;

20 determining whether the difference falls in a predetermined threshold range;

in response to a determination that the difference falls in the predetermined threshold range, decoding the Nth part of the current frame based on the predetermined assignment; and

25 in response to a determination that the difference does not fall in the predetermined threshold range:

resetting the local time of the ancillary computing module based on the reference time contained in the synchronization control information block, and

decoding the Nth part of the current frame.

12. The system of claim 11, wherein the resetting the local time of the ancillary computing module based on the reference time contained in the synchronization control information block comprises:

designating the display time contained in the synchronization control information block as a display time of the ancillary computing module; and

designating the decoding time contained in the synchronization control information block as the decoding time of the ancillary computing module.

13. The system of claim 11, wherein the predetermined threshold range is a time period of persistence of vision of a human eye.

14. The system of claim 9, wherein the ancillary computing module is further configured to call a ffmpeg decoding and display function.

15. One or more computer-readable media storing computer-executable instructions that, when executed by one or more processors associated with a computing system including a main computing module and an ancillary computing module, instruct the one or more processors to perform acts comprising:

reading a video file on the main computing module and the ancillary computing module;

retrieving a current frame of the video file;

obtaining a reference time of the frame based on a frame number of the current frame and a local time of the main computing module, the reference time including a display time or a decoding time associated with the main computing module, or a combination thereof;

transmitting from the main computing module to the ancillary computing module a synchronization control information block containing the frame number and the reference time;

decoding a first part of the current frame on the main computing module;

5 selecting a frame pack having the frame number contained in the synchronization control information block as the current frame on the ancillary computing module;

obtaining the reference time of the current frame based on a local time of the ancillary computing module;

10 decoding a N^{th} part of the current frame based on a predetermined assignment on the ancillary computing module, N being integer and greater than one;

combining decoded parts of the current frame from the ancillary computing module and decoded parts of the current frame from the main computing module to form a decoded content of the current frame; and

15 displaying the decoded content.

16. The one or more computer-readable media claim 15, wherein the decoding the first part of the current frame comprises decoding an upper half of the current frame, and the decoding the N^{th} part of the current frame comprises
20 decoding a lower half of the current frame, or wherein the decoding the first part of the current frame comprises decoding a right half of the current frame, and the decoding the N^{th} part of the current frame comprises decoding a left half of the current frame.

25 17. The one or more computer-readable media claim 15, wherein the obtaining the reference time of the current frame based on the local time of the ancillary computing module and the decoding the N^{th} part of the frame comprise:

calculating a difference between the reference time of the ancillary computing module and the reference time contained in the synchronization control information block;

determining whether the difference falls in a predetermined threshold range;

5 in response to a determination that the difference falls in the predetermined threshold range, decoding the N^{th} part of the current frame based on the predetermined assignment; and

in response to a determination that the difference does not fall in the predetermined threshold range:

10 resetting the local time of the ancillary computing module based on the reference time contained in the synchronization control information block, and
decoding the N^{th} part of the current frame.

15 18. The one or more computer-readable media claim 17, wherein the resetting the local time of the ancillary computing module based on the reference time contained in the synchronization control information block comprises:

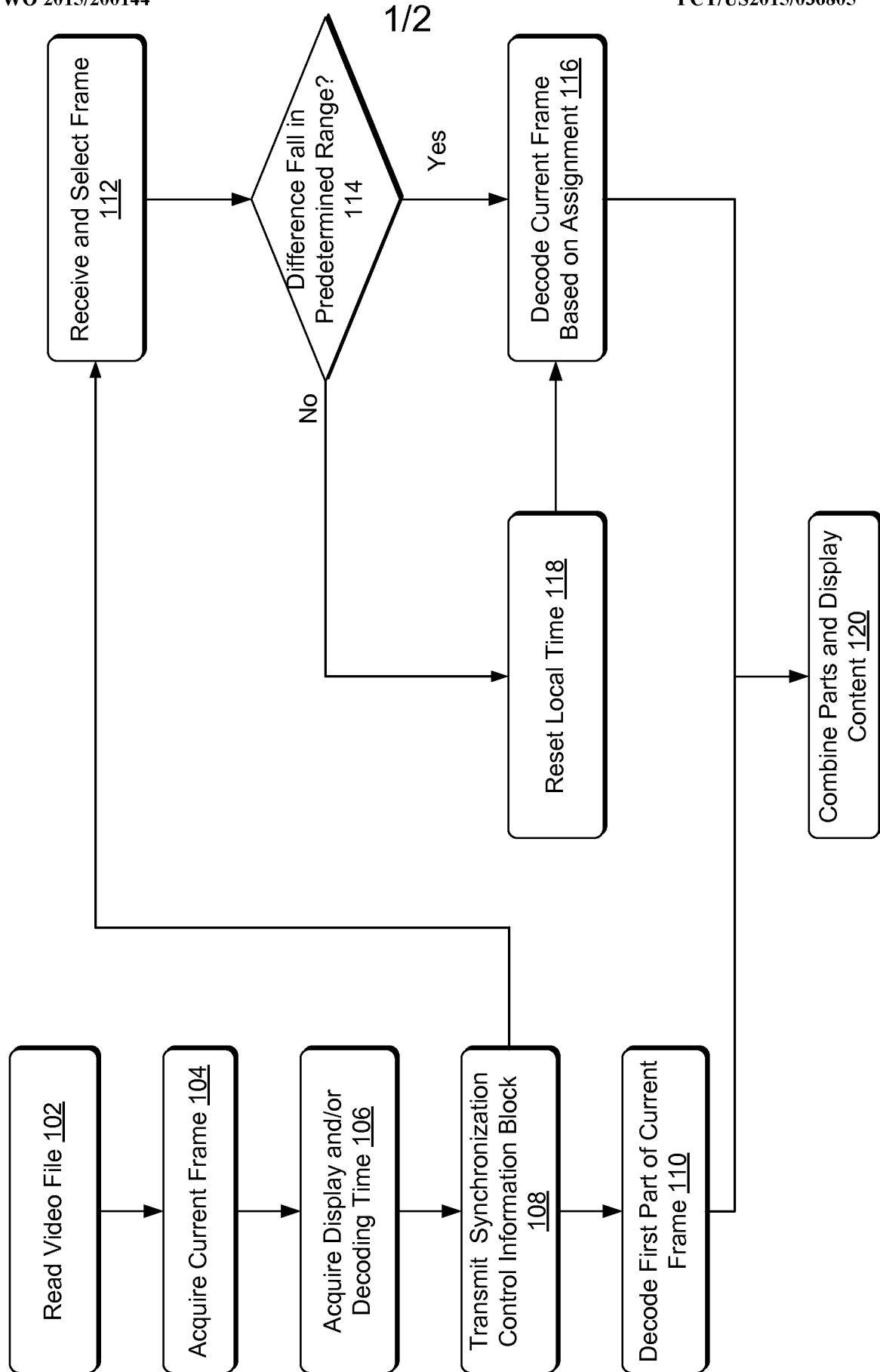
designating the display time contained in the synchronization control information block as a display time of the ancillary computing module; and

20 designating the decoding time contained in the synchronization control information block as the decoding time of the ancillary computing module.

19. The one or more computer-readable media claim 17, wherein the predetermined threshold range is a time period of persistence of vision of a human
25 eye.

20. The one or more computer-readable media claim 17, wherein the acts further comprise:

calling a ffmpeg decoding and display function.

**FIG. 1**

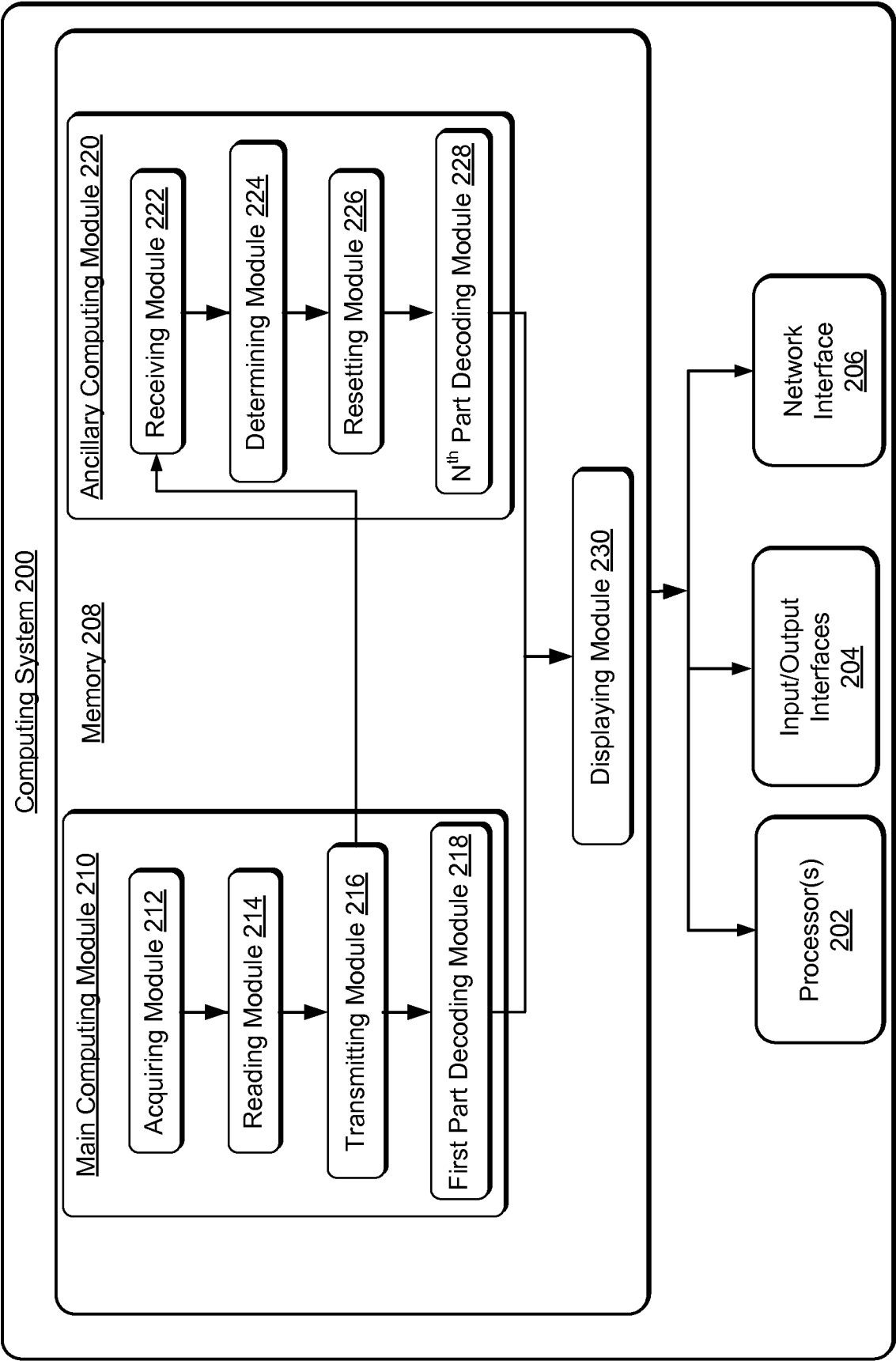


FIG. 2

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US15/36805

A. CLASSIFICATION OF SUBJECT MATTER

IPC(8) - H04B 1/708 (2015.01)

CPC - H04B 1/708

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC(8): H04B 1/708, H04B 1/7073; H04N 7/26 (2015.01)

CPC: H04B 1/708, H04B 1/7073; H04N 7/56, 19/86

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

PatSeer (US, EP, WO, JP, DE, GB, CN, FR, KR, ES, AU, IN, CA, INPADOC Data) IP.com; IEEE; Google/Google Scholar

Keywords: video, reference time, decode, frame, parallel, mpeg, upper, left, synchronize

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2008/0298473 A1 (GOU, D) 04 December 2008; paragraphs [0015], [0032], [0037].	1-20
A	US 2012/0170648 A1 (CHEN, Y et al.) 05 July 2012; entire document.	1-20
A	WO 2008/028013 A2 (ATI TECHNOLOGIES, INC) 06 March 2008; entire document.	1-20
A	US 2001/0038642 A1 (ALVAREZ II, M et. al.) 08 November 2001; entire document.	1-20

☐ Further documents are listed in the continuation of Box C.☐ See patent family annex.

* Special categories of cited documents:

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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

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03 September 2015 (03.09.2015)

Date of mailing of the international search report

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Mail Stop PCT, Attn: ISA/US, Commissioner for Patents
P.O. Box 1450, Alexandria, Virginia 22313-1450

Facsimile No. 571-273-8300

Authorized officer

Shane Thomas

PCT Helpdesk: 571-272-4300
PCT OSP: 571-272-7774