

[54] **FEATURE COUNTER WITH IMPROVED MASKING AND GREY LEVEL DETECTION**

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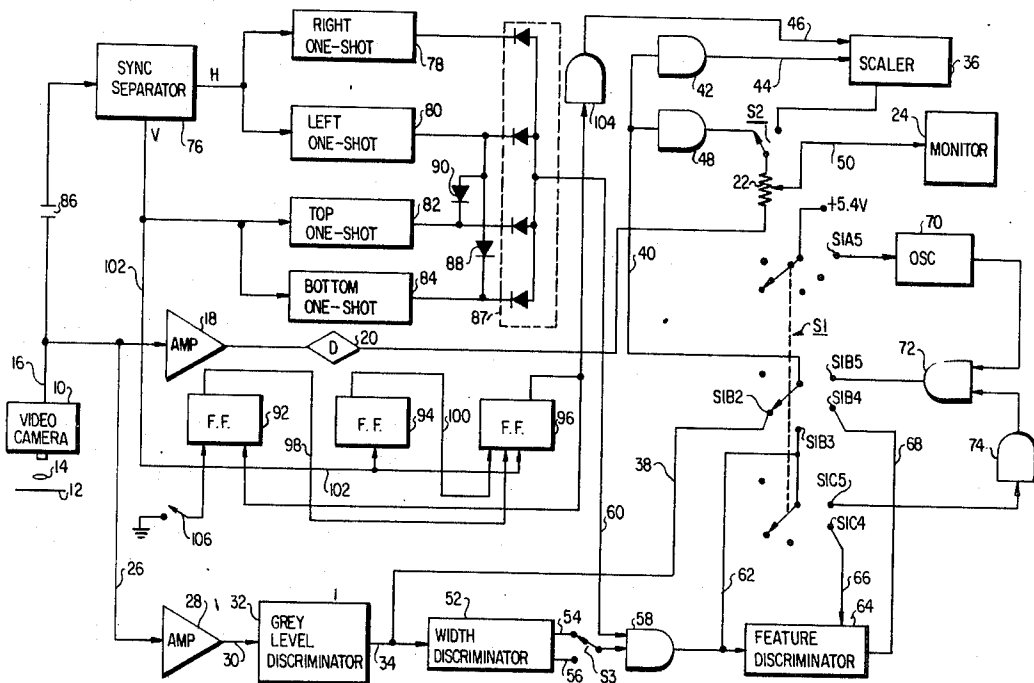
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[57] **ABSTRACT**

A specimen analyzer including a video camera for scanning a specimen and selectively counting features thereof on the basis of grey level and/or size. The device may operate in several modes to count only features darker (or lighter) than the selected grey level, to count only features that are darker than a first grey level but lighter than a second grey level, to count only features wider than a selected width, to count only features wider than a first width but not as wide as a second width, or to count features that meet more than one of these tests. A variable electronic mask permits the operator to select any area of the specimen within the view of the camera for features analysis without moving the specimen. Check spot pulses are generated for each featured counted and these may be displayed on a video monitor superimposed on a video display of the specimen. Provision is made for background compensation when counting features against the background that varies considerably in grey level. Further provision is made for cycling the specimen analyzer through a single cycle, corresponding to the field scan time of the video camera, each time a start button is depressed.

10 Claims, 3 Drawing Figures



FEATURE COUNTER WITH IMPROVED MASKING AND GREY LEVEL DETECTION

RELATED APPLICATIONS

This application is a continuation-in-part of our copending applications Ser. No. U.S. 767,614 filed Oct. 15, 1968, now U.S. PAT. NO. 3,578,904 and Ser. No. 848,474 filed Aug. 8, 1969, now U.S. Pat. No. 3,579,249.

BACKGROUND OF THE INVENTION

Copending application Ser. No. 848,474 (hereinafter referred to as application A) discloses a specimen analyzer for counting features on the surfaces of real objects or in photographs and microscope images. A video camera scans the specimen and produces a video output signal which, at any instant represents the intensity of grey level of that part of the specimen being scanned. Scanning takes place in a manner analogous commercial television, that is, a series of horizontal scans in each of two fields in a frame, the horizontal scans of one field being interlaced with the scans of the preceding field.

The video output from the camera is continuously applied to a video monitor so as to provide display of the specimen being scanned by the camera. The video output from the camera is also applied to a manually adjustable grey level discriminator circuit. The grey level discriminator tests the video signal from the camera to determine if it represents a grey level falling within a particular selected range of grey, and produces a binary type output signal as long as the test is met. The output signal may be applied to the monitor so that the features of the specimen meeting the grey level test will appear "filled" or whiter than those features that did not meet the test.

In some applications of the specimen analyzer, the grey level discriminator may make a direct voltage comparison between reference voltages and the video signal to determine if a grey level test is met. This is, in effect, a direct comparison of the intensity of the specimen with the reference voltage and does not take into account the fact that the background of the features being analyzed may vary greatly. Thus, application A included a background compensation circuit for preventing a background which varied in intensity from being erroneously interpreted as a feature.

The background compensation circuit of application A was designed for use in a specimen analyzer for analyzing specimens containing small features. It was found that when the background compensation circuit was employed in analyzing a specimen containing larger features, the output of the grey level discriminator would not fully "fill" the features displayed on the monitor. The present invention provides means for overcoming this inadequacy.

Since the video camera continuously scans the specimen, application A provided a circuit including a one-shot multivibrator responsive to depression of a start key for enabling the counter or scaler for an interval of time equal to that required for the camera to completely scan one field. The timing of the multivibrator depended upon the RC time constant of the timing circuit and thus was subject to variations resulting from temperature, aging, and voltage supply variations. A feature of the present invention is a provision of a digital type cycle control circuit for enabling the counter.

Applications A and B both disclose a manually controllable masking circuit for selecting any desired area of a specimen for analysis. The masking circuit included four one shot multivibrators independently triggered by horizontal and vertical sync pulses, and an AND gate responsive to the outputs of all four multivibrators. Since the multivibrators controlling the top and bottom of the mask operated independently of the two multivibrators controlling the sides, it was possible to have one or more partial lines of unmasked scanning at the upper and lower margins of the mask. A further feature of the present application is the provision of means for eliminating these partial lines of unmasked scanning.

SUMMARY OF THE INVENTION

An object of this invention is to provide a specimen analyzer for analyzing features of the specimen whether they be large or small, and including a grey level detector having background compensation means.

An object of this invention is to provide a grey level detector which may discriminate between features of a specimen and the background of said features.

An object of this invention is to provide a grey level discriminator employing first and second parallel connected comparator amplifiers, selectively operable means for averaging a specimen representing signal before applying it to said amplifiers, means for applying a reference signal to each of said amplifiers, and logic circuit means for combining the outputs from said amplifiers. A further comparator amplifier connected in parallel with the first amplifier is responsive to a further reference signal and the specimen representing signal and controls the logic circuit means so that the logic circuit means produces an output signal only during intervals when the specimen representing signal represents a feature falling within a preselected range of grey.

A further object of the invention is to provide a digital control circuit responsive to a manually controlled switch and vertical synchronizing pulses produced by a video camera for enabling a counter only for the interval of time required for the camera to scan one field.

Still another object of this invention is to provide a masking circuit which produces an unmasked signal that always begins at one side of an unmasked area and extends to the opposite side of an unmasked area such that all horizontal lines of scan extending through the unmasked area are of equal length. Other objects of the invention and its mode of operation will become apparent upon consideration of the following detailed description and the accompanying drawings.

BRIEF DESCRIPTION OF DRAWINGS

FIG. 1 is a block circuit diagram of a feature counter employing the present invention;

FIG. 2 is a schematic diagram of a grey level discriminator circuit constructed in accordance with the present invention; and,

FIG. 3 is a schematic diagram of a comparator amplifier suitable for use in a grey level discriminator.

GENERAL DESCRIPTION

FIG. 1 shows a feature analyzer similar to the one disclosed in copending application A. Except as hereinafter noted, the elements shown in block form in FIG. 1 may be the same as disclosed in the copending application. A scanning means such as video camera 10 is focused on a specimen 12 through a microscope or other lens system 14. The scanning means 10 may be a conventional video camera which completely scans the specimen 12 during one scan frame made up of two fields. Each field comprises a plurality of horizontal line scans with the line scans of one field being interlaced with the line scans of the other field. The video camera includes synchronizing circuits so that the camera produces on an output lead 16 a composite signal. This signal includes horizontal and vertical sync pulses as well as a video signal which varies in magnitude according to the color or grey level of the specimen being scanned at any particular instant. A composite output signal from the video camera is applied through an amplifier 18, a compensating delay 20, and a potentiometer 22 to a video monitor 24. The video camera continuously scans the specimen 12 so that the monitor 24 continuously presents a visual image of that portion of the specimen 12 which falls within the field of view of the camera.

One function of the specimen analyzer is to distinguish between features on the basis of grey level. The output of the video camera is applied over leads 16 and 26 to an amplifier 28, and the output of amplifier 28 is connected by way of a

lead 30 to a grey level discriminator 32. The grey level discriminator will subsequently be described in detail in connection with FIG. 2. It is sufficient at this time to note that the grey level discriminator includes manually adjustable means for selecting a desired grey level and means for testing the specimen-representing video signal on lead 30 against this grey level. The grey level discriminator produces a binary type output signal on lead 34. The output signal on lead 34 has a first value when the signal on lead 30 meets the grey level test and has a second value when the signal on lead 30 does not meet the grey level test. Thus, as the video camera scans across the specimen the grey level discriminator produces an output signal each time the video camera intercepts a feature which meets the grey level test. These intercept pulses on lead 34 may be counted by a counter or scaler 36 if a switch S1 is set to the position shown in FIG. 1. A circuit extends from lead 34, lead 38, switch contact S1B2, lead 40, inverter 42, and lead 44 to the scaler 36. Assuming that the enabling input lead 46 of the scaler is energized, each pulse on lead 44 will be counted by the scaler 36.

Output pulses from the grey level discriminator may also be applied to the monitor 24 through a circuit which extends from lead 34, lead 38, switch contact S1B2, lead 40, inverter 48, switch S2, potentiometer 22, and lead 50. Thus, the binary output pulses from the grey level discriminator are mixed with the video signal derived from the camera and applied to the monitor 24. The effect of this is to cause the features which meet the grey level test to appear on the monitor 24 as lighter features than those which do not meet the grey level test. Thus, an operator may visually observe on the monitor the features resulting in intercept pulses which are being counted.

The specimen analyzer is also capable of distinguishing between features on the basis of the width of the features. The output of the grey level discriminator is applied directly to a width discriminator 52 which may be of the type disclosed in copending application A. As described in that application, the width discriminator includes manually adjustable means for selecting a desired width or a desired range of widths.

Width discriminator 52 may perform either of two tests. First, it may test each binary pulse appearing on lead 34 and produce an output signal on lead 54 if the test indicates that the binary pulse has a duration greater than a preselected duration. Secondly, the width discriminator 52 may perform a between limits test and produce an output signal on lead 56 for each binary pulse that has a duration greater than a first preselected duration but less than a second preselected duration. As explained in copending application A, manual controls associated with the width discriminator enable the operator to select the desired limits of the test. The switch S3 permits the operator to select the signals appearing on lead 54 or the signals on lead 56 for application to the following circuits.

The selected output signals from the width discriminator are applied to one input of a NAND gate 58. A second input is applied to the NAND gate over a lead 60 from a masking circuit which is subsequently described. Assuming that the NAND gate is conditioned by lead 60, the NAND gate will produce an intercept pulse each time the video camera scans across a feature which meets both the grey level test performed by grey level discriminator 32 and the width test performed by width discriminator 52. The duration of each of these intercept pulses is proportional to the width of the feature which caused it to be produced.

The intercept pulses appearing at the output of NAND gate 58 may be applied to scaler 36. The circuit extends over lead 62, switch contacts S1B3, lead 40, and inverter 42 to the scaler 36. The intercept pulses appearing at the output of NAND gate 58 may also be applied to the monitor 24 so as to brighten on the display those features which have met the grey level and width tests. The circuit for applying the intercept pulses to the monitor extends from NAND gate 58, lead 62, switch contacts S1B3, lead 40, inverter 48, switch S2, and potentiometer 22 to the monitor 24.

In some applications of the feature analyzer, it is preferable to know the number of features which meet the grey level and width tests rather than the number of times the video camera scans across a feature meeting these tests. For example, a large feature may be intercepted several times, once during each of several consecutive horizontal line scan intervals. As explained in copending application A, a feature discriminator 64 delays the output of NAND gate 58 for approximately one line scan interval and then compares this delayed output of the NAND GATE WITH THE CURRENT OUTPUT OF THE NAND gate.

The output of NAND gate 58 is applied to one input of the feature discriminator 64 but the feature discriminator will not produce an output unless the switch S1 is set to position 4. When the switch is so set, the output of NAND gate 58 may pass over lead 62 and through switch contacts S1C4 to the input 66 of the feature discriminator.

As explained in copending application A, the feature discriminator produces a single output pulse for each feature meeting the grey level and width tests. This output pulse occurs one horizontal line scan interval after the video camera last intercepts the feature. The feature pulses may be applied to the scaler 36 over a circuit which extends from the feature discriminator, lead 68, switch contacts S1B4, lead 40, inverter 42, and lead 44 to the scaler 36. The feature pulses may also be displayed as check spots adjacent the feature which caused them to be produced. For this purpose a circuit extends from the feature discriminator over lead 68, switch contact S1B4, lead 40, inverter 48, switch S2, potentiometer 22, and lead 50 to the display monitor 24.

One of the uses of the specimen analyzer is to determine the area of features which meet the grey level and widths test. An oscillator 70 is energized to continuously produce clock pulses when the switch S1 is set to apply an enabling voltage over switch contacts S1A5 to the input of the oscillator. The clock pulses produced by the oscillator are applied to one input of a NAND gate 72. The second input of NAND gate 72 comprises intercept pulses derived from NAND gate 58. A circuit extends from NAND gate 58, over lead 62, switch contacts S1C5, and inverter 74 to the input of NAND gate 72. The output of NAND gate 72 may be applied to the scaler 36 over a circuit which extends through switch contacts S1B5, lead 40, and inverter . Since the output of NAND gate 58 is an intercept pulse which is proportional in duration to the width of the feature which cause it to be produced, NAND gate 72 passes a number of clock pulses proportional to the area of the feature. These pulses are summed by the scaler 36 to provide an indication of the area of the features in the specimen which meet both the grey level and the width tests.

In order that the operator may visually observe which features are contributing to the area count, the output of NAND gate 72 is applied over lead 40 and through inverter 48 to the monitor 24.

In many applications of the specimen analyzer it is desirable to limit the analysis to a particular portion of the specimen. Copending application A discloses an electronic masking circuit which is controllable from the control panel to thereby limit the analysis of the specimen to a predetermined unmasked area. This is accomplished by masking or blocking NAND gate 58 during those intervals wherein the video camera is scanning portion of the specimen which falls outside the area of interest. The masking circuit includes a sync signal separator 76, and four one shot multivibrators 78, 80, 82 and 84. The composite output signal from the video camera is applied through a capacitor 86 to the sync separator 76. Capacitor 86 filters out the video portion of the composite signal so that only the horizontal and vertical sync pulses are applied to the sync separator. The sync separator separates the horizontal and vertical sync pulses, applies the horizontal sync pulses to one shot multivibrators 78 and 80, and applies the vertical sync pulses to one shot multivibrators 82 and 84.

Each of the one shot multivibrators changes state upon receipt of a sync pulse and remains in that state for a period of

time as determined by a timing circuit after which it returns to the initial state. As explained in copending application A, each of these timing circuits is made adjustable from the control panel so that the operator may select the position of each of the four margins of the area which he desires to analyze. The outputs of each of the one shot multivibrators are connected to a logical AND gate 87 such that the AND gate produces an output signal on the lead 60 only when all of the one shot multivibrators are producing a positive output signal. The signal on lead 60 is applied to the NAND gate 58 so as to condition the NAND gate to pass pulses only when the video camera is scanning the area of the specimen falling within the four margins defined by the one shot multivibrators.

In accordance with copending application A, the operation of each one shot multivibrator was entirely independent of the operation of the other multivibrators. Because of this, and because of normal slight slant inherent in the conventional television scanning technique, one or more partial lines of scan might occur at the top and bottom of the unmasked area. For example, the top one shot 82 might first begin to condition AND gate 87 at some point intermediate the right and left margins of the unmasked area. Furthermore, since the multivibrators employ resistance-capacitance timing circuits, the top one shot multivibrator might not begin to condition AND gate 87 at exactly the same time on two successive measurements. This would result in a different count on the two successive measurements.

To avoid this problem it has been found that a more consistent count can be obtained by controlling the left one shot multivibrator so that it cannot condition the AND gate 87 during any horizontal line scan unless the outputs of the top and bottom one shot multivibrators are conditioning the AND gate at the time the left one shot receives a horizontal sync pulse at its input. For the specific one shot multivibrators disclosed in copending application A, this can be accomplished by connecting the top and bottom one shot multivibrators to the output of the left one shot multivibrator through first and second diodes 88 and 90 poled as shown in FIG. 1.

From the foregoing description it is obvious that in order to obtain an accurate count of either feature pulses or intercept pulses, the scaler must be controlled so as to accept pulses only during one field of scan of the video camera even though the video camera continuously scans the specimen. Copending application A employed a cycle control circuit including capacitor timing means for this purpose. Voltage variations, the aging of circuit components, and other factors make the capacitor timing circuit undesirable. In the present invention the cycle control is accomplished in a digital manner.

The cycle control means comprises three bistable flip-flops 92, 94, and 96. The output of flip-flop 92 is connected by way of a lead 98 to one input of flip-flop 96. One output of flip-flop 94 is connected by way of a lead 100 to another input of flip-flop 96. Vertical sync pulses derived from the sync separator 76 are applied over a lead 102 to one input of flip-flops 94 and 96. The output of flip-flop 96 is connected through an inverter 104 to the enabling input 46 of scaler 36. The output of flip-flop 96 is also connected to the reset input of flip-flop 92.

The cycle control circuit operates as follows. As long as the video camera is operating the sync separator circuit 76 produces vertical sync pulses on lead 102 which are applied to the flip-flops 94 and 96. Each sync pulse applied to flip-flop 94 changes the state of the flip-flop so that during alternate fields of scanning an enabling signal is applied over lead 100 to flip-flop 96. The vertical sync pulses on lead 102 are also applied to the flip-flop 96. The internal configuration of flip-flop 96 is such that if the flip-flop is set, a pulse on lead 102 will cause the flip-flop to be reset. On the other hand, if the flip-flop 96 is reset a pulse on lead 102 will set the flip-flop only if there are concurrent enabling signals present on leads 98 and 100. Thus, as long as the video camera is on vertical sync pulses change the state of flip-flop 94 after each field is scanned but nothing further happens.

A manually controllable start switch 106 is connected to the set input of flip-flop 92. When the switch 106 is closed to initiate a cycle, the ground level signal passing through the switch sets flip-flop 92 thereby providing an enabling signal over lead 98 to the flip-flop 96. Either the first or the second vertical sync pulse following the closing of switch 106 will set the flip-flop 94 so as to enable the lead 100. The same sync pulse which enables the lead 100 is also applied to the flip-flop 96 thereby changing it to the set state. Flip-flop 96 produces an output signal that is applied through inverter 104 to the enabling input 46 of the scaler 36. As explained in copending application A, the signal on lead 46 first resets the scaler and then enables it to receive and count pulses applied to it over lead 44.

The output of flip-flop 96 is also applied to the reset input of flip-flop 92 thereby resetting flip-flop 92 even though the switch 106 may still be closed.

The output signal from flip-flop 96 lasts for an interval of time equal to that required to scan one field. At the end of that field the next vertical sync pulse appearing on lead 102 switches the state of flip-flop 94 to remove the enabling signal on lead 100, and resets the flip-flop 96 to remove the enabling signal applied to the scaler.

The flip-flop 92 may be a conventional flip-flop comprising cross-coupled NOR circuits as is well known in the art. Therefore, once switch 106 is depressed to initiate one cycle of operation, it will not again set flip-flop 92 to cause a second cycle of operation unless the switch 106 has been opened. Once the switch 106 has been opened a new count cycle may be initiated by again closing the switch.

A feature of the present invention is an improved grey level discriminator having background compensation means. The grey level discriminator 32, shown in block form in FIG. 1, is shown in detail in FIG. 2. The grey level discriminator comprises three amplifiers 110, 112, and 114. A shown in FIG. 3, each amplifier includes as the basic element a Texas instrument type SN72710L differential comparator. Each amplifier functions to compare a signal applied to a signal input S with a reference voltage applied to a reference input R. Each amplifier produces a binary type output signal that has a first level as long as the signal is greater than the reference voltage and a second level when the signal is less than the reference voltage.

The output of the video camera is applied through amplifier 28 to the input lead 30 of the grey level discriminator. For purposes of the following description it is assumed that the signal on lead 30 is "white positive". That is, the signal on lead 30 varies in magnitude according to the grey level of the portion of the specimen being scanned at any instant, with the signal becoming more positive as the portion scanned becomes lighter, and more negative as the portion scanned becomes darker.

Assuming that the specimen being analyzed is of such character that the grey level of the background remains fairly constant so that the features are easily distinguishable over the background, no background compensation is necessary. In this case a switch S4 may be set to the position shown in FIG. 2 so that the signal from the video camera is applied directly to the signal inputs of amplifiers 110 and 112. The reference voltage applied to comparator amplifier 110 is derived from a voltage divider network including a potentiometer 116 which may be manually set by an operator from the control panel of the analyzer. In like manner, the operator may manually set a potentiometer 118 to determine the reference voltage applied to comparator amplifier 112.

The output of comparator amplifier 110 is connected through an inverter 120 to one input of a NAND gate 122. The NAND gate 122 has a second input connected to the output of comparator amplifier 112. The output of NAND gate 122 is connected to one input of a NAND gate 124 and the output of this NAND gate is connected through an inverter 126 and a switch 128 to the discriminator output line 34.

Assume that it is desired to detect only those features in a specimen which are darker than a first preselected grey level

but not as dark as a second preselected grey level. The operator adjusts potentiometer 116 so as to apply to comparator amplifier 110 a reference voltage corresponding to the first grey level, and adjusts the potentiometer 118 so as to apply to the comparator amplifier 112 a reference voltage corresponding to the second grey level. Both amplifiers 110 and 112 produce positive output signals as long as the reference voltage is more negative than the incoming signal voltage. When the scan of the video camera intercepts a feature which is darker than the first selected grey level but not as dark as the second grey level, comparator amplifier 110 produces a negative output signal while the output of comparator amplifier 112 remains at the positive level. The negative output signal from comparator amplifier 110 is inverted and applied to NAND gate 122 which also receives the positive output of comparator amplifier 112. NAND gate 122 produces a negative output signal that is inverted by NAND gate 124, and inverted again by inverter 126 so as to appear as a negative output signal on the lead 34. The signal on lead 34 remains negative until the signal on lead 30 again becomes more positive than the reference voltage applied to amplifier 110. At this time the output of amplifier 110 becomes positive thereby terminating the signal on lead 34. If the camera should scan a feature which is darker than both the first and second grey levels the signal on lead 30 becomes more negative than the reference voltages applied to both amplifiers 110 and 112. In this case, the outputs of both amplifiers become negative. The output of comparator amplifier 112 drives the output of NAND gate 122 positive and this signal is applied to one input of NAND gate 124. The other input of NAND gate 124 is positive as long as switch S4 is in the position shown. With both inputs positive, NAND gate 124 produces a negative output signal that is inverted by inverter 126 so as to appear as a positive output signal on lead 34. A positive signal on lead 34 is equivalent to no feature. Thus, if the feature scanned by the video camera does not fall within the grey limits as determined by the reference voltages applied to comparator amplifiers 110 and 112, it is effectively ignored.

It will be understood that the grey level discriminator may be made to perform a "greater than" test rather than a "between limits" test by setting the potentiometer 118 so that it applies to the comparator amplifier 112 a reference voltage which is more negative than any signal which may appear on the input lead 30 as a result of scanning the specimen. In this case the output of comparator 112 will remain at the positive level to condition NAND gate 122. The output of the NAND gate will then be entirely dependent upon the output of comparator amplifier 110 and this will be either positive or negative depending upon whether the feature being scanned is lighter than or darker than the grey level determined by the setting of potentiometer 116.

The grey level discriminator of the present invention is adapted to analyze a wide variety of specimens having different characteristics. When the background is fairly constant and contrasts with the features being counted, the grey level discriminator operates quite well in the manner described above. Consider however the case where the specimen being analyzed is a photograph made with an electron microscope. In such photographs there frequently appears in the background a series of interference bands which vary continuously from a light grey level to some dark level and back to the light level. The features to be counted are within the field of interference bands and frequently the features are lighter than the darker levels of the band. Thus, when analyzing such photographs the grey level discriminator will, when operating as described above, erroneously produce an output signal for each interference band intercepted, if the band is darker than the selected grey level of the features to be analyzed. This should be obvious since the comparator amplifier 110 receives a video signal whose magnitude is directly proportional to the grey level seen by the video camera.

However, it will be recognized that the background variation is of a continuous nature so as to produce a relatively slow

variation of the grey level discriminator input signal 30, whereas the changes between the background and each feature is more abrupt and causes a more rapid change in the voltage level of the signal appearing on lead 30. Because of this characteristic difference, a capacitor may be used to average the video signal over an interval of time and detect sudden variations from the average. A .002 microfarad capacitor 128 is provided for this purpose. When the switch S4 is set to the position opposite that shown in FIG. 2, a circuit is formed from input lead 30 through the contacts of switch S4, through capacitor 128 and a potentiometer 130, and through the second set of switch contacts S4 to the signal inputs of comparator amplifiers 110 and 112.

Under these conditions the incoming signal voltage applied to capacitor 128 varies at a relatively slow rate corresponding to the continuous variations in the grey level of the background hence, the capacitor blocks the signal and it does not reach the comparator amplifiers 110 and 112. However, when a feature is intercepted during a scan the signal on lead 30 rapidly becomes more negative. The signal is differentiated by capacitor 128 and applied to amplifiers 110 and 112 which performs the grey level test.

It will be recognized that the differentiated signal from capacitor 128 would normally be quite short in duration and would not correspond to the width of the feature which caused it to be produced. The potentiometer or variable resistor 130 is connected in series with capacitor 128 to slow its discharge rate, thus providing an input signal to amplifiers 110 and 112 which lasts at least until the trailing edge of the feature is sensed. When the trailing edge of the feature is sensed, the input signal on lead 30 rapidly becomes more positive thus immediately discharging capacitor 128 and terminating the input signals to amplifiers 110 and 112.

The operation of the logic circuit elements responsive to the outputs of comparator amplifiers 110 and 112 is the same as described above. That is, these circuits operate in the same manner whether switch S4 is in its first or its second position, provided switch S5 is open.

Since it is desirable to limit the time constant of the RC circuit including capacitor 128 and resistor 130 to the smallest value which will still enable the circuit to produce an output signal as long as the time it takes to scan a feature, and since the size of features may vary depending upon the specimen being analyzed, the variable resistor 130 is mounted so that it may be manually controlled by operator from the console of the analyzer. Thus, the operator may adjust resistor 130 depending upon the characteristics of the specimen being analyzed.

The charge/discharge time of the RC circuit 128, 130 is such that the grey level discriminator may ignore very small features. This results from the fact that a very small feature might be completely scanned and its trailing edge sensed before the capacitor 128 is charged. The change in voltage on input lead 30 as the trailing edge is sensed would thus discharge capacitor 128 before it is fully charged.

The switch S5 is manually controlled by the operator and may be closed when it is desired to analyze a specimen containing small features and requiring background compensation. A circuit is thus formed from the grey level discriminator input lead 30 through switches S4 and S5, and capacitor 132 to the signal input of comparator amplifier 114. A fast discharge of capacitor 132 is provided through a potentiometer 133 to ground. The reference signal input to comparator amplifier 114 is derived through potentiometer 116 and a potentiometer 138. The potentiometer 138 permits the operator to balance the circuit so that comparator amplifier 114 is balanced with or recognizes the same grey level input signals as amplifier 110.

The output of amplifier 114 is connected through an inverter 134 to one input of a NAND gate 136. This NAND gate has a second input connected to the output of amplifier 112, and the output of the NAND gate is connected to one input of NAND gate 124.

Assume that an operator wishes to analyze a specimen requiring background compensation and containing very small features. Assume further that the analyzer is to recognize only those features darker than a preselected grey level. The analyzer is set up closing switches S4 and S5 thus connecting input lead 30 to amplifiers 110 and 114. Potentiometer 116 is set to apply to amplifiers 110 and 114 a reference signal representing the selected grey level. Since a "between limits" test is not being performed, potentiometer 118 is set so as to apply to amplifier 112 a signal representing a grey level that is "blacker than black." Therefore, amplifier 112 will be off and its output positive for the duration of the analysis.

Upon depression of the start button 106 (FIG. 1) the video camera begins scanning the specimen and a video signal is produced on lead 30 of the grey level discriminator, this signal varying in accordance with the grey level of the scanned specimen. If a very small feature darker than the selected grey level is intercepted by the video camera, the signal on lead 30 abruptly becomes more negative. This signal charges capacitor 132 and, because of the connection through potentiometer 133 to ground, the capacitor quickly discharges. The signal from capacitor 132 is of very short duration and, when compared with the grey level reference voltage in amplifier 114, causes this amplifier to produce a negative output signal. The signal passes through logic circuit elements 134, 136, 124 and 126 to appear as a negative grey level discriminator output pulse on lead 34. If the feature is quite small, the amplifier 110 will not produce an output signal.

If the feature happens to be somewhat wider, the capacitor 128 may charge while the feature is still being scanned, and the output from the capacitor will fire comparator amplifier 110 at some period of time after amplifier 114 fires but before amplifier 114 stops producing an output signal. Thus, amplifier 110 begins producing a negative output signal that passes through logic circuit elements 120, 122, 124 and 126 to appear as a negative grey level discriminator output pulse on lead 34. The pulses from amplifiers 110 and 114 partially overlap in time and are logically combined at NAND gate 124 so that, in effect, only a single pulse appears on output line 34. This pulse is somewhat wider than the output pulse from either amplifier 110 or amplifier 114.

The output from amplifier 114 continues until capacitor 128 discharges through potentiometer 130, or until the signal on lead 30 becomes more positive as a result of the trailing edge of the feature having been scanned. It will be understood from the foregoing description that the output pulse from amplifier 114 has a duration determined only by the setting of potentiometer 133 whereas the output pulse from amplifier 110 has a duration dependent on the width of the feature scanned. The logically combined signals result in a grey level discriminator output signal on line 34 that has a duration closely corresponding to the interval of time it takes to scan across the feature.

From FIG. 2 it is evident that a between limits grey level test cannot be performed when switch S5 is closed because signals representing small features or the leading edge of large features are not applied to the amplifier 112 which tests for the darker limit. However, despite this inadequacy, the grey level discriminator of the present invention permits a wider range of uses of the analyzer than the discriminators heretofore known.

The switch 158 at the output of the grey level discriminator enables the operator to select either the output of inverter 126 or the output of NAND gate 124 for application to the width discriminator. The width discriminator responds only to negative pulses. When counting black features on a light background switch 128 is set as shown in FIG. 2. When determining the spacial distribution of white features on a black background switch 128 is set to pass the output of NAND gate 124 directly to the width discriminator.

The embodiments of this invention in which an exclusive property or privilege is shown are defined as follows:

1. In a specimen analyzer for analyzing a specimen and producing an output signal for each feature meeting a preselected grey level test, the combination comprising:

- input means for receiving an analog signal varying in magnitude in accordance with the grey level of features and background in said specimen;
- a source of reference voltage, manually variable to preselect said grey level;
- a comparator means having first and second inputs for producing an output signal only when the signal applied to said first input exceeds the signal applied to said second input;
- means connecting said source of reference voltage to said second input; and,
- background compensation means responsive to said input means for applying to said first input of said comparator only signals representing the grey level of said features.
2. The combination as claimed in claim 1 wherein: said background compensation means comprises a capacitor and resistor connected in series between said input means and the first input of said comparator.
3. The combination as claimed in claim 1 and further comprising switch means for selectively connecting the first input of said comparator means to said background compensation means or to said input means.
4. The combination as claimed in claim 1 and further comprising:
- a second comparator means having a first input, a second input connected to said reference voltage source; means responsive to said input means for applying a signal to the first input of said second comparator means for each feature; and,
- logic circuit means responsive to said first and second comparators for logically combining output signals therefrom so as to produce a single pulse for each feature which meets the preselected grey level test.
5. The combination as claimed in claim 4 wherein: said background compensation means comprises a capacitor and resistor connected in series between said input means and the first input of said comparator.
6. The combination as claimed in claim 4 wherein the means applying a signal to the first input of said second comparator means comprises a capacitor, and means connected to the comparator input side of said capacitor for providing a fast discharge path for said capacitor.
7. The combination as claimed in claim 1 and further comprising scanning means for scanning said specimen and applying said analog signal to said input means.
8. The combination as claimed in claim 7 wherein said scanning means comprises a video camera.
9. In a specimen analyzer for analyzing a specimen containing features, the combination comprising:
- discriminator means responsive to an analog signal representing said features for testing a characteristic of said features and producing a binary type pulse for each feature meeting said test;
- an electronic masking circuit for generating a variable masking signal; and,
- coincidence detection means responsive to said masking signal and said binary type pulses for producing an intercept signal each time said analog signal changes to represent a feature which meets said test and is located in an unmasked area of said specimen;
- said masking circuit comprising,
- means for receiving horizontal and vertical sync pulses and separating them,
- left and right margin control monostable multivibrators responsive to the horizontal sync pulses for producing output signals,
- top and bottom margin control monostable multivibrators responsive to the vertical sync pulses for producing output signals,
- means responsive to said top and bottom margin control monostable multivibrators for inhibiting an output from said left margin control multivibrator unless both said top and bottom multivibrators are producing output signals at the time said left multivibrator receives a horizontal sync pulse,

and gating means for producing said variable masking signal in response to concurrent output signals from all of said multivibrators.

10. The combination as claimed in claim 9 wherein each of said multivibrators includes a timing circuit that is manually adjustable to select the position of one margin of said unmasked area. 5

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