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(74) Agents: WILLIAMS, Gary, S. et al.; Morgan Lewis & Bockius LLP, 2 Palo Alto Square, 3000 El Camino Real, Suite 700, Palo Alto, CA 94306 (US).

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(71) Applicant (for all designated States except US): RAM-BUS INC. [US/US]; 4440 El Camino Real, Los Altos, CA 94022 (US).

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(72) Inventors; and

(75) Inventors/Applicants (for US only): KIM, Jaeha [US/US]; 810 E. Dana Street, Mountain View, CA 94041 (US). HOROWITZ, Mark, A. [US/US]; 1309 San Mateo Drive, Menlo Park, CA 94025 (US). JONES, Kevin, D. [GB/US]; 27475 Dobbels Avenue, Hayward, CA 94542 (US).

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(54) Title: NOISE MODEL METHOD OF PREDICTING MISMATCH EFFECTS ON TRANSIENT CIRCUIT BEHAVIORS

Translation of Device Mismatch Statistics to Low Frequency Noise Statistics

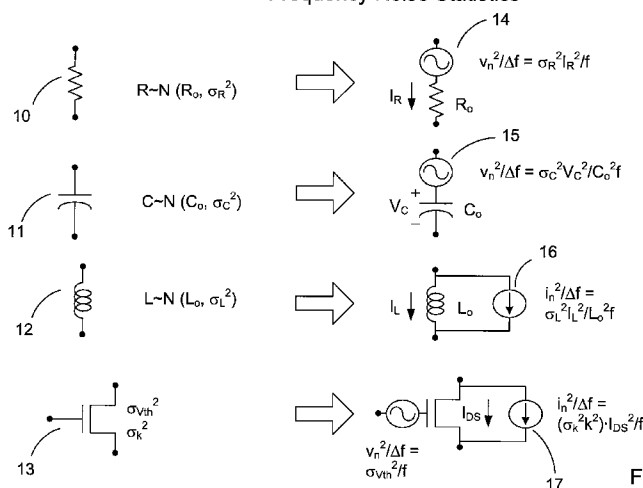


Figure 1

(57) Abstract: A method of simulating device mismatch effects on transient circuit behaviors utilizes a circuit model corresponding to an electronic circuit. The circuit model includes a plurality of circuit elements and one or more noise sources. The noise sources have noise characteristics that correspond to device mismatch effects associated with the circuit elements. A noise analysis is performed on the circuit model to generate a noisy steady-state waveform of a selected output of the electronic circuit. Then, the noisy steady-state waveform is translated into a prediction of the variation of a respective circuit parameter associated with the electronic circuit.



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NOISE MODEL METHOD OF PREDICTING MISMATCH EFFECTS ON TRANSIENT CIRCUIT BEHAVIORS

FIELD

5 **[0001]** The subject matter herein generally relates to simulation methods for predicting mismatch effects of circuits.

BACKGROUND

10 **[0002]** Device mismatch is the difference between two or more nominally identical devices. Device mismatch may be caused by non-uniformity in device fabrication. Device mismatch may also be expressed as uncertainty in the value of device parameters. For MOSFET transistors, device mismatch may affect device parameters such as threshold voltage, current factor, gate oxide thickness, doping levels in one or more device regions, source/drain junction depth, and so on.

15 **[0003]** To simulate random effects in circuit behaviors due to device mismatches, for example, clock skews, receiver offsets, nonlinearities of analog-to-digital converters (ADCs), nonlinearities of digital-to-analog converters (DACs), and nonlinearities of phase interpolators, circuit designers typically run Monte-Carlo simulations. A Monte-Carlo simulation is a collection of repeated simulations with randomized circuit parameters such as resistance, capacitance, inductance, and threshold voltage (V_{th}) and current factor (k) of a transistor. The estimation accuracy depends on the number of runs. Typically a few hundred simulations or more are required to obtain reasonably accurate information about the impact of device mismatches on circuit operation. For DC or AC analysis, this poses little problem since each simulation run executes reasonably fast. However, for transient analysis, which measures the circuit's voltage or current response over time, a Monte-Carlo simulation can be
25 prohibitively time-consuming.

30 **[0004]** A faster method of simulating random transient behaviors of circuits due to device mismatches is therefore needed.

BRIEF DESCRIPTION OF THE DRAWINGS

30 **[0005]** For a better understanding, reference should be made to the following detailed description taken in conjunction with the accompanying drawings, in which:

[0006] Figure 1 illustrates the translation of circuit elements with DC-mismatch statistics into circuit elements with noise sources, sometimes called pseudo-equivalent AC noise sources.

[0007] Figure 2 is an embodiment of the translation of the output noise power spectral density (PSD) to DC variation of a voltage of interest in the circuit.

[0008] Figure 3 is an embodiment of a buffer chain.

[0009] Figure 4 is an embodiment of a modeled buffer chain combining pseudo-equivalent AC noise sources with the model elements shown in Figure 1.

[0010] Figure 5 shows how the output of a circuit simulator can be used to generate the delay variation of the buffer chain in Figure 3 using a frequency-domain periodic noise analysis.

[0011] Figure 6 shows how a circuit simulator can be used to generate the delay variation of the buffer chain in Figure 3 using a time-domain periodic noise analysis.

[0012] Figure 7 is a flow chart illustrating an embodiment of the method of simulating device mismatch effects on transient circuit behaviors described herein.

[0013] Figure 8 shows how the variation of the period of a ring oscillator due to device mismatches can be determined using either a frequency domain analysis or a time domain analysis.

[0014] Figure 9 illustrates a computer that can be used to perform the method described herein.

[0015] Like reference numerals refer to the same or similar components throughout the several views of the drawings.

DETAILED DESCRIPTION OF EMBODIMENTS

[0016] A method of simulating device mismatch effects on transient circuit behaviors includes providing a circuit model that corresponds to an electronic circuit. The circuit model includes a plurality of circuit elements and one or more artificial noise sources that are used for modeling device mismatch effects. These noise sources are artificial in a sense that their characteristics do not correspond to physical noises such as thermal noise, flicker noise, or shot noise that vary over time, but rather their characteristics correspond to device mismatch effects associated with the circuit elements that are static over time (DC) in nature. A periodically time varying noise analysis is performed on the circuit model to generate a simulation output representing a noisy periodic waveform at a selected output of the electronic circuit. The noisy periodic waveform is translated into a variation of a respective

circuit parameter associated with the electronic circuit. The variation corresponds to a predicted magnitude of the device mismatch effects.

[0017] In some embodiments, the noisy periodic waveform is represented in the frequency-domain by a Fourier-series representation of a nominal periodic steady-state waveform and a noise power spectral density (PSD) of the selected output of the electronic circuit. In other embodiments, the noisy periodic waveform is represented in the time domain by a time-series representation of the nominal periodic steady-state waveform and the RMS variation of noise within the nominal periodic steady-state waveform at multiple points in time.

[0018] In some embodiments, mismatch parameters represent variations or uncertainties in device characteristics that are static over time (DC offsets) and noise parameters represent unwanted signals that vary over time (AC noises).

[0019] In some embodiments, the artificial noise sources in the circuit model include one or more noise sources having AC noise parameters that correspond to one or more device mismatches parameters. These AC noise parameters (e.g., noise scaling factors) are sometimes herein called pseudo-equivalent AC noise parameters, and the noise sources are sometimes herein called pseudo-equivalent AC noise sources. Noise sources having pseudo-equivalent AC noise parameters can replace DC offsets in voltage or current, or combinations thereof.

[0020] In this document, the PSD of a noise signal is also called the PSD of the noise source that produces the noise signal.

[0021] In some embodiments, the pseudo-equivalent AC noise sources that are added to the circuit model to model device mismatches are $1/f$ noise sources, which produce "1/f noise." The power (i.e., PSD) of the $1/f$ noise produced by $1/f$ noise sources decreases with frequency (f) in accordance with $1/f$. In other embodiments, the pseudo-equivalent AC noise sources are $\frac{1}{f^n}$ noise sources, where n is a number greater than one. The power (i.e., power spectral density) of the noise ($\frac{1}{f^n}$ noise) produced by $\frac{1}{f^n}$ noise sources decreases with frequency in accordance with $\frac{1}{f^n}$. These $1/f$ and $\frac{1}{f^n}$ noise sources are sometimes called low frequency noise sources because their PSD at a predefined low frequency f_l , where f_l is typically at or below 100 Hz, is much greater (e.g., by at least a factor of 100) than

their PSDs at frequencies beyond the fundamental operating frequency (f_0) of the periodic circuit whose operation is being simulated.

[0022] In some embodiments, one or more of the pseudo-equivalent AC noise parameters varies in response to a bias level of one or more of the circuit elements.

5 [0023] In some embodiments, a circuit simulator performs a periodically time varying noise analysis on the modeled circuit.

[0024] In some embodiments, a sensitivity analysis is performed on the modeled circuit that provides a breakdown of individual noise source contributions to a total noise of the selected output of the circuit. The breakdown can be used to determine which device mismatch most influences a respective circuit parameter of interest.

10 [0025] In some embodiments, the parameter of interest is voltage or current, while in other embodiments the parameter of interest can be current, time delay, signal frequency, signal period, signal phase, differential non-linearity (DNL), integral non-linearity (INL) or a combination thereof.

15 [0026] In some embodiments, the noisy periodic waveform is decomposed into a proportional noise term and an integral noise term so that different types of device mismatch contributions to the circuit's behavior can be calculated separately.

[0027] In some embodiments, the two or more pseudo-equivalent noise sources (i.e., AC noise sources having AC noise parameters that correspond to one or more device mismatch parameters) are correlated and the correlations are realized by linear combinations of common sets of independent noise sources.

20 [0028] In some embodiments, the mismatch effects on two or more selected outputs of an electronic circuit are correlated and the correlations are estimated using the breakdown of individual noise source contributions to a total noise of each output of the circuit.

25 [0029] In another aspect of the invention, a computer-readable medium includes instructions for performing methods of simulating device mismatch effects on transient circuit behaviors.

[0030] In some embodiments, variations of a circuit parameter or performance parameter that may vary due to device mismatch are analyzed. Some mismatch effects of interest are deviations from nominal values, such as variations in delay (e.g., delay of a logic path or clock skews), variations in frequency (e.g., frequency of a ring oscillator), variations of voltage offset (e.g., in a regenerative amplifier or comparator).

[0031] Some other mismatch effects of interest are parameters describing degradations in performance due to device mismatches. Examples of such parameters include integral nonlinearities (INL) and differential nonlinearities (DNL) of digital-to-analog converters (DAC) and analog-to-digital converters (ADC). INL and DNL are measurements of linearity of conversion between digital values and analog quantities such as voltage, current, and phase. In an ideal D/A converter, incrementing the digital code by 1 changes the output voltage by an amount that does not vary across the device's permitted range. Similarly, in an A/D converter, the digital value ramps smoothly as the input is linearly swept across its entire range. DNL measures the deviation from the ideal. Similarly, INL measures another aspect of deviation from the ideal. An ideal converter has a DNL of 0 (zero) and an INL of 0.

[0032] Some circuit designs use replica circuits to measure one or more characteristics of a main circuit in order not to interfere with the operation of the main circuit. Any mismatch between the replica and the main circuit may introduce unintended degradation or deviation from the nominal behavior of a circuit or system. For example, in a phase-locked loop (PLL) that uses a replica-biased charge pump or voltage-controlled oscillator (VCO), mismatch between the replica and the main circuit can cause increased static phase offset, increased clock jitter, degradation in the supply noise rejection, and/or suboptimal scaling of PLL bandwidth.

[0033] Circuit simulators like SPICE or Spectre can perform a noise analysis of a modeled circuit in the frequency domain. To perform the analysis, elements of a particular circuit are first modeled using the conventions of a circuit description language specific to the simulator or using the conventions of a standardized analog behavioral description language, such as Verilog-A or VHDL-A. These conventions define parameters that describe the various elements of the circuit being simulated as well as the placement and power spectral density (PSD) of each noise source in the circuit. The period of the simulation is also defined. These parameters are input into the simulator and the simulator estimates the resulting noise power spectral density of a signal (e.g., a voltage or current) of interest at a specified location in the circuit.

[0034] Advanced RF circuit simulators like HSPICE-RF and SpectreRF extend the conventional noise analysis methods described above to periodically time-varying (PTV) systems, thus enabling the noise on a periodic transient waveform to be simulated. In some embodiments, the noise on a periodic transient waveform is represented in the frequency

domain by the noise power spectral density (PSD). In other embodiments, the noise is represented in the time domain by the RMS variation of the noise within the nominal periodic steady-state waveform at multiple points in time.

[0035] Combining the nominal periodic steady-state waveform and the noise on the nominal periodic steady-state waveform results in a noisy periodic waveform of the selected output in the electronic circuit. In some embodiments, the noisy periodic waveform is represented in the frequency-domain by a Fourier-series representation of the nominal periodic steady-state waveform and a noise power spectral density. In other embodiments, the noisy periodic waveform is represented in the time domain by a time-series representation of the nominal periodic steady-state waveform and the RMS variation of noise within the nominal periodic steady-state waveform at multiple points in time.

[0036] In some embodiments, a method of calculating or simulating the transient behavior of circuits due to device mismatches uses the periodically time-varying noise analysis feature of circuit simulators despite the fact that device mismatches are static (DC offsets). In this method, the DC offsets due to device mismatches are replaced (in the circuit model of the circuit being simulated) with noise sources having AC noise parameters that correspond to one or more device mismatch parameters. These noise sources, sometimes herein called pseudo-equivalent AC noise sources, produce noise having power spectral densities concentrated in a low frequency range. As noted above, in some embodiments the one or more noise sources (used to simulate the transient behavior of a circuit due to one or more device mismatches) may be $1/f$, $1/f^3$ or $\frac{1}{f^n}$ noise sources. The PSD of the noise produced by a $1/f$, $1/f^3$ or $\frac{1}{f^n}$ noise source decreases with frequency as a function of $1/f$, $1/f^3$ or $\frac{1}{f^n}$, respectively. As a result, the $1/f$, $1/f^3$ or $\frac{1}{f^n}$ noise produced by the noise source has very low PSD at the fundamental operating frequency f_0 of the circuit being simulated in comparison with the PSD of the noise at a predefined low frequency f_1 , where f_1 is typically at or below 100 Hz. In some embodiments, the PSD of a noise source used to model a respective device mismatch is much greater (e.g., by at least a factor of 100) than its PSDs at frequencies beyond the fundamental operating frequency f_0 of the periodic circuit whose operation is being simulated. The method takes advantage of the fact that, for a sufficiently short period of observation or simulation time, the DC mismatch and the pseudo-equivalent

AC noise have almost indistinguishable effects on the circuit transient behavior, since a low-frequency noise stays virtually constant for a short, bounded period of time.

[0037] The method of simulating device mismatch effects using pseudo-equivalent AC noises is much faster than using conventional Monte-Carlo methods, particularly when
5 simulating transient circuit behaviors. This speed of calculation is achieved by exploiting the faster execution time of noise analysis available in many circuit simulators and by avoiding the need to perform hundreds of simulations to measure transient circuit characteristics. In some cases, the described method is more than 100 times faster than Monte-Carlo methods.

[0038] In applying the method, the device mismatches (e.g., DC offsets) of the
10 various circuit elements are first translated into pseudo-equivalent AC noise sources. These DC offsets are generally characterized by mismatch statistics. As discussed, the pseudo-equivalent AC noise sources are chosen to be low-frequency noises so that they stay virtually constant over the simulation period. Then, the pseudo-equivalent AC noise sources are appropriately combined with the modeled circuit elements and input into the simulator. A
15 signal (e.g., a voltage or current) of interest at a location in the circuit is selected as an output and the simulation is executed. The output of the simulation can be a frequency domain output or a time domain output.

[0039] In the frequency domain, the output of the simulation is a Fourier-series representation of a periodic steady-state waveform and a noise PSD of the signal of interest.
20 The noise PSD of the signal of interest is translated back into a statistical variation of a circuit parameter of interest. In the time domain, the output of the simulation is a periodic steady-state waveform and associated RMS variation of noise, which are translated back into a statistical variation of a circuit parameter of interest.

[0040] PTV noise analysis provided by RF circuit simulators like HSPICE-RF and
25 SpectreRF enables mismatch effects on transient circuit behaviors to be analyzed using the aforementioned method. The ability of analyzing mismatch effects on transient circuit behaviors distinguishes this method from other non-Monte-Carlo methods such as DCMATCH analysis feature available in HSPICE and Spectre. However, a restriction is that the transient circuit behavior on which mismatch effects are to be analyzed must be periodic.
30 This can be enforced by a proper simulation setup. For example, the periodic state of a logic chain can be enforced by having periodic input stimuli.

[0041] Some circuit simulators including SpectreRF can also perform a sensitivity analysis. A sensitivity analysis provides a breakdown of individual noise source

contributions to the total output noise. When this feature is used with the mismatch analysis method described herein, the simulator determines which device mismatch(es) most influences the parameter of interest. This information can be used to assist in yield optimization. Estimating correlations between different voltages sampled at different times is also possible, thereby determining even more elaborate statistics such as differential nonlinearity (DNL).

[0042] To take advantage of the noise analysis features of circuit simulators, random variations (mismatch parameters) in resistance, capacitance, and inductance, as well as variations in threshold voltage and current factor (k) of a MOS transistor are first translated into AC noise sources and combined with the modeled circuit as current or voltage noise sources. This translation takes advantage of the fact that while circuit simulators do not accept circuit definitions in which circuit characteristics such as resistance, capacitance, inductance and the like include noise, circuit simulators but do accept voltage noise and current noise as inputs.

[0043] Figure 1 illustrates the translation of circuit elements with mismatch statistics into circuit elements with noise sources. Figure 1 shows circuit elements modeled with mismatch statistics, including mismatch modeled resistor 10, capacitor 11, inductor 12, and a MOS transistor 13. Figure 1 also shows the translation of the circuit elements modeled with mismatch statistics into corresponding circuit elements modeled with pseudo-equivalent noise sources (i.e., noise sources having AC noise parameters that correspond to one or more device mismatch parameters), including noise modeled resistor 14, capacitor 15, inductor 16, and MOS transistor 17. As previously mentioned, the PSD of the modeled noise sources is concentrated at low frequencies. Consequently, the PSD of the modeled noise sources is selected so as to minimize high frequency noise components. In Figure 1, the equivalent voltage or current variation due to the mismatch, with standard deviation of σ , is translated to a $1/f$ noise with a PSD that is proportional to σ^2 at 1Hz (i.e., noise power $\propto \sigma^2 \Delta f/f$). The circuit elements with their respective noise parameters can then be input into the simulator for analysis of a particular voltage or current of interest.

[0044] Since only one or two frequency points on the PSD are used in the translation between a circuit characteristic mismatch and noise, the noise PSD (of the modeled noise sources added to a circuit model for simulation) does not have to be a function of $1/f$, but can be a function of $1/f^2$, $1/f^3$, or f^{-n} where n is greater than one, as long as the noise PSD has negligible high-frequency power such that noise folding or harmonic generation does not

contaminate the noise power in the low-frequency range. Also, the noise PSD can be arbitrarily scaled up or down if necessary since the noise analysis is a linear analysis. Moreover, the equivalent noise power need not be fixed, but can vary depending on the circuit's condition. Such bias-dependent noise sources can be conveniently modeled using the Verilog-A model description language as well as other circuit description languages.

[0045] Once the PSD of a circuit signal of interest is obtained by running the simulation, the PSD of the signal of interest is translated back into a measurement of the variability of a circuit parameter. Figure 2 depicts an embodiment of two methods of translating output noise PSD, produced by a circuit simulator while simulating the circuit of interest, to DC variation of a voltage or current of interest in the circuit. Plot 20 illustrates the PSD of a typical, prophetic simulator output voltage. In this case the PSD of the output noise is proportional to the PSD of the input noise. The output noise PSD in this prophetic example is observed to be proportional to $1/f$, and therefore the output noise in this example is called $1/f$ noise. Consequently, the translation may be performed by applying the following equation.

$$\sigma_{\text{out}}^2 = N(f_1),$$

where f_1 is an arbitrary frequency (e.g., a predefined frequency such as 1 Hz) whose period is much larger than the simulation time span (so that the noise stays virtually constant over the simulation time span), $N(f)$ represents the noise PSD at frequency f , and σ_{out}^2 represents the variability of the circuit parameter of interest (e.g., an output voltage). The variability of the circuit parameter corresponds to the variance of the distribution of possible values of the circuit parameter due to device mismatch.

[0046] Plot 21 (Figure 2) illustrates the PSD of another typical, prophetic simulator output voltage. In this case the PSD of the output noise is proportional to the time-integral of the PSD of the input noise. The output noise PSD in this prophetic example is observed to be proportional to $1/f^3$, and therefore the output noise in this example is called $1/f^3$ noise. Consequently, the translation may be performed by applying the following equation.

$$\sigma_{\text{out}}^2 = N(f_1) \cdot 4\pi^2 / f_0^2,$$

where f_1 is an arbitrary frequency (e.g., a predefined frequency such as 1 Hz) whose period is much larger than the simulation time span, and f_0 is the fundamental frequency of the steady-state output waveform of circuit. For some circuits, f_0 is above 1 MHz; while for some other circuits f_0 is above 100 MHz, and for yet other circuits f_0 is above 1 GHz. In some

embodiments, the ratio between f_0 and f_1 is at least 10^6 to 1, while in some other embodiments the ratio between f_0 and f_1 is at least 10^4 to 1.

[0047] The method of predicting mismatch effects on transient circuit behaviors will be demonstrated using a typical buffer chain having mismatch variations. Figure 3 is an embodiment of a buffer chain 22. In this example, buffer chain 22 includes four CMOS buffers 23-26, cascaded in series. In some embodiments, a buffer chain may have more or fewer buffers. Each buffer includes an N-type MOS transistor and a P-type MOS transistor having their gates tied together as well as their respective source and drain tied together. CMOS buffer 23 receives at its gates a periodic input 28. CMOS buffer 26 generates output 29. As periodic input 28 propagates down the buffer chain, each individual buffer adds some time delay resulting in an overall time delay of the buffer chain 22. The variation of the overall delay of the buffer chain as a result of mismatch of the transistors in CMOS buffers 23-26 is of particular interest to circuit designers. This variation can be obtained using the noise simulation method described above.

[0048] Figure 4 is an embodiment of a modeled buffer chain combining noise sources with the model elements shown in Figure 1. Modeled buffer chain 34 includes four modeled MOS buffers 30-33, cascaded in series. Each buffer includes an N-type MOS transistor model and a P-type MOS transistor model, examples of which are shown in Figure 1. Each of modeled buffers 30-33 have their gates tied together as well as their respective source and drain tied together. Modeled MOS buffer 30 receives at its gates a periodic input 28. Modeled MOS buffer 33 generates output 29. As periodic input 28 propagates down the buffer chain, each individual buffer adds some time delay resulting in an overall time delay of the buffer chain 22. In each case, the MOS transistor has been modeled as having a noise source at its gate that simulates threshold voltage mismatches between the transistors in the buffers. Further, in this example, each MOS transistor in the buffers 30-33 has been modeled as having a noise source between its source and drain that simulates current factor (k) mismatches between the MOS transistors in the buffers. The current factor (k) relates the voltages applied to an MOS transistor to the drain current of the MOS transistor. The parameters of modeled buffer chain 34 are then input into a circuit simulator, such as ADS, SpectreRF, and HSPICE-RF, or any other simulator capable of simulating noise in electronic circuits.

[0049] Figure 5 shows how the output of a circuit simulator can be used to generate the delay variation of the buffer chain 22 using a frequency-domain periodic noise analysis.

Plot 40 represents the output PSD of the simulator where the buffer chain is excited by a square wave having a fundamental frequency f_0 . Also shown is the fundamental tone magnitude of the square wave having amplitude A_0 . The frequency f_1 is the frequency that is used for translation from mismatch parameters to noise parameters. From (i) the fundamental tone magnitude A_0 , (ii) f_0 and f_1 , and (iii) the noise PSD at frequency f_0+f_1 , the delay variation σ_{delay} for the buffer chain circuit can be calculated using the following equation:

$$\sigma_{\text{delay}}^2 = N(f_0+f_1)/4(f_0 \cdot A_0)^2.$$

[0050] Figure 6 shows how a circuit simulator can be used to generate the delay variation of the buffer chain 22 using a time-domain periodic noise analysis. To determine delay variation in the buffer chain 22 due to transistor mismatch using the proposed method, the SpectreRF simulator, for example, is configured to calculate a cyclostationary noise PSD at different time points, from which we can derive the voltage statistics of the output 29 over time. The voltage at output 29 is shown in time-domain plot 43 and includes the periodic steady state output of the buffer chain and the RMS variation of the output noise. The periodic steady state output component of the voltage output at output 29 can be represented by a time-series representation. In this example, the variance (of the buffer delay) is equal to the PSD at 1Hz. By superposing the voltage variation onto the nominal voltage waveform (periodic steady-state response), a statistical voltage waveform 44 is constructed. Then, the delay distribution of the buffer chain is derived from the cross-sectional probability distribution 45 at a voltage equal to the transition threshold, thus yielding the delay variation.

[0051] In this example, the simulated variation in delay, produced using the noise analysis simulation method, is very close (within a predefined simulator tolerance bound) to the results produced using a Monte-Carlo simulation method. Other simulated voltage noise-to-timing variation conversions can be used to generated predicted phase interpolator INL, as well as other circuit delay measurements.

[0052] The delay variation can also be calculated by using the equation

$$\sigma_{\text{delay}} = \sigma_{\text{voltage}} / (dV/dt)$$

at the transition threshold of the delay buffers, but the previously described methods tend to give more accurate results when the time resolution is coarse and the slope is not linear.

[0053] Figure 7 is a flow chart illustrating an embodiment of the method of simulating device mismatch effects on the transient circuit behaviors of an electronic circuit. The method includes translating device mismatch parameters into noise sources having AC noise parameters that correspond to the device mismatch parameters (52). Then a circuit

having circuit elements and the noise sources is modeled (53). A periodic time-varying noise analysis is performed on the modeled circuit to generate a noisy periodic steady-state output (also called a noisy periodic waveform) at a selected output of the electronic circuit (54), and the resulting noisy periodic steady-state output is translated into a prediction of the variation of a respective circuit parameter (55). In some embodiments, discussed below with reference to Figure 8, the noisy periodic waveform for the selected output is represented in the frequency domain by a Fourier-series representation of a nominal periodic steady-state waveform and a noise power spectral density of the selected output of the electronic circuit. In some other embodiments, as discussed above with reference to Figure 6, the noisy periodic waveform is represented in the time domain by a time-series representation of a nominal periodic steady-state waveform and an RMS variation of noise within the nominal periodic steady-state waveform at multiple points in time of the selected output of the electronic circuit.

[0054] In some cases, device mismatches may manifest themselves in quantities accumulated over time. An example is the variation in frequency of a ring oscillator, where the simulated voltage noise is the integral of the device-mismatch noise over time. To convert the accumulated noise to a value (i.e., a predicted value) that is proportional to the mismatch noise, e.g., a variation in clock period or frequency, the voltage noise must be scaled down by the oscillation frequency, and also by some constant scale factors, depending on the particular conventions for defining Fourier transforms in different simulators. As in the delay case, the variation in frequency can be simulated either by time-domain (see left portion of Figure 8) or by frequency-domain noise analysis (see right portion of Figure 8). However, the frequency-domain noise analysis is faster in execution as it needs only one simulation point.

[0055] Figure 8 shows how the variation of the period of a ring oscillator due to device mismatches can be determined (i.e., predicted) using either a frequency domain analysis or a time domain analysis. As shown, ring oscillator 60 is similar to the buffer chain from Figures 3, 4, and 6, except that an additional buffer has been added and the output of the last buffer in the chain is tied to the input of the first buffer in the chain.

[0056] In the frequency domain analysis, produced by performing a noise analysis simulation in the frequency domain, the PSD of the output of the ring oscillator 60 is shown in plot 61. Notably, the output noise is observed to be $1/f^3$ noise (because the output noise PSD varies in accordance with $1/f^3$) rather than the $1/f$ noise used for the input noise

parameters. In other words, in a simulation of a model of the ring oscillator 60 that includes noise sources as shown in Figure 4 for the modeled buffer chain 34, the power of the voltage noise (or current noise) at the output of the ring oscillator 60 varies in accordance with the inverse of the frequency cubed (i.e., $1/f^3$). By using the power P_1 of the output noise at f_0+f_1 (where, for example, f_1 is a low frequency such as 1 Hz) and the magnitude A_0 of the fundamental carrier (at frequency f_0) of the periodic steady state waveform, the predicted variation of either frequency or period can be calculated using the following equations:

$$\sigma_{\Delta f} = 2 \cdot P_1 / A_0; \text{ and}$$

$$\sigma_{\Delta T} = \sigma_{\Delta f} / f_0^2.$$

[0057] In the time domain, the periodic steady-state waveform and the RMS noise variation of the output of the ring oscillator 60, shown in plot 62, can be used to calculate the variation of the period or frequency of the ring oscillator as shown in distribution graph 63.

[0058] In some circuits, the simulated voltage noise may consist of both a proportional noise term and an integral or accumulated noise term. In these cases, decomposition of the simulated voltage noise into proportional and integral components can be accomplished by observing two points in the noise PSD. Assuming a mismatch-equivalent noise PSD that varies in accordance with $1/f$, the proportional noise term also has a $1/f$ PSD while the integral or accumulated noise term has $1/f^3$ PSD. The decomposition between proportional noise and accumulated noise is computed based on the slope between the two points in the noise PSD. For example, given two points P1 and P2 in a noise PSD (having units of V^2/Hz) at frequencies f_0+f_1 and f_0+f_2 (not shown), the ratio of the proportional noise power to the total noise power (P_1), gamma (γ), can be derived as follows.

$$-\gamma - 3(1-\gamma) = \frac{\log\left(\frac{P_2}{P_1}\right)}{\log\left(\frac{f_2}{f_1}\right)}$$

which, when solved for gamma, yields:

$$\gamma = \frac{1}{2} \left(\frac{\log\left(\frac{P_2}{P_1}\right)}{\log\left(\frac{f_2}{f_1}\right)} + 3 \right)$$

[0059] Having solved for gamma (γ), the proportional noise power is γP_1 and the integral noise power is $(1-\gamma)P_1$. Once the voltage noise is decomposed into the proportional

term and the accumulated terms, the corresponding delay variation or frequency variation can be calculated separately using the methodology explained above.

[0060] Mismatches in different circuit parameters of a circuit may be correlated. For example, transistors that are closely placed are likely to have more similar threshold voltages than those that are far apart. Without taking correlation into account and assuming all mismatches are independently random, one can get misleading estimates on the mismatch effects. For example, by assuming that the gates in the local logic path have independent variations in delay, one can over-estimate the minimum total delay while under-estimating the maximum total delay, which is undesirable for reliable timing closure.

[0061] While all noise sources in Verilog-A are assumed independent of one another, we can construct correlated noise sources by letting them share common noise sources. For example, assume that X, Y, and Z are independent noises with variance of 1 and zero mean. If we construct new noise sources A and B by the linear combination of X, Y, and Z, e.g., $A=a_1X+a_2Y$ and $B=b_1Y+b_2Z$, then A and B have variances of $a_1^2+a_2^2$ and $b_1^2+b_2^2$, respectively, and their correlation is equal to

$$\frac{a_2b_1}{\sqrt{(a_1^2 + a_2^2) \cdot (b_1^2 + b_2^2)}}.$$

Y is the common noise term shared by A and B, reflecting the correlation between them.

In general, N correlated noise sources $Y_1, Y_2, \dots, Y_N$ constructed by linearly combining N independent noise sources $X_1, X_2, \dots, X_N$ each with variance of 1 and mean of 0, i.e.,

$$Y = AX$$

have a covariance matrix C equal to:

$$C = AA^T$$

where X and Y are N-by-1 matrices with $\{X_i\}$'s and $\{Y_i\}$'s, respectively, and A is a N-by-N matrix with real elements. A^T is the transpose of the matrix A. The covariance matrix C is defined as $C = \{C_{ij}\}$'s where $\{C_{ij}\} = \text{cov}(Y_i, Y_j) = E(Y_i Y_j) - E(Y_i)E(Y_j)$.

[0062] The correlation matrix can be derived from this covariance matrix since the correlation coefficient between two variables X and Y, $\rho(X, Y)$ is defined as:

$$\rho(X, Y) = \frac{\text{cov}(X, Y)}{\sqrt{\text{cov}(X, X) \cdot \text{cov}(Y, Y)}}.$$

[0063] The variations that we observe in circuit performance parameters may have correlations as well. We can calculate this correlation between two performance variations based on their breakdowns of contributions from the individual independent noise sources. In other words, the RF circuit simulator reports the total noise power as a sum of individual contributions from the independent noise sources. This information is available to the user without any additional simulation.

[0064] If the two performance results share large contributions from the common noise sources, they are strongly correlated. To determine the correlation between two circuit performance results at two nodes of a circuit (e.g., delay variations at two nodes of the circuit), the covariance is first calculated, by multiplying each noise source's contributions to the two nodes and summing the square-roots of the products. Then, the correlation coefficient is equal to the covariance divided by the product of the two standard deviations ($\sigma_A \cdot \sigma_B$) of the circuit performance measurements at the two nodes. In some situations, two delays or two other performance parameters will be correlated with respect to variations (caused by device mismatches) induced when the circuit responds to a first sequence of input signals, but uncorrelated when the circuit responds to a second sequence of input signals.

[0065] In general, if we have N independent noise sources modeling device mismatches in the circuit and we are interested in the correlations among M different parameters, we can derive an equation

$$Y = AX$$

where X is a N-by-1 matrix with N independent noise sources with variance 1 and mean 0 and Y is a M-by-1 matrix denoting variations in the M result parameters. The M-by-N matrix $A = \{A_{ij}\}$ is derived from the breakdown of contributions, e.g., A_{ij} is equal to a square-root of the noise power contribution (expressed in V^2/Hz) from the j-th noise source to the i-th result parameter. Then the covariance matrix among the M result parameters are derived as:

$$C = AA^T.$$

The correlation matrix can be derived from this covariance matrix as previously described.

[0066] Figure 9 illustrates a computer 70 that can be used to perform the method described herein. The computer 70 typically includes one or more processing units (CPUs) 72, one or more network or other optional communications interfaces 74, memory 76, and one or more communication buses 78 for interconnecting these components. The communication buses 78 may include circuitry (sometimes called a chipset) that

interconnects and controls communications between system components. The front end server 108 may optionally include a user interface comprising a display device and a keyboard. Memory 76 includes high speed random access memory, such as DRAM, SRAM, DDR RAM or other random access solid state memory devices; and may include non-volatile memory, such as one or more magnetic disk storage devices, optical disk storage devices (e.g., CDROM or DVD), flash memory devices, other non-volatile solid state storage devices, or other computer-readable medium. Memory 76 may optionally include one or more storage devices remotely located from the CPU(s) 72. Memory 76 stores the following programs, modules and data structures, or a subset or superset thereof:

- an operating system 80 that includes procedures for handling various basic system services and for performing hardware dependent tasks;
- an optional network communication module (or instructions) 82 used for connecting the computer 70 to other computers (e.g., client computers or devices, web hosts, server computers) via the one or more optional communication network interfaces 74 and one or more communication networks, such as the Internet, other wide area networks, local area networks, metropolitan area networks, and the like;
- a circuit simulator (or instructions) 84 for simulating the operation of one or more specified circuits, including performing time domain and/or frequency domain noise analysis on specified circuits.

[0067] The circuit simulator (or instructions) 84 may include device models 86, for modeling devices such as resistors, transistors and other circuit elements; one or more circuit descriptions 88 (e.g., a circuit description specified using a circuit description language, such as Verilog-A or VHDL-A); and one or more programs that produce simulation results 90. In some embodiments, the circuit simulator can be executed remotely from a computer at another point in a network coupled to the computer 70 via communication interface 74.

[0068] Each of the above identified elements may be stored in one or more of the previously mentioned memory devices, and corresponds to a set of instructions for performing a function described above. The above identified modules or programs (i.e., sets of instructions) need not be implemented as separate software programs, procedures or modules, and thus various subsets of these modules may be combined or otherwise re-arranged in various embodiments. In some embodiments, memory 76 may store a subset of

the modules and data structures identified above. Furthermore, memory 76 may store additional modules and data structures not described above.

[0069] The method described herein may be performed using various simulation software products along with the additional translation steps. The additional translation steps may be integrated into the software products as add-on software or can be performed using a separate computer program. Alternatively, the method may be implemented in a single software program other than those software programs described herein. Finally, the additional translation steps may be carried out by hand or by using a calculator.

[0070] The foregoing descriptions of specific embodiments of the present invention are presented for purposes of illustration and description. They are not intended to be exhaustive or to limit the invention to the precise forms disclosed. Rather, it should be appreciated that many modifications and variations are possible in view of the above teachings. The embodiments were chosen and described in order to best explain the principles of the invention and its practical applications, to thereby enable others skilled in the art to best utilize the invention and various embodiments with various modifications as are suited to the particular use contemplated.

WHAT IS CLAIMED IS:

1. A method of simulating device mismatch effects on transient circuit behaviors, comprising:
 - 5 providing a circuit model, corresponding to an electronic circuit, the circuit model including a plurality of circuit elements and one or more noise sources, wherein the one or more noise sources have AC noise parameters that correspond to one or more device mismatch parameters associated with one or more circuit elements of the plurality of circuit elements;
 - 10 performing a periodically time varying noise analysis on the circuit model to generate a simulation output corresponding to a noisy periodic waveform at a selected output of the electronic circuit; and
translating the noisy periodic waveform into a result, the result representing a variation of a respective circuit parameter associated with the electronic circuit.
- 15 2. The method of claim 1, wherein the noisy periodic waveform is represented in the frequency domain by a Fourier-series representation of a nominal periodic steady-state waveform and a noise power spectral density of the selected output of the electronic circuit.
3. The method of claim 1, wherein the noisy periodic waveform is represented in the time domain by a time-series representation of a nominal periodic steady-state waveform and
20 an RMS variation of noise within the nominal periodic steady-state waveform at multiple points in time of the selected output of the electronic circuit.
4. The method of claim 1, wherein the mismatch parameters represent DC offsets.
5. The method of claim 1, wherein the one or more noise sources include one or more $1/f$ noise sources.
- 25 6. The method of claim 1, wherein the one or more noise sources include one or more $1/f^n$ noise sources, where n is a number greater than one.
7. The method of claim 1, wherein at least one of the noise sources represents voltage noise.

8. The method of claim 1, wherein at least one of the noise sources represents current noise.

9. The method of claim 1, wherein one or more of the AC noise parameters varies in response to a bias level of one or more of the circuit elements.

5 10. The method of claim 1, further comprising performing a sensitivity analysis on the modeled circuit that provides a breakdown of individual noise source contributions to a total noise of the noisy periodic waveform.

10 11. The method of claim 10, further comprising using the breakdown of the individual noise source contributions to determine which device mismatch most influences the respective circuit parameter.

12. The method of claim 1, further comprising constructing the AC noise sources from linear combinations of shared independent noise sources to simulate the effects of correlations between two or more mismatch parameters.

15 13. The method of claim 10, further comprising using the breakdown of individual noise source contributions to simulate correlations between variations in two or more circuit parameters due to device mismatches.

14. The method of claim 1, wherein the variation of the respective circuit parameter is variation of a voltage.

20 15. The method of claim 1, wherein the variation of the respective circuit parameter is variation of a current.

16. The method of claim 1, wherein the variation of the respective circuit parameter is variation of a time delay.

17. The method of claim 1, wherein the variation of the respective circuit parameter is variation of a frequency.

25 18. The method of claim 1, wherein the variation of the respective circuit parameter is variation of a time period.

19. The method of claim 1, wherein the variation of the respective circuit parameter is an integral nonlinearity value.

20. The method of claim 1, wherein the variation of the respective circuit parameter is a differential nonlinearity value.

21. The method of claim 1, wherein the noisy periodic waveform is decomposed into a proportional noise term and an integral noise term so that the resulting variations can be calculated separately.

22. A computer-readable medium comprising one or more computer programs that are stored on the computer-readable medium and that are executable by a computer so as to perform a process, the one or more computer programs including instructions for performing a method of simulating device mismatch effects on transient circuit behaviors, the instructions comprising:

instructions for providing a circuit model, corresponding to an electronic circuit, the circuit model including a plurality of circuit elements and one or more noise sources, wherein the one or more noise sources have AC noise parameters that correspond to one or more device mismatch parameters associated with one or more circuit elements of the plurality of circuit elements;

instructions for performing a periodically time varying noise analysis on the circuit model to generate a simulation output representing a noisy periodic waveform at a selected output of the electronic circuit; and

instructions for translating the noisy periodic waveform into a result, the result representing a variation of a respective circuit parameter associated with the electronic circuit.

23. The computer-readable medium of claim 22, wherein the noisy periodic waveform is represented in the frequency domain by a Fourier-series representation of a nominal periodic steady-state waveform and a noise power spectral density of the selected output of the electronic circuit.

24. The computer-readable medium of claim 22, wherein the noisy periodic waveform is represented in the time domain by a time-series representation of a nominal periodic steady-state waveform and an RMS variation of noise within the nominal periodic steady-state waveform at multiple points in time of the selected output of the electronic circuit.

25. The computer-readable medium of claim 22, wherein the mismatch parameters represent DC offsets.

26. The computer-readable medium of claim 22, wherein the one or more noise sources include one or more $1/f$ noise sources.

5 27. The computer-readable medium of claim 22, wherein the one or more noise sources include one or more $1/f^n$ noise sources, where n is a number greater than one.

28. The computer-readable medium of claim 22, wherein at least one of the noise sources represents voltage noise.

10 29. The computer-readable medium of claim 22, wherein at least one of the noise sources represents current noise.

30. The computer-readable medium of claim 22, wherein one or more of the AC noise parameters varies in response to a bias level of one or more of the circuit elements.

31. The computer-readable medium of claim 22, wherein the instructions for performing a periodically time varying noise analysis on the modeled circuit comprise a circuit simulator.

15 32. The computer-readable medium of claim 22, further comprising instructions for performing a sensitivity analysis on the modeled circuit that provides a breakdown of individual noise source contributions to a total noise of the noisy periodic waveform.

20 33. The computer-readable medium of claim 32, further including instructions for using the breakdown of the individual noise source contributions to determine which device mismatch most influences the respective circuit parameter.

34. The computer-readable medium of claim 32, further comprising instructions for using the breakdown of individual noise source contributions to simulate correlations between variations in two or more circuit parameters due to device mismatches.

25 35. The computer-readable medium of claim 22, further comprising instructions for constructing the AC noise sources from linear combinations of shared independent noise sources to simulate the effects of correlations between two or more mismatch parameters.

36. The computer-readable medium of claim 22, wherein the variation of the respective circuit parameter is variation of a voltage.

37. The computer-readable medium of claim 22, wherein the variation of the respective circuit parameter is variation of a current.

5 38. The computer-readable medium of claim 22, wherein the variation of the respective circuit parameter is variation of a time delay.

39. The computer-readable medium of claim 22, wherein the variation of the respective circuit parameter is variation of a frequency.

10 40. The computer-readable medium of claim 22, wherein the variation of the respective circuit parameter is variation of a time period.

41. The computer-readable medium of claim 22, wherein the variation of the respective circuit parameter is an integral nonlinearity value.

42. The computer-readable medium of claim 22, wherein the variation of the respective circuit parameter is a differential nonlinearity value.

15 43. The computer-readable medium of claim 22, wherein the noisy periodic waveform is decomposed into a proportional noise term and an integral noise term so that the resulting variations can be calculated separately.

Translation of Device Mismatch Statistics to Low
Frequency Noise Statistics

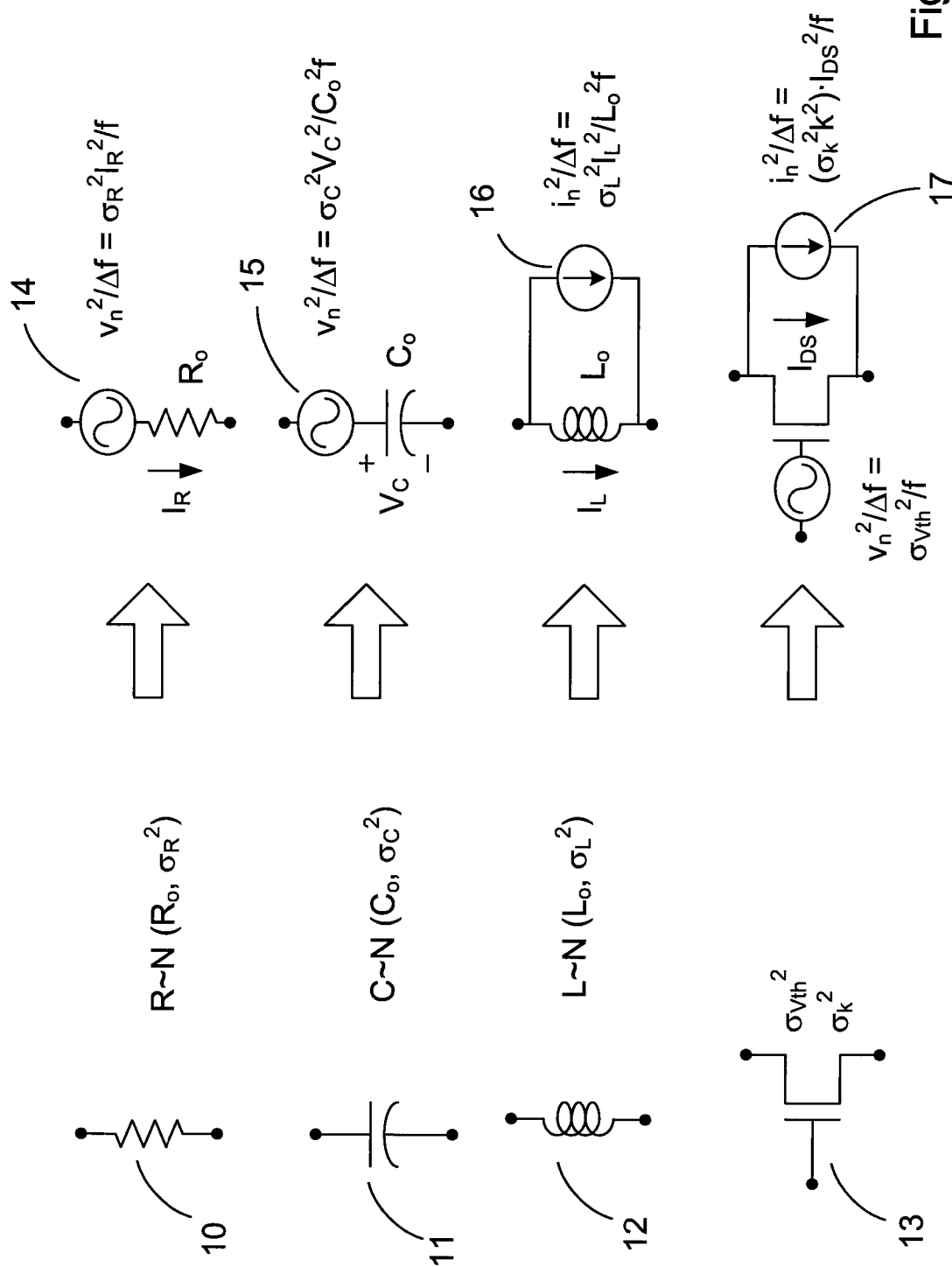


Figure 1

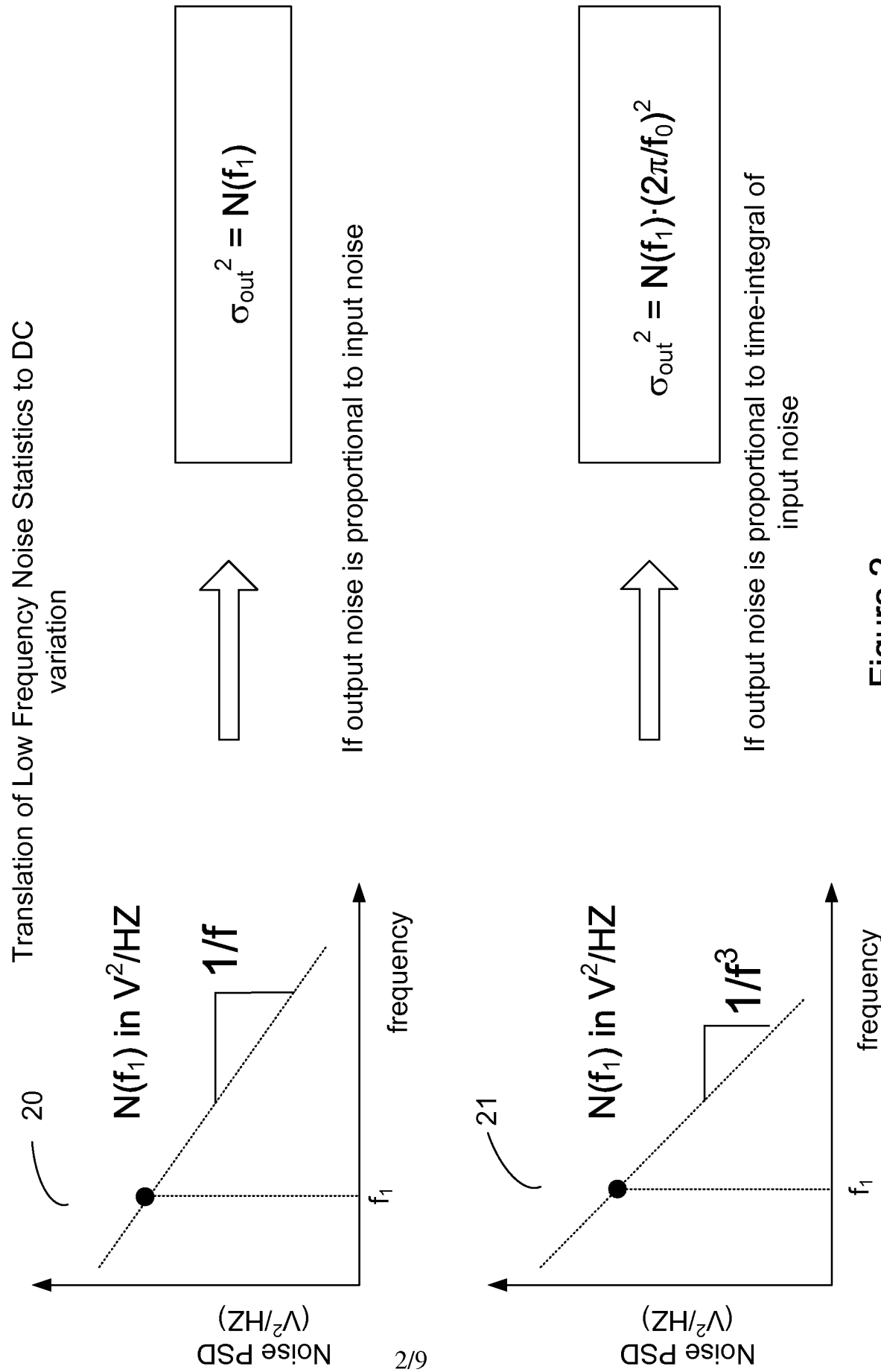


Figure 2

Buffer Chain

22

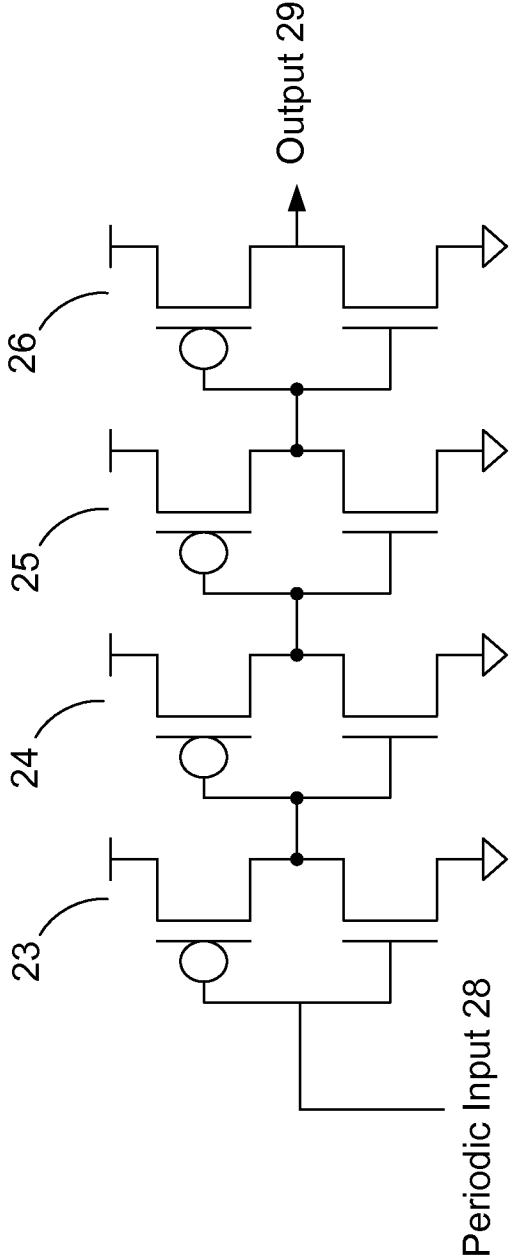


Figure 3

Modeled Buffer Chain Using Noise Sources

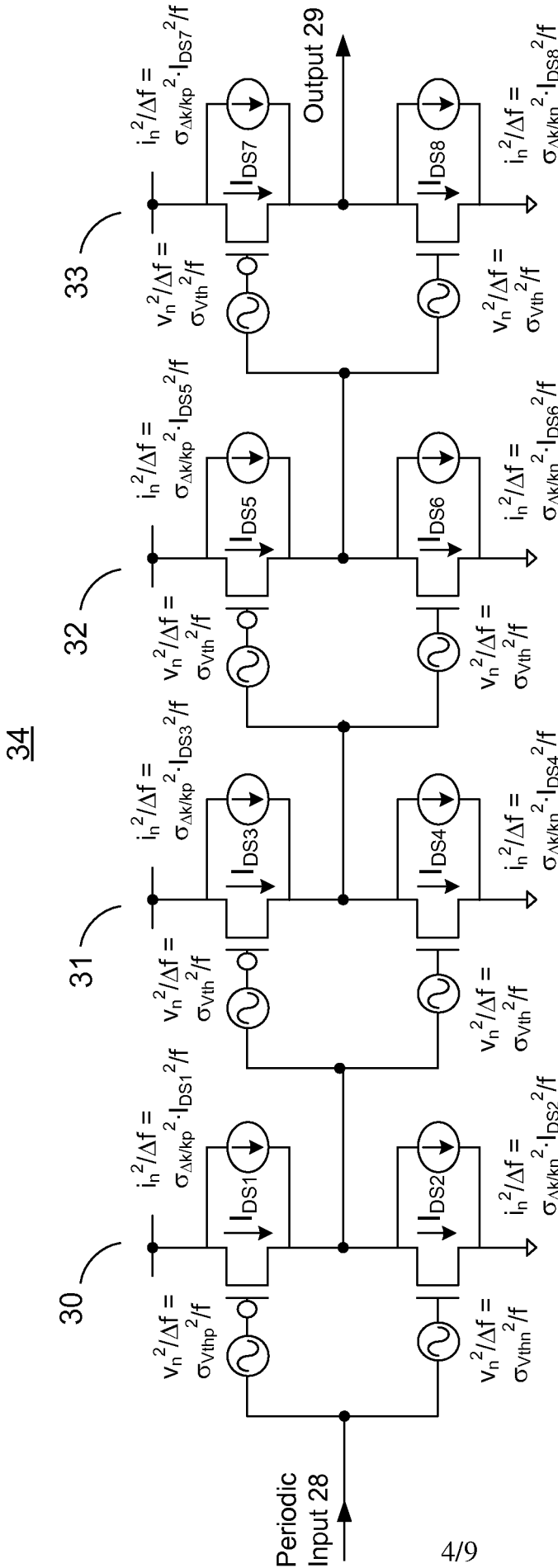


Figure 4

Translation of Low Frequency Noise Statistics In a Buffer Chain to a Delay Variation

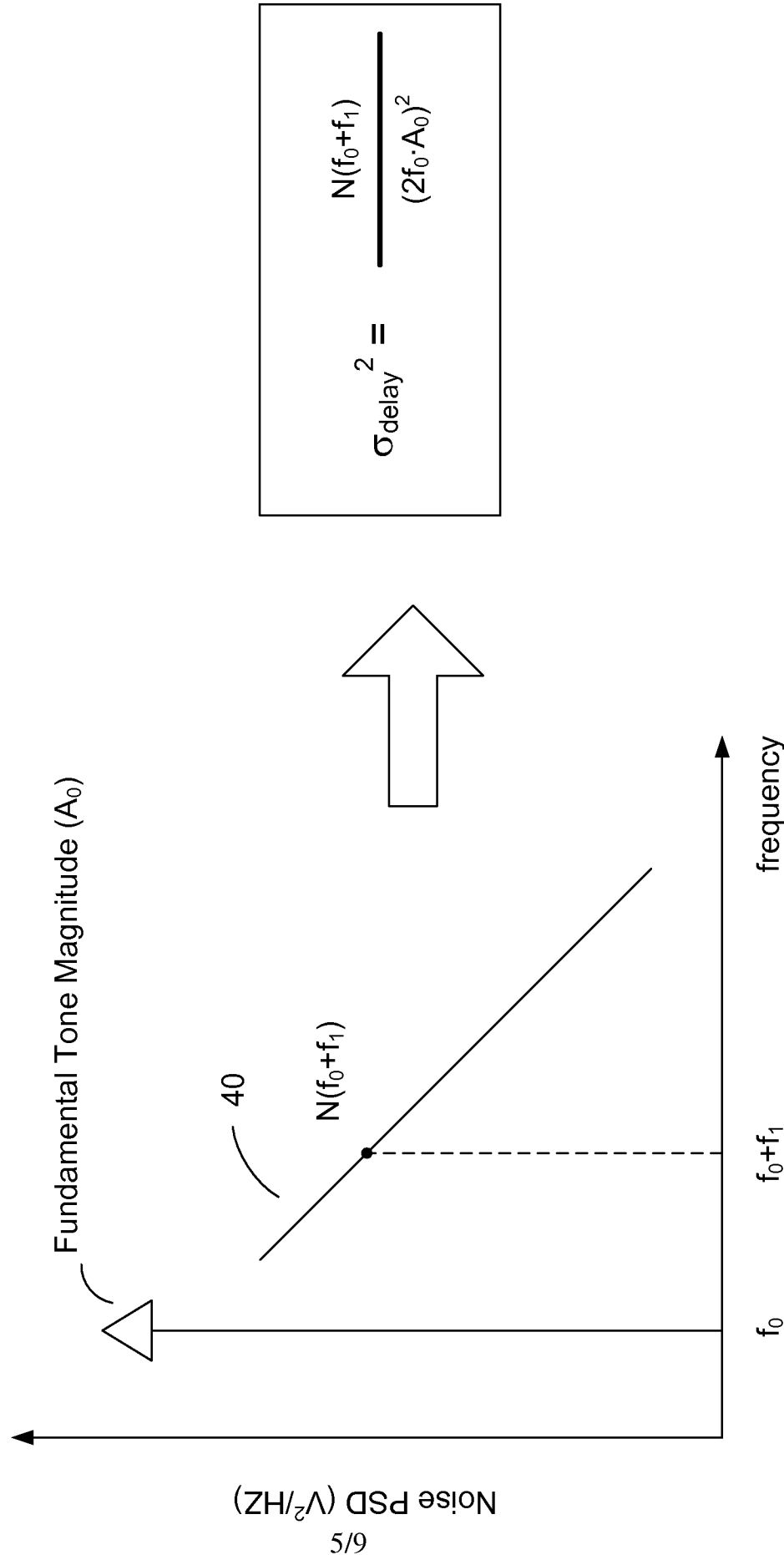


Figure 5

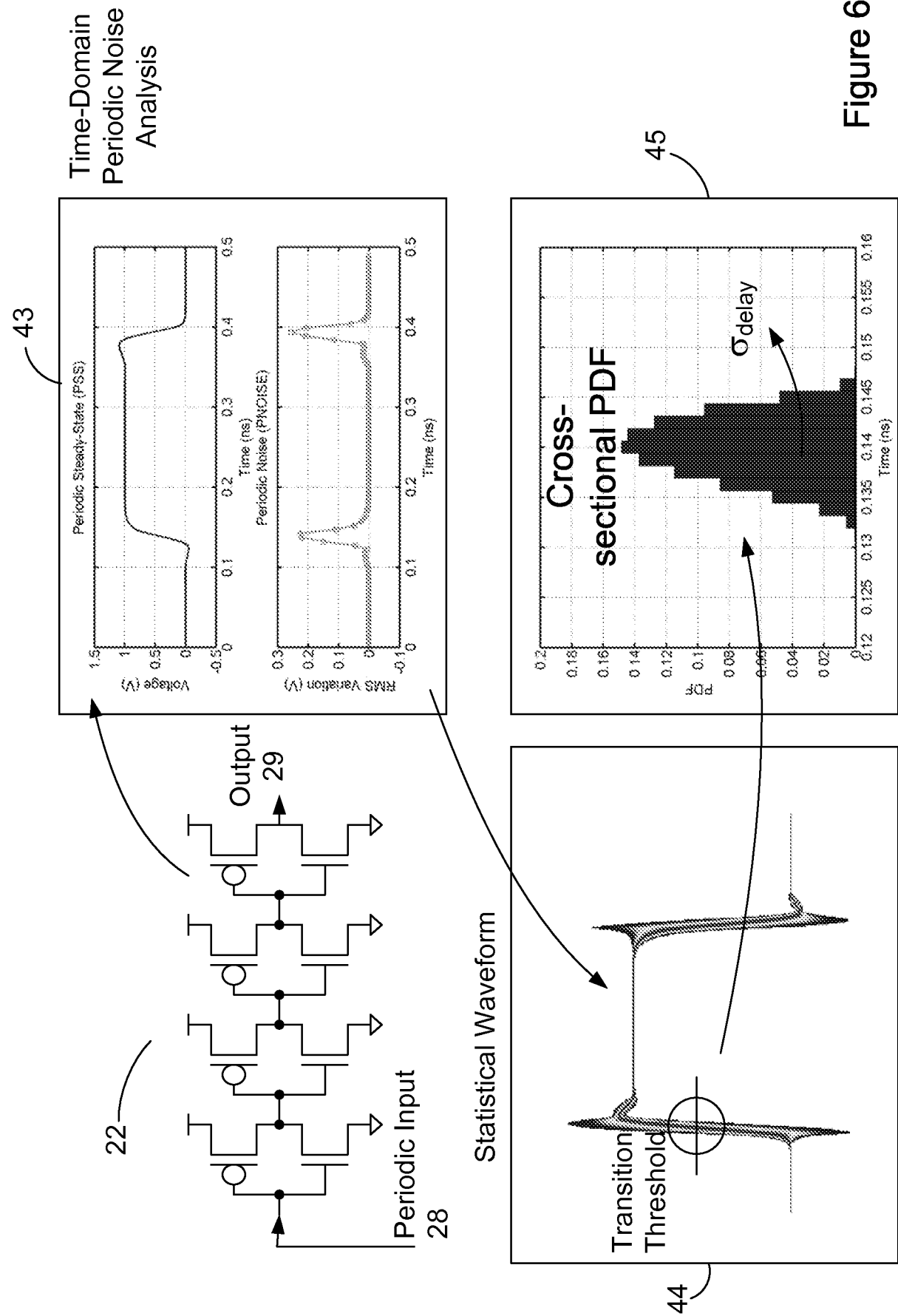
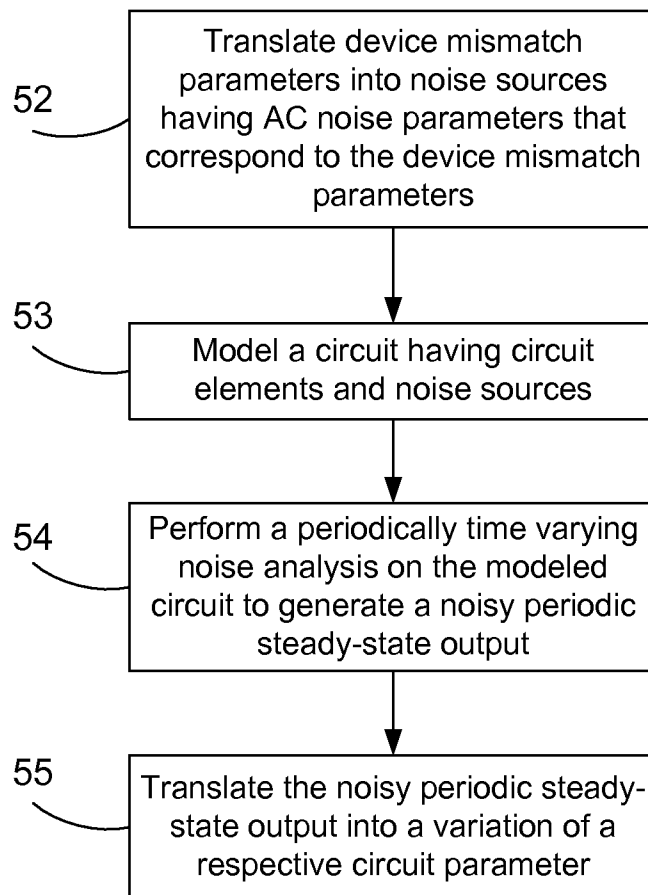


Figure 6

**Figure 7**

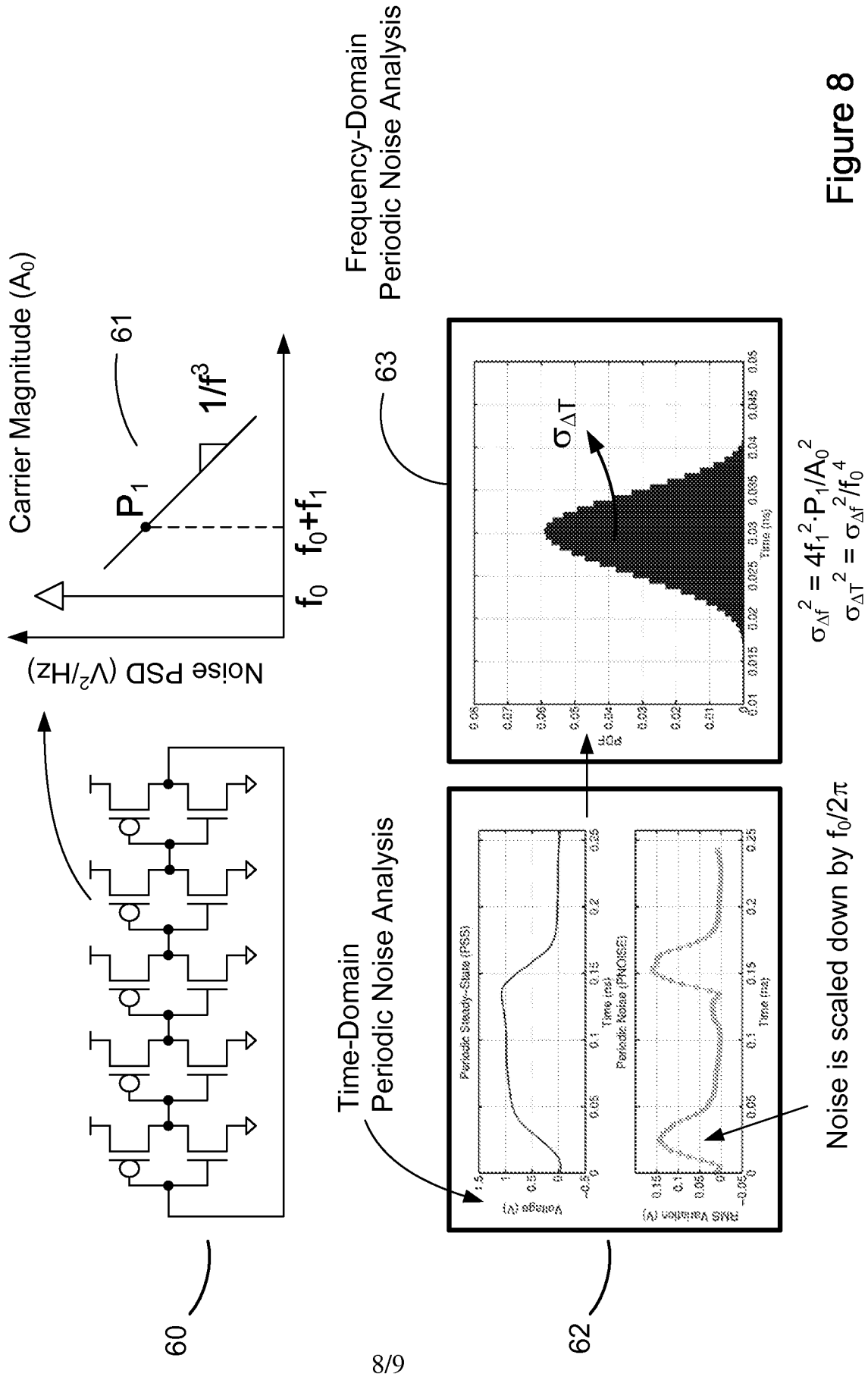


Figure 8

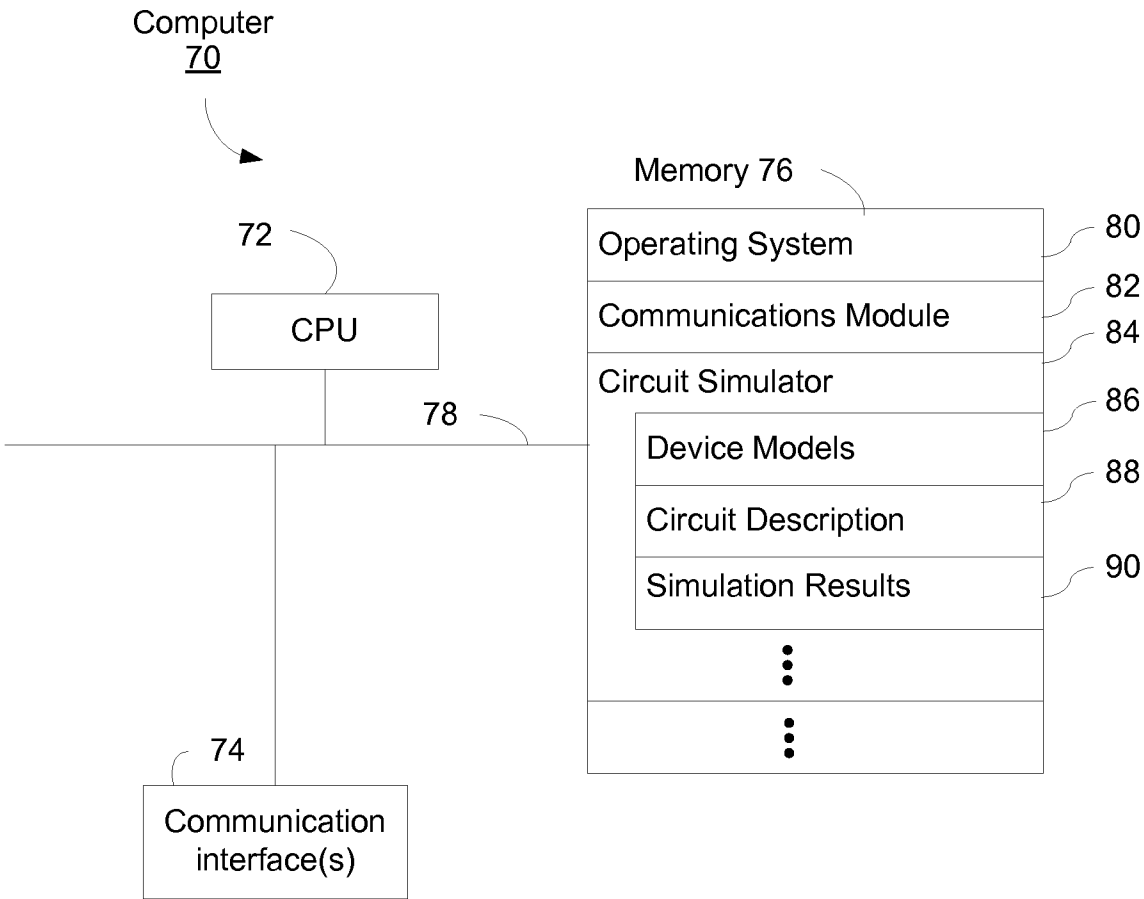


Figure 9