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(54) **Title**: PAUSING COLUMN READOUT IN IMAGE SENSORS

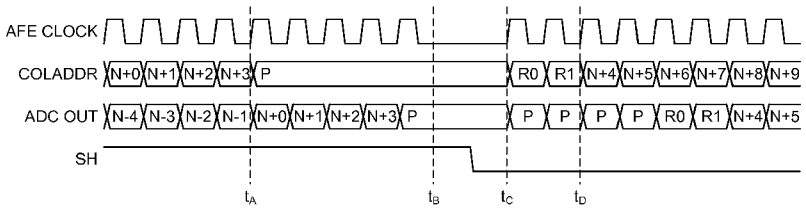

FIG. 9

(57) **Abstract**: An image sensor includes a two-dimensional array of pixels having multiple column outputs and an output circuit connected to each column output. Each output circuit is configured to operate concurrent sample and read operations. An analog front end (AFE) circuit processes pixel data output from the output circuits and an AFE clock controller transmits an AFE clocking signal to the AFE circuit to effect processing of the pixel data. A timing generator outputs a column address sequence that is received by a column decoder. During one or more sample operations the timing generator suspends the column address sequence and subsequently during the one or more sample operations the AFE clock controller suspends the AFE clocking signal. The AFE clocking signal and the column address sequence resume at the end of the one or more sample operations.

WO 2011/081978 A1

PAUSING COLUMN READOUT IN IMAGE SENSORS

TECHNICAL FIELD

The present invention relates generally to electronic image sensors for use in digital cameras and other image capture devices, and more particularly to sampling and readout techniques for use with an electronic image sensor.

BACKGROUND

A typical solid-state electronic image sensor comprises a number of light-sensitive picture elements ("pixels") arranged in a two-dimensional array. These pixels are generally formed in a semiconductor material and have the property of accumulating electric charges resulting from electron-hole pairs created by the photons entering the pixels. In a charge-coupled device (CCD) image sensor, the accumulated charges may be read out of the image sensor by shifting the charge out of the array. Alternatively, in an active pixel sensor (APS), the charge may be converted to a voltage by circuitry located within the array in proximity to the pixel and the resulting voltages may be sampled and read in a scanning fashion. APS image sensors are also known as Complementary Metal Oxide Semiconductor (CMOS) image sensors.

In accordance with conventional practice, sampling and readout of the pixel signals in a CMOS image sensor generally involves sampling all the pixel signals in a given row into column circuits, and then reading out the entire row of sampled pixel signals in a sequential fashion from the column circuits. This sampling and readout operation proceeds row by row until the entire pixel array is read out. In conventional practice, the sampling and readout operations do not overlap in time, and the sampling operation represents a significant fraction of the total time required to read the pixel signals from the array.

U.S. Patent Application Publication No. 2009/0195681, entitled "Sampling and Readout of an Image Sensor Having a Sparse Color Filter Array Pattern," which is incorporated by reference herein, discloses sampling and readout for a CMOS image sensor where sampling of pixel signals occurs concurrently with readout of previously sampled pixels. In this scheme, two column circuits are

provided for each column signal output from the pixel array. A pixel signal from a selected pixel is sampled by one of the column circuits at the same time that a previously sampled pixel signal in the other column circuit is being read out. By overlapping the sampling and readout operations in this way, the amount of time used for the sampling operation is eliminated. This reduces the total time required to read the pixel signals from the array and increases the frame readout rate of the image sensor.

The sampling operation may sample system noise in addition to pixel signals. Since the sampling operation described above occurs simultaneously for an entire row of pixel signals, there is the potential for captured system noise to be correlated for an entire row or a portion of a row of sampled pixel signals. In an imaging system as described above, this row correlated noise produces an objectionable visual artifact in the captured image. In conventional non-overlapping sampling and readout of a CMOS image sensor, the system noise may be reduced by shutting off noise generators during the sampling time, notably clock signals to portions of the readout circuitry. However, in the overlapping sampling and readout operation outlined above, turning off the clock signals to the readout circuitry during sampling is not an option as the readout operation takes place concurrently with the sampling operation. Consequently, although the concurrent sampling and readout technique provides an improvement in readout time, it also increases susceptibility to sampling system noise and incurring objectionable row-correlated visual artifacts.

SUMMARY

Briefly summarized, according to one aspect of the present invention, the invention provides an image sensor that includes a two-dimensional array of pixels having multiple column outputs and an output circuit connected to each column output. Each output circuit is configured to operate concurrent sample and read operations. An analog front end (AFE) circuit processes pixel data output from the output circuits and an AFE clock controller transmits an AFE clocking signal to the AFE circuit to effect processing of the pixel data. A timing generator outputs a column address sequence that is received by a column

decoder. During one or more sample operations the timing generator suspends the column address sequence and subsequently during the one or more sample operations the AFE clock controller suspends the AFE clocking signal. The AFE clocking signal and the column address sequence resume at the end of the sample operation.

Another aspect of the present invention provides a method for reading out an image from an image sensor. The image sensor includes a two-dimensional array of pixels having a plurality of column outputs and an output circuit connected to each column output, where each output circuit is configured to operate concurrent sample and read operations. The method begins by initiating concurrent sample and read operations in each output circuit. During a first sample operation, such as a sample operation for pixel RESET signals, a column address sequence is suspended. Subsequently during the first sample operation, an AFE clocking signal is suspended. After the first sample operation is complete, the AFE clocking signal and the column address sequence resume. During a second sample operation, such as a sample operation for a pixel SIGNAL signals, the column address sequence is suspended again. Subsequently during the second sample operation the AFE clocking signal is suspended again. After the second sample operation is complete, the AFE clocking signal and the column address sequence resume. Suspension of the AFE clocking signal and the column address sequence can repeat until all of the signals have been sampled and read out of the pixel array. The pixel data output from each output circuit can be stored while the AFE clocking signal and the column address sequence are suspended. Storing of the pixel data selectively delays the output of the pixel data to effect an uninterrupted output data flow of pixel data.

ADVANTAGEOUS EFFECT

Image sensors and image capture methods in accordance with the present invention are useful for reducing the time required to capture images while reducing noise in the captured images. These image sensors and methods have a broad application and numerous types of image capture devices can effectively use these sensors and methods.

BRIEF DESCRIPTION OF THE DRAWINGS

Embodiments of the invention are better understood with reference to the following drawings. The elements of the drawings are not necessarily to scale relative to each other.

FIG. 1 is a simplified block diagram of an image capture device in an embodiment in accordance with the invention;

FIG. 2 is a block diagram of a top view of a CMOS image sensor in an embodiment in accordance with the invention;

FIG. 3 is a more detailed diagram of pixel array 202 shown in **FIG. 2**;

FIG. 4 is a block diagram of AFE circuit 212 shown in **FIG. 2**;

FIG. 5 is a circuit diagram of a portion of sampling and readout output circuitry 210 shown in **FIG. 2**;

FIG. 6 depicts an exemplary timing diagram for non-concurrent sample and read operations for sampling and readout output circuits 210 shown in **FIG. 2**;

FIG. 7 depicts an exemplary timing diagram for concurrent sample and read operations for column output circuits 210 shown in **FIG. 2**;

FIG. 8 is a flowchart of a method for pausing column readout in an embodiment in accordance with the invention;

FIG. 9 depicts an exemplary timing diagram for the method shown in **FIG. 8**;

FIG. 10 depicts a block diagram of a circuit that is used to make the interrupted data stream from **FIG. 9** continuous with the use of a digital buffer;

FIG. 11 depicts an exemplary timing diagram for the circuit shown in **FIG. 10**; and

FIG. 12 is a circuit diagram of a portion of an alternate sampling and readout output circuitry 210 shown in **FIG. 2**.

DETAILED DESCRIPTION

Throughout the specification and claims, the following terms take the meanings explicitly associated herein, unless the context clearly dictates otherwise. The meaning of "a," "an," and "the" includes plural reference, the

meaning of "in" includes "in" and "on." The term "connected" means either a direct electrical connection between the items connected, or an indirect connection through one or more passive or active intermediary devices. The term "circuit" means either a single component or a multiplicity of components, either active or passive, that are connected together to provide a desired function. The term "signal" means at least one current, voltage, or data signal.

Additionally, directional terms such as “on”, “over”, “top”, “bottom”, are used with reference to the orientation of the Figure(s) being described. Because components of embodiments of the present invention can be positioned in a number of different orientations, the directional terminology is used for purposes of illustration only and is in no way limiting.

Referring to the drawings, like numbers indicate like parts throughout the views.

FIG. 1 is a simplified block diagram of an image capture device in an embodiment in accordance with the invention. Image capture device 100 is implemented as a digital camera in **FIG. 1**. Those skilled in the art will recognize that a digital camera is only one example of an image capture device that can utilize an image sensor incorporating the present invention. Other types of image capture devices, such as, for example, cell phone cameras, scanners, and digital video camcorders, can be used with the present invention.

In digital camera 100, light 102 from a subject scene is input to an imaging stage 104. Imaging stage 104 can include conventional elements such as a lens, a neutral density filter, an iris and a shutter. Light 102 is focused by imaging stage 104 to form an image on image sensor 106. Image sensor 106 captures one or more images by converting the incident light into electrical signals. Digital camera 100 further includes processor 108, memory 110, display 112, and one or more additional input/output (I/O) elements 114. Although shown as separate elements in the embodiment of **FIG. 1**, imaging stage 104 may be integrated with image sensor 106, and possibly one or more additional elements of digital camera 100, to form a camera module. For example, a processor or a memory may be integrated with image sensor 106 in a camera module in embodiments in accordance with the invention.

Processor 108 may be implemented, for example, as a microprocessor, a central processing unit (CPU), an application-specific integrated circuit (ASIC), a digital signal processor (DSP), or other processing device, or combinations of multiple such devices. Various elements of imaging stage 104 and image sensor 106 may be controlled by timing signals or other signals supplied from processor 108.

Memory 110 may be configured as any type of memory, such as, for example, random access memory (RAM), read-only memory (ROM), Flash memory, disk-based memory, removable memory, or other types of storage elements, in any combination. A given image captured by image sensor 106 may be stored by processor 108 in memory 110 and presented on display 112. Display 112 is typically an active matrix color liquid crystal display (LCD), although other types of displays may be used. The additional I/O elements 114 may include, for example, various on-screen controls, buttons or other user interfaces, network interfaces, or memory card interfaces.

It is to be appreciated that the digital camera shown in **FIG. 1** may comprise additional or alternative elements of a type known to those skilled in the art. Elements not specifically shown or described herein may be selected from those known in the art. As noted previously, the present invention may be implemented in a wide variety of image capture devices. Also, certain aspects of the embodiments described herein may be implemented at least in part in the form of software executed by one or more processing elements of an image capture device. Such software can be implemented in a straightforward manner given the teachings provided herein, as will be appreciated by those skilled in the art.

Referring now to **FIG. 2**, there is shown a block diagram of a top view of image sensor 106 in an embodiment in accordance with the invention. Image sensor 106 includes a number of pixels 200 that are typically arranged in rows and columns to form a pixel array 202. Image sensor 106 further includes column decoder 204, row decoder 206, digital logic 208, multiple sampling and readout output circuits 210, and analog front end (AFE) circuit 212. Row decoder 206 provides control signals to the rows of pixels 200 in pixel array 202. Some of

these control signals are used to read out the signals from individual rows of pixels. Other control signals are used to reset individual rows of pixels to a known potential.

Digital logic 208 includes control register 214, timing generator 216, analog front end (AFE) clock controller 218, analog front end (AFE) interface 220, and digital buffer 222. In an embodiment in accordance with the invention, control register 214 stores the number of clock periods that occur prior to pausing the column addressing signals. Control register 214 can store one or more values that collectively control the respective onsets and durations of the suspensions of the column address sequence and the AFE clocking signal. The column addressing signals are preferably paused near the end of the sampling operation. If the addressing signals are paused too close to the end of the sampling period, there can still be noise from the clocking/addressing that will show as image artifacts. If the addressing signals are paused too soon, then performance will be degraded. The timing of when the addressing signals are paused is determined by the minimum length of the pause that effectively reduces or eliminates noise.

Timing generator 216 produces the timing and control signals needed to operate image sensor 106, including address signals to column decoder 204 and row decoder 206 that control the output of the column and row addressing signals. AFE clock controller 218 enables and disables (i.e., suspends) the AFE clock signal input to AFE circuit 212. The AFE clock controller receives an ENABLE signal from the timing generator, and when enabled it produces the AFE clock signal. The timing generator counts clock pulses and produces the ENABLE signal (used by the AFE clock controller) to suspend the AFE clock signal in an embodiment in accordance with the invention. AFE interface 220 receives data output from AFE circuit 212 and digital buffer 222 stores the data output from AFE circuit 212 to produce a non-interrupted flow of data output from the image sensor.

Each column of pixels in pixel array 202 is electrically connected to a sampling and readout output circuit 210. Sampling and readout output circuits 210 sample and hold the analog signals output from the columns of pixels. Column decoder 204 sequentially addresses sampling and readout output circuits

210 to read out the sampled analog signals. Each analog signal output from the sampling and readout output circuits 210 is amplified, conditioned, and converted to a digital signal by AFE circuit 212.

Column decoder 204 and row decoder 206 have several alternative implementations that are well known to those skilled in the art. For example, column decoder 204 may be a one-of-many decoder that accepts a digital column address in binary code, Gray code, or some other code and provides an output that selects a specific sampling and readout output circuit based on the column address. Alternatively, column decoder 204 may be a shift register that selects the sampling and readout output circuits in sequence. Similar options are available for row decoder 206.

Furthermore, the sequence of reading the sampled pixel signals from the sampling and readout output circuits is not required to follow a strict order or numerical sequence, but can include skipping one or more sampling and readout output circuits, reading different blocks of sampling and readout output circuits in different sequence orders, and reading sampling and readout output circuits in a pseudo-random sequence. Similar options apply to the row control signals provided by row decoder 206. All these options and others known to skilled practitioners are within the scope of this invention, and the terms column decoder and row decoder do not limit any methods and apply broadly to all methods for selecting columns and rows, respectively. Additionally, all sequences of selecting sampling and readout output circuits for reading and all sequences of controlling row-based operations are within the scope of this invention.

Image sensor 106 is implemented as an x-y addressable image sensor formed on a single monolithic semiconductor die in an embodiment in accordance with the invention. In another embodiment in accordance with the invention, image sensor 106 is implemented as an x-y addressable image sensor with the components or circuitry formed on two or more stacked semiconductor die. A CMOS image sensor is one example of an x-y addressable image sensor.

Portions of the functional blocks of image sensor 106 may be implemented external to image sensor 106 in other embodiments in accordance with the invention. By way of example only, timing generator 216 may be implemented in

a field programmable gate array (FPGA). Alternatively, AFE circuit 212 may be included in a separate integrated circuit.

Functionality associated with the sampling and readout of pixel array 202 and the processing of corresponding image data may be implemented at least in part in the form of software that is stored in memory 110 (see **FIG. 1**) and executed by processor 108. Portions of the sampling and readout circuitry may be arranged external to image sensor 106, or formed integrally with pixel array 200, for example, on a common integrated circuit with photodetectors and other elements of the pixel array. Those skilled in the art will recognize that other peripheral circuitry configurations or architectures can be implemented in other embodiments in accordance with the invention.

FIG. 3 is a more detailed diagram of pixel array 202 shown in **FIG. 2**. Pixel array 200 includes an active area 300 having columns 302 and rows 304 of photoactive pixels 300. Photoactive pixels 300 each include one or more photodetectors (not shown) that collect and store photo-generated charge carriers in response to incident light. Photoactive pixels 300 are used to capture an image of a scene.

Reference area 306 includes rows of dark reference pixels while reference area 308 includes columns of dark reference pixels. Dark reference pixels are typically covered by an opaque layer or light shield to prevent light from striking the pixels. The dark reference pixels are used to measure the amount of charge produced in image sensor 106 without light. Dark reference pixels may be constructed with or without photodetectors in embodiments in accordance with the invention.

The signals read out of the rows of dark reference pixels in reference area 306 are averaged together to provide a column-by-column dark offset reference in an embodiment in accordance with the invention. The dark offset reference is used to correct for column fixed pattern offset (column fixed pattern noise). The signals read out of the columns of dark reference pixels in area 308 are averaged together to provide a row-by-row dark offset reference in an embodiment in accordance with the invention. The dark offset reference is used to correct for row temporal offset (row temporal noise).

Those skilled in the art will recognize pixel array 202 can have millions to tens of millions of pixels that can be arranged in any configuration. By way of example only, rows of dark reference pixels can be situated at the top and bottom of pixel array 202. Alternatively, the photoactive pixels can be confined in a sub-array with rows and columns of dark reference pixels surrounding each edge of the sub-array. Another alternative disperses the dark reference pixels within pixel array 202 such that dark reference pixels are intermingled with photoactive pixels.

Referring now to **FIG. 4**, there is shown a block diagram of AFE circuit 212 shown in **FIG. 2**. AFE circuit 212 receives a differential pair of analog signals from each pixel in an embodiment in accordance with the invention. One analog signal is identified as RESET and the other signal as SIGNAL. AFE circuit 212 amplifies and conditions the RESET and SIGNAL analog signals, and converts the analog signals to digital signals.

AFE circuit 212 includes one or more signal processing blocks. In the illustrated embodiment, AFE circuit 212 includes analog to digital converter (ADC) 400 and analog signal processor (ASP) 402. In an embodiment in accordance with the invention, ASP 402 includes two cascaded variable gain amplifiers 404, 406 connected in series, a signal summing node 408 connected to an input of the first variable gain amplifier in the series (e.g., amplifier 406), and a digital to analog converter (DAC) 410 connected to the signal summing node. RESET and SIGNAL signals are input into signal summing node 408 and the output of the second variable gain amplifiers (e.g., amplifier 404) is input into ADC 400. Other embodiments in accordance with the invention include one or more variable gain amplifiers. DAC 410 and signal summing node 408 are used for analog dark offset correction. A clock signal, AFE CLOCK, is provided to the ADC 400 and the ASP 402. This clock signal synchronizes the sampling and conversion operations of the ADC 400 and ASP 402 with the sequential output of the sampling and readout output circuits 210. Although typical design of the elements of ASP 402 includes switched capacitor or other design approaches that require the use of a clocking signal such as AFE CLOCK, alternative non-

switching design approaches that do not require AFE CLOCK may be used for the elements of ASP 402.

FIG. 5 is a circuit diagram of a portion of sampling and readout output circuitry 210 shown in **FIG. 2**. Sampling and readout output circuitry 210 includes including sampling switches 500, sample and hold capacitors 502, readout (or column enable) switches 504, and differential analog output bus 506. Differential analog output bus 506 connects to AFE circuit 212 shown in **FIG. 2**.

FIG. 5 depicts an exemplary arrangement of output circuits that permits a row of pixels to be sampled concurrently with the read out of a previously sampled row of pixels. This is known as a concurrent sample and read operation. Each column output in pixel array 202 (N+0_PIXOUT, N+1_PIXOUT,…) is connected to the inputs of four sampling switches 500 in a respective output circuit 210. An output of each sampling switch 500 is connected to a sample and hold capacitor 502. Each sample and hold capacitor 502 is connected to an input of a readout switch 504. The outputs of readout switches 504 are connected to output bus 506.

In the illustrated embodiment, output bus 506 includes two signal lines, one for the RESET signal and one for the SIGNAL signal. The outputs of two readout switches in each group of four readout switches are connected to the RESET signal line in output bus 506. The outputs of the other two readout switches in each group of four readout switches are connected to the SIGNAL signal line in output bus 506.

Each column output is selectively connected to one of the four sample and hold capacitors 502 in a respective output circuit 210 via respective sampling switches 500. Two sample and hold capacitors 502 in each output circuit 210 are provided to sample and hold a reset signal from a pixel while the other two sample and hold capacitors 502 sample and hold an image signal from the pixel. The sampling switches 500 connected to the two sample and hold capacitors 502 for the reset signal are controlled by the Sample and Hold Reset (SHR) signal. The sampling switches 500 connected to the two sample and hold capacitors 502 for the image signal are controlled by Sample and Hold Signal (SHS).

Although the internal details of pixel array 202 are not shown in **FIG. 5**, those skilled in the art will recognize that individual pixel readout circuits in the array may be shared by two or more pixels. For example, a physical row of pixels in pixel array 202 may comprise pairs of pixels with each pair sharing a common output signal. In this case, each of the signals provided on the outputs (N+0_PIXOUT, N+1_PIXOUT,…) will represent the output of only one of each pair of pixels, or possibly the combined outputs of both pixels in each pair. Consequently, in order to read out each individual pixel in a physical row, two sampling and readout operations are used; one sampling and readout operation for each of the two pixels in the pairs constituting the rows. Therefore, the reference to sampling or reading a row of pixels is to be understood to include full physical rows of pixels, alternate pixels from a physical row, combined pairs of pixels from a physical row, or other alternatives depending on the details of pixel structures and readout circuit sharing arrangements within the pixel array.

The signals held in sample and hold capacitors 502 are read out by sequentially connecting the sample and hold capacitors 502 to output bus 506 by means of the readout switches 504. Each output in column decoder 204 is electrically connected to respective readout switches 504 in each group of four readout switches via logic gates (e.g., AND gates 514, 520). Column decoder 204 decodes the column address COLADDR in order to selectively enable two readout switches 504 in each group of four readout switches and select one differential pair of sample and hold capacitors 502 for readout.

The SELECT signal determines which sample and hold capacitors 502 are available for sampling and which sample and hold capacitors 502 are available for readout. For example, when SELECT is low, AND gate 508 permits the SHR signal to operate the leftmost sampling switch (e.g., switch 510) in each group of four sampling switches 500 to allow a reset signal to be stored in the leftmost sample and hold capacitor (e.g., capacitor 512). AND gate 514 permits the N+x_COLEN signals (i.e., N+0_COLEN, N+1_COLEN, …) to select the right pair of each group of four sampling capacitors 502 for readout.

When SELECT is high, AND gate 516 permits sampling into the third from the left of each group of four sample and hold capacitors 502 (e.g., capacitor 518), while AND gate 520 permits the N+x_COLEN signals to select the left pair of each group of four sample and hold capacitors 502. The AND gates ensure that sampling and readout operations are mutually exclusive with regard to the use of the sampling capacitors 502.

The SHS signal operates similarly to the SHR signal. For example, when SELECT is low, AND gate 522 permits the SHS signal to operate the sampling switch 524 in each group of four sampling switches 500 to allow an image signal to be stored in sample and hold capacitor 526. AND gate 514 permits the N+x_COLEN signals to select the right pair of each group of four sampling capacitors 502 for readout.

When SELECT is high, AND gate 528 permits sampling into the rightmost sample and hold capacitor 502 (capacitor 530), while AND gate 520 permits the N+x_COLEN signals to select the left pair of each group of four sample and hold capacitors 502.

Referring now to **FIG. 6**, there is shown an exemplary timing diagram for non-concurrent sample and read operations for sampling and readout output circuits 210 shown in **FIGS. 2** and **5**. The SELECT line is held low during sampling and high during readout so only one set of sample and hold switches 500, a corresponding set of sample and hold capacitors 502, and a corresponding set of readout switches 504 are used. During sampling (the time period between times t_0 and t_2), the column address COLADDR is held at a given state X that does not address any active columns for readout. The SHR and SHS signals operate to sample and hold the pixel RESET signals (time t_0 to time t_1) followed by the pixel SIGNAL signals (time t_1 to time t_2). After sampling all of the RESET and SIGNAL signals in a row of pixels (time period after time t_2), COLADDR begins to provide sequential addresses in order to read out the sampled signals.

FIG. 7 depicts an exemplary timing diagram for concurrent sample and read operations for sampling and readout output circuits 210 shown in **FIGS. 2** and **5**. Assuming that a previous sampling operation has stored signals in the

sampling and readout capacitors for readout, COLADDR begins immediately reading out the signals from the right pair of sampling and readout capacitors in each group of four sampling and readout capacitors 502 (see time t_3), while SHR (time t_3 to time t_4) and SHS (time t_4 to time t_5) sample into the left pair of sampling and readout capacitors in each group of four sampling and readout capacitors 502. The X in COLADDR means the addressing sequence has completed and the COLADDR is set to a value that does not address any active column for readout.

When the sampling and readout operations are complete at time t_6, the SELECT line switches the functions of the two sets of sampling and readout capacitors in each group of four sampling and readout capacitors 502. COLADDR then begins reading out the left pair of sampling and readout capacitors while SHR and SHS sample into the right pair of sampling and readout capacitors in each group of four sampling and readout capacitors 502. In the **FIG. 7** embodiment, readout activity is occurring at the critical falling edges of SHR and SHS. This raises the potential for system noise that can be sampled into the sampling capacitors along with the desired pixel reset or signal.

Referring now to **FIG. 8**, there is shown a flowchart of a method for pausing column readout in an embodiment in accordance with the invention. Initially, concurrent sample and read operations are initiated, as shown in block 800. The sampling of signals from a row of pixels along with column readout of previously sampled signals both begin at essentially the same time, such that sampling and column readout are performed concurrently (e.g., time t_3 in **FIG. 7**).

Next, as shown in block 802, the column addressing sequence supplied to the column decoder is suspended before the end of the SHR period (SHR period is time t_3 to time t_4 in **FIG. 7**). The column address supplied to the column decoder optionally is changed so as to select a static "parking" column outside the column address range corresponding to active pixel columns. The parking column address selects an individual sampling and readout output circuit 210 (**FIGS. 2** and **5**), or it selects reference voltages to be applied to the inputs of the AFE circuit 212 as will be described in detail later. This optional selection of a parking column or reference voltages is alternatively provided by a dedicated control signal separate

from the column address. The AFE clock signal transmitted to AFE circuit 212 continues after suspension of the column addressing sequence so that the signal contents of at least a portion of the pipeline stages of the AFE are read out of the AFE (block 804). As the signal contents of the pipeline stages are read out, the pipeline stages are sequentially filled with signals from the sampling and readout output circuit corresponding to the final address in the suspended column addressing sequence or from the parking column address, or with signals from reference voltages.

After all or some of the contents of the AFE pipeline have been read out, the AFE clock signal is stopped N clock periods before the end of the SHR period (block 806). In order for the AFE clock signal to be stopped N clock periods before the end of the SHR period, the column addressing sequence must be suspended a sufficient number of clock periods earlier to allow the signal contents of the AFE pipeline to be read out before stopping the clock. As will be recognized by someone skilled in the art, the timing parameters associated with blocks 802, 804, and 806, particularly the value of N and the number of clock periods to allow the AFE pipeline to be read, are specified in programmable control registers or fixed by the design in embodiments in accordance with the invention. For example, the value of N and the number of clock periods to allow the AFE pipeline to be read are specified in control register 214 shown in **FIG. 2** in an embodiment in accordance with the invention.

After the SHR period is completed at the falling edge of the SHR signal, transmission of the AFE clock signal to AFE circuit 212 and supply of the column addressing sequence to the column decoder resume (block 808). The column address sequence resumes where it was suspended in block 802 in an embodiment in accordance with the invention. Optionally, a programmable or fixed number of AFE clock periods is inserted between restarting the AFE clock and resuming the column addressing sequence. An additional option provides for supplying column addresses corresponding to dark reference columns between restarting the AFE clock and resuming the column addressing sequence in order to provide dark signal data to the AFE input. Yet another option is to provide reference voltages to

the AFE input between restarting the AFE clock and resuming the column addressing sequence.

FIG. 9 is a timing diagram that shows graphically the operations described in blocks 802, 804, 806, and 808. The SH signal in **FIG. 9** corresponds to either the SHR signal or the SHS signal in **FIG. 7**. **FIG. 9** provides additional detail and shows an embodiment of the present invention around the falling edge of either SHR at time t_4 in **FIG. 7** or SHS at time t_5 in **FIG. 7**. The **FIG. 9** embodiment recognizes the pipeline nature of the AFE circuit 212 (**FIG. 2**) and flushes the pipeline of signals prior to pausing the AFE clock. The gain stages and the ADC in a CMOS image sensor (for example, gain stages 404, 406 and ADC 400 in **FIG. 4**) are typically constructed using switched capacitor circuit elements, so each stage introduces a one clock delay. In the exemplary timing diagrams shown in **FIG. 9**, the ADC OUT data is delayed from the ASP IN signal by four clock cycles, so the analog front end (AFE) pipeline delay is four clock cycles. Note that the AFE pipeline delay could be significantly greater than four, with a pipeline delay of 10 or 15 clock cycles as common delays. For the embodiment shown in **FIG. 9**, an AFE pipeline delay of four clock cycles is used to illustrate a pausing column readout operation.

When considered in the context of blocks 802, 804, 806, and 808, the SH signal in **FIG. 9** should be regarded as the SHR signal. As shown in **FIG. 9**, the column addressing sequence (identified as COLADDR) is suspended at time t_A before the end of the SHR sampling period as described in block 802. In the embodiment shown in **FIG. 9**, COLADDR is set to some non-imaging column P (sometimes referred to as a parking column) at this time. The address P may be the address of a reference column or it may select a circuit that provides a reference voltage. The AFE clock signal (AFE CLOCK) to AFE circuit 212 continues for a period of time in order to read out at least a portion of the AFE pipeline as described in block 804. AFE CLOCK is suspended at subsequent time t_B before the end of the SHR sampling period, as described in block 806. Coincident with or shortly after the end of the SHR sampling period at time t_C, AFE CLOCK and the column addressing sequence shown in COLADDR resume, as described in block 808. In the embodiment shown in **FIG. 9**, the first addresses

provided in the resumed column addressing sequence (R0 and R1) are the addresses of reference columns or select a circuit that provides a reference voltage. This provides one or more clock periods of reference signals (dark reference signals or reference voltages, for example) to the input to AFE circuit 212. Then, at time t_D in **FIG. 9**, the column addressing sequence continues with the next sequential column address from where it was suspended at time t_A.

Next, as shown in block 810, the column addressing sequence supplied to the column decoder is suspended before the end of the SHS (sample signal level) period. As with the similar suspension of the column addressing sequence in block 802, there are several options for providing signals to the inputs of the AFE circuit 212 while the column addressing sequence is suspended. The clock to the AFE continues after suspension of the column addressing sequence so that the signal contents of at least a portion of the pipeline stages of the AFE are read out of the AFE (block 812).

After all or some of the contents of the AFE pipeline have been read out, the AFE clock signal is stopped M clock periods before the end of the SHS period (block 814). In order for the AFE clock to be stopped M clock periods before the end of the SHS period, the column addressing sequence must be suspended a sufficient number of clock periods earlier to allow the signal contents of the AFE pipeline to be read out before stopping the clock. As with the similar stopping of the AFE clock in block 806, there are several options for specifying the timing parameters associated with blocks 810, 812, and 814.

After the SHS period is completed at the falling edge of the SHS signal, transmission of the AFE clock signal to AFE circuit 212 and supply of the column addressing sequence to the column decoder resumes (block 816). The column address sequence resumes where it was suspended in block 810 in an embodiment in accordance with the invention. As with the similar restarting of the AFE clock and resumption of the column address sequence following the SHR period in block 808, there are options for providing a delay between restarting the AFE clock and resuming the column address sequence and for providing dark signals or reference signals to the AFE input during this time.

As with blocks 802, 804, 806, and 808, **FIG. 9** is a timing diagram that shows graphically the operations described in blocks 810, 812, 814, and 816, and the previous discussion of FIG. 9 applies to the corresponding blocks 810, 812, 814, and 816. When considered in the context of blocks 810, 812, 814, and 816, the SH signal in **FIG. 9** should be regarded as the SHS signal.

Suspension of the AFE clocking signal and the column address sequence can repeat until all of the signals have been sampled and readout of the pixel array. As is described in more detail in conjunction with **FIGS. 10** and **11**, the pixel data output from each output circuit can be stored while the AFE clocking signal and the column address sequence are suspended. Storing of the pixel data selectively delays the output of the pixel data to effect an uninterrupted output data flow of pixel data.

As described earlier, the embodiment shown in **FIG. 9** suspends the AFE clock signal transmitted to the entire AFE at the end of each sampling period. Other embodiments in accordance with the invention can suspend the AFE clock signal to only a portion of the AFE. For example, sufficient reduction in system noise may be achieved by suspending the clock to only the ASP portion of the AFE.

In one or more embodiments in accordance with the invention, the output of the image sensor may be received by an imaging system or processing system that cannot handle the interruptions in the flow of data caused by the suspensions of the AFE clock signal and the column addressing sequence. **FIG. 10** depicts a block diagram of a circuit that is used to make the interrupted data stream from **FIG. 9** continuous with the use of a digital buffer. **FIG. 11** illustrates an exemplary timing diagram for the circuit shown in **FIG. 10**.

The circuit 1000 receives the interrupted ADC output ADC OUT (see **FIG. 9**) and outputs the desired non-interrupted data flow DOUT (see **FIGS. 10** and **11**) from the image sensor. ADC OUT output from ADC 400 is received in the digital logic 208 (**FIG. 2**) by AFE interface 220. This data output stream will have one or more interruptions in it due to one or more suspensions of the column addressing sequence. Furthermore, the data output stream from the ADC 400 will

include data that is not part of the desired image data as a consequence of filling the AFE pipeline with signals from a parking column or from reference voltages when the AFE pipeline is emptied of image data prior to shutting off the AFE clock. This undesired data must be discarded. The data captured by AFE interface 220 is stored in digital buffer 222 as it is received. The readout of each row of data from digital buffer 222 begins a number of clock periods after the first data is written into the buffer, where the number of clock periods is greater than or equal to the total number of clock periods that the column address sequence is suspended during each row of readout as shown in **FIG. 11**. In an embodiment in accordance with the invention, digital buffer 222 consists of a first-in-first-out (FIFO) memory with selectable depth, but those skilled in the art will recognize that other implementations are possible.

Although **FIG. 11** shows recovering from a single interruption of the column addressing sequence, multiple interruptions could take place when sampling a row of pixels. Multiple interruptions could occur, for example, when separately sampling pixel reset and signal levels (using the SHR and SHS signals, for example). In the case of multiple interruptions, the start of output data from DOUT must be delayed sufficiently to anticipate the total combined times of all column addressing interruptions. Digital buffer 222 stores the interrupted ADC output ADC OUT during all of the interruptions in the same row.

Referring now to **FIG. 12**, there is shown a circuit diagram of a portion of an alternate sampling and readout output circuitry 210 shown in **FIG. 2**. Column read decoder 1200, which acts as a selecting circuit, includes the functionality to select reference voltages VREFR 1202 and VREFS 1204 for readout. The use of reference voltages instead of non-imaging columns for parking and startup (P and R in **FIGS. 9** and **11**) ensures that the signal levels provided to the analog front end circuit 212 (**FIG. 2**) remain well-controlled and within the proper operating range of analog front end circuit 212. The use of reference voltages VREFR 1202 and VREFS 1204 mitigates the need to provide startup pixels after pausing.

The invention has been described in detail with particular reference to certain preferred embodiments thereof, but it will be understood that variations and modifications can be effected within the spirit and scope of the invention. For

example, embodiments in accordance with the invention have been described herein with respect to concurrent sampling and readout of the reset signals and image signals. Other embodiments in accordance with the invention are not limited to these signals. Embodiments of the present invention can concurrently read out and sample any signal and any number of signals.

Additionally, the illustrated embodiments have been described with reference to specific components and circuits. Other embodiments in accordance with the invention are not limited to these particular components. For example, logic gates other than AND gates and different types of switches can be used in the embodiment shown in **FIG. 5**.

PARTS LIST

100	image capture device
102	light
104	imaging stage
106	image sensor
108	processor
110	memory
112	display
114	input/output (I/O) elements
200	pixel
202	pixel array
204	column decoder
206	row decoder
208	digital logic
210	sampling and readout circuit
212	analog front end (AFE)
214	control register
216	timing generator
218	analog front end clock controller
220	analog front end interface
222	digital buffer
300	active area
302	column of photoactive pixels
304	row of photoactive pixels
306	row reference area
308	column reference area
400	analog to digital converter (ADC)
402	analog signal processor (ASP)
404	variable gain amplifier
406	variable gain amplifier
408	signal summing node

410	digital to analog converter (DAC)
500	sampling switches
502	sample and hold capacitors
504	readout switches
506	differential analog output bus
508	AND gate
510	sampling switch
512	sample and hold capacitor
514	AND gate
516	AND gate
518	sample and hold capacitor
520	AND gate
522	AND gate
524	sampling switch
526	sample and hold capacitor
528	AND gate
530	sample and hold capacitor
1000	non-interrupted data flow output circuit
1200	column read decoder
1202	reference voltage
1204	reference voltage

CLAIMS:

1. An image sensor comprising:

a two-dimensional array of pixels, the array including a plurality of column outputs;

an output circuit connected to each column output, wherein each output circuit is configured to operate concurrent sample and read operations;

a column decoder electrically connected to each output circuit;

an analog front end (AFE) circuit for processing pixel data;

an AFE clock controller for transmitting an AFE clocking signal to the AFE circuit to effect processing of the pixel data; and

a timing generator for outputting a column address sequence that is received by the column decoder, wherein during a sample operation the timing generator suspends the column address sequence and subsequently during the sample operation the AFE clock controller suspends the AFE clocking signal, and coincident with or after the end of the sample operation the AFE clock controller resumes the AFE clocking signal and the timing generator resumes the column address sequence.

2. The image sensor as in claim 1, further comprising a digital buffer configured to selectively store output of a portion of the pixel data from the AFE circuit.

3. The image sensor as in claim 1, further comprising a plurality of sampling switches connected to each column output.

4. The image sensor as in claim 3, further comprising a sample and hold capacitor connected to each sampling switch.

5. The image sensor as in claim 4, further comprising a readout switch connected to each sample and hold capacitor.

6. The image sensor as in claim 5, wherein a select signal is used to activate respective readout switches and the column decoder selects individual output circuits in a sequence to read out previously sampled pixel signals.

7. The image sensor as in claim 1, wherein the image sensor is included in an image capture device.

8. The image sensor as in claim 1, further comprising at least one control register for storing one or more values that collectively control the respective onsets and durations of the suspensions of the column address sequence and the AFE clocking signal.

9. The image sensor as in claim 1, further comprising a selecting circuit that permits selecting reference voltages for readout, wherein the reference voltages are selected for readout during at least part of the time that the column address sequence is suspended.

10. A method for reading out an image from an image sensor including a two-dimensional array of pixels having a plurality of column outputs and an output circuit connected to each column output, wherein each output circuit is configured to operate concurrent sample and read operations, the method comprising:

initiating concurrent sample and read operations in each output circuit;

during a first sample operation, suspending a column address sequence;

subsequently during the first sample operation, suspending an AFE clocking signal; and

at or after the completion of the first sampling operation, resuming the AFE clocking signal and the column address sequence.

11. The method as in claim 9, further comprising:

during a second sample operation, suspending a column address sequence;

subsequently during the second sample operation, suspending an AFE clocking signal; and

at or after the completion of the second sampling operation, resuming the AFE clocking signal and the column address sequence.

12. The method as in claim 10, further comprising selectively storing pixel data output from each output circuit while the AFE clocking signal and the column address sequence are suspended.

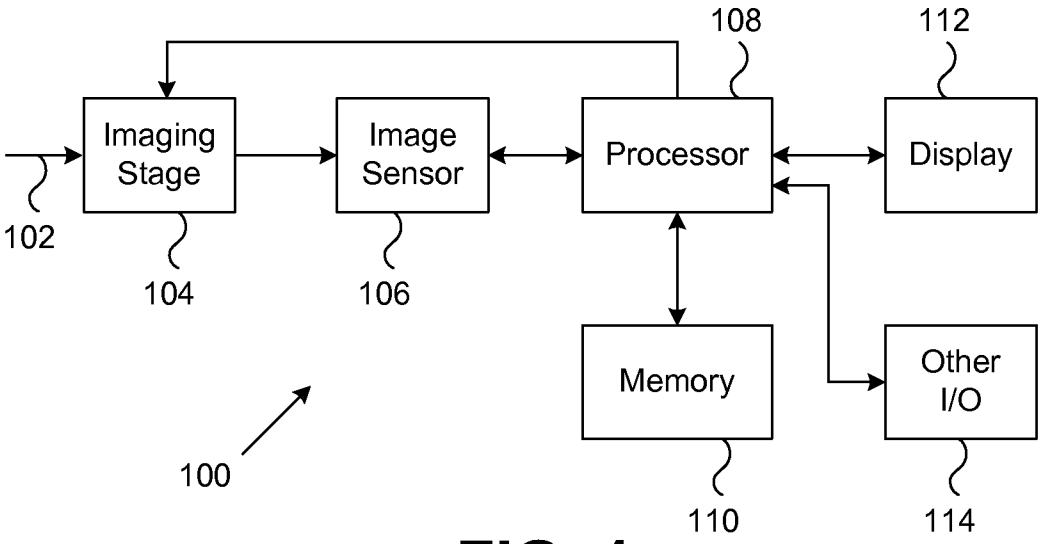
108
112
Imaging Stage
Image Sensor
Processor
Display
102
104
106
Memory
Other I/O
100
110
114

FIG. 1

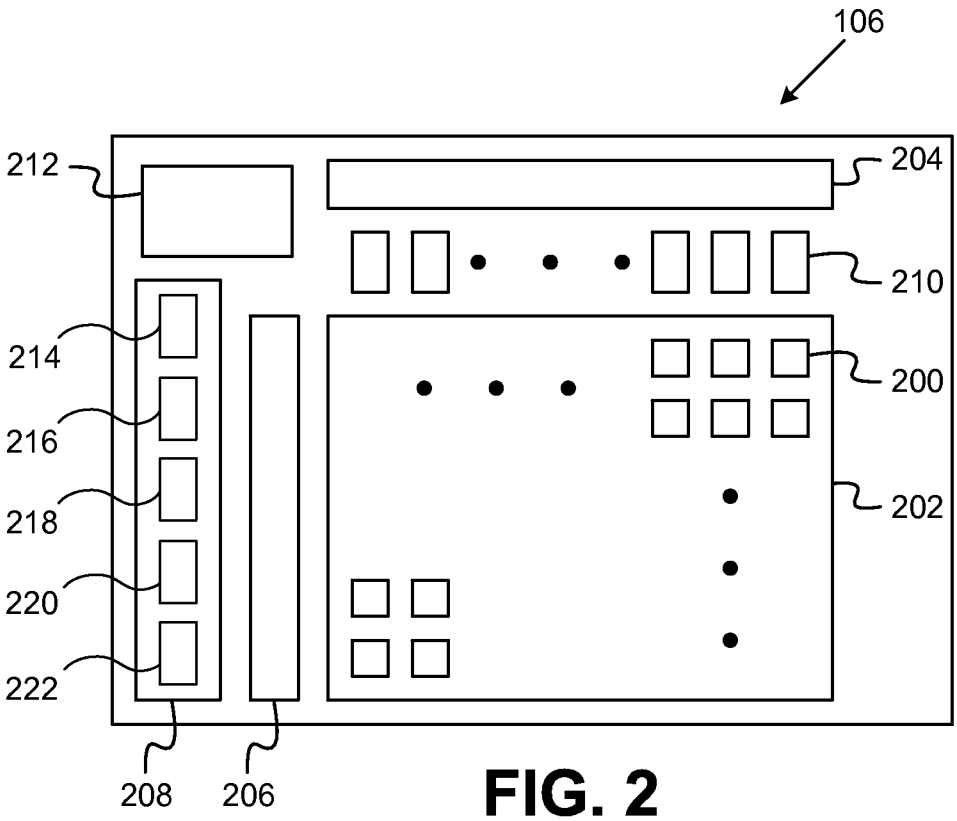
106
212
204
210
214
216
218
220
222
200
202
208
206

FIG. 2

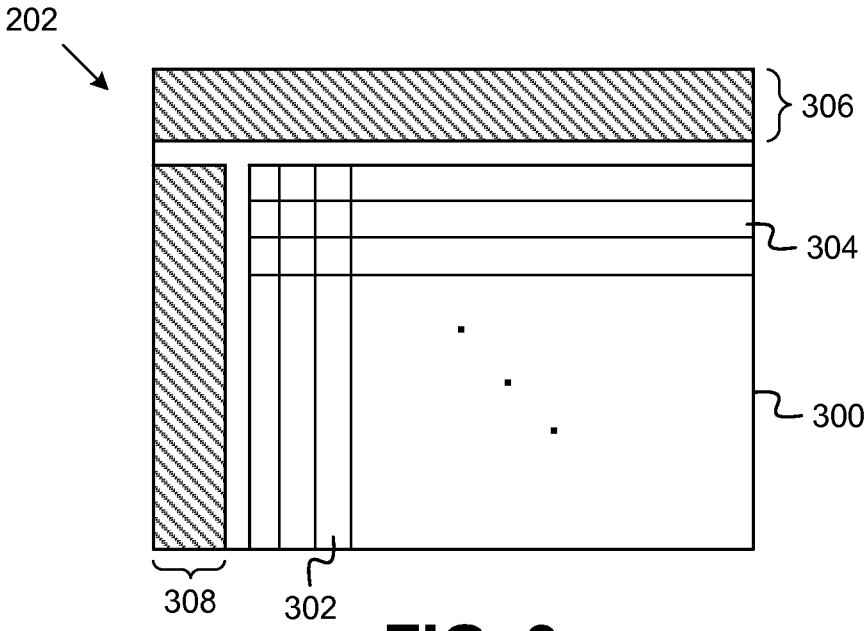
202
306
304
300
308
302

FIG. 3

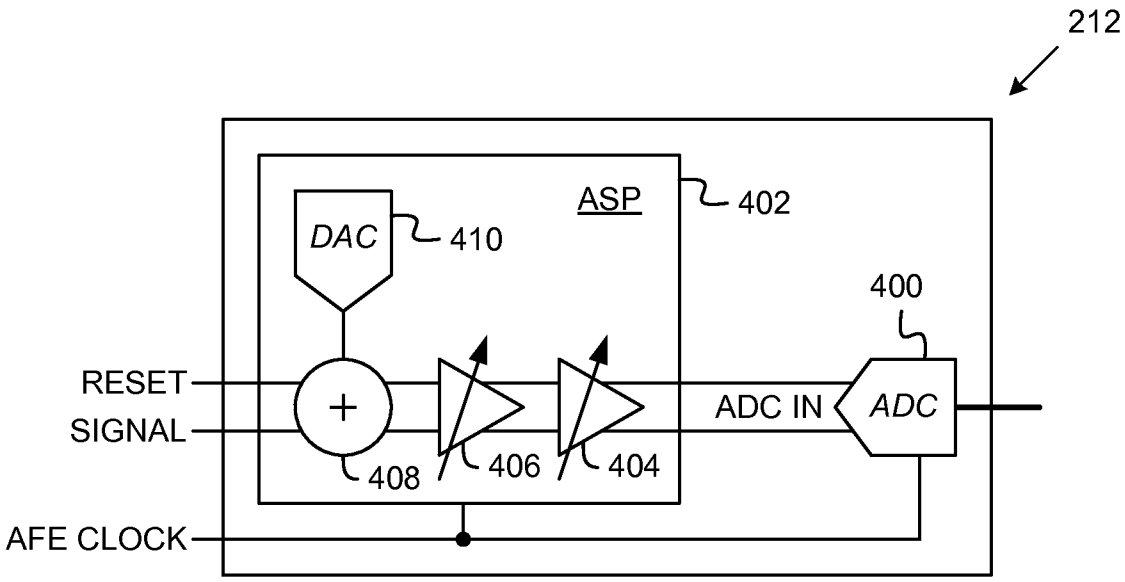
212
ASP
402
DAC
410
400
RESET
SIGNAL
ADC IN
ADC
408
406
404
AFE CLOCK

FIG. 4

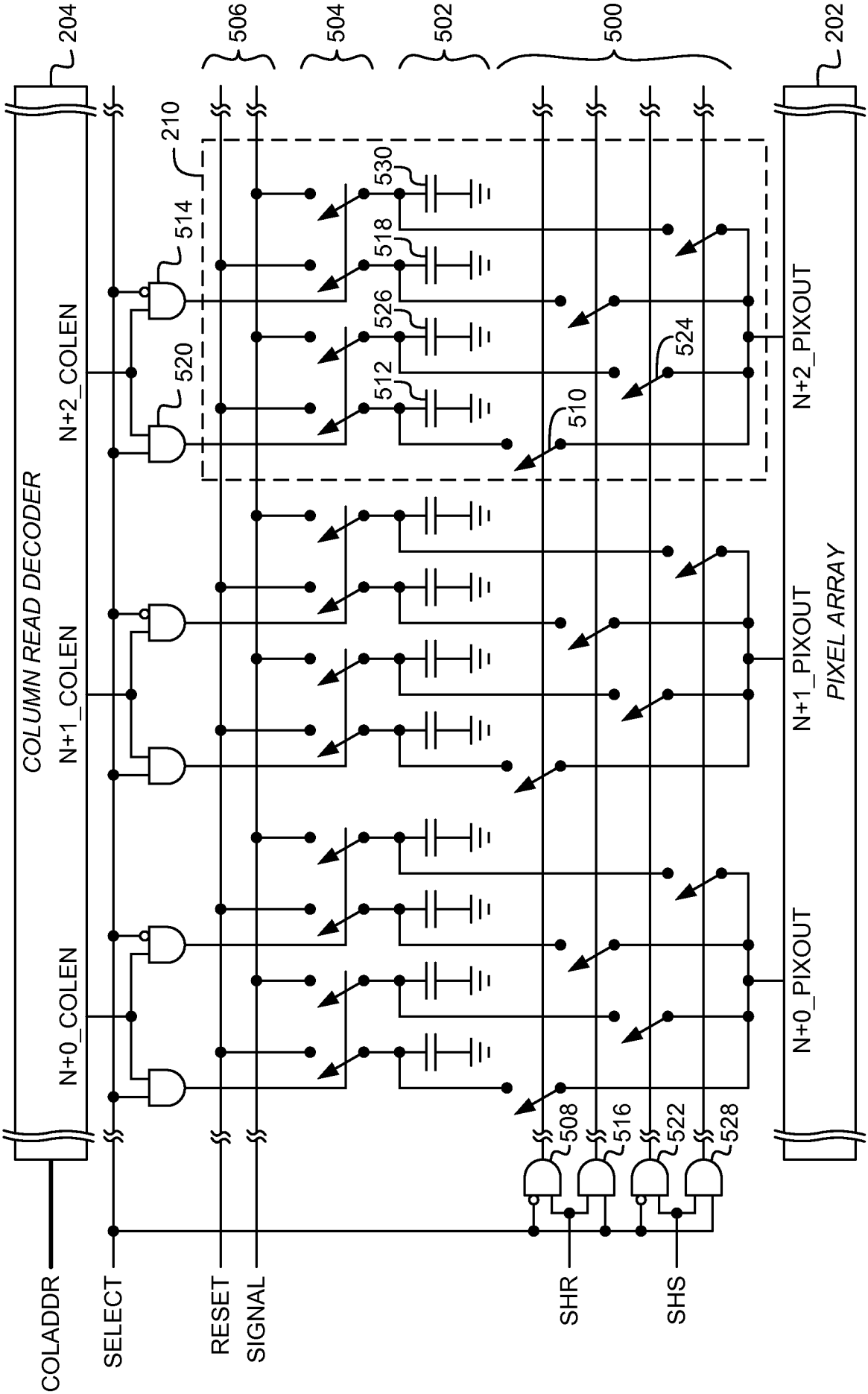
204
506
504
502
500
202
210
530
514
518
526
520
524
512
510
COLUMN READ DECODER
N+2_COLEN
N+1_COLEN
N+0_COLEN
N+2_PIXOUT
N+1_PIXOUT
N+0_PIXOUT
PIXEL ARRAY
508
516
522
528
COLADDR
SELECT
RESET
SIGNAL
SHR
SHS

FIG. 5

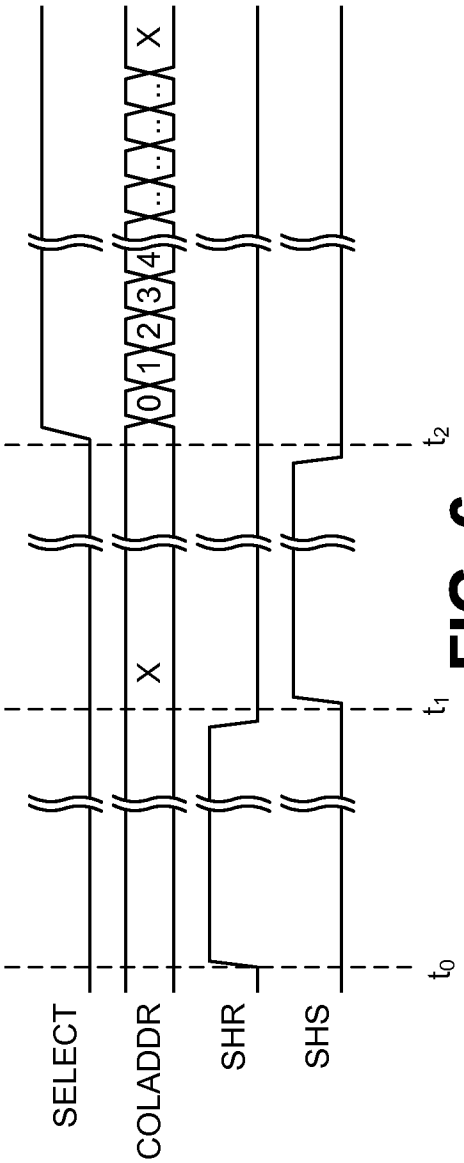
SELECT
COLADDR
SHR
SHS
0
1
2
3
4
X
X
t0
t1
t2

FIG. 6

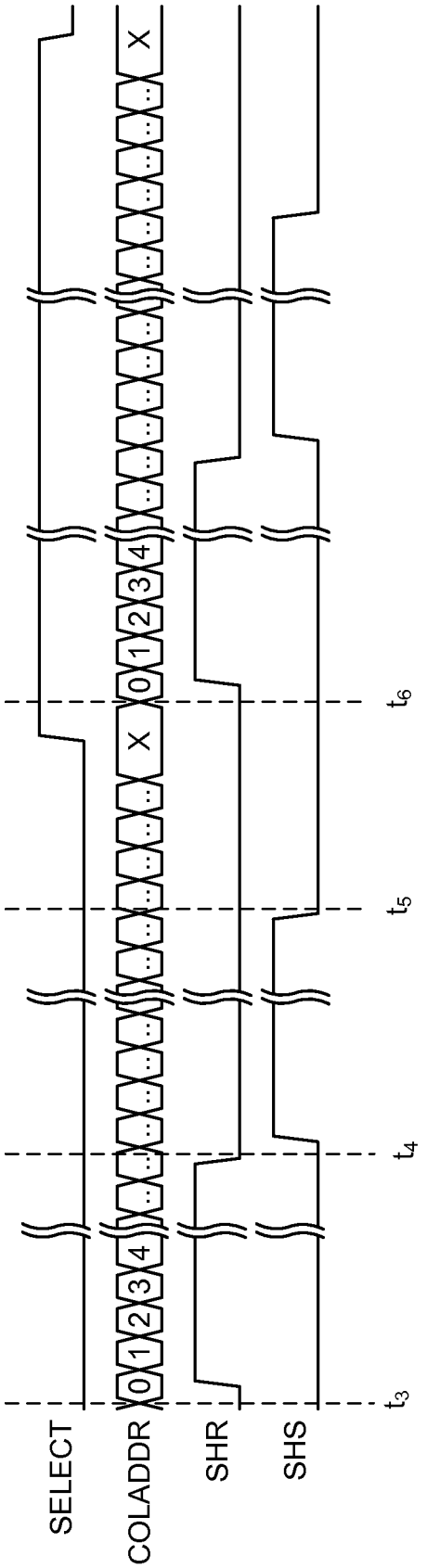
SELECT
COLADDR
SHR
SHS
0
1
2
3
4
X
X
t3
t4
t5
t6

FIG. 7

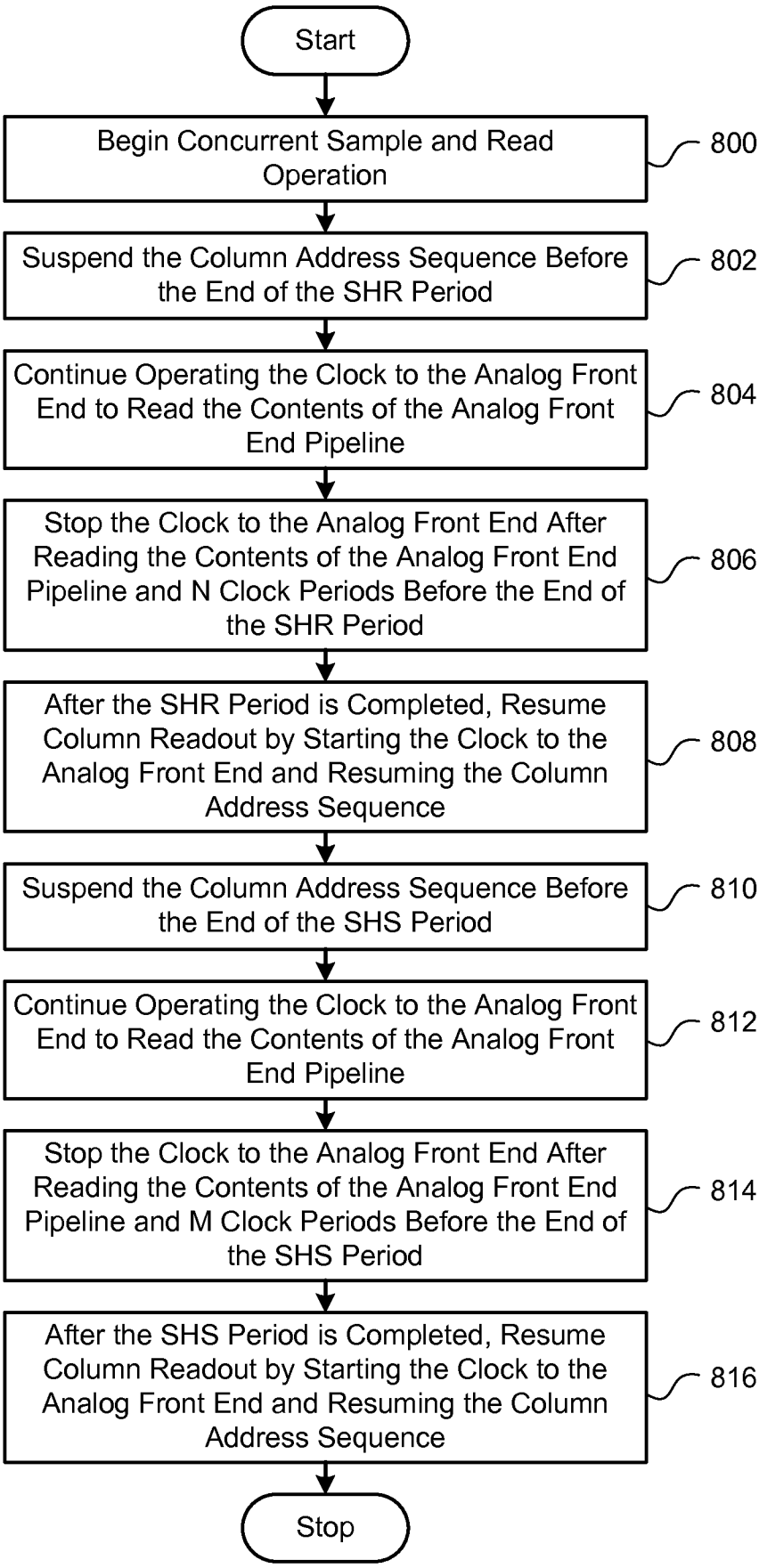
Start
Begin Concurrent Sample and Read Operation
800
Suspend the Column Address Sequence Before the End of the SHR Period
802
Continue Operating the Clock to the Analog Front End to Read the Contents of the Analog Front End Pipeline
804
Stop the Clock to the Analog Front End After Reading the Contents of the Analog Front End Pipeline and N Clock Periods Before the End of the SHR Period
806
After the SHR Period is Completed, Resume Column Readout by Starting the Clock to the Analog Front End and Resuming the Column Address Sequence
808
Suspend the Column Address Sequence Before the End of the SHS Period
810
Continue Operating the Clock to the Analog Front End to Read the Contents of the Analog Front End Pipeline
812
Stop the Clock to the Analog Front End After Reading the Contents of the Analog Front End Pipeline and M Clock Periods Before the End of the SHS Period
814
After the SHS Period is Completed, Resume Column Readout by Starting the Clock to the Analog Front End and Resuming the Column Address Sequence
816
Stop

FIG. 8

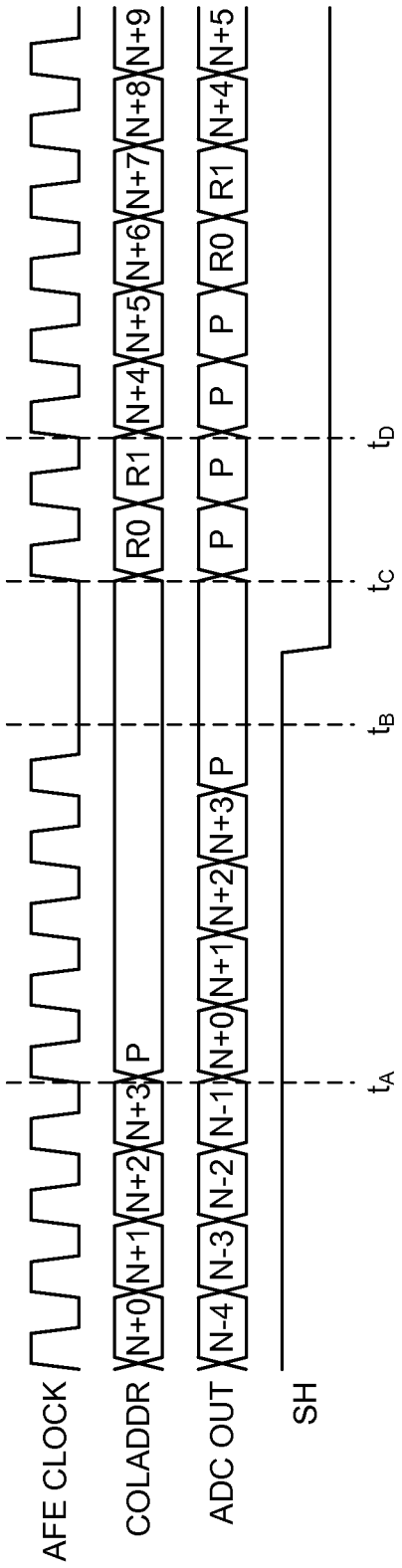
AFE CLOCK
COLADDR
ADC OUT
SH
N+0
N+1
N+2
N+3
P
R0
R1
N+4
N+5
N+6
N+7
N+8
N+9
N-4
N-3
N-2
N-1
N+0
N+1
N+2
N+3
P
P
P
P
R0
R1
N+4
N+5
t_A
t_B
t_C
t_D

FIG. 9

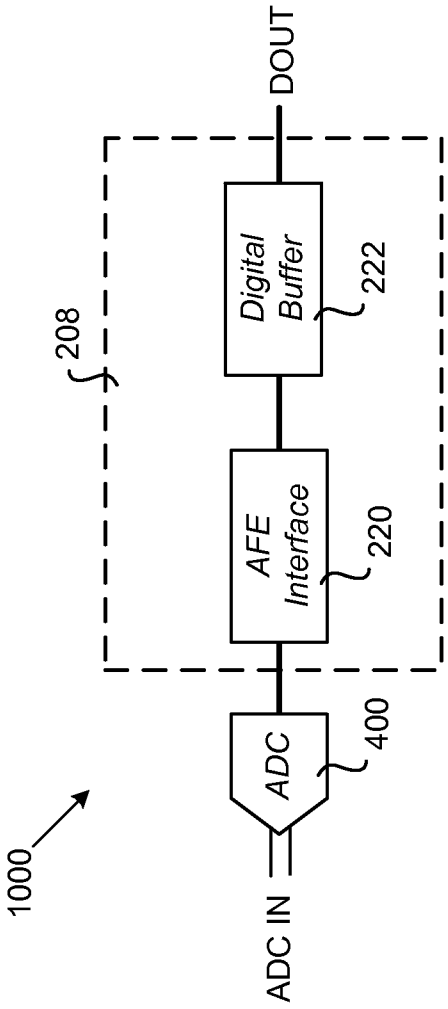
1000
208
ADC
400
AFE Interface
220
Digital Buffer
222
ADC IN
DOUT

FIG. 10

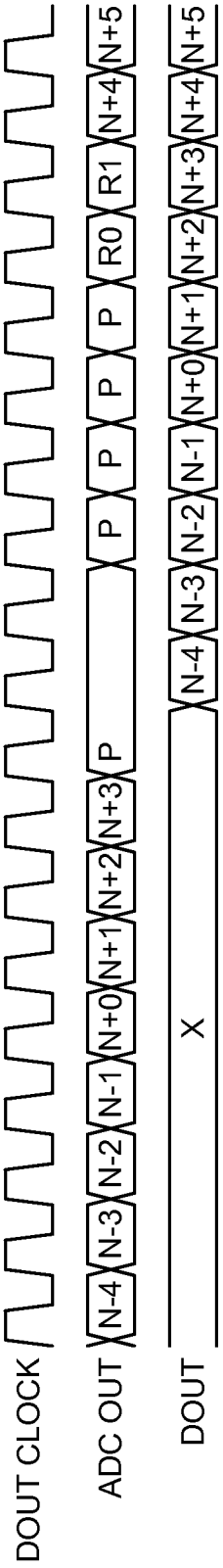
DOUT CLOCK
ADC OUT
N-4 N-3 N-2 N-1 N+0 N+1 N+2 N+3 P P P P R0 R1 N+4 N+5
DOUT
X N-4 N-3 N-2 N-1 N+0 N+1 N+2 N+3 N+4 N+5

FIG. 11

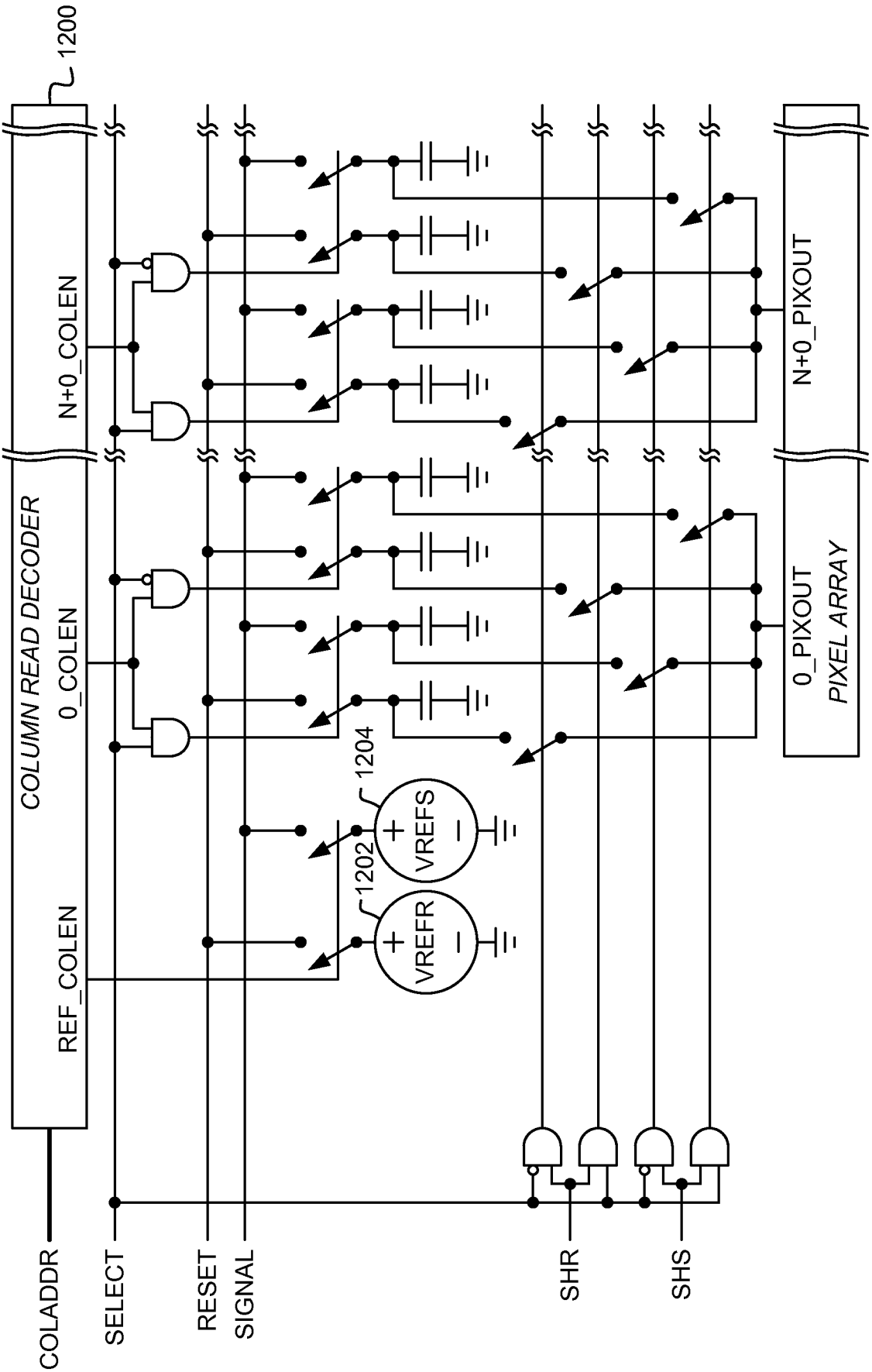
1200
COLUMN READ DECODER
N+0_COLEN
0_COLEN
REF_COLEN
1204
1202
VREFS
VREFR
N+0_PIXOUT
0_PIXOUT
PIXEL ARRAY
COLADDR
SELECT
RESET
SIGNAL
SHR
SHS

FIG. 12

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2010/060766

A. CLASSIFICATION OF SUBJECT MATTER
INV. H04N5/357
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H04N

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2008/284887 A1 (TOYA HIROSHI [JP] ET AL) 20 November 2008 (2008-11-20)	1-8, 10-12
A	the whole document	9

Y	US 6 541 751 B1 (BIDERMANN WILLIAM R [US]) 1 April 2003 (2003-04-01)	1-8, 10-12
A	the whole document	9

Y	US 2006/022862 A1 (EGAWA YOSHITAKA [JP] ET AL) 2 February 2006 (2006-02-02)	2
A	the whole document	1,3-12

A	US 2003/234881 A1 (MITANI KOHJI [JP]) 25 December 2003 (2003-12-25) the whole document	1-12

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
23 February 2011	02/03/2011

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Doswald, Daniel

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2010/060766

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2008284887 A1	20-11-2008	NONE	
US 6541751 B1	01-04-2003	NONE	
US 2006022862 A1	02-02-2006	JP 4481758 B2	16-06-2010
		JP 2006042033 A	09-02-2006
US 2003234881 A1	25-12-2003	JP 4243457 B2	25-03-2009
		JP 2004032212 A	29-01-2004