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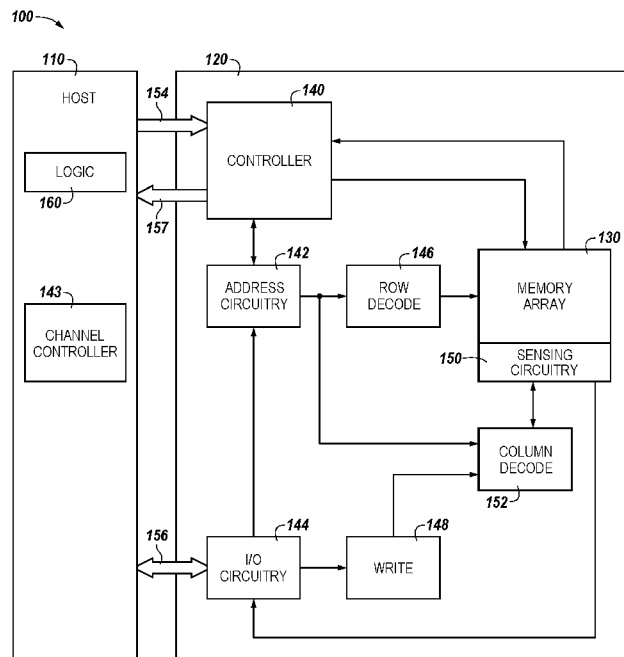


Fig. 1

(57) Abstract: The present disclosure includes apparatuses and methods related to logical operations using memory cells. An example apparatus comprises a first memory cell controlled to invert a data value stored therein and a second memory cell controlled to invert a data value stored therein. The apparatus may further include a controller coupled to the first memory cell and the second memory cell. The controller may be configured to cause performance of a logical operation between the data value stored in the first memory cell and the data value stored in the second memory cell.



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Logical Operations Using Memory Cells

Technical Field

[0001] The present disclosure relates generally to semiconductor memory and methods, and more particularly, to apparatuses and methods related to logical operations using memory cells.

Background

[0002] Memory devices are typically provided as internal, semiconductor, integrated circuits in computing systems. There are many different types of memory including volatile and non-volatile memory. Volatile memory can require power to maintain its data (e.g., host data, error data, etc.) and includes random access memory (RAM), dynamic random access memory (DRAM), static random access memory (SRAM), synchronous dynamic random access memory (SDRAM), and thyristor random access memory (TRAM), among others. Non-volatile memory can provide persistent data by retaining stored data when not powered and can include NAND flash memory, NOR flash memory, and resistance variable memory such as phase change random access memory (PCRAM), resistive random access memory (RRAM), and magnetoresistive random access memory (MRAM), such as spin torque transfer random access memory (STT RAM), among others.

[0003] Computing systems often include a number of processing resources (e.g., one or more processors), which may retrieve and execute instructions and store the results of the executed instructions to a suitable location. A processing resource can comprise a number of functional units such as arithmetic logic unit (ALU) circuitry, floating point unit (FPU) circuitry, and a combinatorial logic block, for example, which can be used to execute instructions by performing logical operations such as AND, OR, NOT, NAND, NOR, and XOR, and invert (e.g., inversion) logical operations on data (e.g., one or more operands). For example, functional unit circuitry may be used to perform arithmetic operations such as addition, subtraction, multiplication, and division on operands via a number of logical operations.

[0004] A number of components in a computing system may be involved in providing instructions to the functional unit circuitry for execution. The

instructions may be executed, for instance, by a processing resource such as a controller and/or host processor. Data (e.g., the operands on which the instructions will be executed) may be stored in a memory array that is accessible by the functional unit circuitry. The instructions and data may be retrieved from the memory array and sequenced and/or buffered before the functional unit circuitry begins to execute instructions on the data. Furthermore, as different types of operations may be executed in one or multiple clock cycles through the functional unit circuitry, intermediate results of the instructions and data may also be sequenced and/or buffered.

[0005] In many instances, the processing resources (e.g., processor and/or associated functional unit circuitry) may be external to the memory array, and data is accessed via a bus between the processing resources and the memory array to execute a set of instructions. Processing performance may be improved in a processing-in-memory (PIM) device, in which a processing resource may be implemented internal and/or near to a memory (e.g., directly on a same chip as the memory array). A PIM device may reduce time in processing and may also conserve power. Data movement between and within arrays and/or subarrays of various memory devices, such as PIM devices, can affect processing time and/or power consumption.

Brief Description of the Drawings

[0006] Figure 1 is a block diagram of an apparatus in the form of a computing system including a memory device in accordance with a number of embodiments of the present disclosure.

[0007] Figure 2A is a schematic drawing illustrating a portion of a memory array in accordance with a number of embodiments of the present disclosure.

[0008] Figure 2B is another schematic drawing illustrating a portion of a memory array in accordance with a number of embodiments of the present disclosure.

[0009] Figure 3 is a schematic diagram illustrating sensing circuitry in accordance with a number of embodiments of the present disclosure.

[0010] Figure 4 is a schematic diagram illustrating sensing circuitry in accordance with a number of embodiments of the present disclosure.

[0011] Figure 5 is another schematic diagram illustrating sensing circuitry in accordance with a number of embodiments of the present disclosure.

[0012] Figure 6 is a flow diagram for performing logical operations using memory cells in accordance with a number of embodiments of the present disclosure.

Detailed Description

[0013] The present disclosure includes apparatuses and methods related to logical operations using memory cells. An example apparatus comprises a first memory cell controlled to invert a data value stored therein and a second memory cell controlled to invert a data value stored therein. The apparatus may further include a controller coupled to the first memory cell and the second memory cell. The controller may be configured to cause performance of a logical operation between the data value stored in the first memory cell and the data value stored in the second memory cell.

[0014] Dynamic random access memory (DRAM) may be provided as part of a computing system to store data associated with the computing system. In some approaches, DRAM may comprise multiple one transistor, one capacitor (1T1C) memory cells, which may be coupled together to form a memory array. In 1T1C DRAM environments, binary data information may be stored in the capacitor in the form of an electric charge. Once a 1T1C memory cell has been read (e.g., once a read operation has been performed using data stored in the 1T1C memory cell), the electric charge corresponding to the binary data information stored in the capacitor may discharge (e.g., leak, become depleted, etc.) thereby destroying the binary data information that was stored in the capacitor. This phenomenon may be referred to as a “destructive read” or “destructive memory cell read.”

[0015] In contrast, DRAM memory cells having three transistors (3T) may preserve the binary data information (e.g., may preserve the charge stored therein) subsequent to performance of a read operation. This may allow for multiple word lines (e.g., read row lines, write row lines, etc.) to be fired without the need to refresh the memory cells or re-write data to the memory cells subsequent to performance of a read operation. This may reduce power consumption of a memory device since the memory cells do not need to be re-

written or refreshed in comparison to conventional 1T1C DRAM memory cells, and may reduce an amount of time (e.g., a read-to-read delay) required between performance of read operations in comparison to conventional 1T1C DRAM memory cells.

[0016] In some approaches, performing logical operations between binary data (e.g., operands) stored in memory cells and binary data stored in an accumulator may require multiple latches per column because binary data may need to be inverted (e.g., using a latch in addition to a sense amplifier latch) prior to performance of a logical operation. For example, in some approaches, data would be transferred to a first latch to be inverted, and the inverted data stored in the first latch may have been used as an operand in a logical operation between the inverted operands and operands stored in an accumulator. In contrast, embodiments disclosed herein allow for logical operations to be performed between binary data (e.g., operands) stored in the memory cells without using an additional latch to perform the inversion. For example, a 3T memory cell may be controlled to invert the data stored therein without the need for an additional latch. In some embodiments, the inverted data associated with the 3T memory cell may then be used as an operand for a logical operation.

[0017] In some embodiments, when the word lines (e.g., read row lines, write row lines, etc.) coupled to a memory cell are enabled, the read digit lines of the memory device may be driven low thereby creating a NOR read. The number of word lines enabled corresponds to the number of inputs of a NOR gate created by enabling the word lines.

[0018] In the following detailed description of the present disclosure, reference is made to the accompanying drawings that form a part hereof, and in which is shown by way of illustration how one or more embodiments of the disclosure may be practiced. These embodiments are described in sufficient detail to enable those of ordinary skill in the art to practice the embodiments of this disclosure, and it is to be understood that other embodiments may be utilized and that process, electrical, and/or structural changes may be made without departing from the scope of the present disclosure. As used herein, designators such as “n, “N,” etc., particularly with respect to reference numerals in the drawings, indicate that a number of the particular feature so designated can be included. As used herein, “a number of” a particular thing refers to one or more

of such things (e.g., a number of memory arrays can refer to one or more memory arrays). A “plurality of” is intended to refer to more than one of such things.

[0019] The figures herein follow a numbering convention in which the first digit or digits correspond to the drawing figure number and the remaining digits identify an element or component in the drawing. Similar elements or components between different figures may be identified by the use of similar digits. For example, 306 may reference element “06” in Figure 3, and a similar element may be referenced as 406 in Figure 4. As will be appreciated, elements shown in the various embodiments herein can be added, exchanged, and/or eliminated so as to provide a number of additional embodiments of the present disclosure. In addition, as will be appreciated, the proportion and the relative scale of the elements provided in the figures are intended to illustrate certain embodiments of the present invention, and should not be taken in a limiting sense.

[0020] Figure 1 is a block diagram of an apparatus in the form of a computing system 100 including a memory device 120 in accordance with a number of embodiments of the present disclosure. As used herein, a memory device 120, controller 140, channel controller 143, memory array 130, and/or sensing circuitry 150 might also be separately considered an “apparatus.”

[0021] System 100 includes a host 110 coupled (e.g., connected) to memory device 120, which includes a memory array 130. Host 110 can be a host system such as a personal laptop computer, a desktop computer, a digital camera, a smart phone, or a memory card reader, among various other types of hosts. Host 110 can include a system motherboard and/or backplane and can include a number of processing resources (e.g., one or more processors, microprocessors, or some other type of controlling circuitry). The system 100 can include separate integrated circuits or both the host 110 and the memory device 120 can be on the same integrated circuit. The system 100 can be, for instance, a server system and/or a high performance computing (HPC) system and/or a portion thereof. Although the example shown in Figure 1 illustrates a system having a Von Neumann architecture, embodiments of the present disclosure can be implemented in non-Von Neumann architectures, which may

not include one or more components (e.g., CPU, ALU, etc.) often associated with a Von Neumann architecture.

[0022] For clarity, the system 100 has been simplified to focus on features with particular relevance to the present disclosure. The memory array 130 can be a DRAM array (e.g., a 3T DRAM array), SRAM array, STT RAM array, PCRAM array, TRAM array, RRAM array, NAND flash array, and/or NOR flash array, for instance. The array 130 can comprise memory cells arranged in rows coupled by word lines, which may be referred to herein as access lines or select lines, and columns coupled by digit lines, which may be referred to herein as data lines or sense lines. Although a single array 130 is shown in Figure 1, embodiments are not so limited. For instance, memory device 120 may include a number of arrays 130 (e.g., a number of banks of DRAM cells, NAND flash cells, etc.). In some embodiments, the memory array may include the sense amplifier 150 in addition to the memory cells arranged in rows coupled by word lines and columns coupled by digit lines.

[0023] The memory device 120 includes address circuitry 142 to latch address signals for data provided over a data bus 156 (e.g., an I/O bus) through I/O circuitry 144. Status and/or exception information can be provided from the controller 140 on the memory device 120 to a channel controller 143, through a high speed interface (HSI) including an out-of-band bus 157, which in turn can be provided from the channel controller 143 to the host 110. Address signals are received through address circuitry 142 and decoded by a row decoder 146 and a column decoder 152 to access the memory array 130. Data can be read from memory array 130 by sensing voltage and/or current changes on the digit lines using sensing circuitry 150. The sensing circuitry 150 can read and latch a page (e.g., row) of data from the memory array 130. The I/O circuitry 144 can be used for bi-directional data communication with host 110 over the data bus 156. The write circuitry 148 can be used to write data to the memory array 130.

[0024] Controller 140 (e.g., memory controller) decodes signals provided by control bus 154 from the host 110. These signals can include chip enable signals, write enable signals, and address latch signals that are used to control operations performed on the memory array 130, including data read, data write, and data erase operations. In various embodiments, the controller 140 is responsible for executing instructions from the host 110 and sequencing access

to the array 130. The controller 140 can be a state machine, sequencer, or some other type of controller, and include hardware and/or firmware (e.g., microcode instructions) in the form of an application specific integrated circuit (ASIC), field programmable gate array, etc. The controller 140 can control, for example, performance of logical operations between operands stored in the memory array 130.

[0025] As described further below, in a number of embodiments, the sensing circuitry 150 and/or the array 130 can comprise a sense amplifier. The sense amplifier may also be referred to herein as an accumulator, and can be used in the performance of logical operations.

[0026] In a number of embodiments, the sensing circuitry 150 can be used to perform logical operations using data stored in array 130 as inputs and/or store the results of the logical operations back to the array 130 without transferring data via a digit line address access (e.g., without firing a column decode signal). As such, various compute functions can be performed using, and within, sensing circuitry 150 rather than (or in association with) being performed by processing resources external to the sensing circuitry (e.g., by a processing resource associated with host 110 and/or other processing circuitry, such as ALU circuitry, located on device 120 (e.g., on controller 140 or elsewhere)).

[0027] In various previous approaches, data associated with an operand, for instance, would be read from memory via sensing circuitry and provided to external ALU circuitry via I/O lines (e.g., via local I/O lines and/or global I/O lines). The external ALU circuitry could include a number of registers and would perform compute functions using the operands, and the result would be transferred back to the array via the I/O lines. In contrast, in a number of embodiments of the present disclosure, sensing circuitry 150 is configured to perform logical operations on data stored in memory array 130 and store the result back to the memory array 130 without enabling an I/O line (e.g., a local I/O line) coupled to the sensing circuitry 150. The sensing circuitry 150 can be formed on pitch with the memory cells of the array.

[0028] In a number of embodiments, circuitry external to array 130 and sensing circuitry 150 is not needed to perform compute functions as the sensing circuitry 150 can perform the appropriate logical operations to perform such compute functions without the use of an external processing resource.

Therefore, the sensing circuitry 150 may be used to compliment and/or to replace, at least to some extent, such an external processing resource (or at least the bandwidth consumption of such an external processing resource).

[0029] However, in a number of embodiments, the sensing circuitry 150 may be used to perform logical operations (e.g., to execute instructions) in addition to logical operations performed by an external processing resource (e.g., host 110). For instance, host 110 and/or sensing circuitry 150 may be limited to performing only certain logical operations and/or a certain number of logical operations.

[0030] Enabling an I/O line can include enabling (e.g., turning on) a transistor having a gate coupled to a decode signal (e.g., a column decode signal) and a source/drain coupled to the I/O line. However, embodiments are not limited to performing logical operations using sensing circuitry (e.g., 150) without enabling column decode lines of the array. Whether or not local I/O lines are used in association with performing logical operations via sensing circuitry 150, the local I/O line(s) may be enabled in order to transfer a result to a suitable location other than back to the array 130 (e.g., to an external register).

[0031] Figure 2A is a schematic drawing illustrating a portion of a memory array in accordance with a number of embodiments of the present disclosure. Figure 2A illustrates one memory cell 232, which can be one of a number of memory cells corresponding to memory array 130 shown in Figure 1. In the example shown in Figure 2, the memory cell 232 is a 3T DRAM memory cell. In this example, the memory cell 232 comprises three transistors 202-1, 202-2, and 202-3. The memory cell 232 may be operated to store a data value (e.g., stored charge at node 204). In some embodiments, a charge associated with the data value may be stored at node 204 using the parasitic capacitance generated between transistor 202-3 and transistor 203-2. Embodiments are not so limited; however, and the memory cell 232 may optionally include a discrete capacitor 203 to store the data value.

[0032] The memory cell 232 includes two word lines 209-1/209-2 (e.g., row lines) and two digit lines 205-1/205-2 (e.g., bit lines). Word line 209-1 may be referred to herein as a read row line, and the word line 209-2 may be referred to herein as a write row line. Digit line 205-1 may be referred to herein as a write digit line, and digit line 205-2 may be referred to herein as a read digit line.

The word lines 209-1/209-2 and the digit lines 205-1/205-2 may be enabled and/or disabled in conjunction with reading and writing data to the node 204 of the memory cell 232.

[0033] As shown in Figure 2A, the transistors 203-2, 203-2, and 203-3 are coupled to the word lines 209-1/209-2 and digit lines 205-1/205-2. In association with performing a write operation, the write row line 209-2 may be enabled, and data may be placed on the write digit line 205-1, thereby causing the data to be stored at node 204. Similarly, in association with performing a read operation, the read row line 209-1 may be enabled and the data may be transferred out of the node 204 via the read digit line 205-2. In some embodiments, the data value read out of the memory cell 232 as part of a read operation may be inverted in comparison to the data value written to the memory cell 232 as part of the write operation. For example, if a value of “1” is written to the memory cell 232, a value of “0” may be read out of the memory cell 232. Conversely, if a value of “0” is written to the memory cell 232, a value of “1” may be read out of the memory cell 232.

[0034] For example, memory cell 232 can be coupled to different digit lines 205-1/205-2 and word lines 209-1/209-2. For instance, in this example, a first source/drain region of transistor 202-3 is coupled to digit line 205-1, a second source/drain region of transistor 202-3 is coupled to node 204, and a gate of transistor 202-3 is coupled to word line 209-2. A first source/drain region of transistor 202-1 is coupled to digit line 205-2, a second source/drain region of transistor 202-1 is coupled to a first source/drain region of transistor 202-2, and a gate of transistor 202-1 is coupled to word line 209-1.

[0035] In some embodiments, the data value stored at node 204 of the memory cell 232 may be used as an operand for performance of a logical operation. For example, a data value stored at node 204 of the memory cell 232 may be used as an operand to perform a logical operation with a data value stored at node 204 of a different memory cell, as described in more detail in association with Figures 3-5. In some embodiments, the logical operation may comprise a NOR operation; however, embodiments are not so limited, and various logical operations such as ANDs, ORs, XORs, NANDs etc. operations may be performed by performing multiple combinations of NOR operations in the manner described herein.

[0036] In some embodiments, the memory cell 232 may be controlled to store a data value at node 204 subsequent to performance of a read operation. For example, the memory cell 232 may be controlled such that read operations are non-destructive. This may allow for multiple rows (e.g., read rows) to be fired without refreshing or re-writing data to the memory cell 232, which may allow for improved performance and reduced power consumption in comparison with previous approaches that utilize destructive read cells such as 1T1C memory cells.

[0037] Although schematically represented in a planar orientation, the transistors 202-1, 202-2, and/or 202-3 may be arranged in a vertical orientation (e.g., extending upward out of the page or downward into the page in Figure 2). In some embodiments, the transistors 202-1, 202-2, and/or 202-3 of the memory cell 232 may be formed such that the transistors 202-1, 202-2, and/or 202-3 are contained within an area defined by the digit lines 205-1/205-2. For example, the transistors 202-1, 202-2, and/or 202-3 of the memory cell 232 may be formed on pitch with digit lines 205-1/205-2 of the memory cell 232. In some embodiments, the memory cell 232 may be formed such that the transistors 202-1, 202-2, and/or 202-3 of the memory cell 232 are disposed within an area that equal to or less than an area used by a conventional 1T1C DRAM memory cell.

[0038] Figure 2B is another schematic drawing illustrating a portion of a memory array 230 in accordance with a number of embodiments of the present disclosure. As shown in Figure 2B, the memory array 230 comprises a plurality of memory cells 232. For clarity, only one memory cell 232 is labeled in Figure 2B; however, each set of three transistors illustrated in Figure 2B represents one of a plurality of memory cells 232 associated with the memory array 230.

[0039] A plurality of memory cells 232 are coupled to a plurality of digit lines 205 and row lines 209. For example, a first memory cell 232 is coupled to digit lines 205-1₀/205-2₀ (e.g., write digit₀ line 205-1₀ and read digit₀ line 205-2₀) and row lines 209-1₀/209-2₀ (e.g., read row₀ line 209-1₀ and write row₀ line 209-2₀). Similarly, a second memory cell is coupled to digit lines 205-1₁/205-2₁ (e.g., write digit₁ line 205-1₁ and read digit₁ line 205-2₁) and word lines 209-1₀/209-2₀ (e.g., read row₀ line 209-1₀ and write row₀ line 209-2₀), a third memory cell is coupled to digit lines 205-1₀/205-2₀ (e.g., write digit₀ line 205-1₀

and read digit0 line 205-2₀) and word lines 209-1₁/209-2₁ (e.g., read row1 line 209-1₁ and write row1 line 209-2₁, etc.

[0040] In operation, the memory array 230 may be controlled to perform a logical operation using data values (e.g., operands) stored in the memory cells. In some embodiments, performance of such logical operations can include precharging at least one of the digit lines 205-2₀, . . . , 205-2_N. Once the at least one digit line is precharged (e.g., to a supply voltage such as V_{cc}), one or more word lines 209-1₀, . . . , 209-1_N and/or 209-2₀, . . . , 209-2_N may be enabled. Each word line 209-1₀, . . . , 209-1_N and/or 209-2₀, . . . , 209-2_N that is enabled may correspond to an input of a K-input NOR operation where K is the quantity of word lines enabled. For example, if only two word lines (e.g., word line 209-1₀ and word line 209-1₁) are enabled, a 2-input NOR gate results, if three word lines (e.g., word line 209-1₀, word line 209-1₁, and word line 209-1₂) are enabled, a 3-input NOR operation results, etc. Further, each digit line 205-2₀, . . . , 205-2_N that is enabled may correspond to an additional K-input NOR gate. Accordingly, each digit line 205-2₀, . . . , 205-2_N that is enabled may correspond to N NOR gates that each comprise K-inputs where N is the number of enabled digit line 205-2₀, . . . , 205-2_N. As an example, if three word lines (e.g., word lines 209-1₀, . . . , 209-1₃ and/or word lines 209-2₀, . . . , 209-2₃) are enabled and each word line enables 1024 digit lines (e.g., when K=3 and N=1024), then 1024 3-input NOR gates result. That is, in some embodiments, enabling combinations of K word lines and N digit lines yields N NOR gates each having K inputs associated therewith.

[0041] In some embodiments, if one or more memory cells 232 coupled to a particular digit line 205-2₀, . . . , 205-2_N (e.g., if one or more memory cells in a particular column of memory cells) contains a high voltage (e.g., a logical value of “1”), the associated digit line 205-2₀, . . . , 205-2_N will be driven to a ground reference potential. For example, if memory cell 232 (or any other memory cell in the column of memory cells coupled to digit line 205-2₀) contains a high voltage, digit line 205-2₀ will be driven to a ground reference potential.

[0042] As described in more detail in association with Figure 3, herein, a sense amplifier (e.g., sense amplifier 306 illustrated in Figure 3) is coupled to respective pairs of digit lines 205-1₀, . . . , 205-1_N and 205-2₀, . . . , 205-2_N. The

sense amplifier may sense a low voltage (e.g., a logical value of “0”) if one or more of the memory cells coupled to a same pair of digit lines 205-1₀, . . . , 205-1_N and 205-2₀, . . . , 205-2_N that are also coupled to the sense amplifier contains a high voltage (e.g., a logical value of “1”). Conversely, the sense amplifier may sense a high voltage (e.g., a logical value of “1”) if one or more of the memory cells coupled to a same pair of digit lines 205-1₀, . . . , 205-1_N and 205-2₀, . . . , 205-2_N that are also coupled to the sense amplifier contains a low voltage (e.g., a logical value of “0”). That is, in some embodiments, the sense amplifier may sense a particular value (e.g., a “1” or a “0”) based on the value stored in the memory cell that is coupled thereto.

[0043] As mentioned above, because a read operation using the memory cell 232 described in Figures 2A and 2B may be non-destructive, the memory cell 232 may still contain the original data value (e.g., the same high or low voltage) that was stored therein prior to performance of the read operation and/or performance of the logical operation, while the sense amplifier may contain a result of the logical operation after performance of the logical operation. In some embodiments, the data value (e.g., the logical value of “0” or “1”) stored in the sense amplifier subsequent to performance of the logical operation may be written back to any memory cell 232 (or row of memory cells) in the memory array 230, as described in more detail in association with Figure 3, herein.

[0044] Figure 3 is a schematic diagram illustrating sensing circuitry 350 in accordance with a number of embodiments of the present disclosure. Figure 3 illustrates one sensing component 350 which can be one of a number of sensing components corresponding to sensing circuitry 150 shown in Figure 1. The sensing component 350 may be coupled to a memory cell, such as memory cell 232 shown in Figure 2 via the digit line 305-2 (e.g., read digit line 305-2) and the digit line 305-1 (e.g., write digit line 305-1). In some embodiments, the sensing component 350 includes a sense amplifier 306. As shown in Figure 3, the sense amplifier 306 is a current mode sense amplifier; however embodiments are not so limited and the sense amplifier 306 may be any suitable type of differential or non-differential sense amplifier.

[0045] The sense amplifier 306 can be operated to determine a data value (e.g., logic state) stored in a selected memory cell. The sense amplifier 306 can comprise a cross coupled latch 315 (e.g., gates of a pair of transistors, such as n-

channel transistors 327-1 and 327-2 that are cross coupled with the gates of another pair of transistors, such as p-channel transistors 329-1 and 329-2); however, embodiments are not limited to this example. The sense amplifier 306 may further include a transistor 333-1, which is coupled to the digit line 305-2, and transistor 333-2, which is coupled to a reference potential (e.g., a reference voltage).

[0046] In some embodiments, a source/drain region of a transistor 331 is coupled to the digit line 305-2 and a gate region of the transistor 331 is coupled to a Read enable signal line. In operation, when a memory cell (e.g., memory cell 232 illustrated in Figure 2) is being sensed (e.g., read), the transistor 331 is operable to allow signals to pass between a memory cell coupled to the digit line 305-2 and the sense amplifier 306 when the Read enable signal line is driven high. In some embodiments, the transistor 331 may be operable to gate signals on the digit line 305-2 when the Read enable signal line is driven low.

[0047] The cross-coupled latch 315 includes a plurality of transistors 327-1, 327-2, 329-1, and 329-2. The gates of transistors 327-2 and 329-2 are coupled to common node 317-1, while the source/drain region of transistors 327-2 and 329-2 are coupled to common node 317-2. In a complementary fashion, the gates of transistors 327-1 and 329-1 are coupled to common node 317-2, while the source/drain region of transistors 327-1 and 329-1 are coupled to common node 317-1. In some embodiments, the sense amplifier 306 may be operated to amplify a differential voltage between common node 317-1 and common node 317-2 such that the common node 317-1 is driven to one of V_{cc} and a ground reference potential.

[0048] Embodiments are not limited to the sensing component configuration illustrated in Figure 3. As an example, the sense amplifier 306 can be a single-ended sense amplifier (e.g., sense amplifier coupled to one digit line), or other suitable sense amplifier. Also, embodiments of the present disclosure are not limited to a single-ended sense amplifier architecture such as that shown in Figure 3.

[0049] Memory cells (e.g., memory cell 232 illustrated in Figure 2) can be arranged in rows coupled by word lines (e.g., row lines 209-1 and 209-2 illustrated in Figure 2A and 2B), etc., and columns coupled by digit lines 305-1 and 305-2. Although only two digit lines 305-1/305-2 are shown in Figure 3,

embodiments of the present disclosure are not so limited, and an array of memory cells can include additional columns of memory cells and digit lines (e.g., 4,096, 8,192, 16,384, etc.).

[0050] The digit lines 305-1 and 305-2 of memory array (e.g., memory array 130 shown in Figure 1) are coupled to sensing component 350 in accordance with a number of embodiments of the present disclosure. In this example, the sensing component 350 comprises a sense amplifier 306 corresponding to a respective column of memory cells (e.g., coupled to respective digit lines 305-1/305-2). For example, the sense amplifier 306 is coupled to the digit lines 305-1 and 305-2, which may also be coupled to a memory cell (e.g., memory cell 232 shown in Figure 2A) or column of memory cells (as shown in Figure 2B).

[0051] The digit line 305-1 is coupled to write transistor 313-1 and write complement transistor 313-2. A gate region of the write transistor 313-1 is coupled to a write true signal line (“Write true”) and a gate region of the write complement transistor is coupled to a write complement signal line (“Write comp”). Source/drain regions of the write transistor 313-2 and the write complement transistor 313-2 are coupled to common nodes 317-1 and 317-2 of the sense amplifier, respectively. In some embodiments, the write transistor 313-1 is operable to transfer a data value stored in the sense amplifier 306 to the memory cell (e.g., memory cell 232 illustrated in Figure 2) via the digit line 305-1, while in some embodiments the write complement transistor 313-2 is operable to transfer a complement of the data value stored in the sense amplifier 306 to the memory cell via the digit line 305-1. Providing the ability to write either the true or the complement of the data value stored in the sense amplifier 306 may facilitate performance of logical operations between operand stored in the memory cell(s) and/or performance of logical operations between operands stored in the memory cell and the sense amplifier 306 in accordance with a number of embodiments of the disclosure.

[0052] For example, when the write true signal line is driven high, the write transistor 313-1 is enabled such that a data value associated with common node 317-1 is transferred from the sense amplifier via the digit line 305-2. When the write complement signal line is driven high, the write complement transistor 313-2 is enabled such that a complement of the data value stored in the

sense amp (e.g., a data value associated with common node 317-2) is transferred from the sense amplifier 306 via the digit line 305-1.

[0053] The digit line 305-1 may be coupled to a precharge line (“Precharge1”), which may be configured to drive the voltage at transistor 316-1 either low or high depending on whether the Precharge1 line is driven high or low. A pair of transistors 316-2/316-3 may be coupled to a precharge line (“Precharge2”) line, which may be configured to drive the transistors 316-2/316-3 either high or low depending on whether the Precharge2 line is driven high or low.

[0054] As shown in Figure 3, each of the precharge transistors 316-1, 316-2, 316-3 can have a source/drain region that is driven to V_{cc} and a gate coupled to a respective one of the Precharge lines. For example, the gate of transistor 316-1 is coupled to the Precharge1 line and the gates of transistors 316-2 and 316-3 are coupled to the Precharge2 line. A drain/source region of transistor 316-1 is coupled to digit line 305-2 via sense amplifier input node 319, while respective source/drain regions of transistors 316-2 and 316-3 are coupled to digit line 305-1. As will be appreciated, a charge present on digit line 305-2 will be the same as a charge present at sense amplifier input node 319 during operation of the sensing component 350.

[0055] In operation, the sense amplifier 306 is configured to latch a data value (e.g., a data value read from a memory cell via digit line 305-1). In contrast to approaches that utilize a 1T1C DRAM memory cell, in order to write the data value from the sense amplifier 306 to the memory cell (e.g., memory cell 232 illustrated in Figure 2), the digit line 305-1 is enabled by, for example, operating the write true transistor 313-1 and/or the write complement transistor 313-2. In some embodiments, this is due to the non-destructive nature of read operations performed by the memory cell when the memory cell is a 3T memory cell.

[0056] Figure 4 is a schematic diagram illustrating sensing circuitry in accordance with a number of embodiments of the present disclosure. Figure 4 shows a number of sense amplifiers 406 coupled to respective digit lines 405-1 and 405-2. The sense amplifiers 406 shown in Figure 4 can correspond to sensing circuitry 150 shown in Figure 1 and/or sense amplifier 306 shown in Figure 3, for example.

[0057] Although not shown, memory cells, such as those described in Figure 2, are coupled to the respective digit lines 405-1 and 405-2. The cells of the memory array can be arranged in rows coupled by word lines and columns coupled by pairs of digit lines Read digit(n-1)/Write digit(n-1)_, Read digit(n)/Write digit(n)_, Read digit(n+1)/Write digit(n+1)_, etc. The individual digit lines corresponding to each pair of respective digit lines can also be referred to as data lines. Although only three pairs of digit lines (e.g., three columns) are shown in Figure 4, embodiments of the present disclosure are not so limited.

[0058] A data value present on a digit line 405-2 can be loaded into the corresponding sense amplifier 406. In some embodiments, the data value may be shifted from a memory cell associated with a first column of the array to sense amplifier 406 associated with a second column of the array. For example, a data value present on the Read digit_n digit line 405-2 can be loaded into sense amplifier 406-3, which is in a column adjacent to the column associated with the Read digit_n digit line 405-2. In some embodiments, the data may be shifted in this manner by enabling shift right transistor 421-3. Similarly, a data value present on the Read digit_n digit line 405-2 can be loaded into sense amplifier 406-1, which is in a column adjacent to the column associated with the Read digit_n digit line 405-2 by enabling shift left transistor 421-1. As will be appreciated, when the no shift transistor 421-2 is enabled, a data value present on the Read digit_n digit line 405-2 may be read into sense amplifier 406-2.

[0059] Embodiments are not limited to shifting data that is being read into the sense amplifier 406, and the shift left transistor 421-1, the no shift transistor 421-2, and/or the shift right transistor 421-3 may be individually enabled to shift data being written out the sense amplifiers 406 via digit line 405-1 to memory cells coupled to columns adjacent to the sense amplifier 406 from which the data value is being written.

[0060] Although not shown in Figure 4, each column may be coupled to memory cells (e.g., memory cell 232 shown in Figure 2), which can be coupled to a column decode line that can be activated to transfer, via a local I/O line, data values from corresponding sense amplifiers 406 to a control component external to the array such as an external processing resource (e.g., host processor and/or other functional unit circuitry). The column decode line can be coupled to a

column decoder. However, as described herein, in a number of embodiments, data need not be transferred via such I/O lines to perform shift operations in accordance with embodiments of the present disclosure. In a number of embodiments, shift circuitry (e.g., shift left transistor 421-1, the no shift transistor 421-2, and/or the shift left transistor 421-3) can be operated in conjunction with sense amplifiers 406 to perform shift operations without transferring data to a control component external to the array, for instance. As used herein, transferring data, which may also be referred to as moving data or shifting data is an inclusive term that can include, for example, copying data from a source location to a destination location and/or moving data from a source location to a destination location without necessarily maintaining a copy of the data at the source location (e.g., at the sense amplifier 406).

[0061] Figure 5 is another schematic diagram illustrating sensing circuitry in accordance with a number of embodiments of the present disclosure. Figure 5 shows a number of sense amplifiers 506 coupled to respective digit lines 505-1 and 505-2. The sense amplifiers 506 shown in Figure 5 can correspond to sensing circuitry 150 shown in Figure 1 and/or sense amplifier 306 shown in Figure 3, for example.

[0062] Although not shown, memory cells, such as those described in Figure 2, are coupled to the respective digit lines 505-1 and 505-2. The cells of the memory array can be arranged in rows coupled by word lines and columns coupled by pairs of digit lines Read digit(n-1)/Write digit(n-1)_, Read digit(n)/Write digit(n)_, Read digit(n+1)/Write digit(n+1)_, etc. The individual digit lines corresponding to each pair of respective digit lines can also be referred to as data lines. Although only three pairs of digit lines (e.g., three columns) are shown in Figure 5, embodiments of the present disclosure are not so limited.

[0063] A data value present on a digit line 505-1 can be loaded into the corresponding sense amplifier 506 via sense amplifier input node 519. In some embodiments, the data value may be shifted from a sense amplifier 506 associated with a first column of the array to sense amplifier 506 associated with a second column of the array. For example, a data value present on the Read digit_n digit line 505-2 can be loaded into the middle sense amplifier 506, which is in a column adjacent to the column associated with the Read digit_n-1 digit

line 505-2 and the Read digit_{n+1} digit line 506-2. The data value can then be shifted to the right sense amplifier 506 by enabling shift right transistor 521-3. Similarly, a data value present on the Read digit_n digit line 505-2 can be loaded into the middle sense amplifier 506 and shifted from the middle sense amplifier 506 to the left sense amplifier 506 by enabling shift left transistor 521-1. Accordingly, data values latched by the sense amplifiers 506 illustrated in Figure 5 may be shifted to the left or right from one sense amplifier to another by enabling the shift left and shift right transistors, which connect an output of one sense amplifier 506 to the input of an adjacent sense amplifier 506, as shown in Figure 5.

[0064] Figure 6 is a flow diagram 670 for performing logical operations using memory cells in accordance with a number of embodiments of the present disclosure. At block 671, a digit line may be precharged to a first voltage (e.g., a high voltage corresponding to a logical value of “1”). The digit line may be one or more of the digit lines 205 illustrated in Figure 2, for example. In some embodiments, the digit line that is precharged to the first voltage may be a read digit line.

[0065] At block 672, at least one word line of a memory array may be enabled (e.g., activated). The at least one word line may correspond to one or more of the word lines 209 illustrated in Figure 2, for example. The enabled word line may be a read row word line. As discussed above, each word line that is enabled can correspond a quantity of inputs (e.g., K inputs, where K is a non-zero integer) of a logical operation such as a NOR logical operation. Accordingly, the NOR logical operation may be a K-input NOR logical NOR operation. For example, if two word lines are enabled, a 2-input NOR operation results, if three word lines are enabled, a 3-input NOR operations results, etc. In some embodiments, each one of the K memory cells may store a data value corresponding to a respective one of the K-inputs. Further, as described above, each digit line enabled may correspond to a number (N) of NOR gates that each have K inputs corresponding the number (K) of word lines enabled associated therewith.

[0066] In some embodiments, a read word line can be activated. The read word line may be a read word line corresponding to the K memory cells. While at least one of the read word lines corresponding to the K memory cells is

activated, a sense amplifier coupled to the read digit line can be enabled. In some embodiments, subsequent to enabling the sense amplifier, a result of the K-input logical operation resides in the sense amplifier. The read word lines corresponding to the K memory cells may be activated simultaneously, or they may be activated at different times.

[0067] The sense amplifier may be configured to sense a particular logic value responsive to one or more of the K memory cells storing a first data value and sense a different logic value responsive to all of the K memory cells storing a second data value that is different than the first data value.

[0068] At block 674, a data value corresponding to the voltage of the digit line may be sensed by a sense amplifier coupled to the digit line. In some embodiments, if one more memory cells coupled to the digit line contains a first voltage (e.g., a logical value of “1”), the sense amplifier senses a second voltage (e.g., a low voltage corresponding to a logical value of “0”). Conversely, if one more memory cells coupled to the digit line contains the second voltage (e.g., a logical value of “0”), the sense amplifier senses the first voltage (e.g., a logical value of “1”).

[0069] As discussed above, a read operation may be non-destructive such that the original data value stored in the memory cell (e.g., the data value stored in the memory cell prior to performance of the logical operation) is still stored in the memory cell after performance of the logical operation. In some embodiments, the result of the logical operation may be stored in a sense amplifier coupled to the memory cell.

[0070] At block 675, a word line may be enabled to write the data value sensed by the sense amplifier to a row of the memory array associated with the word line. In some embodiments, the word line that is enabled to write the data value sensed by the sense amplifier to the memory array may be a write row word line. In some embodiments, the word line may be enabled to write the data value sensed by the sense amplifier to a row of the memory array while at least digit line (e.g., a row line) is enabled. This may allow for data to be written and read concurrently.

[0071] Finally, at block 676, the digit lines may be precharged to a first voltage again in anticipation of performing another logical operation.

[0072] Operations to perform a logical NOR operation in accordance with the disclosure can be summarized as follows:

Enable Precharge1 to precharge one or more read digit lines (e.g., digit lines 305-2 illustrated in Figure 3) to V_{cc} (e.g., to a high voltage)

Enable Precharge2 to precharge sense amplifier (e.g., digit lines 317-1 and 317-2 illustrated in Figure 3) to V_{cc} (e.g., to a high voltage)

Disable Precharge1

Disable Precharge2

Enable one or more read row lines

Fire sense amplifier (e.g., toggle RNL illustrated in Figure 3 from a low voltage to a high voltage)

Sense amplifier (e.g., sense amplifier 306 illustrated in Figure 3) senses a low voltage (e.g., a logic value of "0") if one or more cells on a read digit line contains a high voltage (e.g., a logic value of "1")

Sense amplifier senses a high voltage (e.g., a logic value of "1") if all cells on a read digit line contain a low voltage (e.g., a logic value of "0")

Disable read row lines

Enable one or more write row lines to write the value sensed by the sense amplifier to that row

Disable write row lines

Disable sense amplifier (e.g., toggle RNL illustrated in Figure 3 from a high voltage to a low voltage)

Enable Precharge1 to precharge one or more read digit lines to V_{cc} in preparation for a subsequent read and/or logical operation

Enable Precharge2 to precharge sense amplifier to V_{cc} in preparation for a subsequent read and/or logical operation

[0073] As described above in more detail, the read is non-destructive so the memory cells contain their original data. Accordingly, in some embodiments, only the sense amplifier contains the result of the NOR operation.

[0074] Operations to write the data value sensed by the sense amplifier to the memory array can be summarized as follows:

Enable one or more write row lines to write the value sensed by the sense amplifier

Enable write true transistor (e.g., WRITE TRUE transistor 313-1

illustrated in Figure 3) to write the data value stored in the sense amplifier to a memory cell array

Enable write comp transistor (e.g., WRITE COMP transistor 313-2 illustrated in Figure 3) to write the complement of the data value stored in the sense amplifier to a memory cell of the array

Disable write row lines

[0075] Although specific embodiments have been illustrated and described herein, those of ordinary skill in the art will appreciate that an arrangement calculated to achieve the same results can be substituted for the specific embodiments shown. This disclosure is intended to cover adaptations or variations of one or more embodiments of the present disclosure. It is to be understood that the above description has been made in an illustrative fashion, and not a restrictive one. Combination of the above embodiments, and other embodiments not specifically described herein will be apparent to those of skill in the art upon reviewing the above description. The scope of the one or more embodiments of the present disclosure includes other applications in which the above structures and methods are used. Therefore, the scope of one or more embodiments of the present disclosure should be determined with reference to the appended claims, along with the full range of equivalents to which such claims are entitled.

[0076] In the foregoing Detailed Description, some features are grouped together in a single embodiment for the purpose of streamlining the disclosure. This method of disclosure is not to be interpreted as reflecting an intention that the disclosed embodiments of the present disclosure have to use more features than are expressly recited in each claim. Rather, as the following claims reflect, inventive subject matter lies in less than all features of a single disclosed embodiment. Thus, the following claims are hereby incorporated into the Detailed Description, with each claim standing on its own as a separate embodiment.

What is claimed is:

1. An apparatus, comprising:
 - a first memory cell controlled to invert a data value stored therein;
 - a second memory cell controlled to invert a data value stored therein; and
 - a controller coupled to the first memory cell and second memory cell,wherein the controller is configured to cause performance of a logical operation between the data value stored in the first memory cell and the data value stored in the second memory cell.
2. The apparatus of claim 1, wherein the first memory cell and the second memory cell each comprise a three transistor (3T) dynamic random access memory cell.
3. The apparatus of claim 1, further comprising a write complement transistor coupled to the first memory cell, the write complement transistor operable to transfer a complement of a result of the logical operation via a digit line coupled to the first memory cell.
4. The apparatus of any of claims 1-3, wherein the first memory cell and the second memory cell are oriented vertically and are disposed within an area defined by respective first digit lines and respective second digit lines coupled to the first memory cell and the second memory cell.
5. The apparatus of any of claims 1-3, wherein the logical operation comprises a NOR logical operation.
6. The apparatus of any of claims 1-3, wherein the controller is further configured to cause a result of the logical operation to be stored in a sense amplifier coupled to the first memory cell or the second memory cell.
7. An apparatus, comprising:
 - an array of memory cells; and
 - a controller coupled to the array of memory cells, the controller

a first charge corresponding to a first operand of a logical operation to be inverted in a first memory cell of the array of memory cells;

a second charge corresponding to a second operand of the logical operation to be inverted in a second memory cell of the array of memory cells;
and

performance of a logical operation between the inverted first operand and the inverted second operand.

8. The apparatus of claim 7, wherein the controller is further configured to cause performance of logical operations without transferring the first operand, the second operand, and a result of the logical operation out of the memory array.

9. The apparatus of any of claims 7-8, wherein the inverted first logical operand and the second inverted logical operand are stored in the first memory cell and the second memory cell, respectively, after performance of the logical operation.

10. The apparatus of any of claims 7-8, wherein the first memory cell is configured to:

preserve the first charge corresponding to the first operand subsequent to performance of a write operation; and

preserve the second charge corresponding to the second operand subsequent to performance of the write operation.

11. The apparatus of any of claims 7-8, wherein the first memory cell is coupled to a first read row line and a first write row line of the array, and wherein the second memory cell is coupled to a second read row line and a second write row line of the array; and wherein the first memory cell and the second memory cell are coupled to a same read digit line of the array.

12. The apparatus of any of claims 7-8, wherein at least one of the first memory cell and the second memory cell is disposed within an area equal to or

less than an area defined by a single transistor, single capacitor (1T1C) memory cell.

13. An apparatus, comprising:
 - a plurality of three-transistor (3T) memory cells coupled to respective write digit lines, read digit lines, read row lines, and write row lines; and
 - a controller coupled to the plurality of 3T memory cells, wherein the controller is configured to cause:
 - a first data value stored in a first 3T memory cell to be inverted;
 - a second data value stored in a second 3T memory cell to be inverted; and
 - performance of a logical operation between the first inverted data value and the second inverted data value.
14. The apparatus of claim 13, further comprising a plurality of sense amplifiers coupled to respective memory cells among the plurality of 3T memory cells.
15. The apparatus of claim 14, wherein the controller is configured to cause:
 - a result of the logical operation to be stored in a first sense amplifier among the plurality of sense amplifiers; and
 - the result of the logical operation to be shifted from the first sense amplifier to a second sense amplifier among the plurality of sense amplifiers.
16. The apparatus of claim 14, further comprising write complement transistors coupled to respective write digit lines, wherein the write complement transistors are operable to transfer a complement of a result of the logical operation via the write digit line.
17. A method, comprising:
 - operating a memory cell to invert a data value corresponding to a first operand for a logical operation;

performing the logical operation between the inverted data value and a data value corresponding to a second operand stored in a storage location associated with a memory device.

18. The method of claim 17, further comprising preserving the data value corresponding to the first operand subsequent to performing the logical operation.

19. The method of any of claims 17-18, further comprising shifting a result of the logical operation from a first sense amplifier associated with the memory device to a second sense amplifier associated with the memory device.

20. The method of any of claims 17-18, further comprising transferring a complement of a result of the logical operation to at least one of a different memory cell associated with the memory device and a sense amplifier associated with the memory device.

21. A method, comprising:

performing a K-input logical operation by:

charging, to a first voltage, a read digit line coupled to K memory cells, wherein each one of the K memory cells stores a data value corresponding to a respective one of the K-inputs;

activating read word lines corresponding to the K memory cells;

while at least one of the read word lines corresponding to the K memory cells is activated, enabling a sense amplifier coupled to the read digit line, wherein subsequent to enabling the sense amplifier, a result of the K-input logical operation resides in the sense amplifier, and wherein the sense amplifier is configured to:

sense a particular logic value responsive to one or more of the K memory cells storing a first data value; and

sense a different logic value responsive to all of the K memory cells storing a second data value that is different than the first data value.

22. The method of claim 21, wherein the method includes activating the read word lines corresponding to the memory cells simultaneously.

23. The method of any of claims 21-22, wherein the K memory cells are three transistor dynamic random access memory (3T DRAM) cells



Fig. 1

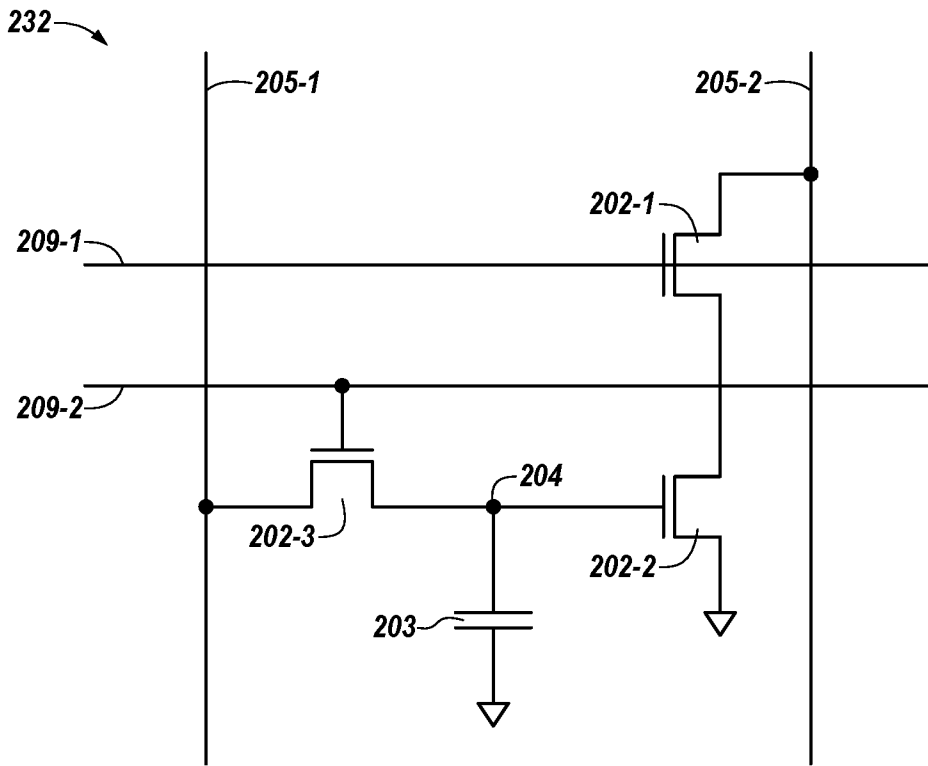


Fig. 2A

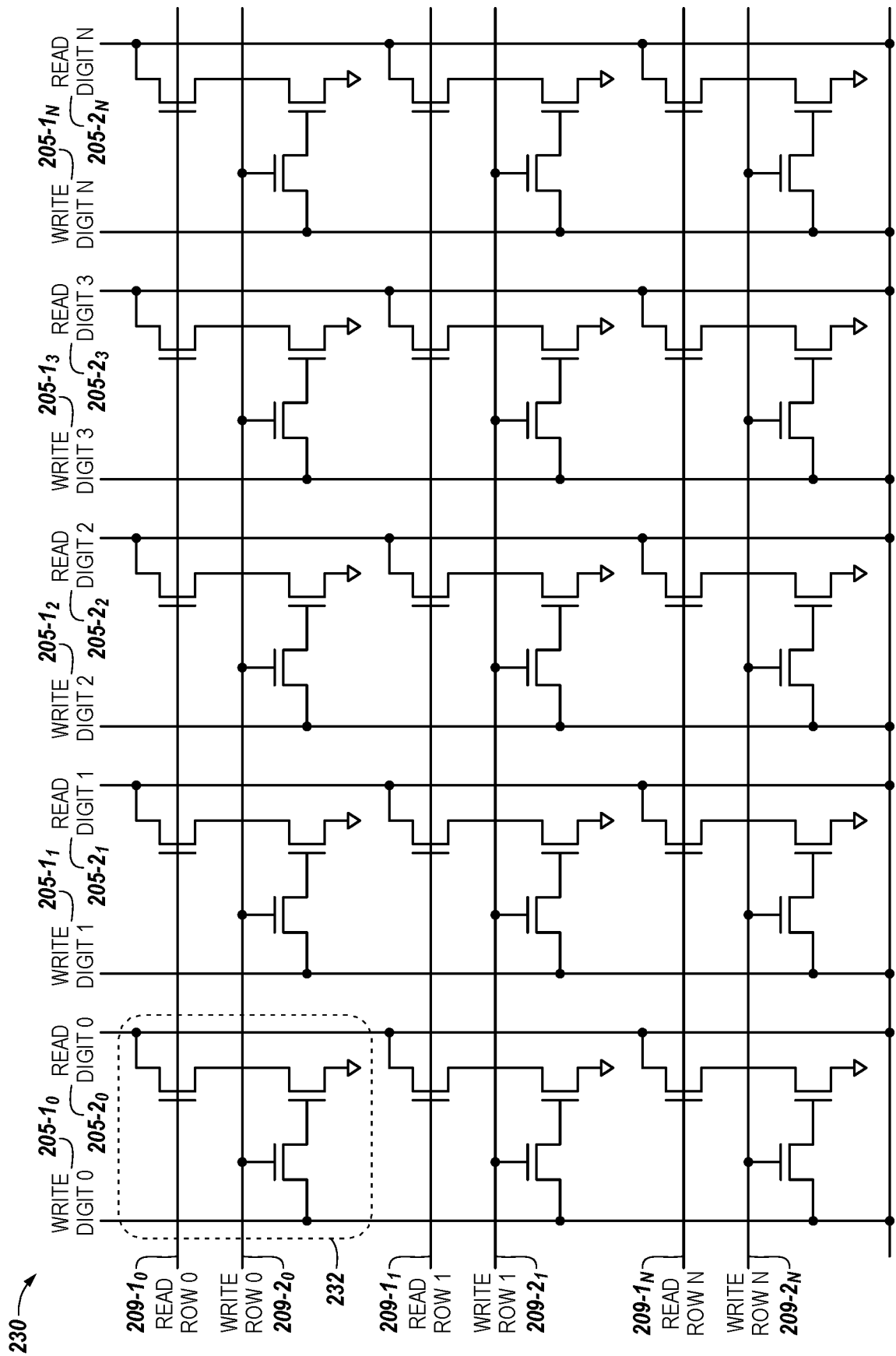


Fig. 2B

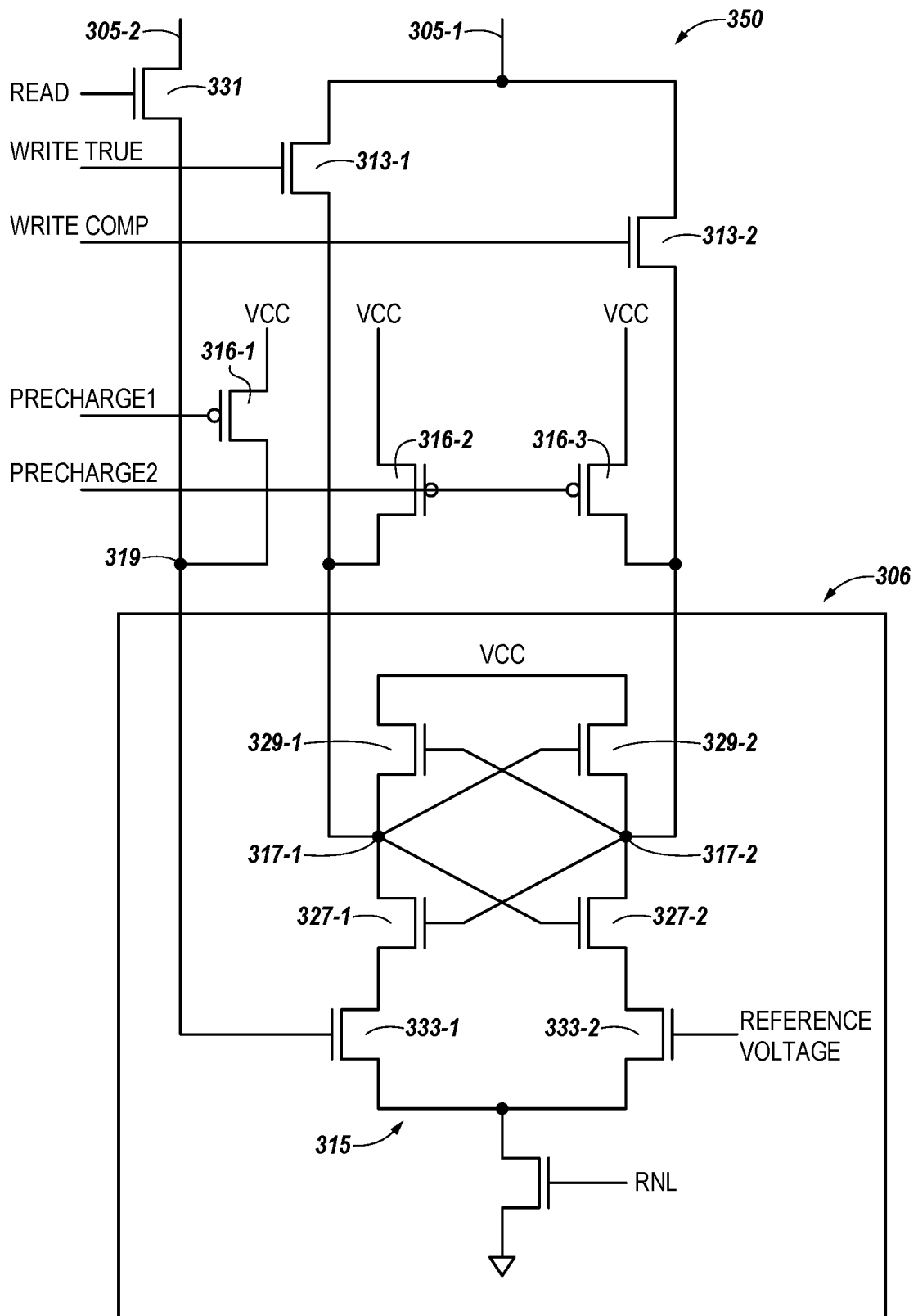


Fig. 3

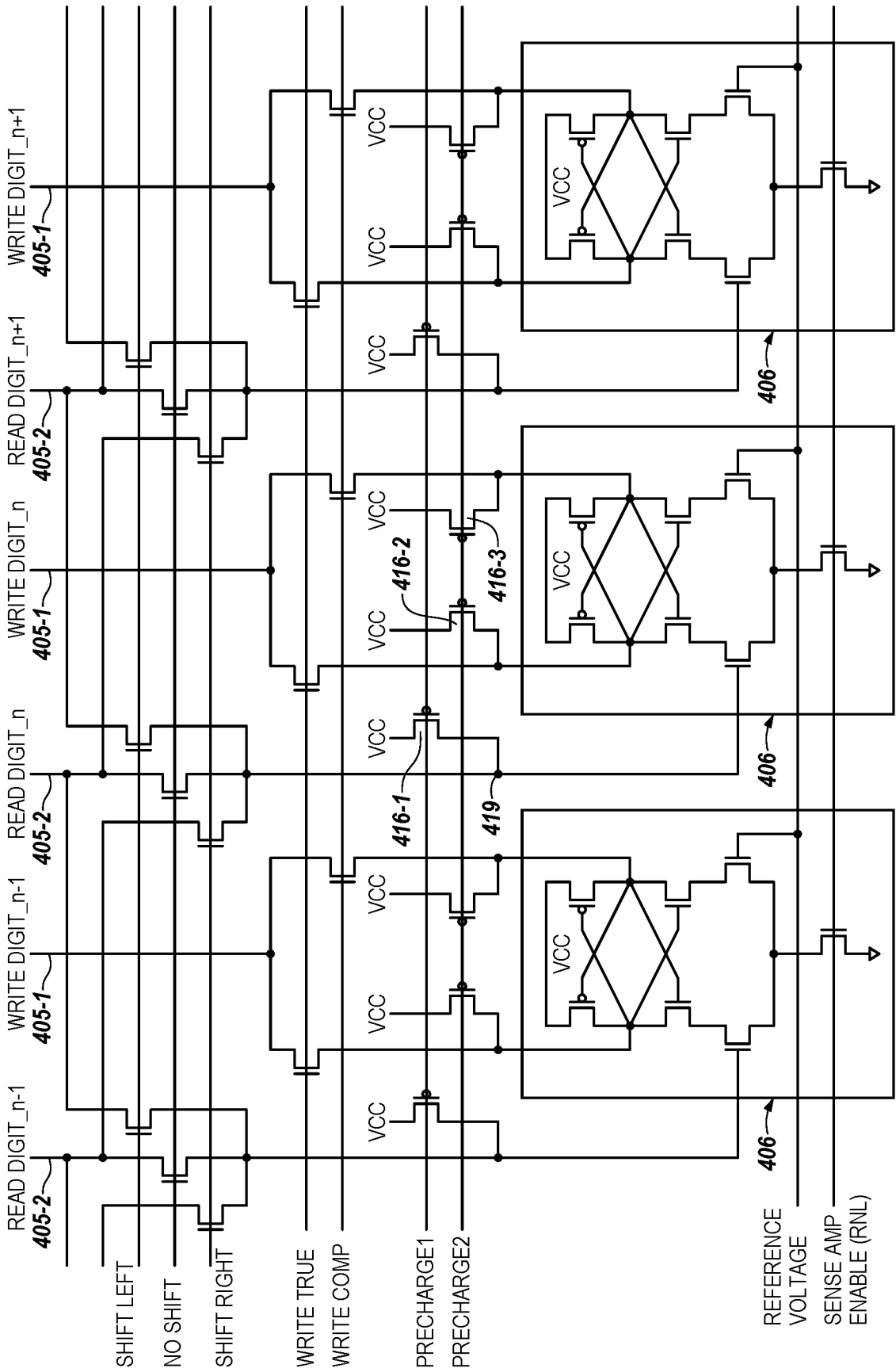


Fig. 4

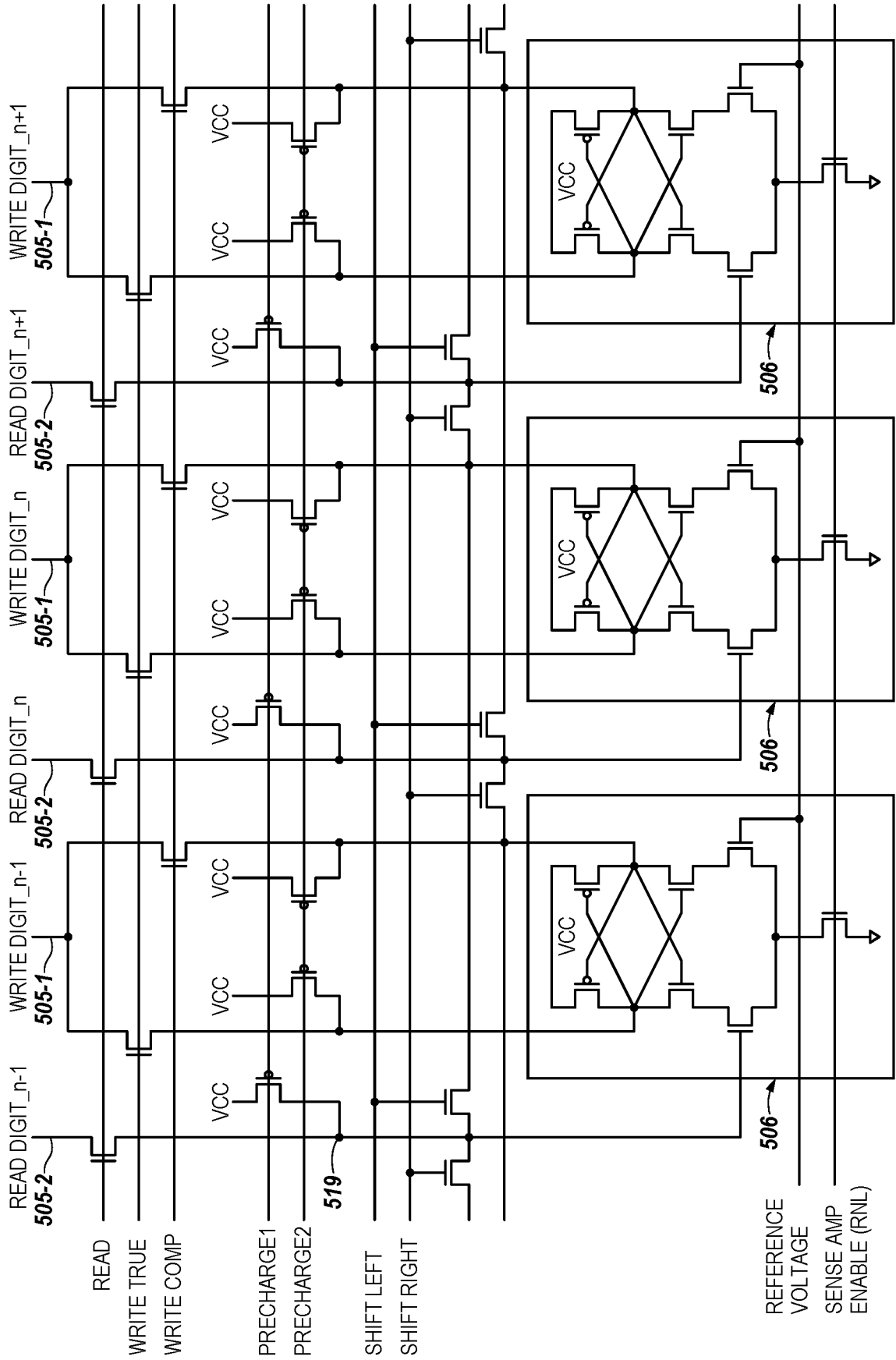


Fig. 5

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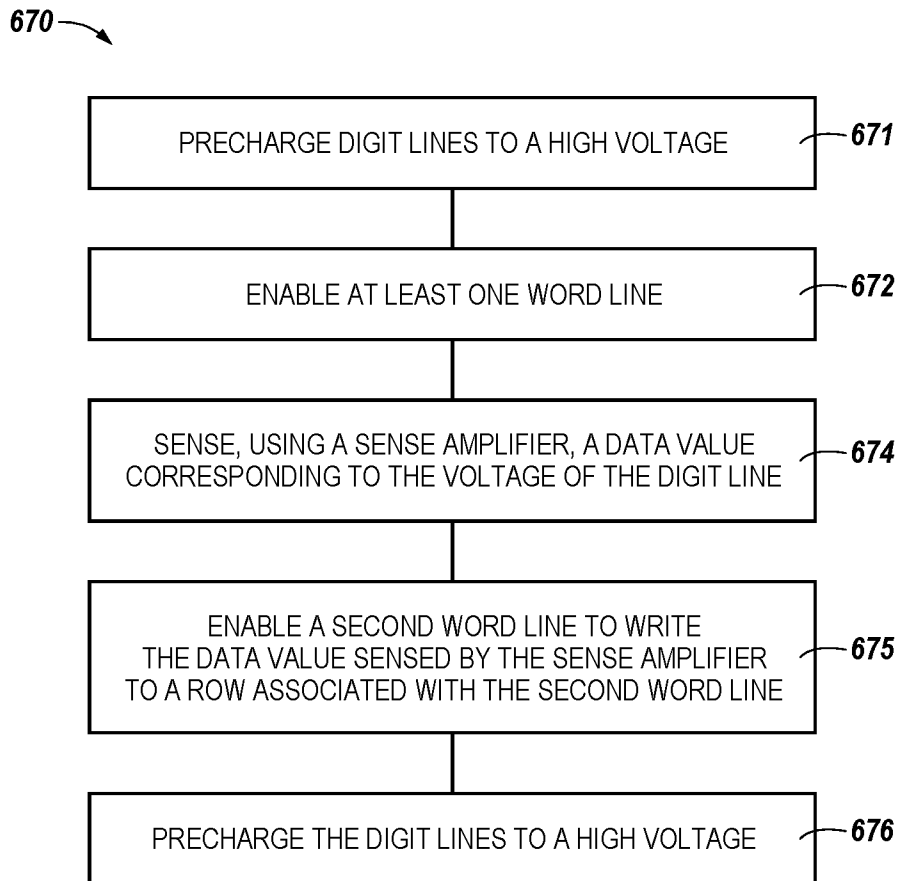


Fig. 6

A. CLASSIFICATION OF SUBJECT MATTER**G11C 11/4093(2006.01)i, G11C 11/4091(2006.01)i, G11C 7/06(2006.01)i, G11C 7/10(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G11C 11/4093; G06F 12/00; G11C 11/00; G11C 11/4091; G11C 7/00; G11C 7/08; G11C 7/10; G11C 7/22; H01L 27/115; G11C 7/06

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & keywords: memory cell, invert, logical operation, three transistor(3T) DRAM, sense amplifier, write complement transistor, digit line

C. DOCUMENTS CONSIDERED TO BE RELEVANT

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Y		2,13-16,23
Y	US 2014-0374747 A1 (SEMICONDUCTOR ENERGY LABORATORY CO., LTD.) 25 December 2014 See paragraphs [0299]-[0300]; and figure 16.	2,13-16,23
A	US 2014-0250279 A1 (MICRON TECHNOLOGY, INC.) 04 September 2014 See paragraphs [0021]-[0046]; and figures 2A-2B.	1-23
A	US 2009-0141537 A1 (IGOR ARSOVSKI) 04 June 2009 See paragraphs [0052]-[0057]; and figures 12-17.	1-23
A	US 2017-0323674 A1 (SK HYNIX INC.) 09 November 2017 See paragraphs [0039]-[0059]; and figures 2-3.	1-23

 Further documents are listed in the continuation of Box C. See patent family annex.

* Special categories of cited documents:

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

30 April 2019 (30.04.2019)

Date of mailing of the international search report

01 May 2019 (01.05.2019)

Name and mailing address of the ISA/KR

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2019/013765

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