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(54) Title: A CONTROL IC OF A SWITCH POWER SUPPLY AND A SWITCH POWER SUPPLY USING THE SAME

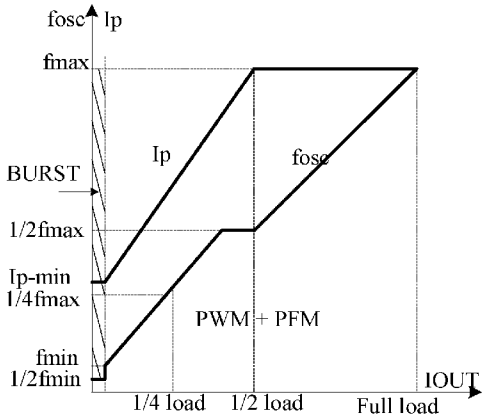

FIG. 4

(57) Abstract: A control IC of a switch power supply, connected with a switch of the switch power supply, comprises: a voltage collecting module (112), configured to collect a feedback voltage of an output voltage of the switch power supply; an error amplifying module (113), configured to compare the feedback voltage and a reference voltage and output a error voltage; a time collecting module (114), configured to obtain a degaussing time signal according to the feedback voltage, and a control module (115), configured to collect a peak current feedback signal of the switch, control a frequency and duty ratio of a control signal according to the error voltage (VEA), the degaussing time signal (Tds) and the peak current feedback signal (CS), and control the switch according to the control signal. A switch power supply is also provided.

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A CONTROL IC OF A SWITCH POWER SUPPLY AND A SWITCH POWER SUPPLY USING THE SAME

CROSS-REFERENCE TO RELATED APPLICATION

This application claims priority to, and benefits of Chinese Patent Application Serial No. 201110215457.0, filed with the State Intellectual Property Office of P. R. C. on July 29, 2011, the entire contents of which are incorporated herein by reference.

TECHNICAL FIELD

Example embodiments of the present disclosure relate generally to an IC, and more particularly, to a control IC of a switch power supply and a switch power supply using the same.

BACKGROUND

Almost all the main power supply of the household appliance or the power supply for the control part of the household appliance need to use a low voltage direct current (DC) power supply, but considering the voltage transmission loss problem, only 220V or 110V alternating current (AC) power supply can be provided. Therefore, a high efficiency and cost-effective AC-DC converter is indispensable. The traditional AC-DC device is achieved by using a linear converter. Butwith the disadvantage of huge volume, heavy weight, low convert efficiency and unobvious cost advantage, the linear converter is being eliminated. And the switch power supply becomes a mainstream in the AC-DC devices. To satisfy the accuracy and the isolation safety requirement, a switch power supply with secondary feedback control is generally used.

FIG. 1 shows a switch power supply circuit with feedback control in the prior art. The main AC passes through the full-wave rectifier and is converted to high voltage DC and stored in the capacitor C1. R2 and C2 provide power to the IC. The output voltage is divided by the resistor R6 and R7, then amplified by the amplifier TL431 and transmitted to the voltage sampling terminal of the IC by the optocoupler H1. The IC controls the open time and frequency of switchQ1 according to the sampled output voltage and then adjust the energy of the present cycle stored by the primary side winding, so a close loop negative feedback system is formed to maintain the value of the output voltage. But the work current of optocoupler H1 and TL431 is larger than 1 mA, the standby power consumption of the power system increases.

SUMMARY

According to one exemplary embodiment of the present invention, a control IC of a switch power supply is provided to decrease the standby power consumption of the power system. The control IC of a switch power supply, connected with a switch of the switch power supply, comprises: a voltage collecting module, configured to collect a feedback voltage of an output voltage of the switch power supply; an error amplifying module, configured to compare the feedback voltage and a reference voltage and output a error voltage; a time collecting module, configured to obtain a degaussing time signal according to the feedback voltage; and a control module, configured to collect a peak current feedback signal of the switch, control a frequency and duty ratio of a control signal according to the error voltage, the degaussing time signal and the peak current feedback signal, and control the switch according to the control signal.

According to one exemplary embodiment of the present invention, switch power supply is also provided. The switch power supply comprises a control IC mentioned above; an input filter and rectification module, configured to remove an unwanted frequency from an alternating current (AC) voltage and convert the alternating current (AC) voltage to a direct current (DC) voltage; a switch; a primary side winding, configured to convert the DC voltage to an electromagnetic signal under a control of the switch; a power supply module, configured to provide a voltage to the control IC; a primary side feedback module, configured to divide the voltage of the power supply module and feedback the divided voltage to the control IC; a primary side collecting module, configured to collect the peak current feedback signal of the switch; a secondary side winding, configured to convert the electromagnetic signal to an electric signal and generate an output AC voltage; an output rectification module, configured to convert the output AC voltage to a DC voltage; a voltage regulating module, configured to store the DC voltage from the output rectification module and provide an output power to maintain the value of the output voltage when the switch is closed; and a dummy load module, configured to consume the output AC voltage from the secondary side winding in no-load situation.

The error amplifying module compares the feedback voltage and a reference voltage and output an error voltage, the load situation of the power system may be judged. The frequency and duty ratio of the control signal is controlled according to the load situation of the power system, the degaussing time signal and the peak current feedback signal, to make the power system output a constant voltage and current signal, and the work frequency of a control IC

may be reduced when in the low load situation. Therefore, the switch loss of the power system is reduced and then the standby power consumption of the power system decreases.

BRIEF DESCRIPTION OF THE DRAWINGS

Having thus described example embodiments of the present disclosure in general terms, reference will now be made to the accompanying drawings, which are not necessarily drawn to scale, and wherein:

FIG. 1 illustrates a circuit of a switch power supply in the prior art;

FIG. 2 illustrates a block diagram of a switch power supply according to one exemplary embodiment of the present invention;

FIG. 3 illustrates a block diagram of a control module according to one exemplary embodiment of the present invention;

FIG. 4 illustrates a schematic diagram of the change trend of the IC work frequency and primary side winding current corresponding to the load according to one exemplary embodiment of the present invention;

FIG. 5 illustrates a schematic diagram method of a PMW mode according to one exemplary embodiment of the present invention;

FIG. 6 illustrates a schematic diagram method of a PFM/BURST mode according to one exemplary embodiment of the present invention;

FIG. 7 illustrates a word process diagram of a control module in PFM/BURST mode according to one exemplary embodiment of the present invention;

FIG. 8 illustrates a circuit of a switch power supply according to one exemplary embodiment of the present invention; and

FIG. 9 illustrates a circuit of a switch power supply according to one exemplary embodiment of the present invention.

DETAILED DESCRIPTION

The present invention now will be described more fully hereinafter with reference to the accompanying drawings, in which preferred embodiments of the invention are shown. This

invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein; rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art.

Referring to FIG. 2, a control IC of a switch power supply is provided. The control IC is connected to a switch of the switch power supply and comprises: a voltage collecting module 112, configured to collect a feedback voltage of an output voltage of the switch power supply; an error amplifying module 113, configured to compare the feedback voltage and a reference voltage and output an error voltage; a time collecting module 114, configured to obtain a degaussing time signal according to the feedback voltage; and a control module 115, configured to collect a peak current feedback signal of the switch, control a frequency and duty ratio of a control signal according to the error voltage, the degaussing time signal and the peak current feedback signal, and control the switch according to the control signal.

The degaussing time signal Tds is obtained according to the feedback voltage, and the feedback voltage is relative to the output voltage of the switch power supply. When the switch of the switch power supply is switched on, an auxiliary winding of the switch power supply couple a primary side winding of the switch power supply and the obtained feedback voltage is a minus voltage. When the switch is switched off and a diode of the switch power supply is switched on, the output voltage of a secondary side winding of the switch power supply is the output voltage of the switch power supply, and the auxiliary winding couple the secondary side winding and the obtained feedback voltage is a plus voltage. When the switch is switched off and a diode is switched off, the feedback voltage is a oscillation voltage. So when the voltage collecting module collects the feedback voltage, the degaussing time signal is obtained. The value of the degaussing signal is equal to the turn on time of the diode.

The error amplifying module compares the feedback voltage and a reference voltage and output an error voltage, the load situation of the power system may be judged. The frequency and duty ratio of the control signal is controlled according to the load situation of the power system, the degaussing time signal and the peak current feedback signal to make the power system output a constant voltage and current signal, and the work frequency of a control IC may be reduced when in the low load situation. Therefore, the switch loss of the power system is reduced and then the standby power consumption of the power system decreases.

Referring to FIG. 2, VDD is the power terminal, GND is the ground, COMP is the compensation terminal, CS is the collecting terminal of the peak current feedback signal, INV is the collecting terminal of the feedback voltage, DRI is the driving terminal to drive the switch.

In some embodiment of the present invention, the control IC further comprises a compensating module 116, configured to compensate the feedback voltage according to the error voltage. Different voltage compensation may be achieved. The heavier is the load, the larger is the voltage compensation, which is to compensate the loss voltage that is loss in the wire.

In some embodiment of the present invention, the control IC further comprises a circuit starting module 111, configured to output an enable signal when the voltage of the circuit starting module reaches a preset start voltage and provide power to the voltage collecting module, error amplifying module, time collecting module and control module; wherein the control module further configured to receive the enable signal and output the control signal. When the control IC powers on, the circuit starting module 111 resets the other module of the control IC. When the voltage of the power supply module reaches the preset start voltage, the circuit starting module outputs the enable signal and the control IC starts to work and output the control signal, and the switch starts to work according to the control signal at the same time.

In some embodiment of the present invention, the control IC further comprises a high voltage to low voltage converting module 117, configured to provide power and a enable signal to the low voltage part of the control IC according to the output voltage of the power supply module and a reference and bias module 118, configured to provide a reference voltage and a bias voltage.

Referring to FIG. 3, the control module 115 comprises: a collecting unit 1151, configured to collect the peak current feedback signal of the switch of the switch power supply; a mode judging unit 1152, configured to modulate the value of a judging current according to the error voltage of the error amplifying module; a mode controlling unit 1153, configured to modulate the value of a controlling current according to the error voltage of the error amplifying module; a reference current providing unit 1154, configured to provide a preset reference current; a pulse width modulating unit 1155, configured to obtain a first comparison voltage VOCP by overlapping the output current of the mode controlling unit and the preset reference current of

the reference current providing unit, and output a turn-off pulse OFF for the control signal when the first comparison voltage VOCP is equal to the value of the peak current feedback signal VCS; and a frequency modulating unit 1156, configured to output a turn-on pulse ON for the control signal according to the output current of the mode judging unit, the output current of the mode controlling unit and the degaussing time signal Tds.

When the pulse width modulating unit 1155 operates pulse width modulation, the control IC enters in the PWM mode; when the frequency modulating unit 1156 operates pulse frequency modulation, the control IC enters in the PFM mode; when the pulse width modulating unit 1155 operates pulse width modulation and the frequency modulating unit 1156 operates pulse frequency modulation simultaneously, the control IC enters in the BURST mode.

The output power of the switch power supply is constant, according to the formula P=UI, when the load connected the switch power supply is large, the output current I of the switch power supply increases and the output voltage U of the switch power supply deceases. The feedback voltage collected by the voltage collecting module 112 is far less than the reference voltage, and the error amplifying module 113 outputs a high level, that is the value of the output voltage VEA of the error amplifying module 113 is VDD. The mode judging unit 1152 maintains the judging current and output the judging current to the frequency modulating unit 1156, the mode controlling unit 1153 outputs a maximum current of the controlling current to the pulse width modulating unit 1155 and stops outputting current to the frequency modulating unit 1156 to maintain the peak current feedback signal. Then the peek current Ip of the primary side winding is maintained and Tds/T is maintained. According to the formula $Iout = 0.5 \cdot \frac{NP}{NS} \cdot \frac{Tds}{T} \cdot Ip$ (1), wherein NP is the turns of the primary side winding and NS is the turns of the secondary side winding, when the turns ratio between the primary side winding and the secondary side winding is constant, the output current Iout of the switch power supply is maintained. If the degaussing time signal Tds changes, the frequency modulating unit 1156 modulates the work cycle of the control IC, that is, modulates the work frequency fosc, so Tds/T is maintained. So when the output current of the switch power supply is maintained, the control IC enters in the PFM mode.

With the decrease of the load, the value feedback voltage gradually approaches the reference voltage and the error voltage VEA decreases gradually from VDD. When VEA< V 1, the work situation of the pulse width modulating unit 1155 and the frequency modulating unit

1156 is modulated according to the value of the error voltage VEA, and the pulse width modulating unit 1155 operates pulse width modulation and the frequency modulating unit 1156 operates pulse frequency modulation simultaneously, according to negative feedback voltage, the output voltage of the switch power supply is maintained; when the error voltage VEA decreases to V2, the control IC is adjusted to reach a limit, then if the load decreases further, the output voltage of the switch power supply may increase and the error voltage VEA decrease further; when VEA<V4, the mode judging unit 1153 modulates the judging current and the control IC enter in the BURST mode. When the control IC works under the BURST mode, the control IC process frequency division on the basis of the minimum work frequency, if the load increases, the output voltage of the switch power supply decreases, then the error voltage VEA increase; when VEA>V3, the control IC jump out of the BURST mode. There is a delay between V2 and V3. The V1、V2、V3 and V4 decrease successively.

FIG. 4 illustrates a schematic diagram of the change trend of the IC work frequency and primary side winding current corresponding to the load according to one exemplary embodiment of the present invention. Referring to the shadow part, the control IC works under the BURST mode. In this part of the diagram, the control IC works under the PWM mode and PFM mode. When the control IC works under the PWM mode and PFM mode, with the load decrease from heavy to light, the control IC works under PFM mode, then works under PWM mode and then works under the PWM mode and PFM mode. The above mentioned work procedure satisfies the requirement of the dynamic characteristic and decreases the work frequency when the load is light, so the work efficiency may be increased. In the BURST mode, the peek current of the primary side winding IP may be maintained the minimum value, the value of the work frequency is changed to a half of the minimum work frequency when the control IC work under the PFM mode, the loss of the switch power supply and the loss of a fake is decreased, so the loss of the switch power supply with no load may be decreased.

Referring to FIG. 5 and FIG. 6, the mode controlling unit 1153 comprises a first current source, connected with the pulse width modulating unit 1155, configured to increase a value of a first output current I1 when the error voltage increases; and a second current source, connected with the frequency modulating unit 1156, configured to decrease a value of a second output current I2 when the error voltage decreases, stop outputting the second output current when the error voltage is equal to the first preset voltage and maintain the value of the second output current when the error voltage is less than a second preset voltage. When the value of

the first reset voltage is VDD, that is when VEA=VDD, I2=0, when the error voltage is less than V4, I2 is maintained.

In FIG. 5, the reference current providing unit is a constant current source and the output voltage of the constant current source is I0. The pulse width modulating unit 1155 comprises a resistor R0, a first capacitor C0 and a first comparator A1, one terminal of the resistor R0 is connected to an output terminal of the first current source, an output terminal of the reference current providing unit, an terminal of the capacitor C0 and an negative terminal of the comparator A1, the other terminal of the resistor R0 is connected to the other terminal of the first capacitor C0 and the ground, an positive terminal of the comparator A1 is connected to the collecting unit. The positive terminal of the comparator A1 is connected to the collecting unit to collect a peak current feedback signal VCS, the negative terminal of the comparator receives a first comparison voltage VOCP, VOCP=R0×(I0+I1).

When the switch power supply is full load or over load, the output voltage of the switch power supply is small, so the collected feedback voltage is small and the error voltage VEA=VDD. The first current is controlled by the error voltage, accordingly, when the error reaches the maximum value, the first current reaches the maximum value and the error voltage reaches the maximum value, and the primary peak current Ip obtained according to the peak current feedback signal is maintained. The turn-on time of the switch is from receiving the turn-on pulse ON for the control signal to receiving the turn-off pulse OFF for the control signal. When the primary peak current Ip is maintained, the time for the first comparator to output the turn-off pulse OFF is constant, so the turn-on duty ratio of the switch is maintained.

When the load of the switch supply decreases to a preset value, the output voltage of the switch power supply increases, and the error voltage VEA decreases from VDD. The first current I1 decreases with the decrease of the error voltage VEA, and the turn-on duty ratio decreases with the decrease of the first current I1, so the output voltage of the switch power supply decreases and a negative feedback is formed. If the load of the switch power supply become heavy but is not the full load, with the increase of the load, the output voltage of the switch power supply decreases and the error voltage VEA increases. The first current I1 increases with the increase of the error voltage VEA, and the turn-on duty ratio increases with the increase of the first current I1, so the output voltage of the switch power supply increases and the output voltage of the switch power supply is maintained to a constant voltage.

FIG. 6 illustrates a schematic diagram method of a PFM/BURST mode according to one exemplary embodiment of the present invention. In some embodiments of the present invention, the mode judging unit 1152 is a third current source. The third current source may reduce the value of a third output current I3 to less than a preset reference current value when the error voltage of the error amplifying module is less than the second preset voltage, and maintain the value of the third output current I3 when the error voltage is equal to or larger than the second preset voltage.

The frequency modulating unit 1156 comprises: a second capacitor C1; a third capacitor C2; a second comparator A2; a first switch K1, of which a first terminal is connected to the output terminal of the second current source and a second terminal is connected to a terminal of the second capacitor C1 and a negative terminal of the second comparator A2, configured to close or open according to the degaussing time signal; and a second switch K2, of which a first terminal is connected to the output terminal of the second current source, a second terminal is connected to a second terminal of the first switch K1, and a third terminal is connected to a terminal of the third capacitor C2 and a positive terminal of the second comparator A2, configured to connect the first terminal and the second terminal of the second switch or to connect the first terminal and the third terminal of the second switch according to the degaussing time signal.

Referring to FIG. 7, in some embodiment of the present invention, the procedure of the PFM/BURST mode comprises four stages:

The first stage: in the beginning of the first cycle T, the second capacitor C1 and the third capacitor C2 are reset.

The second stage: receiving the turn-on pulse ON for the control signal VCOMP, the switch is switched on and the degaussing time signal Tds is low level, the third current source may charge the third capacitor C2 through the third output current I3, the voltage of the third capacitor VC2 increases and the second comparator A2 output the high level.

The third stage: a time Ton is ended, the switch is switched off and the procedure may enter the degaussing stage . The degaussing time signal Tds is high level, the second output current I2 and the third output current I3 charge the second capacitor C1 together, so the voltage of the second capacitor VC1 increase and the voltage of the third capacitor VC2 is maintained. When VC1>VC2, the second comparator A2 turns to low level from high level.

The fourth stage: the degaussing stage is ended, when VC1>VC2, the second comparator A2 outputs low level and the degaussing time signal Tds is low level, the voltage of the second capacitor VC1 is maintained and the third output current I3 charges the third capacitor C2 continuously until VC2>VC1. When VC2>VC1, the second comparator A2 turns to high level from low level and the control signal VCOMP turns to low level from high level and output the turn-on pulse ON, the switch is switched on, and resets the second capacitor C1 and the third capacitor C2. The first cycle is ended.

According to the work procedure mentioned above, some formulas described below are obtained:

$$\Delta Vc1 = \frac{(I2 + I3) \cdot Tds}{C1} \quad (2);$$

$$Toff + Ton = \frac{C2 \cdot \Delta Vc1}{I3} = \frac{C2(I3 + I2) \cdot Tds}{I3 \cdot C1} \quad (3);$$

The formula $\frac{Tds}{T} = \frac{Tds}{Tds + Ton + Toff} = \frac{I3 \cdot C1}{I3 \cdot C1 + C2(I3 + I2)}$ (4) is obtained according to formula (2) and (3).

When the switch power supply is full load or over load, the output voltage of the switch power supply is small, so the collected feedback voltage is small and the error voltage VEA=VDD. When VEA=VDD, I2=0, the change of the second current is opposite to the change of VEA, the third current I3 is maintain, so the charge current for the second capacitor C1 and the third capacitor C2 is the same, the formula $\frac{Tds}{T} = \frac{C1}{C1 + C2}$ (5) is obtained according to formula (4). That is the value of Tds/T is determined by the ratio of the value of the second capacitor C1 and the third capacitor C2. When the value of the second capacitor C1 and the third capacitor C2 is determined, then when the switch power supply outputs the constant current, the value of Tds/T is maintained.

When the load of the switch supply decreases to a preset value, the output voltage of the switch power supply increases, and the error voltage VEA decreases from VDD. The second current I2 increases with the decrease of the error voltage VEA. According to formula (4), the work cycle T increases make the work frequency fosc of the control IC decreases, and the output energy of the switch power supply decreases and the output voltage of the switch power supply decrease; if the load become heavy, the error voltage decreases. The second current I2

decreases with the increase of the error voltage, and the work frequency fosc of the control IC is increased. So the output voltage of the switch power supply increases and the negative feedback loop is formed to output a constant voltage.

When V2<VEA<V1, the control IC enters in the PWM and PFM mode, the second current I2 is changed with the error voltage VEA. The smaller is the error voltage VEA, the larger is the second current I2. According to formula (4), Tds/T decreases with the decrease of the error voltage VEA, if Tds is maintained, the work cycle T increases with the decrease of the error voltage VEA. That is with the decrease of the error voltage VEA, the work frequency fosc of the control IC is decreased, the purpose of the PFM is achieved.

When VEA<V4, the control IC enters in the BURST mode, the second current I2 is maintained, the value of the third current I3 will jump to a small value and be maintained. According to formula (4), the value of Tds/T may increase further, the work frequency fosc of the control IC decreases further until the control IC jump out of the BURST mode. When VEA<V4, it may be known the switch power supply is light load or no load, the work frequency fosc of the control IC is decreased further, so switch consumption of the switch power supply decreases and the purpose of decreasing the standby power consumption is achieved.

Referring to FIG. 8, a switch power supply comprising: a control IC mentioned above; an input filter and rectification module 11, configured to remove an unwanted frequency from an alternating current (AC) voltage and convert the alternating current (AC) voltage to a direct current (DC) voltage; a switch; a primary side winding 13, configured to convert the DC voltage to a electromagnetic signal under the control of the switch; a power supply module 14, configured to provide a voltage to the control IC; a primary side feedback module 15, configured to divide the voltage of the power supply module and feedback the divided voltage to the control IC; a primary side collecting module16, configured to collect the peak current feedback signal of the switch; a secondary side winding 17, configured to convert the electromagnetic signal to a electric signal and generate an output AC voltage; an output rectification module 18, configured to convert the output AC voltage to a DC voltage; a voltage regulating module 19, configured to store the DC voltage from the output rectification module and provide an output power to maintain the value of the output voltage when the switch is closed; and a dummy load module 20, configured to consume the output AC voltage from the secondary side winding in no-load situation.

The error amplifying module compares the feedback voltage and a reference voltage and output an error voltage, the load situation of the power system may be judged. The frequency and duty ratio of the control signal is controlled according to the load situation of the power system, the degaussing time signal and the peak current feedback signal to make the power system output a constant voltage and current signal, and the work frequency of a control IC may be reduced when in the low load situation. Therefore, the switch loss of the power system is reduced and then the standby power consumption of the power system decreases.

In some embodiment of the present invention, the switch power supply further comprises a first voltage absorbing module 21, connected between the input filter and rectification module and the primary side winding and configured to absorb a peak voltage caused by a leakage inductance to avoid breaking the switch.

In some embodiment of the present invention, the switch power supply further comprises a second voltage absorbing module 22, connected between the secondary side winding and the voltage regulating module and configured to absorb a peak voltage generated during a reverse recovery stage of the output rectification module.

Referring to FIG. 9, the primary side of the switch power supply comprises a primary side winding Np, a switch Q1configured to control the primary side winding Np and the control IC1 configured to control the switch Q1 to turn on or turn off. The switch power supply further comprises a fuse FR1 configured to cute off the AC input to protect the switch power supply when a fault appears. The input filter and rectification module comprises a full wave rectifier and a filter. The full wave rectifier comprises diodes D1-D4, configured to convert the alternating current (AC) voltage to a direct current (DC) voltage. The filter comprises capacitors C01, C02 and inductance L1 configured to remove the unwanted frequency from the AC voltage. The power supply module comprises resistors R3, R4, and capacitor C4, auxiliary winding Nd and a diode D6. The capacitor C4 is charged through R3and R4 and provides the power to the control IC1. When the voltage of the control IC1 reaches a preset start voltage, the switch power supply starts normally, the primary side winding Np starts to store energy until the primary current reaches a certain value. The switch Q1 is switched off when the primary current reaches a certain value. The output voltage by the auxiliary winding Nd is divided by R6 and R7 and the divided voltage is feedback to the control IC1, and the control IC1 sample the voltage of R9 and obtains the peak current feedback signal, so the load situation of the switch power supply may be judged and the work status of the switch may be adjusted. When

the switch Q1 is switched off, the energy of Np couples to the output winding Ns, the AC output voltage of Ns is rectified by the output rectification module to a DC voltage. In this embodiment, the output rectification module is a diode D7. The DC voltage output by D7 is stored by the capacitor C7 and provides output voltage when the switch is switched off to maintain the stability of the output voltage. In this embodiment, the dummy load module is resistor R12 configured to consume energy the output winding Ns to maintain the value of the output voltage.

It will be appreciated by those skilled in the art that changes could be made to the examples described above without departing from the broad inventive concept. It is understood, therefore, that this invention is not limited to the particular examples disclosed, but it is intended to cover modifications within the spirit and scope of the present invention as defined by the appended claims.

WHAT IS CLAIMED IS:

1. A control IC of a switch power supply, connected with a switch of the switch power supply, comprising:

a voltage collecting module, configured to collect a feedback voltage of an output voltage of the switch power supply;

an error amplifying module, configured to compare the feedback voltage and a reference voltage and output an error voltage;

a time collecting module, configured to obtain a degaussing time signal according to the feedback voltage; and

a control module, configured to collect a peak current feedback signal of the switch, control a frequency and duty ratio of a control signal according to the error voltage, the degaussing time signal and the peak current feedback signal, and control the switch according to the control signal.

2. The control IC of a switch power supply of claim 1, wherein the control module comprises:

a collecting unit, configured to collect the peak current feedback signal of the switch;

a mode judging unit, configured to modulate a value of a judging current according to the error voltage;

a mode controlling unit, configured to modulate a value of a controlling current according to the error voltage;

a reference current providing unit, configured to provide a preset reference current;

a pulse width modulating unit, configured to obtain a first comparison voltage by overlapping an output current of the mode controlling unit and the preset reference current, and output a turn-off pulse for the control signal when the first comparison voltage is equal to the value of the peak current feedback signal; and

a frequency modulating unit, configured to output a turn-on pulse for the control signal according to an output current of the mode judging unit, the output current of the mode controlling unit and the degaussing time signal.

3. The control IC of a switch power supply of claim 2, wherein the mode controlling unit comprises:

a first current source, connected with the pulse width modulating unit and configured to increase a value of a first output current when the error voltage increases; and

a second current source, connected with the frequency modulating unit and configured to decrease a value of a second output current when the error voltage decreases, stop outputting the second output current when the error voltage is equal to a first preset voltage and maintain the value of the second output current when the error voltage is less than a second preset voltage.

4. The control IC of a switch power supply of claim 3, wherein the reference current providing unit is a constant current source.

5.The control IC of a switch power supply of claim 2, wherein the pulse width modulating unit comprises a resistor, a first capacitor and a first comparator, one terminal of the resistor is connected to an output terminal of the first current source, an output terminal of the reference current providing unit, an terminal of the capacitor and an negative terminal of the comparator, the other terminal of the resister is connected to the other terminal of the capacitor and is grounded respectively, a positive terminal of the comparator is connected to the collecting unit.

6. The control IC of a switch power supply of claim 2, wherein the mode judging unit is a third current source and is configured to reduce a value of a third output current to less than a preset reference current value when the error voltage is less than the second preset voltage, and maintain the value of the third output current when the error voltage is equal to or larger than the second preset voltage.

7. The control IC of a switch power supply of claim 2, wherein the frequency modulating unit comprises:

a second capacitor;

a third capacitor;

a second comparator;

a first switch, of which a first terminal is connected to an output terminal of the second current source and a second terminal is connected to a terminal of the second capacitor and a negative terminal of the second comparator, configured to close or open according to the degaussing time signal; and

a second switch, of which a first terminal is connected to an output terminal of the second current source, a second terminal is connected to a second terminal of the first

switch, and a third terminal is connected to a terminal of the third capacitor and a positive terminal of the second comparator, configured to connect the first terminal and the second terminal of the second switch or to connect the first terminal and the third terminal of the second switch according to the degaussing time signal.

8. The control IC of a switch power supply of claim 1, further comprising:

a circuit starting module, configured to output an enable signal when a voltage of the circuit starting module reaches a preset start voltage;

wherein the control module is further configured to output the control signal when receiving the enable signal.

9. The control IC of a switch power supply of claim 1, further comprising a compensating module, configured to compensate the feedback voltage according to the error voltage.

10. A switch power supply, comprising:

a control IC of any of claims 1-9;

an input filter and rectification module, configured to remove an unwanted frequency from an alternating current (AC) voltage and convert the alternating current (AC) voltage to a direct current (DC) voltage;

a switch;

a primary side winding, configured to convert the DC voltage to an electromagnetic signal under a control of the switch;

a power supply module, configured to provide a voltage to the control IC;

a primary side feedback module, configured to divide the voltage of the power supply module and feedback the divided voltage to the control IC;

a primary side collecting module, configured to collect the peak current feedback signal of the switch;

a secondary side winding, configured to convert the electromagnetic signal to an electric signal and generate an output AC voltage;

an output rectification module, configured to convert the output AC voltage to a DC voltage;

a voltage regulating module, configured to store the DC voltage from the output rectification module and provide an output power to maintain the value of the output

voltage when the switch is closed; and

a dummy load module, configured to consume the output AC voltage from the secondary side winding in no-load situation.

11. The switch power supply of claim 10, further comprising:

a first voltage absorbing module, connected between the input filter and rectification module and the primary side winding and configured to absorb a peak voltage caused by a leakage inductance.

12. The switch power supply of claim 10, further comprising:

a second voltage absorbing module, connected between the secondary side winding and the voltage regulating module and configured to absorb a peak voltage generated during a reverse recovery stage of the output rectification module.

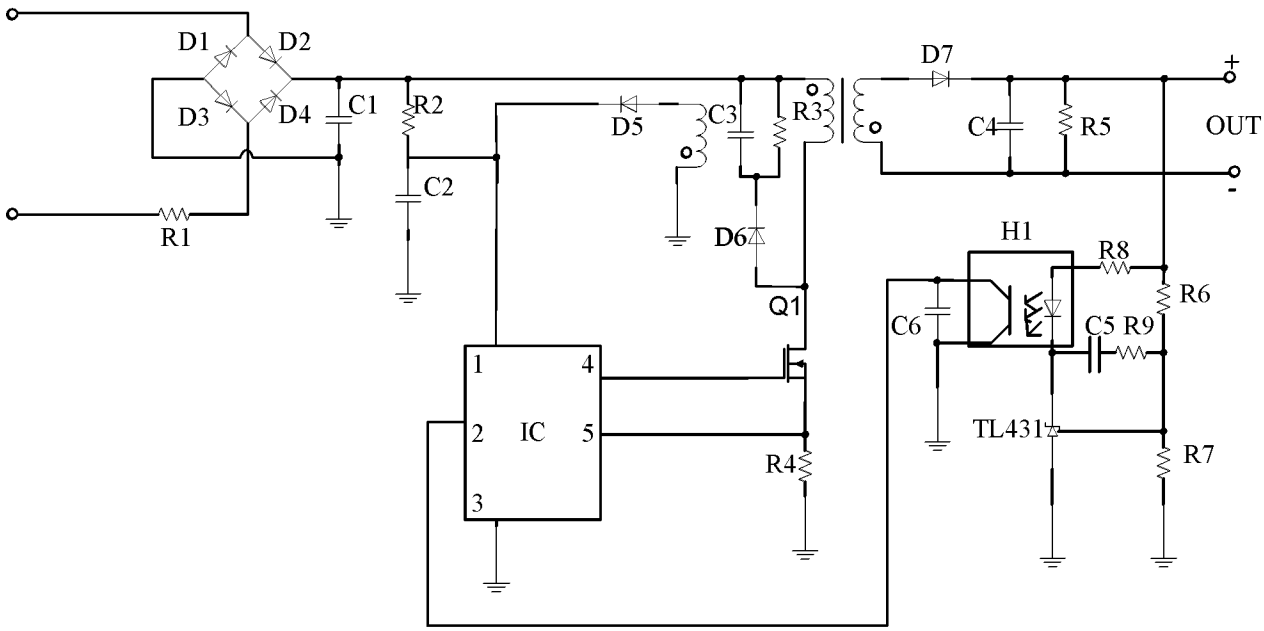
D1
D2
D3
D4
C1
R2
C2
R1
D5
C3
R3
D6
Q1
IC
R4
D7
C4
R5
OUT
H1
R8
R6
C6
C5
R9
TL431
R7

FIG. 1

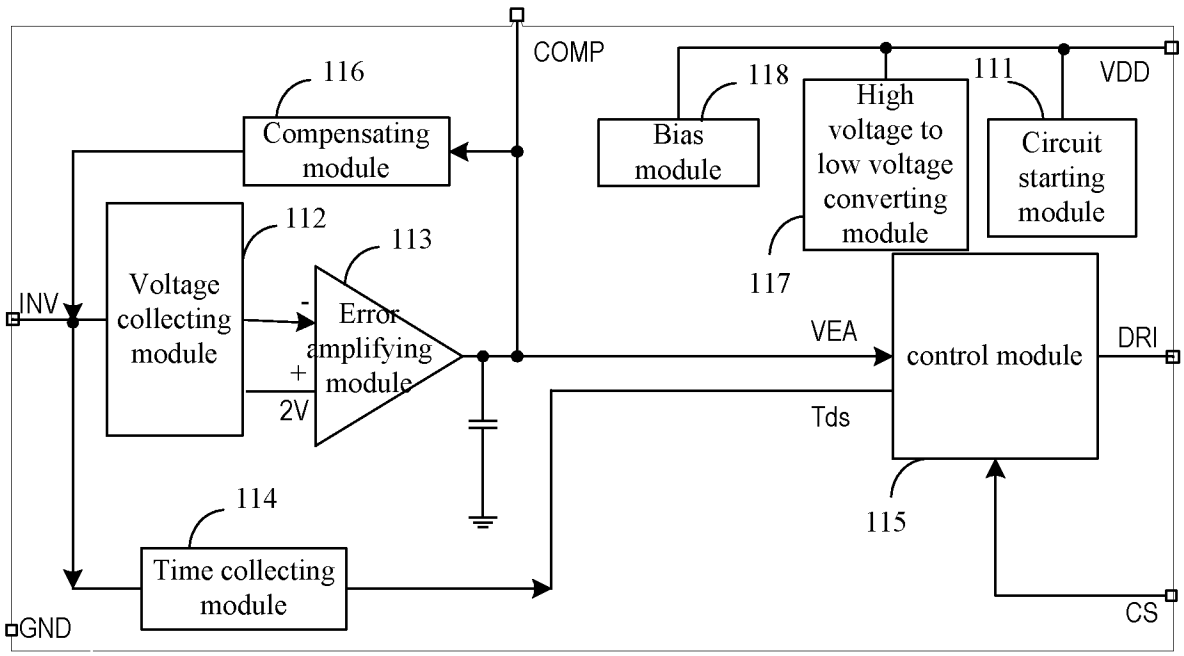
COMP
116
Compensating module
118
Bias module
111
VDD
High voltage to low voltage converting module
Circuit starting module
112
113
INV
Voltage collecting module
Error amplifying module
2V
117
VEA
control module
DRI
Tds
114
Time collecting module
115
GND
CS

FIG. 2

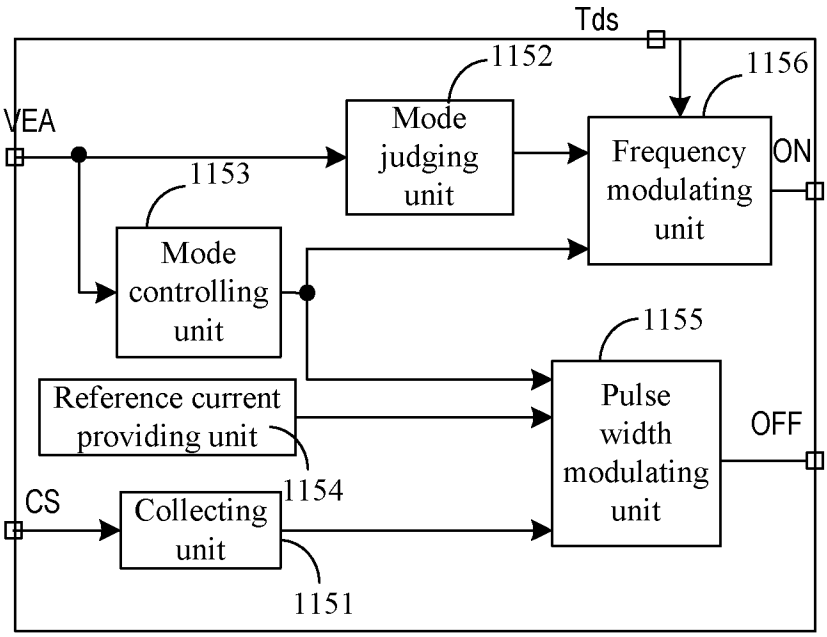
Tds
1152
1156
VEA
Mode judging unit
Frequency modulating unit
ON
1153
Mode controlling unit
1155
Reference current providing unit
Pulse width modulating unit
OFF
1154
CS
Collecting unit
1151

FIG. 3

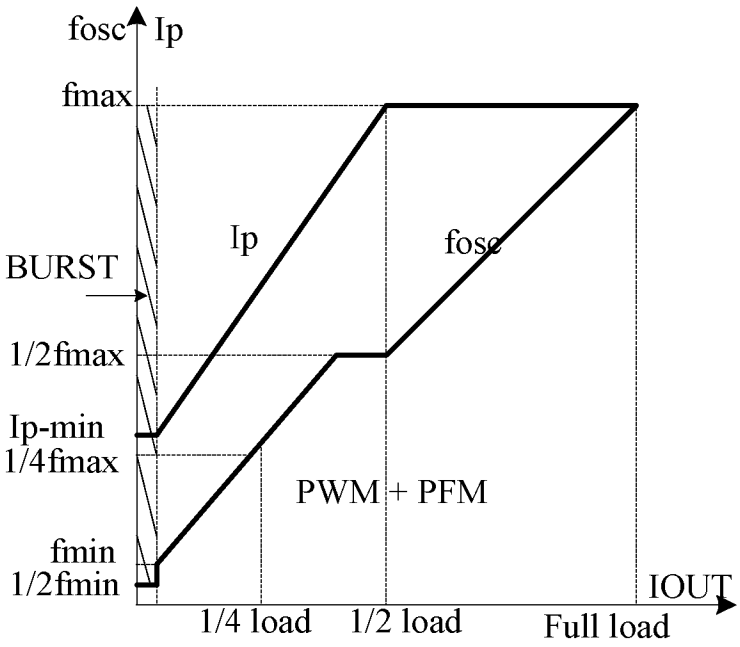
fosc
Ip
fmax
Ip
fosc
BURST
1/2fmax
Ip-min
1/4fmax
PWM + PFM
fmin
1/2fmin
IOUT
1/4 load
1/2 load
Full load

FIG. 4

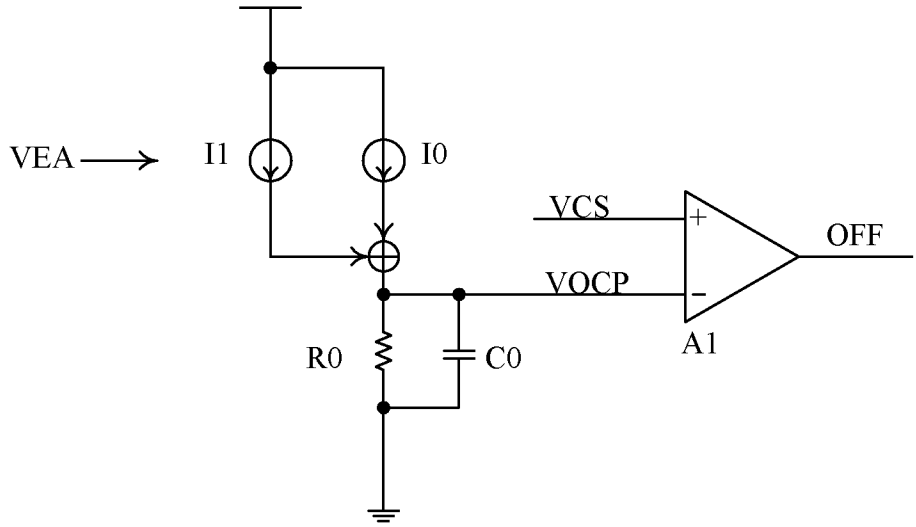
VEA
I1
I0
VCS
OFF
VOCP
A1
R0
C0

FIG. 5

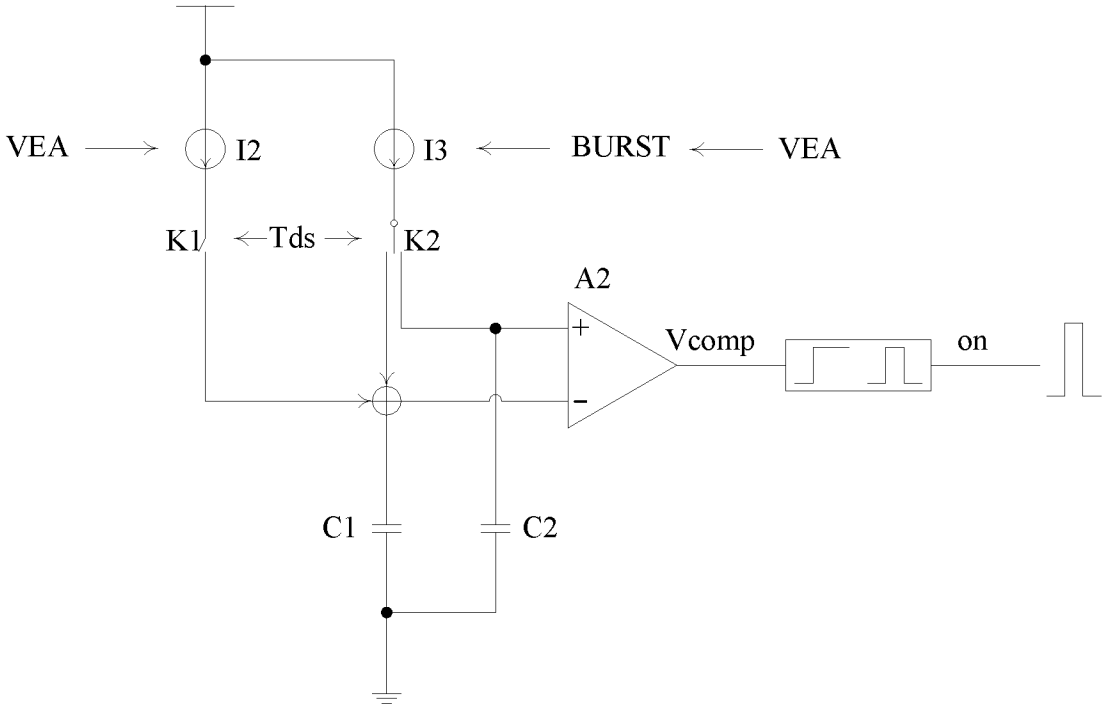
VEA
I2
I3
BURST
VEA
K1
Tds
K2
A2
Vcomp
on
C1
C2

FIG. 6

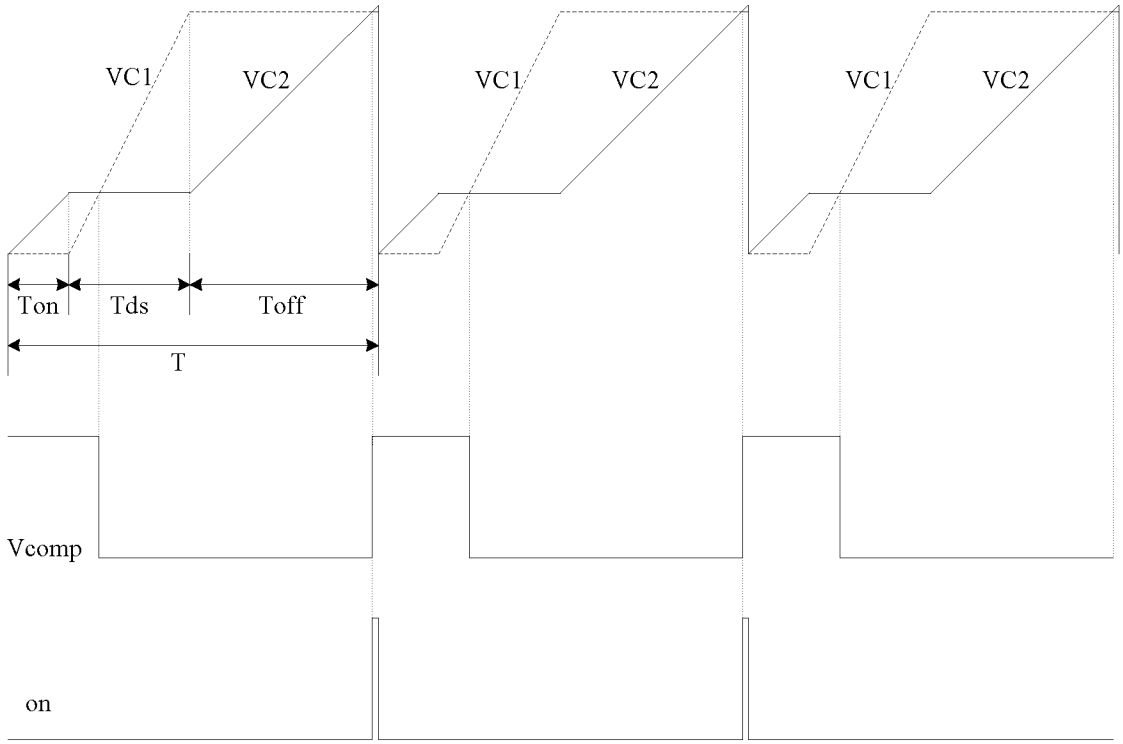
VC1
VC2
VC1
VC2
VC1
VC2
Ton
Tds
Toff
T
Vcomp
on

FIG. 7

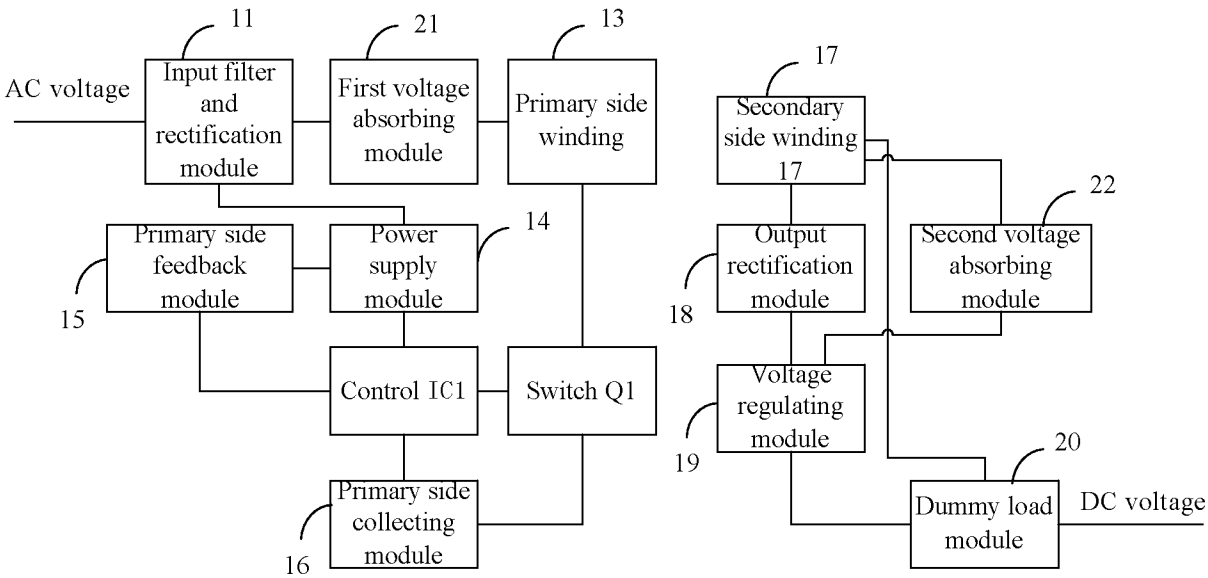
AC voltage
11
Input filter and rectification module
21
First voltage absorbing module
13
Primary side winding
17
Secondary side winding
17
22
Second voltage absorbing module
Primary side feedback module
15
Power supply module
14
Output rectification module
18
Control IC1
Switch Q1
Voltage regulating module
19
20
Primary side collecting module
16
Dummy load module
DC voltage

FIG. 8

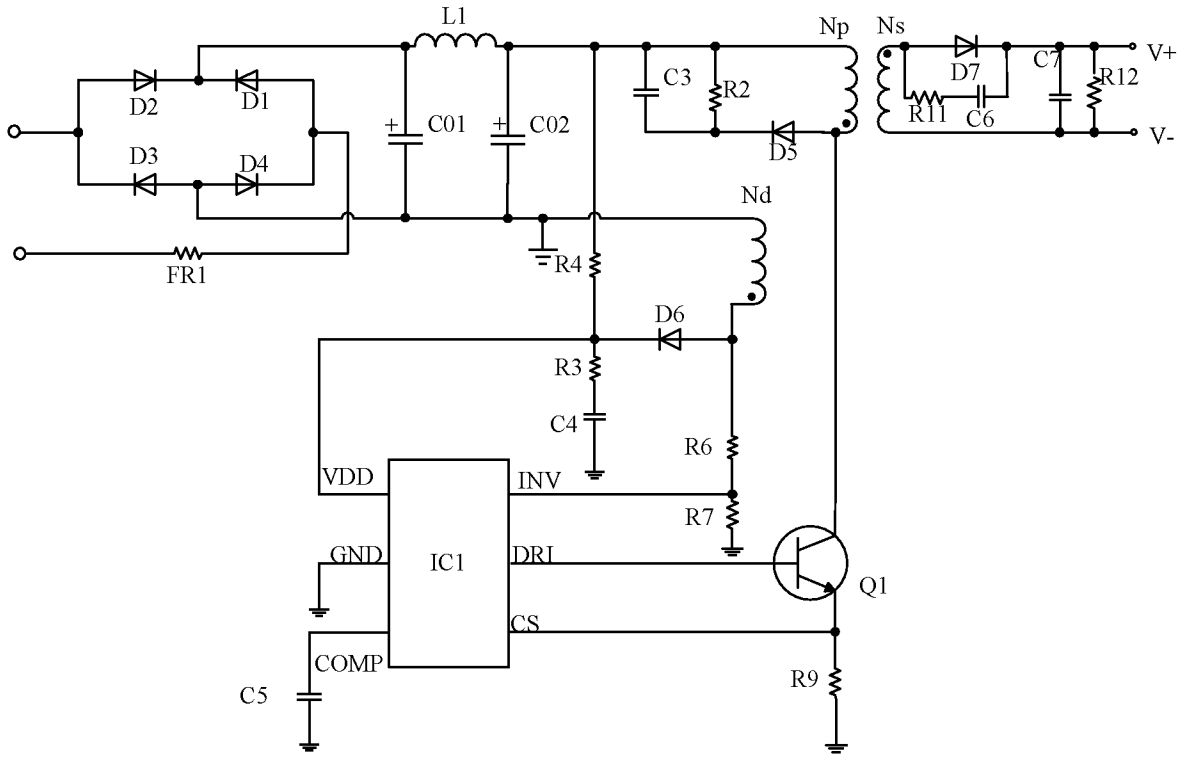
L1
Np
Ns
V+
V-
D2
D1
D3
D4
C01
C02
C3
R2
D5
D7
C7
R12
R11
C6
Nd
FR1
R4
D6
R3
C4
R6
VDD
INV
R7
GND
IC1
DRI
Q1
CS
COMP
C5
R9

FIG. 9

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2012/079294

A. CLASSIFICATION OF SUBJECT MATTER

H02M 7/217 (2006.01) i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC: H02M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

WPI;EPODOC;CNKI;CNPAT: Switch+ power supply, IC, chip, duty cycle, pulse width, PWM, Frequency, PFM, feedback, degauss+ time, current

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	WO 2007/003967 A2 (CAMBRIDGE SEMICONDUCTOR LTD) 11 Jan. 2007 (11.01.2007) paragraph 4 page 9 to paragraph 3 page 10 of the description, figures 1-2	1-12
A	US 2008/0180078 A1 (FUJI ELECTRIC DEVICE TECHNOLOGY CO LTD) 31 Jul. 2008 (31.07.2008) the whole document	1-12
A	CN 101924471 A (SHENZHEN SUNMOON MICROELECTRONICS CO LTD) 22 Dec.2010 (22.12.2010) the whole document	1-12
A	US 2009/0059632 A1 (IWATT INC) 05 Mar.2009 (05.03.2009) the whole document	1-12

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim (S) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&"document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
12 Sep.2012 (12.09.2012)	**25 Oct. 2012 (25.10.2012)**
Name and mailing address of the ISA/CN The State Intellectual Property Office, the P.R.China 6 Xitucheng Rd., Jimen Bridge, Haidian District, Beijing, China 100088 Facsimile No. 86-10-62019451	Authorized officer TAO, Ying Telephone No. (86-10)62411803

Form PCT/ISA /210 (second sheet) (July 2009)

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CN2012/079294

Patent Documents referred in the Report	Publication Date	Patent Family	Publication Date
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		EP 1900087 A2	19.03.2008
		INDELNP 200709924 E	20.06.2008
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		CN 101411048 A	15.04.2009
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		JP 2008187813 A	14.08.2008
CN 101924471 A	22.12.2010	NONE	
US 2009/0059632 A1	05.03.2009	CN 101790708 A	28.07.2010
		WO 2009032685 A1	12.03.2009
		US 7974107 B2	05.07.2011