



(51) International Patent Classification:

H01L 21/311 (2006.01) C23C 16/50 (2006.01)

H01L 21/3065 (2006.01) C23C 16/52 (2006.01)

C23C 16/04 (2006.01) H01J 37/32 (2006.01)

(21) International Application Number:

PCT/US2023/015028

(22) International Filing Date:

10 March 2023 (10.03.2023)

(25) Filing Language:

English

(26) Publication Language:

English

(30) Priority Data:

63/269,328 14 March 2022 (14.03.2022) US

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(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ,

CA, CH, CL, CN, CO, CR, CU, CV, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IQ, IR, IS, IT, JM, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, WS, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, CV, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SC, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, ME, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— with international search report (Art. 21(3))

(54) Title: SIDEWALL PASSIVATION USING ALDEHYDE OR ISOCYANATE CHEMISTRY FOR HIGH ASPECT RATIO ETCH

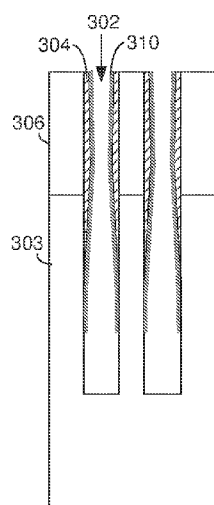


FIG. 3D

(57) Abstract: Various embodiments herein relate to methods, apparatus and systems for forming a recessed feature in dielectric material on a semiconductor substrate. Separate etching and deposition operations are employed in a cyclic manner. Each etching operation partially etches the feature. Each deposition operation forms a protective coating on the sidewalls of the feature to prevent lateral etch of the dielectric material during the etching operations. The protective coating may be deposited using methods that result in formation of the protective coating along the sidewalls. In some cases, the protective coating is deposited using molecular layer deposition techniques. The protective coating may be deposited using particular reactants that result in relatively complete sidewall coating at relatively low temperatures. In some implementations, one or more of the reactants include an aldehyde functional group. In some implementations, one or more of the reactants include an isocyanate functional group.



SIDEWALL PASSIVATION USING ALDEHYDE OR ISOCYANATE CHEMISTRY FOR HIGH ASPECT RATIO ETCH

INCORPORATION BY REFERENCE

5 [0001] A PCT Request Form is filed concurrently with this specification as part of the present application. Each application that the present application claims benefit of or priority to as identified in the concurrently filed PCT Request Form is incorporated by reference herein in its entirety and for all purposes.

BACKGROUND

10 [0002] One process frequently employed during fabrication of semiconductor devices is formation of an etched cylinder in dielectric material. Example contexts where such a process may occur include, but are not limited to, memory applications such as DRAM and 3D NAND structures. As the semiconductor industry advances and device dimensions become smaller, such cylinders become increasingly harder to etch in a uniform manner, especially for high aspect ratio
15 cylinders having narrow widths and/or deep depths.

SUMMARY

[0003] Certain embodiments herein relate to methods and apparatus for forming an etched feature in a stack that includes dielectric material on a semiconductor substrate. The disclosed embodiments may utilize certain techniques to deposit a passivating material on sidewalls of the
20 etched feature, thereby allowing etch to occur at high aspect ratios. In some embodiments, particular reactants or classes of reactants may be used to deposit the passivating material. In some instances, one or more reactants may comprise an aldehyde functional group. In other instances, one or more reactants may comprise an isocyanate functional group.

[0004] In one aspect of the disclosed embodiments, a method of forming an etched feature in
25 a stack including a dielectric material on a semiconductor substrate is provided. The method includes: (a) generating a first plasma including an etching reactant, exposing the substrate to the first plasma, and partially etching the feature in the dielectric material; (b) after (a), depositing a protective film on sidewalls of the feature by (i) exposing the substrate to a first reactant and

allowing the first reactant to adsorb onto the substrate, where the first reactant includes an aldehyde functional group, (ii) exposing the substrate to a second reactant, where the first and second reactants react with one another to form the protective film, and (iii) repeating (i) and (ii) in a cyclic manner until the protective film reaches a target thickness, where the protective film is an organic polymeric film; and (c) repeating (a)-(b) until the feature is etched to a final depth, where the protective film deposited in (b) substantially prevents lateral etch of the feature during (a), and where the feature has an aspect ratio of about 5 or greater at its final depth.

[0005] In some implementations, the first reactant includes a dialdehyde or trialdehyde. In some implementations, the first reactant includes succindialdehyde ($C_4H_6O_2$), glutaraldehyde ($C_5H_8O_2$), adipaldehyde ($C_6H_{10}O_2$), terephth-aldehyde ($C_8H_6O_2$), 1,4-benzenedicarboxaldehyde ($C_6H_4(CHO)_2$), ortho-phthalaldehyde ($C_8H_6O_2$), 1,2 benzenedicarboxaldehyde ($C_6H_4(CHO)_2$), and 2-methylglutaraldehyde ($C_6H_{10}O_2$). In some implementations, the second reactant comprises at least one of the following: diamine, a diol, a thiol, and a trifunctional compound. In some cases, the second reactant comprises diamine. In some cases, the second reactant includes at least one of the following: 1,2-ethanediamine, 1,3-propanediamine, 1,4-butanediamine, ethylenediamine, m-xylylenediamine, isophoronediamine, 1,3-cyclohexanebis(methylamine), 1,4-bis(aminomethyl)cyclohexane, 4,4'-methylenebis(2-methylcyclohexylamine), 4,4'-methylenebis(cyclohexylamine), m-phenylenediamine, p-phenylenediamine, 4-aminobenzylamine, 3-aminobenzylamine, 4-(2-aminoethyl)aniline, p-xylylenediamine, m-xylylenediamine, ethylene glycol, 1,3-propanediol, 1,4-butanediol, 1,2-ethanedithiol, 1,3-propanedithiol, 1,4-butanedithiol, ($\pm$)-3-amino-1,2-propanediol, glycerol, bis(hexamethylene)tri-amine, melamine, diethylenetriamine, ($\pm$)-1,2,4-butanetriol, cyanuric chloride, and trimethylaluminum.

[0006] In some implementations, depositing the protective film in (b) is accomplished without exposing the substrate to plasma energy. In some implementations, the protective coating includes a polyazomethine or a polythioacetal. In some implementations, etching the feature in the stack in (a) is performed in a reaction chamber, where depositing the protective film on the sidewalls of the feature in (b) is performed in the same reaction chamber. In some implementations, the etching reactant includes one or more fluorocarbons or hydrofluorocarbons. In some implementations, depositing the protective film in (b) occurs in a reaction chamber, where depositing the protective

film in (b) further includes purging the reaction chamber at least once during each iteration of operation (b). In some implementations, the stack includes alternating layers of (i) a silicon oxide material, and (ii) a silicon nitride material or polysilicon material. In some implementations, the protective film is deposited along substantially an entire depth of the feature. In some
 5 implementations, the feature has an aspect ratio of about 20 or greater at its final depth.

[0007] In another aspect of the disclosed embodiments, a method of forming an etched feature in a stack including a dielectric material on a semiconductor substrate is provided. The method includes: (a) generating a first plasma including an etching reactant, exposing the substrate to the first plasma, and partially etching the feature in the dielectric material; (b) after (a), depositing a
 10 protective film on sidewalls of the feature by (i) exposing the substrate to a first reactant and allowing the first reactant to adsorb onto the substrate, where the first reactant includes an isocyanate functional group, (ii) exposing the substrate to a second reactant, where the first and second reactants react with one another to form the protective film, and (iii) repeating (i) and (ii) in a cyclic manner until the protective film reaches a target thickness, where the protective film is
 15 an organic polymeric film; and (c) repeating (a)-(b) until the feature is etched to a final depth, where the protective film deposited in (b) substantially prevents lateral etch of the feature during (a), and where the feature has an aspect ratio of about 5 or greater at its final depth.

[0008] In some implementations, the first reactant includes diisocyanate. In some cases, the diisocyanate includes at least one of the following: tolylene-2,4-diisocyanate, 1,3-
 20 bis(isocyanatomethyl)cyclohexane, hexamethylene diisocyanate, m-xylylene diisocyanate, 1,3-bis(1-isocyanato-1-methylethyl)benzene, isophorone diisocyanate, diphenylmethane 4,4'-diisocyanate, 4,4'-methylenebis(cyclohexyl isocyanate), tolylene-2,6-diisocyanate, 1,4-phenylene diisocyanate, 1,3-phenylene diisocyanate, and 3,3'-dimethyl-4,4'-biphenylene diisocyanate.

[0009] In some implementations, the second reactant comprises at least one of the following:
 25 diamine, a diol, a thiol, and a trifunctional compound. In some cases, the second reactant comprises diamine. In some cases, the second reactant includes at least one of the following: 1,2-ethanediamine, 1,3-propanediamine, 1,4-butanediamine, ethylenediamine, m-xylylenediamine, isophoronediamine, 1,3-cyclohexanebis(methylamine), 1,4-bis(aminomethyl)cyclohexane, 4,4'-methylenebis(2-methylcyclohexylamine), 4,4'-methylenebis(cyclohexylamine), m-

phenylenediamine, p-phenylenediamine, 4-aminobenzylamine, 3-aminobenzylamine, 4-(2-aminoethyl)aniline, p-xylylenediamine, m-xylylenediamine, ethylene glycol, 1,3-propanediol, 1,4-butanediol, 1,2-ethanedithiol, 1,3-propanedithiol, 1,4-butanedithiol, ($\pm$)-3-amino-1,2-propanediol, glycerol, bis(hexamethylene)triamine, melamine, diethylenetriamine, ($\pm$)-1,2,4-butanetriol, cyanuric chloride, and trimethylaluminum.

[0010] In some implementations, depositing the protective film in (b) is accomplished without exposing the substrate to plasma energy. In some implementations, the protective coating includes a polyurethane or a polyurea. In some implementations, etching the feature in the stack in (a) is performed in a reaction chamber, where depositing the protective film on the sidewalls of the feature in (b) is performed in the same reaction chamber. In some implementations, the etching reactant includes one or more fluorocarbons or hydrofluorocarbons. In some implementations, depositing the protective film in (b) occurs in a reaction chamber, where depositing the protective film in (b) further includes purging the reaction chamber at least once during each iteration of operation (b). In some implementations, the stack includes alternating layers of (i) a silicon oxide material, and (ii) a silicon nitride material or polysilicon material. In some implementations, the protective film is deposited along substantially an entire depth of the feature. In some implementations, the feature has an aspect ratio of about 20 or greater at its final depth.

[0011] These and other features will be described below with reference to the associated drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] FIG. 1 illustrates an etched cylinder having an undesirable bow due to over-etching of the sidewalls.

[0013] FIG. 2A presents a flowchart for a method of forming an etched feature on a semiconductor substrate according to various disclosed embodiments.

[0014] FIG. 2B presents a flowchart for a method of depositing a protective film on sidewalls of a partially etched feature according to certain embodiments.

[0015] FIGS. 2C and 2D illustrate particular deposition reactions for forming the protective film where the reactants used include glutaraldehyde and ethylenediamine.

[0016] FIGS. 3A–3D depict etched cylinders in a semiconductor substrate as the cylinders are cyclically etched and coated with a protective sidewall coating according to various embodiments.

5 [0017] FIGS. 4A–4C illustrate a reaction chamber that may be used to perform the etching processes described herein according to certain embodiments.

[0018] FIG. 5 depicts a reaction chamber that may be used to perform the deposition processes described herein according to certain embodiments.

10 [0019] FIG. 6 shows a multi-station apparatus that may be used to perform the deposition processes in certain implementations.

[0020] FIG. 7 presents a cluster tool that may be used to practice both deposition and etching according to certain embodiments.

DETAILED DESCRIPTION

15 [0021] In this application, the terms “semiconductor wafer,” “wafer,” “substrate,” “wafer substrate,” and “partially fabricated integrated circuit” are used interchangeably. One of ordinary skill in the art would understand that the term “partially fabricated integrated circuit” can refer to a silicon wafer during any of many stages of integrated circuit fabrication thereon. A wafer or substrate used in the semiconductor device industry typically has a diameter of 200 mm, or 300 mm, or 450 mm. The following detailed description assumes the invention is implemented on a
20 wafer. However, the invention is not so limited. The work piece may be of various shapes, sizes, and materials. In addition to semiconductor wafers, other work pieces that may take advantage of this invention include various articles such as printed circuit boards, magnetic recording media, magnetic recording sensors, mirrors, optical elements, micro-mechanical devices and the like.

25 [0022] In the following description, numerous specific details are set forth in order to provide a thorough understanding of the presented embodiments. The disclosed embodiments may be practiced without some or all of these specific details. In other instances, well-known process operations have not been described in detail to not unnecessarily obscure the disclosed

embodiments. While the disclosed embodiments will be described in conjunction with the specific embodiments, it will be understood that it is not intended to limit the disclosed embodiments.

I. Technology for Etching High Aspect Ratio Features in a Dielectric Material

[0023] Fabrication of certain semiconductor devices involves etching features into a dielectric material or materials. The dielectric material may be a single layer of material or a stack of materials. In some cases a stack includes alternating layers of dielectric material (e.g., silicon nitride and silicon oxide). One example etched feature is a cylinder, which may have a high aspect ratio. As the aspect ratio of such features continues to increase, it is increasingly challenging to etch the features into dielectric materials. One problem that arises during etching of high aspect ratio features is a non-uniform etching profile. In other words, the features do not etch in a straight downward direction. Instead, the sidewalls of the features are often bowed such that a middle portion of the etched feature is wider (i.e., further etched) than a top and/or bottom portion of the feature. This over-etching near the middle portion of the features can result in compromised structural and/or electronic integrity of the remaining material. The portion of the feature that bows outwards may occupy a relatively small portion of the total feature depth, or a relatively larger portion. The portion of the feature that bows outward is where the critical dimension (CD) of the feature is at its maximum. The critical dimension corresponds to the diameter of the feature at a given spot. It is generally desirable for the maximum CD of the feature to be about the same as the CD elsewhere in the feature, for example at or near the bottom of the feature.

[0024] Without being bound by any theory or mechanism of action, it is believed that the over-etching at the middle portion of the cylinder or other feature occurs at least partially because the sidewalls of the cylinder are insufficiently protected from etching. Conventional etch chemistry utilizes fluorocarbon etchants to form the cylinders in the dielectric material. The fluorocarbon etchants are excited by plasma exposure, which results in the formation of various fluorocarbon fragments including, for example, CF, CF₂, and CF₃. Reactive fluorocarbon fragments etch away the dielectric material at the bottom of a feature (e.g., cylinder) with the assistance of ions. Other fluorocarbon fragments are deposited on the sidewalls of the cylinder being etched, thereby forming a protective polymeric sidewall coating. This protective sidewall coating promotes preferential etching at the bottom of the feature as opposed to the sidewalls of the feature. Without

this sidewall protection, the feature begins to assume a non-uniform profile, with a wider etch/cylinder width where the sidewall protection is inadequate.

[0025] Sidewall protection is especially difficult to achieve in high aspect ratio features. One reason for this difficulty is that existing fluorocarbon-based processes cannot form the protective polymeric sidewall coating deep in the cylinder being etched. FIG. 1 presents a figure of a cylinder 102 being etched in a dielectric material 103 coated with a patterned mask layer 106. While the following discussion sometimes refers to cylinders, the concepts apply to other feature shapes such as rectangles and other polygons. A protective polymeric sidewall coating 104 is concentrated near the top portion of the cylinder 102. C_xF_y chemistry provides both the etch reactant(s) for etching the cylinder vertically, as well as the reactant(s) that form the protective polymeric sidewall coating 104. Because the protective polymeric sidewall coating 104 does not extend deep into the cylinder (i.e., there is insufficient deposition on the sidewall), the middle portion of the cylinder 102 becomes wider than the top portion of the cylinder 102. The wider middle portion of the cylinder 102 is referred to as the bow 105. The bow can be numerically described in terms of a comparison between the critical dimension of the feature at the bow region (the relatively wider region) and the critical dimension of the feature below the bow region. The bow may be numerically reported in terms of distance (e.g., the critical dimension at the widest part of the feature minus the critical dimension at the narrowest part of the feature below the bow) or in terms of a ratio/percent (the critical dimension at the widest part of the feature divided by the critical dimension at the narrowest part of the feature below the bow). This bow 105, and the related non-uniform etch profile, is undesirable. Because of the high ion energies often used in this type of etching process, bows are often created when etching cylinders of high aspect ratios. In some applications, bows are created even at aspect ratios as low as about 5. As such, conventional fluorocarbon etch chemistry is typically limited to forming relatively low aspect ratio cylinders in dielectric materials. Some modern applications require cylinders having higher aspect ratios than those that can be achieved with conventional etch chemistry.

II. Context and Applications

[0026] In various embodiments herein, features are etched in a substrate (typically a semiconductor wafer) having dielectric material on the surface. The etching processes are

generally plasma-based etching processes. The overall feature formation process may occur in stages: one stage directed at etching the dielectric material and another stage directed at forming a protective sidewall coating without substantially etching the dielectric material. The protective sidewall coating passivates the sidewalls and prevents the feature from being over-etched (i.e., the sidewall coating prevents lateral etch of the feature). These two stages can be repeated until the feature is etched to its final depth. By cycling these two stages, the diameter of the feature can be controlled over the entire depth of the feature, thereby forming features having more uniform diameters/improved profiles.

[0027] “Features” as used herein may refer to non-planar structures of a substrate, typically a surface being modified in a semiconductor device fabrication operation. Examples of features, which may also be referred to as “negative features” or “recessed features,” include trenches, holes, vias, gaps, recessed regions, and the like. These terms may be used interchangeably in the present disclosure. One example of a feature is a recess in the surface of the substrate. A feature typically has an aspect ratio (depth to lateral dimension). A feature may be characterized by one or more of narrow and/or re-entrant openings, constrictions within the feature, and high aspect ratios. Features can have many different shapes including, but not limited to, cylinders, rectangles, squares, other polygonal recesses, trenches, etc.

[0028] Aspect ratios are a comparison of the depth of a feature to the critical dimension of the feature (often its width/diameter). For example, a cylinder having a depth of 2 μm and a width of 50 nm has an aspect ratio of 40:1, often stated more simply as 40. Since the feature may have a non-uniform critical dimension over the depth of the feature, the aspect ratio can vary depending on where it is measured. For instance, sometimes an etched cylinder may have a middle portion that is wider than the top and bottom portions. This wider middle section may be referred to as the bow, as noted above. An aspect ratio measured based on the critical dimension at the top of the cylinder (i.e., the neck) would be higher than an aspect ratio measured based on the critical dimension at the wider middle/bow of the cylinder. As used herein, aspect ratios are measured based on the critical dimension proximate the opening of the feature, unless otherwise stated.

[0029] The features formed through the disclosed methods may be high aspect ratio features. In some applications, a high aspect ratio feature is one having an aspect ratio of at least about 5, at

least about 10, at least about 20, at least about 30, at least about 40, at least about 50, at least about 60, at least about 80, or at least about 100. The critical dimension of the features formed through the disclosed methods may be about 200 nm or less, for example about 100 nm or less, about 50 nm or less, or about 20 nm or less.

5 [0030] The material into which the feature is etched may be a dielectric material in various cases. Example materials include, but are not limited to, silicon oxides, silicon nitrides, silicon carbides, oxynitrides, oxycarbides, carbo-nitrides, doped versions of these materials (e.g., doped with boron, phosphorus, etc.), and laminates from any combinations of these materials. Particular
10 example materials include stoichiometric and non-stoichiometric formulations of SiO₂, SiN, SiON, SiOC, SiCN, etc. The material or materials being etched may also include other elements, for example hydrogen in various cases. In some embodiments, a nitride and/or oxide material being etched has a composition that includes hydrogen. As used herein, it is understood that silicon oxide materials, silicon nitride materials, etc. include both stoichiometric and non-stoichiometric versions of such materials, and that such materials may have other elements included, as described
15 above.

[0031] One application for the disclosed methods is in the context of forming a DRAM device. In this case, the feature may be etched primarily in silicon oxide. The substrate may also include one, two, or more layers of silicon nitride, for instance. In one example, a substrate includes a silicon oxide layer sandwiched between two silicon nitride layers, with the silicon oxide layer
20 being between about 800 nm and about 1200 nm thick and one or more of the silicon nitride layers being between about 300 nm and about 400 nm thick. The etched feature may be a cylinder having a final depth between about 1 μm and about 3 μm, for example between about 1.5 μm and about 2 μm. The cylinder may have a width between about 20 nm and about 50 nm, for example between about 25 nm and about 30 nm. After the cylinder is etched, a capacitor memory cell can be formed
25 therein.

[0032] Another application for the disclosed methods is in the context of forming a vertical NAND (VNAND, also referred to as 3D NAND) device. In this case, the material into which the feature is etched may have a repeating layered structure. For instance, the material may include alternating layers of oxide (e.g., SiO₂) and nitride (e.g., SiN), or alternating layers of oxide (e.g.,

SiO₂) and polysilicon. The alternating layers form pairs of materials. In some cases, the number of pairs may be at least about 20, at least about 30, at least about 40, at least about 60, or at least about 70. The oxide layers may have a thickness between about 20 nm and about 50 nm, for example between about 30 nm and about 40 nm. The nitride or polysilicon layers may have a thickness between about 20 nm and about 50 nm, for example between about 30 nm and about 40 nm. The feature etched into the alternating layer may have a depth between about 2 μm and about 6 μm, for example between about 3 μm and about 5 μm. The feature may have a width between about 50 nm and about 150 nm, for example between about 50 nm and about 100 nm.

III. Etching/Deposition Processes

[0033] FIG. 2A presents a flowchart for a method of forming an etched feature in a semiconductor substrate. The operations shown in FIG. 2A are described in relation to FIGS. 3A–3D, which show a partially fabricated semiconductor substrate as the feature is etched. At operation 201, a feature 302 is etched to a first depth in a substrate having dielectric material 303 and a patterned mask layer 306. This first depth is only a fraction of the final desired depth of the feature. The chemistry used to etch the feature may be a fluorocarbon-based chemistry (C_xF_y) or hydrofluorocarbon-based chemistry (H_xF_yC_z). Other etch chemistries may be used. This etching operation 201 may result in formation of a first sidewall coating 304. The first sidewall coating 304 may be a polymeric sidewall coating, as described with relation to FIG. 1. The first sidewall coating 304 extends toward the first depth, though in many cases the first sidewall coating 304 does not actually reach the bottom of the feature 302.

[0034] The first sidewall coating 304 indirectly forms from the C_xF_y etching chemistry as certain fluorocarbon species/fragments deposit on the sidewalls of the feature (i.e., certain fluorocarbon species are precursors for the first sidewall coating 304). One reason that the first sidewall coating 304 does not reach the bottom of the feature 302 may relate to the sticking coefficient of the precursors that form the coating. In particular, it is believed that for certain etchants the sticking coefficient of these first sidewall coating precursors is too high, which causes the substantial majority of the precursor molecules to attach to the sidewalls soon after entering the feature. As such, few sidewall coating precursor molecules are able to penetrate deep into the feature where sidewall protection is beneficial. The first sidewall coating 304 therefore provides

only partial protection against over-etching of the sidewalls of the feature 302. In some implementations, the etch conditions provide little, if any, sidewall protection.

[0035] Next, at operation 203 the etching process is stopped. After the etching is stopped, a second sidewall coating 310 is deposited in operation 205. In some cases, the second sidewall coating 310 may be effectively the first sidewall coating. This deposition may occur through various reaction mechanisms including, but not limited to, chemical vapor deposition (CVD) methods, atomic layer deposition (ALD) methods (either of which may or may not be plasma-assisted), and molecular layer deposition (MLD) methods. MLD methods may deposit thin films of organic polymer using ALD-like cycles involving two half-reactions. In some cases MLD methods may be driven in a less adsorption-limited manner than conventional ALD methods. For example, certain MLD methods may utilize under- or over-saturation of reactants. ALD and MLD methods are particularly well suited for forming conformal films that line the sidewalls of the features in certain embodiments. For instance, ALD and MLD methods are useful for delivering reactants deep into features due to the adsorption-related nature of such methods. While the embodiments herein are not limited to methods in which the second sidewall coating 310 is deposited through cyclic layer-by-layer deposition methods such as ALD and MLD, the method chosen to deposit the second sidewall coating 310 should allow for the protective layer to be formed deep in the etched feature 302. CVD and other deposition processes may be suitable in various implementations.

[0036] FIG. 2B illustrates a flowchart for a method 250 of depositing an organic polymeric second protective sidewall coating 310 through an MLD process. As noted, ALD and CVD methods may also be used, as described further below. Method 250 begins with operation 251, where a first reactant is flowed into the reaction chamber and adsorbs onto the substrate surface. The reactant may penetrate deep into a partially etched feature and adsorb onto the sidewalls of the feature. In some embodiments the first reactant is a dialdehyde or trialdehyde. In a particular embodiment the first reactant may be glutaraldehyde ($C_5H_8O_2$). The first reactant forms an adsorbed layer, as shown by adsorbed precursor layer 312 in FIG. 3B.

[0037] Next, at operation 253, the reaction chamber may be optionally purged to remove excess first reactant from the reaction chamber. Next, at operation 255, the second reactant is

delivered to the reaction chamber. In some embodiments the second reactant may be a diamine, a diol, a thiol, or a trifunctional compound. In a particular embodiment the second reactant may be ethylenediamine ($C_2H_8N_2$). The second reactant reacts with the first reactant to form a protective film on the substrate. The protective film formed may be the second sidewall coating 310 as shown in FIGS. 3C and 3D. The protective film may form through a thermal reaction, without reliance on any plasma.

[0038] Next, at operation 257, the reaction chamber may be optionally purged. The purges in operations 253 and 257 may occur by sweeping the reaction chamber with a non-reactive gas, by evacuating the reaction chamber, or some combination thereof. The purpose of the purges is to remove any non-adsorbed reactants and byproducts from the reaction chamber. While the purge operations 253 and 257 are both optional, they may help prevent unwanted gas phase reactions, and may result in improved deposition results.

[0039] Next, at operation 259, it is determined whether the protective film is sufficiently thick. Such a determination may be made based on the thickness deposited per cycle and the number of cycles performed. In various embodiments, each cycle deposits between about 0.1 nm and about 1 nm of film, with the thickness dependent upon the length of time that the reactants are flowed into the reaction chamber and the resulting level of reactant saturation. If the film is not yet sufficiently thick, the method 250 repeats from operation 251 to build additional film thickness by depositing additional layers. Otherwise, the method 250 is complete. In subsequent iterations, operation 251 may involve both adsorbing additional first reactant onto the substrate, and reaction of the first reactant with the second reactant, which may be present due to a previous iteration of operation 255. In other words, after the first cycle, both operations 251 and 255 may involve a reaction between the first and second reactants. After the protective film is sufficiently thick, the substrate may be subject to another etching process as shown in operation 211 of FIG. 2A.

[0040] The deposition method 250 may be used to form a layer of organic polymeric film in a number of cases. FIG. 2C illustrates steps 251–257 of FIG. 2B in a particular context where the first reactant is glutaraldehyde and the second reactant is ethylenediamine. In operation 251, a first reactant of glutaraldehyde is flowed in vapor phase into the reaction chamber and adsorbs onto the substrate 260. The portion of the substrate 260 shown in FIG. 2C is a sidewall of a

partially etched cylinder. In operation 253, the reaction chamber is optionally purged, for example by flowing a non-reactive purge gas through the reaction chamber. In operation 255, a second reactant of ethylenediamine is flowed in vapor phase into the reaction chamber. The first and second reactants react to form a layer of an organic polymeric film on the exposed surfaces of the substrate 260, for example along the sidewalls of partially etched features. Next, at operation 257, the reaction chamber may be optionally purged, for example by flowing another purge gas into the reaction chamber. These operations can be repeated until the organic polymeric film is grown to a desired thickness.

[0041] FIG. 2D further illustrates the reaction that occurs in operation 255 where the first reactant is glutaraldehyde and the second reactant is ethylenediamine. Without being limited by any theory, the reactions shown in FIG. 2D may be result in two possible reaction products. One reaction product may be shown in the first row and is a partial reaction product. Another reaction product may be shown in the second row and is a full reaction product resulting in an imine product.

[0042] These reactants may be particularly useful in applications where it is desired to form the protective film at a relatively low temperature. These reactants have been shown to effectively and efficiently react with one another even at temperatures much lower than are typically used in similar MLD and ALD reactions. Many thermal ALD reactions (which do not use plasma) are performed at much higher temperatures, for example at least about 200°C. Low temperature deposition is particularly useful in certain contexts. In some cases, the use of a low temperature non-plasma deposition may help enable the deposition to occur in the same reaction chamber as the etching reaction, such that transfer between two different reaction chambers is not needed. MLD processes are further discussed in U.S. Patent Application No. 14/446,427, filed July 30, 2014, and titled "METHOD OF CONDITIONING VACUUM CHAMBER OF SEMICONDUCTOR SUBSTRATE PROCESSING APPARATUS," which is herein incorporated by reference in its entirety and for all purposes.

[0043] The disclosed MLD method 250 of FIG. 2B is well suited for forming a conformal film that coats the entire sidewalls of the feature. One reason that MLD methods may be particularly useful is that they can achieve a very high degree of conformality because the reaction is driven

by thermal energy rather than plasma energy. When plasmas are used to generate one or more of the reactants in a plasma assisted ALD approach, the resulting reactants may be radical species with high surface reactivity. This approach therefore may create reactants with a limited ability to penetrate into high aspect ratio features and therefore results in poorer conformality and/or higher dosage requirements compared to thermal methods. Further, because plasmas used in semiconductor fabrication are not uniform within a reaction chamber, plasma non-uniformities can lead to non-uniform deposition results across the substrate. To contrast, it is easier to deliver uniform thermal energy to a substrate, for example by providing a uniform heat source on a substrate support. Plasma energy is often used to drive reactions at relatively low temperatures (e.g., less than about 200°C). Often, a semiconductor device has a particular thermal budget during fabrication, and care may be taken to process the substrate at lower temperatures to conserve the thermal budget and therefore avoid damaging the device. However, the use of plasma can also have a deleterious effect on conformality and/or uniformity, as mentioned. In various embodiments herein, particular reactants are used to deposit a protective layer at a relatively low temperature, thereby capturing both the uniformity benefits related to thermal processing and the low temperature/thermal budget benefits often associated with plasma processing. One example of a pair of reactants that may be used at a relatively low temperature to deposit a protective layer include glutaraldehyde and ethylenediamine, as discussed in relation to FIGS. 2C and 2D.

[0044] Returning to FIG. 2A, the method continues at operation 207 where the deposition process is stopped. The method then repeats the operations of partially etching a feature in the substrate (operation 211, analogous to operation 201), stopping the etch (operation 213, analogous to operation 203), depositing protective coating on sidewalls of the partially etched features (operation 215, analogous to operation 205), and stopping the deposition (operation 217, analogous to operation 207). Next, at operation 219, it is determined whether the feature is fully etched. If the feature is not fully etched, the method repeats from operation 211 with additional etching and deposition of protective coatings. The etching operation 211 may alter the second sidewall coating 310 to form a film that is even more etch resistant than the film deposited in operations 205 and 215. In one example, the deposition operation 205 is performed through the method 250, to thereby form an organic polymer film layer that includes carbon, nitrogen, oxygen, and hydrogen. Once the feature is fully etched, the method is complete.

[0045] In various embodiments, the etching operation 201 and the protective sidewall coating deposition operation 205 are cyclically repeated a number of times. For instance, these operations may each occur at least twice (as shown in FIG. 2A), for example at least about three times, or at least about 5 times. In some cases, the number of cycles (each cycle including etching operation 201 and protective sidewall coating deposition operation 205, with etching operation 211 and deposition operation 215 counting as a second cycle) is between about 2–10, for example between about 2–5. Each time the etching operation occurs, the etch depth increases. The distance etched may be uniform between cycles, or it may be non-uniform. In certain embodiments, the distance etched in each cycle decreases as additional etches are performed (i.e., later performed etching operations may etch less extensively than earlier performed etching operations). The thickness of the second sidewall coating 310 deposited in each deposition operation 205 may be uniform between cycles, or the thickness of such coatings may vary. Example thicknesses for the second sidewall coating 310 during each cycle may range between about 1 nm and about 10 nm, for example between about 3 nm and about 5 nm. Further, the type of coating that is formed may be uniform between the cycles, or it may vary.

[0046] The etching operation 201 and the deposition operation 205 may occur in the same reaction chamber or in different reaction chambers. In one example, the etching operation 201 occurs in a first reaction chamber and the deposition operation 205 occurs in a second reaction chamber, with the first and second reaction chambers together forming a multi-chamber processing apparatus such as a cluster tool. Load locks and other appropriate vacuum seals may be provided for transferring the substrate between the relevant chambers in certain cases. The substrate may be transferred by a robot arm or other mechanical structure. A reaction chamber used for etching (and in some cases deposition) may be a Flex™ reaction chamber, for example from the 2300® Flex™ product family available from Lam Research Corporation of Fremont, CA. A reaction chamber used for deposition may be chamber from the Vector® product family or the Altus® product family, both available from Lam Research Corporation. The use of a combined reactor for both etching and deposition may be beneficial in certain embodiments as the need to transfer the substrate is avoided. The use of different reactors for etching and deposition may be beneficial in other embodiments where it is desired that the reactors are particularly optimized for each operation. In a particular embodiment both the etching and the deposition operations occur in the same reaction chamber (e.g., a Flex™ reaction chamber), and the deposition reaction occurs

through an MLD method such as the method 250 of FIG. 2B. Low-temperature thermally-driven deposition reactions may be particularly well suited for performing in a reaction chamber that is otherwise designed to perform etching. The relevant reaction chambers are discussed further below.

5 [0047] As noted, the deposition operation helps optimize the etching operation by forming a deeply penetrating protective layer that minimizes or prevents lateral etch of the feature during the etching operation. This promotes formation of etched features having very vertical sidewalls with little or no bowing. In certain implementations, a final etched feature having an aspect ratio of at least about 80 has a bow less than about 60% (measured as the widest critical dimension-narrowest
10 critical dimension below that/narrowest critical dimension above that *100). For example, a feature having a widest CD of 50 nm and a narrowest CD of 40 nm (the 40 nm CD being positioned below the 50 nm CD in the feature) has a bow of 25% ($100 \times (50 \text{ nm} - 40 \text{ nm}) / 40 \text{ nm} = 25\%$). In another implementation, a final etched feature having an aspect ratio of at least about 40 has a bow less than about 20%.

15 IV. Materials and Parameters of the Process Operations

A. Substrate

[0048] The methods disclosed herein are particularly useful for etching semiconductor substrates having dielectric materials thereon. Example dielectric materials include silicon oxides, silicon nitrides, silicon carbides, oxynitrides, oxycarbides, carbo-nitrides, doped versions of these
20 materials (e.g., doped with boron, phosphorus, etc.), and laminates from any combinations of these materials. Particular example materials include stoichiometric and non-stoichiometric formulations of SiO₂, SiN, SiON, SiOC, SiCN, etc. As noted above, the dielectric material that is etched may include more than one type/layer of material. In particular cases, the dielectric material may be provided in alternating layers of SiN and SiO₂ or alternating layers of polysilicon and SiO₂.
25 Further details are provided above. The substrate may have an overlying mask layer that defines where the features are to be etched. In certain cases, the mask layer is Si, and it may have a thickness between about 500 nm and about 1500 nm.

B. Etching Process

[0049] In various embodiments, the etching process is a reactive ion etch process that involves flowing a chemical etchant into a reaction chamber (often through a showerhead), generating a plasma from, *inter alia*, the etchant, and exposing a substrate to the plasma. The plasma dissociates the etchant compound(s) into neutral species and ion species (e.g., charged or neutral materials such as CF, CF₂ and CF₃). The plasma is a capacitively coupled plasma in many cases, though other types of plasma may be used as appropriate. Ions in the plasma are directed toward the wafer and cause the dielectric material to be etched away upon impact.

[0050] Example apparatus that may be used to perform the etching process include the 2300[®] FLEX[™] product family of reactive ion etch reactors available from Lam Research Corporation of Fremont, CA. This type of etch reactor is further described in the following U.S. Patents, each of which is herein incorporated by reference in its entirety and for all purposes: U.S. Patent No. 8,552,334, and U.S. Patent No. 6,841,943.

[0051] Various reactant options are available to etch the features into the dielectric material. In certain cases, the etching chemistry includes one or more fluorocarbons. In these or other cases, the etching chemistry may include other etchants such as NF₃. One or more co-reactants may also be provided. In some cases oxygen (O₂) is provided as a co-reactant. The oxygen may help moderate formation of a protective polymer sidewall coating (e.g., the first sidewall coating 304 of FIGS. 3A–3D).

[0052] In certain implementations, the etching chemistry includes a combination of fluorocarbons and oxygen. For instance, in one example the etching chemistry includes C₄F₆, C₄F₈, N₂, CO, CF₄, and O₂. Other conventional etching chemistries may also be used, as may non-conventional chemistries. The fluorocarbons may flow at a rate between about 0 sccm and about 500 sccm, for example between about 10 sccm and about 200 sccm. Where C₄F₆ and C₄F₈ are used, the flow of C₄F₆ may range between about 10 sccm and about 200 sccm and the flow of C₄F₈ may range between about 10 sccm and about 200 sccm. The flow of oxygen may range between about 0 sccm and about 500 sccm, for example between about 10 sccm and about 200 sccm. The flow of nitrogen may range between about 0 sccm and about 500 sccm, for example between about 10 sccm and about 200 sccm. The flow of tetrafluoromethane may range between about 0 sccm

and about 500 sccm, for example between about 10 sccm and about 200 sccm. The flow of carbon monoxide may range between about 0 sccm and about 500 sccm, for example between about 10 sccm and about 200 sccm. These rates are appropriate in a reactor volume of approximately 50 liters.

5 [0053] In some embodiments, the substrate temperature during etching is between about 30°C and about 200°C. In some embodiments, the pressure during etching is between about 5 mTorr and about 80 mTorr. The ion energy may be relatively high, for example between about 1 kV and about 10 kV. The ion energy is determined by the applied RF power. In various cases, dual-frequency RF power is used to generate the plasma. Thus, the RF power may include a first
10 frequency component (e.g., about 2 MHz) and a second frequency component (e.g., about 60 MHz). Different powers may be provided at each frequency component. For instance, the first frequency component (e.g., about 2 MHz) may be provided at a power between about 3 kW and about 24 kW, for example about 10 kW, and the second frequency component (e.g., about 60 MHz) may be provided at a lower power, for example between about 0.5 kW and about 10 kW, for
15 example about 2 kW. In some embodiments, three different frequencies of RF power are used to generate the plasma. For example, the combination could be 2 MHz, 27 MHz, and 60 MHz. Power levels for the third frequency component (e.g. about 27 MHz) may be similar to those powers specified above for the second frequency component. These power levels assume that the RF power is delivered to a single 300 mm wafer. The power levels can be scaled linearly based on
20 substrate area for additional substrates and/or substrates of other sizes (thereby maintaining a uniform power density delivered to the substrate). In some embodiments, the applied RF power during etching may be modulated between a higher power and a lower power at a repetition rate between about 100 Hz and about 40,000 Hz.

[0054] Each cycle of the etching process etches the dielectric material to some degree. The
25 distance etched during each cycle may be between about 10 nm and about 500 nm, for example between about 50 nm and about 200 nm. The total etch depth will depend on the particular application. For some cases (e.g., DRAM) the total etch depth may be between about 1.5 µm and about 2 µm. For other cases (e.g., VNAND) the total etch depth may be at least about 3 µm, for example at least about 4 µm. In these or other cases, the total etch depth may be about 5 µm or
30 less.

[0055] As explained in the discussion of FIGS. 3A–3D, the etching process can produce a first sidewall coating (e.g., first sidewall coating 304, which may be polymeric). However, the depth of this sidewall coating may be limited to the area near the upper portion of the feature, and may not extend all the way down into the feature where the sidewall protection is also needed. Thus, a separate deposition operation is performed, as described herein, to form a sidewall coating that covers more depth of the etched feature.

C. Deposition Process

[0056] The deposition process is performed primarily to deposit a protective layer on the sidewalls within the etched features. This protective layer should extend deep into the feature, even in high aspect ratio features. Formation of the protective layer deep within high aspect ratio features may be enabled by reactants that have relatively low sticking coefficients. Further, reaction mechanisms that rely on adsorption of reactants (e.g., ALD and MLD reactions) can promote formation of the protective layer deep within the etched features. Deposition of the protective layer begins after the feature is partially etched. As noted in the discussion of FIG. 2A, the deposition operation may be cycled with the etching operation to form additional sidewall protection as the feature is etched deeper into the dielectric material. In some cases, deposition of the protective layer begins at or after the feature is etched to at least about 1/3 of its final depth. In some embodiments, deposition of the protective layer begins once the feature reaches an aspect ratio of at least about 2, at least about 5, at least about 10, at least about 15, at least about 20, or at least about 30. In these or other cases, the deposition may begin before the feature reaches an aspect ratio of about 4, about 10, about 15, about 20, about 30, about 40, or about 50. In some embodiments, deposition begins after the feature is at least about 1 μm deep, or at least about 1.5 μm deep (e.g., in VNAND embodiments where the final feature depth is 3–4 μm). In other embodiments, deposition begins after the feature is at least about 600 nm deep, or at least about 800 nm deep (e.g., in DRAM embodiments where the final feature depth is 1.5–2 μm deep). The optimal time for initiating deposition of the protective layer is immediately before the sidewalls would otherwise become overetched to form a bow. The exact timing of this occurrence depends on the shape of the feature being etched, the material being etched, the chemistry used to etch and to deposit the protective layer, and the process conditions used to etch and deposit the relevant materials.

[0057] The protective layer that forms during the deposition process may have various compositions. As explained, the protective layer should penetrate deep into an etched feature, and should be relatively resistant to the etching chemistry used to etch the feature. In some cases the protective layer is a ceramic material or an organic polymer. Example organic materials may include polyolefins, for example polyfluoroolefins in some cases. One particular example is a polytetrafluoroethylene. A precursor fragment used for forming some polyfluoroolefins is CF_2 (which may come from hexafluoropropylene oxide (HFPO) in certain cases), which has a very low sticking coefficient and is therefore good at penetrating deep into an etched feature.

[0058] In certain embodiments, the protective layer that forms during the deposition process is an organic polymer. In some cases the organic polymer is a polyazomethine. In a particular case, a polyazomethine protective layer is formed from a combination of an amine (e.g., diamine) and an aldehyde (e.g., dialdehyde). In some cases, the organic polymer is a polythioacetal. For instance, the polythioacetal protective layer is formed from a combination of an aldehyde (e.g., dialdehyde) and a thiol. In some cases the organic polymer is a polyurea. For example, the polyurea protective layer is formed from a combination of an isocyanate (e.g., diisocyanate) and an amine (e.g., diamine). In some cases the organic polymer is a polyurethane. In particular, the polyurethane protective layer is formed from a combination of an isocyanate (e.g., diisocyanate) and an alcohol (e.g., diol). Such reactants may be used in an MLD process to form the protective layer in various embodiments, for example as shown in FIGS. 2C and 2D.

[0059] Where the protective film includes nitrogen – e.g., a nitrogen-containing polymer – a nitrogen-containing reactant may be used. A nitrogen-containing reactant contains at least one nitrogen, for example, nitrogen, ammonia, hydrazine, amines (e.g., amines bearing carbon) such as methylamine, dimethylamine, ethylamine, ethylenediamine, isopropylamine, t-butylamine, di-t-butylamine, cyclopropylamine, sec-butylamine, cyclobutylamine, isoamylamine, 2-methylbutan-2-amine, trimethylamine, diisopropylamine, diethylisopropylamine, di-t-butylhydrazine, as well as aromatic containing amines such as anilines, pyridines, and benzylamines. Amines may be primary, secondary, tertiary or quaternary (for example, tetraalkylammonium compounds). A nitrogen-containing reactant can contain heteroatoms other than nitrogen, for example, hydroxylamine, t-butyloxycarbonyl amine and N-t-butyl hydroxylamine are nitrogen-containing reactants. Another example is nitrous oxide.

[0060] Where the protective film includes oxygen – e.g., an oxygen-containing polymer – an oxygen-containing reactant may be used. Examples of oxygen-containing reactants include, but are not limited to, oxygen, ozone, nitrous oxide, nitric oxide, nitrogen dioxide, carbon monoxide, carbon dioxide, sulfur oxide, sulfur dioxide, oxygen-containing hydrocarbons ($C_xH_yO_z$), water, acyl halides, acid anhydrides, mixtures thereof, etc. The disclosed precursors are not intended to be limiting.

[0061] In certain implementations where the protective coating includes an organic polymer, the first reactant may be an acyl halide (e.g., a diacyl halide), for example an acyl chloride (e.g., a diacyl chloride), (though other acyl halides may be used in some cases). In various embodiments, the first reactant of diacyl chloride can be ethanedioyl dichloride (also referred to as oxalyl dichloride, $ClCOCOC l$), malonyl dichloride (also referred to as malonyl chloride, $CH_2(COCl)_2$), succinyl dichloride (also referred to as succinyl chloride, $ClCOCH_2CH_2COCl$), pentanedioyl dichloride (also referred to as glutaryl chloride, $ClCO(CH_2)_3COCl$), or combinations thereof. In some other implementations, the first reactant may be an acid anhydride such as an anhydride of a dicarboxylic acid giving rise to any of the above diacyl chlorides. One example of an acid anhydride that may be used is maleic anhydride. In yet other implementations, the first reactant may be an organic metal-containing precursor, one example of which is trimethylaluminum (TMA).

[0062] In certain implementations, where the protective film includes an organic polymer, the first reactant may alternatively be an aldehyde (e.g., dialdehyde or trialdehyde) or at least include an aldehyde functional group. In various embodiments, the first reactant can be succindialdehyde ($C_4H_6O_2$), glutaraldehyde ($C_5H_8O_2$), adipaldehyde ($C_6H_{10}O_2$), terephthalaldehyde ($C_8H_6O_2$), 1,4-benzenedicarboxaldehyde ($C_6H_4(CHO)_2$), ortho-phthalaldehyde ($C_8H_6O_2$), 1,2-benzenedicarboxaldehyde ($C_6H_4(CHO)_2$), 2-methylglutaraldehyde ($C_6H_{10}O_2$), or combinations thereof.

[0063] In some implementations, where the protective film includes an organic polymer, the first reactant may alternatively be an isocyanate (e.g., diisocyanate) or at least include an isocyanate functional group. The diisocyanate in some cases may be: tolylene-2,4-diisocyanate, 1,3-bis(isocyanatomethyl)cyclohexane, hexamethylene diisocyanate, m-xylylene diisocyanate,

1,3-bis(1-isocyanato-1-methylethyl)benzene, isophorone diisocyanate, diphenylmethane 4,4'-diisocyanate, 4,4'-methylenebis(cyclohexyl isocyanate), tolylene-2,6-diisocyanate, 1,4-phenylene diisocyanate, 1,3-phenylene diisocyanate, 3,3'-dimethyl-4,4'-biphenylene diisocyanate, or combinations thereof.

5 [0064] In some embodiments, aldehydes or isocyanates may be used in the alternative to acyl halides. Acyl halides may have a propensity for self-reaction, thereby resulting in a short shelf life even at low temperatures.

[0065] Dialdehydes are generally more stable than acyl halides such as di-acyl chlorides. Dialdehydes also tend to be more volatile than acyl halides such as di-acyl chlorides. Dialdehydes
10 typically have higher vapor pressures so that they are easier to vaporize and deliver to the substrate. Higher dosing pressures reduce dose times and reduce deposition process times, thereby increasing throughput. That way, repeated deposition and etch processes may be performed without deposition processes substantially slowing down formation of a recessed feature.

[0066] Dialdehydes may have a propensity to stick to etched surfaces. Without being limited
15 by any theory, dialdehydes may tend to stick to surfaces that have been etched by fluorocarbon chemistries. One of the challenges of depositing conformal liners by MLD is initiating deposition on etched surfaces. Dialdehydes may selectively adhere to surfaces etched by fluorocarbon or hydrofluorocarbon chemistries to improve initiation of the protective film on sidewalls within the etched features.

[0067] Where the protective coating includes an organic polymer, the second reactant may
20 include an amine or alcohol functional group. In these or other embodiments where the protective coating includes an organic polymer, the second reactant may be a diamine. The diamine in some cases may be 1,2-ethanediamine (also referred to as ethylenediamine, $(\text{NH}_2(\text{CH}_2)_2\text{NH}_2)$), 1,3-propanediamine ($\text{NH}_2(\text{CH}_2)_3\text{NH}_2$), 1,4-butanediamine ($\text{NH}_2(\text{CH}_2)_4\text{NH}_2$), or combinations thereof.
25 The diamine in some other cases may be ethylenediamine, m-xylylenediamine, isophoronediamine, 1,3-cyclohexanebis(methylamine), 1,4-bis(aminomethyl)cyclohexane, 4,4'-methylenebis(2-methylcyclohexylamine), 4,4'-methylenebis(cyclohexylamine), m-phenylenediamine, p-phenylenediamine, 4-aminobenzylamine, 3-aminobenzylamine, 4-(2-aminoethyl)aniline, p-xylylenediamine, m-xylylenediamine, or combinations thereof. The second

reactant may be a diol in some cases. Example diols include ethylene glycol, 1,3-propanediol, 1,4-butanediol, or combinations thereof. The second reactant may be a thiol in some cases. Example thiols include 1,2-ethanedithiol, 1,3-propanedithiol, 1,4-butanedithiol, or combinations thereof. In certain embodiments, the second reactant may be a trifunctional compound such as (±)-3-amino-1,2-propanediol, glycerol, bis(hexamethylene)triamine, melamine, diethylenetriamine, (±)-1,2,4-butanetriol, cyanuric chloride, or combinations thereof.

[0068] In a particular embodiment, a dialdehyde such as glutaraldehyde may be used with ethylenediamine to form a polyamide protective coating. Where the first reactant is a dialdehyde and the second reactant is a diamine, the deposited organic polymer protective coating may have greater etch resistance than if the first reactant were an acyl halide. In fact, the deposited organic polymer protective coating may be highly resistant to plasma etching, thereby providing an effective sidewall protective film against subsequent lateral etch of dielectric material during etching operations.

[0069] In some implementations, the organic polymer protective coating may be deposited as an in-situ process in an etch reactor. Dialdehydes may react with diamines at relatively low temperatures (e.g., less than 100°C) and at relatively low doses (e.g., less than 10 Torr-sec). Accordingly, the organic polymer coating may be deposited in a reaction chamber between etch operations without introducing an air break. In some embodiments, deposition of the organic polymer coating may occur in the same reaction chamber as etch operations during formation of recessed features in the substrate.

[0070] In another particular embodiment, a diisocyanate may be used with ethylenediamine to form a polyurea protective coating.

[0071] Example purge gases include, but are not limited to, He, Ar, Ne, H₂, N₂, and combinations thereof.

[0072] Other reactants may also be used as known by those of ordinary skill in the art. For example where the protective film includes a metal, a metal-containing reactant may be used, and where the protective film includes carbon, a carbon-containing reactant may be used.

[0073] A few particular examples of reactant combinations will be provided, though these examples are not intended to be limiting. In one example, a dialdehyde such as glutaraldehyde is adsorbed on to the surface of a substrate to form a precursor film. The precursor film may be exposed to ethylenediamine to thereby form a protective organic polymer film as shown in FIGS. 2C and 2D. The reaction may occur without exposure to plasma, relying instead on thermal energy to drive the reaction. These reactants have been shown to react without plasma energy at relatively low temperatures as described above.

[0074] As noted above, the precursor(s) used to form the protective layer may have relatively low sticking coefficients, thereby enabling the precursors to penetrate deep into the etched features. In some cases, the sticking coefficient of the precursors (at the relevant deposition conditions) may be about 0.05 or less, for example about 0.001 or less.

[0075] The reaction mechanism may be cyclic (e.g., ALD or MLD) or continuous (e.g., CVD). Any method that results in the formation of the protective sidewall film at high aspect ratios may be used. As mentioned, ALD and MLD reactions may be particularly well suited for this purpose due to their conformality and adsorption-based mechanisms. However, other types of reactions may be used so long as the film is able to form at high aspect ratios to protect the sidewalls deep in an etched feature.

[0076] Briefly, plasma assisted ALD reactions involve cyclically performing the following operations: (a) delivery of a first reactant to form an adsorbed precursor layer, (b) an optional purge operation to remove the first reactant from the reaction chamber, (c) delivery of a second reactant (often provided in the form of a plasma), where plasma energy drives a reaction between the first and second reactants, (d) an optional purge to remove excess reactant and byproducts, and (e) repeating (a)–(d) until the film reaches a desired thickness.

[0077] Similarly, MLD reactions may involve cyclically performing the operations of: (a) delivery of a first reactant to form an adsorbed precursor layer, (b) an optional purge operation to remove unadsorbed first reactant from the reaction chamber, (c) delivery of a second reactant, where thermal energy drives a reaction between the first and second reactants to form the protective film, (d) an optional purge operation to remove unadsorbed reactants and byproducts,

and (e) repeating (a)–(d) until the protective film reaches a desired thickness. The first and second reactants may be delivered in gas phase, and the reaction may occur without the use of plasma.

[0078] Because the reactants are provided at separate times and the reaction is a surface reaction in the case of ALD and MLD methods, the film may be adsorption limited to some degree.

5 This adsorption-based regime results in the formation of very conformal films that can line substantially the entire depth of the feature. In various cases, the protective coating may be deposited along a substantial fraction of the length/depth of a partially etched feature. In some cases, the protective film may be deposited along at least about 80%, at least about 90%, or at least about 95% of the length/depth of the feature. In particular embodiments the protective film
10 deposits along the entire length/depth of the feature. By contrast, plasma assisted CVD reactions involve delivering reactant(s) to the substrate continuously while the substrate is exposed to plasma. CVD reactions are gas phase reactions, which deposit reaction products on the substrate surface.

[0079] The following reaction conditions may be used in certain embodiments where the
15 deposition reaction occurs through MLD methods. The conditions are described in relation to the method 250 shown in FIG. 2B. In operation 251, the first reactant may be flowed into the reaction chamber. In certain embodiments, the first reactant may flow at a rate between about 0.1 sccm and about 5000 sccm, for example between about 500 sccm and about 2000 sccm, for a duration between about 0.1 s and about 30 s, for example between about 0.2 s and about 5 s. At operation
20 253, the reaction chamber may be optionally purged for a duration between about 0.05 s and about 10 s, for example between about 0.2 s and about 3 s. The purge may occur by evacuating the reaction chamber and/or by flowing an inert gas through the reaction chamber. Where inert gas is used, it may flow at a rate between about 20 sccm and about 5000 sccm in some cases. Next, at operation 255, the second reactant may be flowed into the reaction chamber. In certain
25 embodiments, the second reactant may flow at a rate between about 10 sccm and about 5000 sccm, or between about 500 sccm and about 2000 sccm, for a duration between about 0.1 s and about 30 s, for example between about 0.2 s and about 5 s.

[0080] Thermal energy may be provided to drive a reaction between the first and second reactants. Thermal energy is available to an extent primarily controlled by the temperature of the

substrate. In some cases, thermal energy may be regulated by controlling the substrate temperature via a substrate support/pedestal. In these or other cases, thermal energy may be provided by delivering the reactants at particular temperatures. In some cases, the temperature of the substrate may be maintained between about -10°C and about 350°C, for example between about 0°C and about 200°C, or between about 10°C and about 100°C, or between about 20°C and about 50°C. In certain embodiments, the substrate is maintained at a temperature below about 200°C, below about 100°C, below about 50°C, or below about 30°C. In these or other embodiments, the temperature of one or both of the reactant gases delivered to the reaction chamber (and/or inert gases used to purge) may correspond to the substrate temperatures recited in this paragraph. At operation 257, the reaction chamber may be optionally purged using the conditions described above in relation to operation 253. At operation 259 it is determined whether the protective film is sufficiently thick. If not, the method may be repeated from operation 251. In certain cases, a pressure within the reaction chamber may be between about 1 Torr and about 4 Torr. In various cases, the protective film in each iteration of operation 205 or 215 of FIG. 2A may be deposited over a duration that is about 10 minutes or less.

[0081] In certain embodiments, terminal ends of the molecules forming the organic polymeric film form a hydroxyl, an amine, or a thiol. For example, if a diamine is used as the second reactant, -NH₂ may form the terminal ends of the molecules forming the organic polymeric film. If a diol is used as the second reactant, -OH may form the terminal ends of the molecules forming the organic polymeric film. Similarly, if a thiol is used as the second reactant, -SH may form the terminal ends of the molecules forming the organic polymeric film.

[0082] In certain embodiments the first reactant and the second reactant used to form the organic polymeric film may be flowed into the vacuum chamber until they reach about 100% saturation on a plasma or process gas exposed surface of the vacuum chamber such that a layer of the organic polymeric film deposited on the plasma or process gas exposed surface of the vacuum chamber has a maximum thickness. Under- and over-saturation may also be practiced in some embodiments, for example to tailor the deposition rate as desired.

[0083] The reaction conditions herein are provided as guidance and are not intended to be limiting.

V. Apparatus

[0084] The methods described herein may be performed by any suitable apparatus or combination of apparatus. A suitable apparatus includes hardware for accomplishing the process operations and a system controller having instructions for controlling process operations in accordance with the present invention. For example, in some embodiments, the hardware may include one or more process stations included in a process tool. One process station may be an etching station and another process station may be a deposition station. In another embodiment, etching and deposition occur in a single station/chamber.

[0085] FIGS. 4A–4C illustrate an embodiment of an adjustable gap capacitively coupled confined RF plasma reactor 400 that may be used for performing the etching operations described herein. As depicted, a vacuum chamber 402 includes a chamber housing 404, surrounding an interior space housing a lower electrode 406. In an upper portion of the chamber 402 an upper electrode 408 is vertically spaced apart from the lower electrode 406. Planar surfaces of the upper and lower electrodes 408, 406 are substantially parallel and orthogonal to the vertical direction between the electrodes. Preferably the upper and lower electrodes 408, 406 are circular and coaxial with respect to a vertical axis. A lower surface of the upper electrode 408 faces an upper surface of the lower electrode 406. The spaced apart facing electrode surfaces define an adjustable gap 410 therebetween. During operation, the lower electrode 406 is supplied RF power by an RF power supply (match) 420. RF power is supplied to the lower electrode 406 through an RF supply conduit 422, an RF strap 424 and an RF power member 426. A grounding shield 436 may surround the RF power member 426 to provide a more uniform RF field to the lower electrode 406. As described in commonly-owned U.S. Patent No. 7,732,728, the entire contents of which are herein incorporated by reference, a wafer is inserted through wafer port 482 and supported in the gap 410 on the lower electrode 406 for processing, a process gas is supplied to the gap 410 and excited into plasma state by the RF power. The upper electrode 408 can be powered or grounded.

[0086] In the embodiment shown in FIGS. 4A–4C, the lower electrode 406 is supported on a lower electrode support plate 416. An insulator ring 414 interposed between the lower electrode 406 and the lower electrode Support plate 416 insulates the lower electrode 406 from the support plate 416.

[0087] An RF bias housing 430 supports the lower electrode 406 on an RF bias housing bowl 432. The bowl 432 is connected through an opening in a chamber wall plate 418 to a conduit support plate 438 by an arm 434 of the RF bias housing 430. In a preferred embodiment, the RF bias housing bowl 432 and RF bias housing arm 434 are integrally formed as one component, however, the arm 434 and bowl 432 can also be two separate components bolted or joined together.

[0088] The RF bias housing arm 434 includes one or more hollow passages for passing RF power and facilities, such as gas coolant, liquid coolant, RF energy, cables for lift pin control, electrical monitoring and actuating signals from outside the vacuum chamber 402 to inside the vacuum chamber 402 at a space on the backside of the lower electrode 406. The RF supply conduit 422 is insulated from the RF bias housing arm 434, the RF bias housing arm 434 providing a return path for RF power to the RF power supply 420. A facilities conduit 440 provides a passageway for facility components. Further details of the facility components are described in U.S. Patent Nos. 5,948,704 and 7,732,728 and are not shown here for simplicity of description. The gap 410 is preferably surrounded by a confinement ring assembly or shroud (not shown), details of which can be found in commonly owned published U.S. Patent No. 7,740,736 herein incorporated by reference. The interior of the vacuum chamber 402 is maintained at a low pressure by connection to a vacuum pump through vacuum portal 480.

[0089] The conduit support plate 438 is attached to an actuation mechanism 442. Details of an actuation mechanism are described in commonly-owned U.S. Patent No. 7,732,728 incorporated herein by above. The actuation mechanism 442, such as a servo mechanical motor, stepper motor or the like is attached to a vertical linear bearing 444, for example, by a screw gear 446 such as a ball screw and motor for rotating the ball screw. During operation to adjust the size of the gap 410, the actuation mechanism 442 travels along the vertical linear bearing 444. FIG. 4A illustrates the arrangement when the actuation mechanism 442 is at a high position on the linear bearing 444 resulting in a small gap 410 *a*. FIG. 4B illustrates the arrangement when the actuation mechanism 442 is at a mid position on the linear bearing 444. As shown, the lower electrode 406, the RF bias housing 430, the conduit support plate 438, the RF power supply 420 have all moved lower with respect to the chamber housing 404 and the upper electrode 408, resulting in a medium size gap 410 *b*.

[0090] FIG. 4C illustrates a large gap 410 *c* when the actuation mechanism 442 is at a low position on the linear bearing. Preferably, the upper and lower electrodes 408, 406 remain co-axial during the gap adjustment and the facing surfaces of the upper and lower electrodes across the gap remain parallel.

5 [0091] This embodiment allows the gap 410 between the lower and upper electrodes 406, 408 in the CCP chamber 402 during multi-step process recipes (BARC, HARC, and STRIP etc.) to be adjusted, for example, in order to maintain uniform etch across a large diameter substrate such as 300 mm wafers or flat panel displays. In particular, this chamber pertains to a mechanical arrangement that permits the linear motion necessary to provide the adjustable gap between lower
10 and upper electrodes 406, 408.

[0092] FIG. 4A illustrates laterally deflected bellows 450 sealed at a proximate end to the conduit support plate 438 and at a distal end to a stepped flange 428 of chamber wall plate 418. The inner diameter of the stepped flange defines an opening 412 in the chamber wall plate 418 through which the RF bias housing arm 434 passes. The distal end of the bellows 450 is clamped
15 by a clamp ring 452.

[0093] The laterally deflected bellows 450 provides a vacuum seal while allowing vertical movement of the RF bias housing 430, conduit support plate 438 and actuation mechanism 442. The RF bias housing 430, conduit support plate 438 and actuation mechanism 442 can be referred to as a cantilever assembly. Preferably, the RF power supply 420 moves with the cantilever
20 assembly and can be attached to the conduit support plate 438. FIG. 4B shows the bellows 450 in a neutral position when the cantilever assembly is at a mid position. FIG. 4C shows the bellows 450 laterally deflected when the cantilever assembly is at a low position.

[0094] A labyrinth seal 448 provides a particle barrier between the bellows 450 and the interior of the plasma processing chamber housing 404. A fixed shield 456 is immovably attached to the
25 inside inner wall of the chamber housing 404 at the chamber wall plate 418 so as to provide a labyrinth groove 460 (slot) in which a movable shield plate 458 moves vertically to accommodate vertical movement of the cantilever assembly. The outer portion of the movable shield plate 458 remains in the slot at all vertical positions of the lower electrode 406.

[0095] In the embodiment shown, the labyrinth seal 448 includes a fixed shield 456 attached to an inner surface of the chamber wall plate 418 at a periphery of the opening 412 in the chamber wall plate 418 defining a labyrinth groove 460. The movable shield plate 458 is attached and extends radially from the RF bias housing arm 434 where the arm 434 passes through the opening 412 in the chamber wall plate 418. The movable shield plate 458 extends into the labyrinth groove 460 while spaced apart from the fixed shield 456 by a first gap and spaced apart from the interior surface of the chamber wall plate 418 by a second gap allowing the cantilevered assembly to move vertically. The labyrinth seal 448 blocks migration of particles spalled from the bellows 450 from entering the vacuum chamber interior 405 and blocks radicals from process gas plasma from migrating to the bellows 450 where the radicals can form deposits which are subsequently spalled.

[0096] FIG. 4A shows the movable shield plate 458 at a higher position in the labyrinth groove 460 above the RF bias housing arm 434 when the cantilevered assembly is in a high position (small gap 410 *a*). FIG. 4C shows the movable shield plate 458 at a lower position in the labyrinth groove 460 above the RF bias housing arm 434 when the cantilevered assembly is in a low position (large gap 410 *c*). FIG. 4B shows the movable shield plate 458 in a neutral or mid position within the labyrinth groove 460 when the cantilevered assembly is in a mid position (medium gap 410 *b*). While the labyrinth seal 448 is shown as symmetrical about the RF bias housing arm 434, in other embodiments the labyrinth seal 448 may be asymmetrical about the RF bias arm 434.

[0097] Figure 5 provides a simple block diagram depicting various reactor components arranged for implementing deposition methods described herein. As shown, a reactor 500 includes a process chamber 524 that encloses other components of the reactor and serves to contain a plasma generated by a capacitive-discharge type system including a showerhead 514 working in conjunction with a grounded heater block 520. A high frequency (HF) radio frequency (RF) generator 504 and a low frequency (LF) RF generator 502 may be connected to a matching network 506 and to the showerhead 514. The power and frequency supplied by matching network 506 may be sufficient to generate a plasma from process gases supplied to the process chamber 524. For example, the matching network 506 may provide 50W to 500W of HFRF power. In some examples, the matching network 506 may provide 100 W to 5000 W of HFRF power and 100 W to 5000 W of LFRF power total energy. In a typical process, the HFRF component may generally

be between 5 MHz to 60 MHz, e.g., 13.56 MHz. In operations where there is an LF component, the LF component may be from about 100 kHz to 2 MHz, e.g., 430 kHz.

[0098] Within the reactor, a wafer pedestal 518 may support a substrate 516. The wafer pedestal 518 may include a chuck, a fork, or lift pins (not shown) to hold and transfer the substrate during and between the deposition and/or plasma treatment reactions. The chuck may be an electrostatic chuck, a mechanical chuck, or various other types of chuck as are available for use in the industry and/or for research.

[0099] Various process gases may be introduced via inlet 512. Multiple source gas lines 510 are connected to manifold 508. The gases may be premixed or not. Appropriate valving and mass flow control mechanisms may be employed to ensure that the correct process gases are delivered during the deposition and plasma treatment phases of the process. In the case where a chemical precursor(s) is delivered in liquid form, liquid flow control mechanisms may be employed. Such liquids may then be vaporized and mixed with process gases during transportation in a manifold heated above the vaporization point of the chemical precursor supplied in liquid form before reaching the deposition chamber.

[0100] Process gases may exit chamber 524 via an outlet 522. A vacuum pump, e.g., a one or two stage mechanical dry pump and/or turbomolecular pump 540, may be used to draw process gases out of the process chamber 524 and to maintain a suitably low pressure within the process chamber 524 by using a closed-loop-controlled flow restriction device, such as a throttle valve or a pendulum valve.

[0101] As discussed above, the techniques for deposition discussed herein may be implemented on a multi-station or single station tool. In specific implementations, a 300 mm Lam Vector™ tool having a 4-station deposition scheme or a 200 mm Sequel™ tool having a 6-station deposition scheme may be used. In some implementations, tools for processing 450 mm wafers may be used. In various implementations, the wafers may be indexed after every deposition and/or post-deposition plasma treatment, or may be indexed after etching operations if the etching chambers or stations are also part of the same tool, or multiple depositions and treatments may be conducted at a single station before indexing the wafer.

[0102] In some embodiments, an apparatus may be provided that is configured to perform the techniques described herein. A suitable apparatus may include hardware for performing various process operations as well as a system controller 530 having instructions for controlling process operations in accordance with the disclosed embodiments. The system controller 530 will typically include one or more memory devices and one or more processors communicatively connected with various process control equipment, e.g., valves, RF generators, wafer handling systems, etc., and configured to execute the instructions so that the apparatus will perform a technique in accordance with the disclosed embodiments. Machine-readable media containing instructions for controlling process operations in accordance with the present disclosure may be coupled to the system controller 530. The system controller 530 may be communicatively connected with various hardware devices, e.g., mass flow controllers, valves, RF generators, vacuum pumps, etc. to facilitate control of the various process parameters that are associated with the deposition operations as described herein.

[0103] In some embodiments, a system controller 530 may control all of the activities of the reactor 500. The system controller 530 may execute system control software stored in a mass storage device, loaded into a memory device, and executed on a processor. The system control software may include instructions for controlling the timing of gas flows, wafer movement, RF generator activation, etc., as well as instructions for controlling the mixture of gases, the chamber and/or station pressure, the chamber and/or station temperature, the wafer temperature, the target power levels, the RF power levels, the substrate pedestal, chuck, and/or susceptor position, and other parameters of a particular process performed by the reactor apparatus 500. The system control software may be configured in any suitable way. For example, various process tool component subroutines or control objects may be written to control operation of the process tool components necessary to carry out various process tool processes. The system control software may be coded in any suitable computer readable programming language.

[0104] The system controller 530 may typically include one or more memory devices and one or more processors configured to execute the instructions so that the apparatus will perform a technique in accordance with the present disclosure. Machine-readable media containing instructions for controlling process operations in accordance with disclosed embodiments may be coupled to the system controller 530.

[0105] One or more process stations may be included in a multi-station processing tool. Figure 6 shows a schematic view of an embodiment of a multi-station processing tool 600 with an inbound load lock 602 and an outbound load lock 604, either or both of which may include a remote plasma source. A robot 606, at atmospheric pressure, is configured to move wafers from a cassette loaded through a pod 608 into inbound load lock 602 via an atmospheric port 610. A wafer is placed by the robot 606 on a pedestal 612 in the inbound load lock 602, the atmospheric port 610 is closed, and the load lock is pumped down. Where the inbound load lock 602 includes a remote plasma source, the wafer may be exposed to a remote plasma treatment in the load lock prior to being introduced into a processing chamber 614. Further, the wafer also may be heated in the inbound load lock 602 as well, for example, to remove moisture and adsorbed gases. Next, a chamber transport port 616 to processing chamber 614 is opened, and another robot (not shown) places the wafer into the reactor on a pedestal of a first station shown in the reactor for processing. While the embodiment depicted includes load locks, it will be appreciated that, in some embodiments, direct entry of a wafer into a process station may be provided.

[0106] The depicted processing chamber 614 includes four process stations, numbered from 1 to 4 in the embodiment shown in Figure 6. Each station has a heated pedestal (shown at 618 for station 1), and gas line inlets. It will be appreciated that in some embodiments, each process station may have different or multiple purposes. For example, each of the process stations 1–4 may be a chamber for performing one or more of ALD, CVD, CFD, or etching (any of which may be plasma assisted). In one embodiment, at least one of the process stations is a deposition station having a reaction chamber as shown in FIG. 5, and at least one of the other process stations is an etching station having a reaction chamber as shown in FIGS. 4A–4C. While the depicted processing chamber 614 includes four stations, it will be understood that a processing chamber according to the present disclosure may have any suitable number of stations. For example, in some embodiments, a processing chamber may have five or more stations, while in other embodiments a processing chamber may have three or fewer stations.

[0107] Figure 6 also depicts an embodiment of a wafer handling system 609 for transferring wafers within processing chamber 614. In some embodiments, wafer handling system 609 may transfer wafers between various process stations and/or between a process station and a load lock. It will be appreciated that any suitable wafer handling system may be employed. Non-limiting

examples include wafer carousels and wafer handling robots. Figure 6 also depicts an embodiment of a system controller 650 employed to control process conditions and hardware states of process tool 600. System controller 650 may include one or more memory devices 656, one or more mass storage devices 654, and one or more processors 652. Processor 652 may include a CPU or computer, analog and/or digital input/output connections, stepper motor controller boards, etc.

[0108] In some implementations, a controller is part of a system, which may be part of the above-described examples. Such systems can comprise semiconductor processing equipment, including a processing tool or tools, chamber or chambers, a platform or platforms for processing, and/or specific processing components (a wafer pedestal, a gas flow system, etc.). These systems may be integrated with electronics for controlling their operation before, during, and after processing of a semiconductor wafer or substrate. The electronics may be referred to as the “controller,” which may control various components or subparts of the system or systems. The controller, depending on the processing requirements and/or the type of system, may be programmed to control any of the processes disclosed herein, including the delivery of processing gases, temperature settings (e.g., heating and/or cooling), pressure settings, vacuum settings, power settings, radio frequency (RF) generator settings, RF matching circuit settings, frequency settings, flow rate settings, fluid delivery settings, positional and operation settings, wafer transfers into and out of a tool and other transfer tools and/or load locks connected to or interfaced with a specific system.

[0109] Broadly speaking, the controller may be defined as electronics having various integrated circuits, logic, memory, and/or software that receive instructions, issue instructions, control operation, enable cleaning operations, enable endpoint measurements, and the like. The integrated circuits may include chips in the form of firmware that store program instructions, digital signal processors (DSPs), chips defined as application specific integrated circuits (ASICs), and/or one or more microprocessors, or microcontrollers that execute program instructions (e.g., software). Program instructions may be instructions communicated to the controller in the form of various individual settings (or program files), defining operational parameters for carrying out a particular process on or for a semiconductor wafer or to a system. The operational parameters may, in some embodiments, be part of a recipe defined by process engineers to accomplish one or

more processing operations during the fabrication of one or more layers, materials, metals, oxides, silicon, silicon dioxide, surfaces, circuits, and/or dies of a wafer.

[0110] The controller, in some implementations, may be a part of or coupled to a computer that is integrated with, coupled to the system, otherwise networked to the system, or a combination thereof. For example, the controller may be in the “cloud” or all or a part of a fab host computer system, which can allow for remote access of the wafer processing. The computer may enable remote access to the system to monitor current progress of fabrication operations, examine a history of past fabrication operations, examine trends or performance metrics from a plurality of fabrication operations, to change parameters of current processing, to set processing operations to follow a current processing, or to start a new process. In some examples, a remote computer (e.g. a server) can provide process recipes to a system over a network, which may include a local network or the Internet. The remote computer may include a user interface that enables entry or programming of parameters and/or settings, which are then communicated to the system from the remote computer. In some examples, the controller receives instructions in the form of data, which specify parameters for each of the processing operations to be performed during one or more operations. It should be understood that the parameters may be specific to the type of process to be performed and the type of tool that the controller is configured to interface with or control. Thus as described above, the controller may be distributed, such as by comprising one or more discrete controllers that are networked together and working towards a common purpose, such as the processes and controls described herein. An example of a distributed controller for such purposes would be one or more integrated circuits on a chamber in communication with one or more integrated circuits located remotely (such as at the platform level or as part of a remote computer) that combine to control a process on the chamber.

[0111] Without limitation, example systems may include a plasma etch chamber or module, a deposition chamber or module, a spin-rinse chamber or module, a metal plating chamber or module, a clean chamber or module, a bevel edge etch chamber or module, a physical vapor deposition (PVD) chamber or module, a chemical vapor deposition (CVD) chamber or module, an atomic layer deposition (ALD) chamber or module, a molecular layer deposition (MLD) chamber or module, an atomic layer etch (ALE) chamber or module, an ion implantation chamber or

module, a track chamber or module, and any other semiconductor processing systems that may be associated or used in the fabrication and/or manufacturing of semiconductor wafers.

[0112] As noted above, depending on the process operation or operations to be performed by the tool, the controller might communicate with one or more of other tool circuits or modules, other tool components, cluster tools, other tool interfaces, adjacent tools, neighboring tools, tools located throughout a factory, a main computer, another controller, or tools used in material transport that bring containers of wafers to and from tool locations and/or load ports in a semiconductor manufacturing factory.

[0113] In certain embodiments, the controller has instructions to perform the operations shown and described in relation to FIG. 2A. For example, the controller may have instructions to cyclically (a) perform an etching operation to partially etch a feature on a substrate, and (b) deposit a protective sidewall coating in the etched feature without substantially etching the substrate. Deposition of the protective sidewall coating may proceed by exposing the substrate to a first reactant and allowing the first reactant to adsorb onto the substrate, where the first reactant may include a dialdehyde or trialdehyde, exposing the substrate to a second reactant, where the first and second reactants react with one another to form the protective sidewall coating. Exposures to the first reactant and the second reactant may be repeated in a cyclic manner until the protective film reaches a target thickness. The instructions may relate to performing these processes using the disclosed reaction conditions. The instructions may also relate to transferring the substrate between etching and deposition chambers in some implementations.

[0114] Returning to the embodiment of FIG. 6, in some embodiments, system controller 650 controls all of the activities of process tool 600. System controller 650 executes system control software 658 stored in mass storage device 654, loaded into memory device 656, and executed on processor 652. Alternatively, the control logic may be hard coded in the system controller 650. Applications Specific Integrated Circuits, Programmable Logic Devices (e.g., field-programmable gate arrays, or FPGAs) and the like may be used for these purposes. In the following discussion, wherever “software” or “code” is used, functionally comparable hard coded logic may be used in its place. System control software 658 may include instructions for controlling the timing, mixture of gases, chamber and/or station pressure, chamber and/or station temperature, wafer temperature,

target power levels, RF power levels, RF exposure time, substrate pedestal, chuck and/or susceptor position, and other parameters of a particular process performed by process tool 600. System control software 658 may be configured in any suitable way. For example, various process tool component subroutines or control objects may be written to control operation of the process tool components necessary to carry out various process tool processes. System control software 658 may be coded in any suitable computer readable programming language.

[0115] In some embodiments, system control software 658 may include input/output control (IOC) sequencing instructions for controlling the various parameters described above. For example, each phase of a CFD process may include one or more instructions for execution by system controller 650. The instructions for setting process conditions for an ALD process phase may be included in a corresponding ALD recipe phase. In some embodiments, the ALD recipe phases may be sequentially arranged, so that all instructions for an ALD process phase are executed concurrently with that process phase.

[0116] Other computer software and/or programs stored on mass storage device 654 and/or memory device 656 associated with system controller 650 may be employed in some embodiments. Examples of programs or sections of programs for this purpose include a substrate positioning program, a process gas control program, a pressure control program, a heater control program, and a plasma control program.

[0117] A substrate positioning program may include program code for process tool components that are used to load the substrate onto pedestal 618 and to control the spacing between the substrate and other parts of process tool 600.

[0118] A process gas control program may include code for controlling gas composition and flow rates and optionally for flowing gas into one or more process stations prior to deposition in order to stabilize the pressure in the process station. In some embodiments, the controller includes instructions for depositing a nanolaminate protective layer on a core layer, and depositing a conformal layer over the protective layer.

[0119] A pressure control program may include code for controlling the pressure in the process station by regulating, for example, a throttle valve in the exhaust system of the process station, a

gas flow into the process station, etc. In some embodiments, the controller includes instructions for depositing a nanolaminate protective layer on a core layer, and depositing a conformal layer over the protective layer.

[0120] A heater control program may include code for controlling the current to a heating unit that is used to heat the substrate. Alternatively, the heater control program may control delivery of a heat transfer gas (such as helium) to the substrate. In certain implementations, the controller includes instructions for depositing a nanolaminate protective layer at a first temperature, and a conformal layer over the protective layer at a second temperature, where the second temperature is higher than the first temperature.

[0121] A plasma control program may include code for setting RF power levels and exposure times in one or more process stations in accordance with the embodiments herein. In some embodiments, the controller includes instructions for depositing a nanolaminate protective layer at a first RF power level and RF duration, and depositing a conformal layer over the protective layer at a second RF power level and RF duration. The second RF power level and/or the second RF duration may be higher/longer than the first RF power level/duration.

[0122] In some embodiments, there may be a user interface associated with system controller 650. The user interface may include a display screen, graphical software displays of the apparatus and/or process conditions, and user input devices such as pointing devices, keyboards, touch screens, microphones, etc.

[0123] In some embodiments, parameters adjusted by system controller 650 may relate to process conditions. Non-limiting examples include process gas composition and flow rates, temperature, pressure, plasma conditions (such as RF bias power levels and exposure times), etc. These parameters may be provided to the user in the form of a recipe, which may be entered utilizing the user interface.

[0124] Signals for monitoring the process may be provided by analog and/or digital input connections of system controller 650 from various process tool sensors. The signals for controlling the process may be output on the analog and digital output connections of process tool 600. Non-limiting examples of process tool sensors that may be monitored include mass flow controllers,

pressure sensors (such as manometers), thermocouples, etc. Appropriately programmed feedback and control algorithms may be used with data from these sensors to maintain process conditions.

[0125] System controller 650 may provide program instructions for implementing the above-described deposition processes. The program instructions may control a variety of process parameters, such as DC power level, RF bias power level, pressure, temperature, etc. The instructions may control the parameters to operate in-situ deposition of film stacks according to various embodiments described herein.

[0126] The system controller will typically include one or more memory devices and one or more processors configured to execute the instructions so that the apparatus will perform a method in accordance with the disclosed embodiments. Machine-readable, non-transitory media containing instructions for controlling process operations in accordance with the disclosed embodiments may be coupled to the system controller.

[0127] The various hardware and method embodiments described above may be used in conjunction with lithographic patterning tools or processes, for example, for the fabrication or manufacture of semiconductor devices, displays, LEDs, photovoltaic panels and the like. Typically, though not necessarily, such tools/processes will be used or conducted together in a common fabrication facility.

[0128] FIG. 7 depicts a semiconductor process cluster architecture with various modules that interface with a vacuum transfer module 738 (VTM). The arrangement of transfer modules to “transfer” substrates among multiple storage facilities and processing modules may be referred to as a “cluster tool architecture” system. Airlock 730, also known as a loadlock or transfer module, is shown in VTM 738 with four processing modules 720a–720d, which may be individual optimized to perform various fabrication processes. By way of example, processing modules 720a–720d may be implemented to perform substrate etching, deposition, ion implantation, substrate cleaning, sputtering, and/or other semiconductor processes as well as laser metrology and other defect detection and defect identification methods. One or more of the processing modules (any of 720a–720d) may be implemented as disclosed herein, i.e., for etching recessed features into substrates, depositing protective films on sidewalls of recessed features, and other suitable functions in accordance with the disclosed embodiments. Airlock 730 and process

modules 720a-720d may be referred to as “stations.” Each station has a facet 736 that interfaces the station to VTM 738. Inside the facets, sensors 1–18 are used to detect the passing of substrate 726 when moved between respective stations.

[0129] Robot 722 transfers substrates between stations. In one implementation, the robot may have one arm, and in another implementation, the robot may have two arms, where each arm has an end effector 724 to pick substrates for transport. Front-end robot 732, in atmospheric transfer module (ATM) 740, may be used to transfer substrates from cassette or Front Opening Unified Pod (FOUP) 734 in Load Port Module (LPM) 742 to airlock 730. Module center 728 inside process modules 720a–720d may be one location for placing the substrate. Aligner 744 in ATM 740 may be used to align substrates.

[0130] In an exemplary processing method, a substrate is placed in one of the FOUPs 734 in the LPM 742. Front-end robot 732 transfers the substrate from the FOUP 734 to the aligner 744, which allows the substrate 726 to be properly centered before it is etched, or deposited upon, or otherwise processed. After being aligned, the substrate is moved by the front-end robot 732 into an airlock 730. Because airlock modules have the ability to match the environment between an ATM and a VTM, the substrate is able to move between the two pressure environments without being damaged. From the airlock module 730, the substrate is moved by robot 722 through VTM 738 and into one of the process modules 720a–720d, for example process module 720a. In order to achieve this substrate movement, the robot 722 uses end effectors 724 on each of its arms. In process module 720a, the substrate undergoes etching as described herein to form a partially etched feature. Next, the robot 722 moves the substrate out of processing module 720a, into the VTM 738, and then into a different processing module 720b. In processing module 720b, a protective film is deposited on sidewalls of the partially etched feature. Then, the robot 722 moves the substrate out of processing module 720b, into the VTM 738, and into processing module 720a, where the partially etched feature is further etched. The etching/deposition can be repeated until the feature is fully etched.

[0131] It should be noted that the computer controlling the substrate movement can be local to the cluster architecture, or can be located external to the cluster architecture in the manufacturing floor, or in a remote location and connected to the cluster architecture via a network.

[0132] Lithographic patterning of a film typically comprises some or all of the following operations, each operation enabled with a number of possible tools: (1) application of photoresist on a workpiece, e.g., a substrate having a silicon nitride film formed thereon, using a spin-on or spray-on tool; (2) curing of photoresist using a hot plate or furnace or other suitable curing tool; 5 (3) exposing the photoresist to visible or UV or x-ray light with a tool such as a wafer stepper; (4) developing the resist so as to selectively remove resist and thereby pattern it using a tool such as a wet bench or a spray developer; (5) transferring the resist pattern into an underlying film or workpiece by using a dry or plasma-assisted etching tool; and (6) removing the resist using a tool such as an RF or microwave plasma resist stripper. In some embodiments, an ashable hard mask 10 layer (such as an amorphous carbon layer) and another suitable hard mask (such as an antireflective layer) may be deposited prior to applying the photoresist.

[0133] It is to be understood that the configurations and/or approaches described herein are exemplary in nature, and that these specific embodiments or examples are not to be considered in a limiting sense, because numerous variations are possible. The specific routines or methods 15 described herein may represent one or more of any number of processing strategies. As such, various acts illustrated may be performed in the sequence illustrated, in other sequences, in parallel, or in some cases omitted. Likewise, the order of the above described processes may be changed.

[0134] The subject matter of the present disclosure includes all novel and nonobvious 20 combinations and sub-combinations of the various processes, systems and configurations, and other features, functions, acts, and/or properties disclosed herein, as well as any and all equivalents thereof.

CLAIMS

What is claimed is:

1. A method of forming an etched feature in a stack comprising a dielectric material on a semiconductor substrate, the method comprising:
 - (a) generating a first plasma comprising an etching reactant, exposing the substrate to the first plasma, and partially etching the feature in the stack;
 - (b) after (a), depositing a protective film on sidewalls of the feature by
 - (i) exposing the substrate to a first reactant and allowing the first reactant to adsorb onto the substrate, wherein the first reactant comprises an aldehyde functional group;
 - (ii) exposing the substrate to a second reactant, and wherein the first and second reactants react with one another to form the protective film, and
 - (iii) repeating (i) and (ii) in a cyclic manner until the protective film reaches a target thickness, wherein the protective film is an organic polymeric film; and
 - (c) repeating (a) and (b) until the feature is etched to a final depth, wherein the protective film deposited in (b) substantially prevents lateral etch of the feature during (a), and wherein the feature has an aspect ratio of about 5 or greater at its final depth.
2. The method of claim 1, wherein the first reactant comprises a dialdehyde or trialdehyde.
3. The method of claim 2, wherein the first reactant comprises at least one of the following: succindialdehyde ($C_4H_6O_2$), glutaraldehyde ($C_5H_8O_2$), adipaldehyde ($C_6H_{10}O_2$), terephthalaldehyde ($C_8H_6O_2$), 1,4-benzenedicarboxaldehyde ($C_6H_4(CHO)_2$), ortho-phthalaldehyde ($C_8H_6O_2$), 1,2 benzenedicarboxaldehyde ($C_6H_4(CHO)_2$), and 2-methylglutaraldehyde ($C_6H_{10}O_2$).
4. The method of claim 1, wherein the second reactant comprises at least one of the following: diamine, a diol, a thiol, and a trifunctional compound.

5. The method of claim 4, wherein the second reactant comprises diamine.
6. The method of claim 4, wherein the second reactant comprises at least one of the following: 1,2-ethanediamine, 1,3-propanediamine, 1,4-butanediamine, ethylenediamine, m-xylylenediamine, isophoronediamine, 1,3-cyclohexanebis(methylamine), 1,4-bis(aminomethyl)cyclohexane, 4,4'-methylenebis(2-methylcyclohexylamine), 4,4'-methylenebis(cyclohexylamine), m-phenylenediamine, p-phenylenediamine, 4-aminobenzylamine, 3-aminobenzylamine, 4-(2-aminoethyl)aniline, p-xylylenediamine, m-xylylenediamine, ethylene glycol, 1,3-propanediol, 1,4-butanediol, 1,2-ethanedithiol, 1,3-propanedithiol, 1,4-butanedithiol, ($\pm$)-3-amino-1,2-propanediol, glycerol,
- 10 bis(hexamethylene)triamine, melamine, diethylenetriamine, ($\pm$)-1,2,4-butanetriol, cyanuric chloride, and trimethylaluminum.
7. The method of claim 1, wherein depositing the protective film in (b) is accomplished without exposing the substrate to plasma energy.
8. The method of claim 1, wherein the protective coating comprises a polythioacetal or a
- 15 polyazomethine.
9. The method of claim 1, wherein etching the feature in the stack in (a) is performed in a reaction chamber, and wherein depositing the protective film on the sidewalls of the feature in (b) is performed in the same reaction chamber.
10. The method of claim 1, wherein the etching reactant comprises one or more
- 20 fluorocarbons or hydrofluorocarbons.
11. The method of claim 1, wherein depositing the protective film in (b) occurs in a reaction chamber, and wherein depositing the protective film in (b) further comprises purging the reaction chamber at least once during each iteration of operation (b).
12. The method of claim 1, wherein the stack comprises alternating layers of (i) a silicon
- 25 oxide material, and (ii) a silicon nitride material or polysilicon material.
13. A method of forming an etched feature in a stack comprising a dielectric material on a semiconductor substrate, the method comprising:

(a) generating a first plasma comprising an etching reactant, exposing the substrate to the first plasma, and partially etching the feature in the stack;

(b) after (a), depositing a protective film on sidewalls of the feature by

(i) exposing the substrate to a first reactant and allowing the first reactant to adsorb onto
5 the substrate, wherein the first reactant comprises an isocyanate functional group;

(ii) exposing the substrate to a second reactant, and wherein the first and second reactants react with one another to form the protective film, and

(iii) repeating (i) and (ii) in a cyclic manner until the protective film reaches a target thickness, wherein the protective film is an organic polymeric film; and

10 (c) repeating (a) and (b) until the feature is etched to a final depth, wherein the protective film deposited in (b) substantially prevents lateral etch of the feature during (a), and wherein the feature has an aspect ratio of about 5 or greater at its final depth.

14. The method of claim 13, wherein the first reactant comprises diisocyanate.

15 15. The method of claim 14, wherein the diisocyanate comprises at least one of the following: tolylene-2,4-diisocyanate, 1,3-bis(isocyanatomethyl)cyclohexane, hexamethylene diisocyanate, m-xylylene diisocyanate, 1,3-bis(1-isocyanato-1-methylethyl)benzene, isophorone diisocyanate, diphenylmethane 4,4'-diisocyanate, 4,4'-methylenebis(cyclohexyl isocyanate), tolylene-2,6-diisocyanate, 1,4-phenylene diisocyanate, 1,3-phenylene diisocyanate, and 3,3'-dimethyl-4,4'-biphenylene diisocyanate.

20 16. The method of claim 13, wherein the second reactant comprises at least one of the following: a diamine, a diol, a thiol, and a trifunctional compound.

17. The method of claim 16, wherein the second reactant comprises diamine.

25 18. The method of claim 17, wherein the diamine comprises at least one of the following: 1,2-ethanediamine, 1,3-propanediamine, 1,4-butanediamine, ethylenediamine, m-xylylenediamine, isophoronediamine, 1,3-cyclohexanebis(methylamine), 1,4-

bis(aminomethyl)cyclohexane, 4,4'-methylenebis(2-methylcyclohexylamine), 4,4'-methylenebis(cyclohexylamine), m-phenylenediamine, p-phenylenediamine, 4-aminobenzylamine, 3-aminobenzylamine, 4-(2-aminoethyl)aniline, p-xylylenediamine, and m-xylylenediamine.

- 5 19. The method of claim 13, wherein depositing the protective film in (b) is accomplished without exposing the substrate to plasma energy.
20. The method of claim 13, wherein the protective coating comprises a polyurea or a polyurethane.
21. The method of claim 13, wherein depositing the protective film in (b) occurs in a reaction
10 chamber, and wherein depositing the protective film in (b) further comprises purging the reaction chamber at least once during each iteration of operation (b).
22. The method of claim 13, wherein the stack comprises alternating layers of (i) a silicon oxide material, and (ii) a silicon nitride material or polysilicon material.

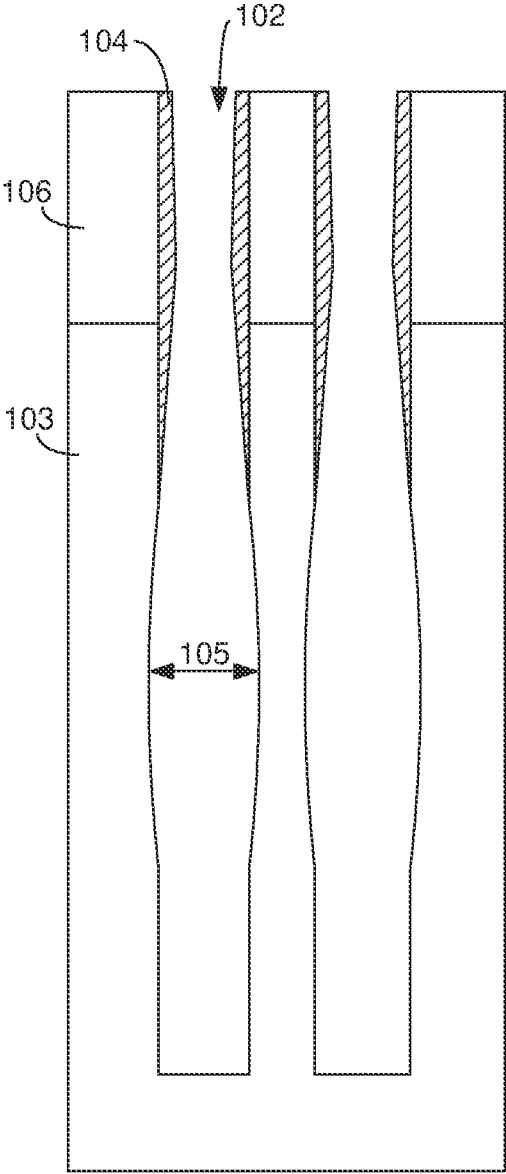


FIG. 1

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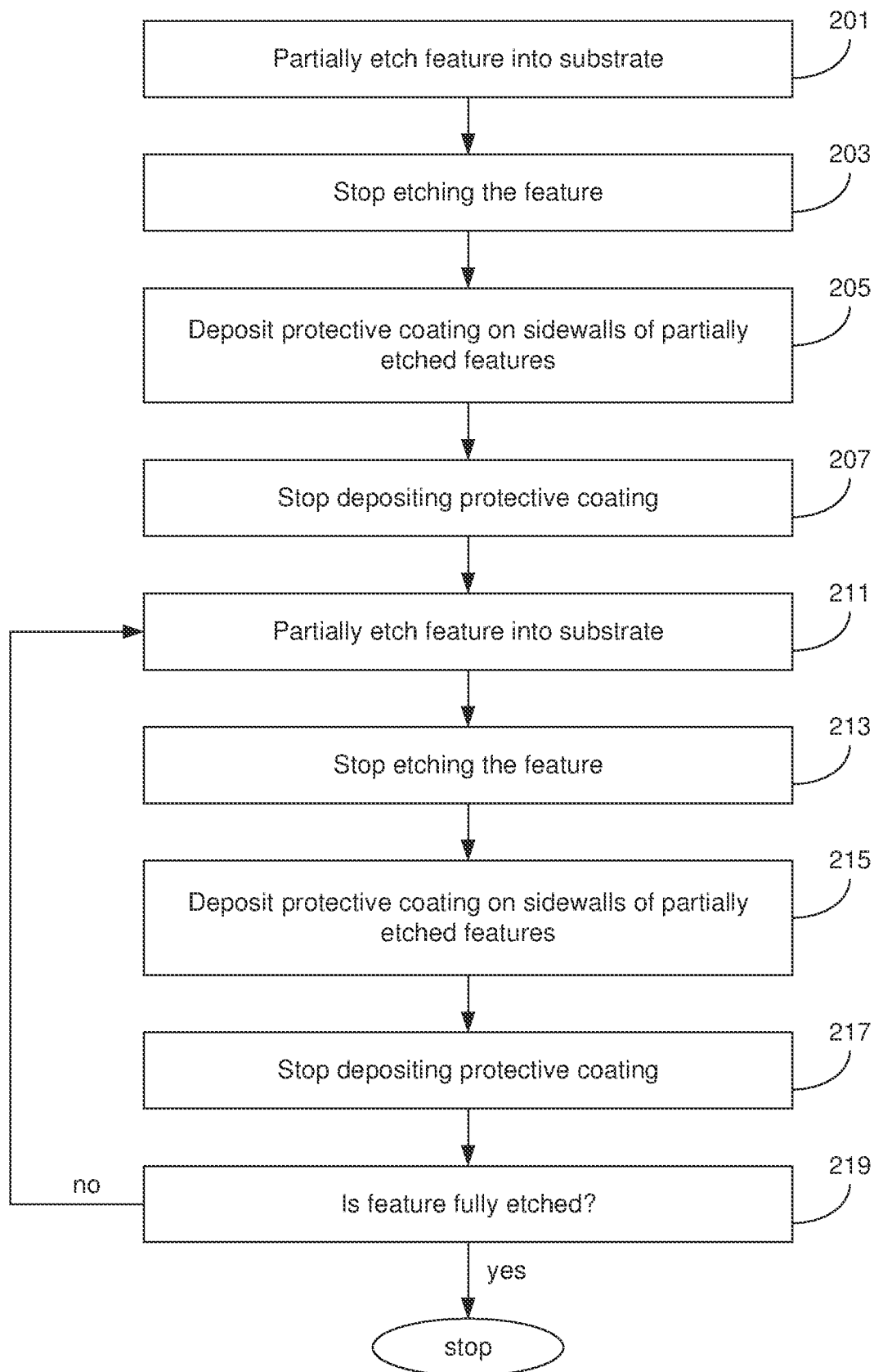


FIG. 2A

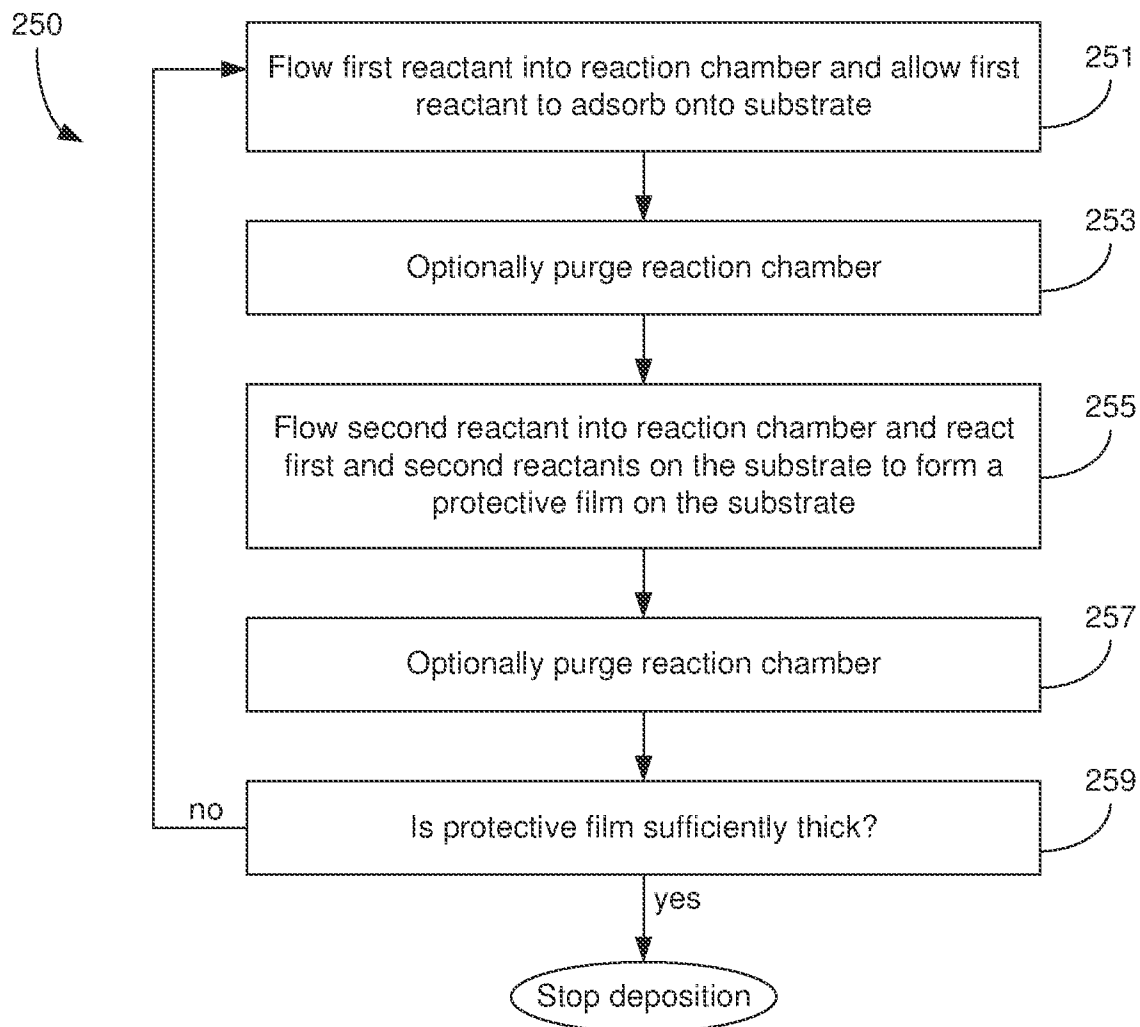


FIG. 2B

4/12

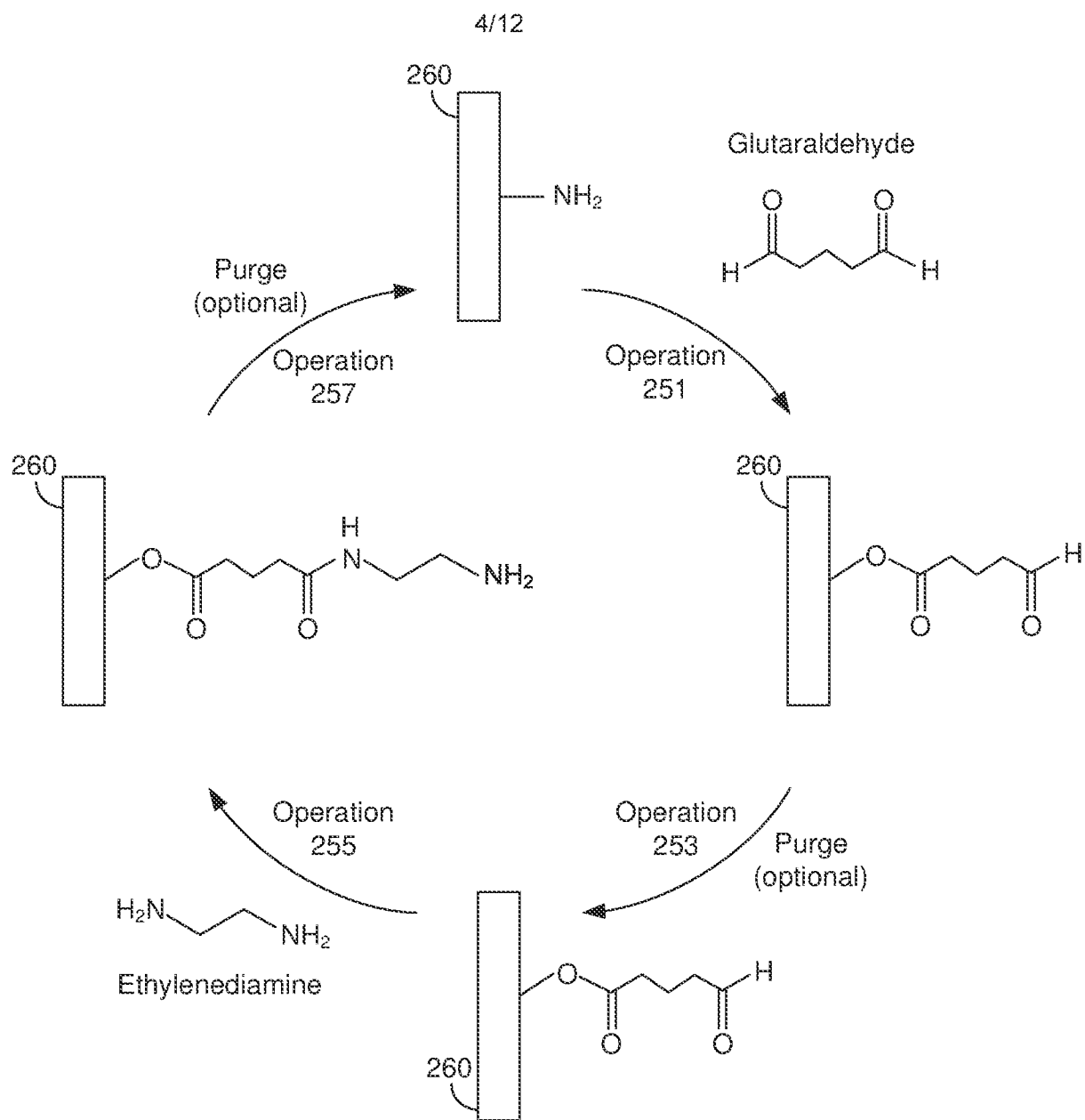


FIG. 2C

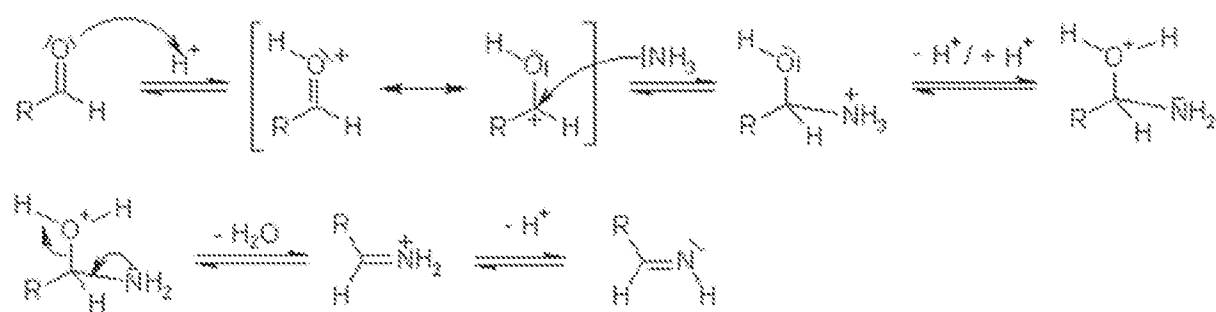


FIG. 2D

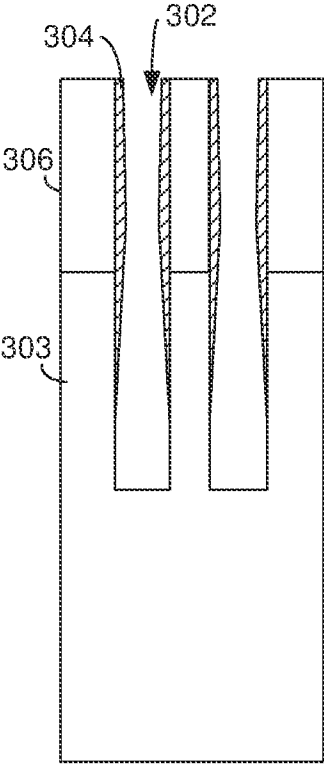


FIG. 3A

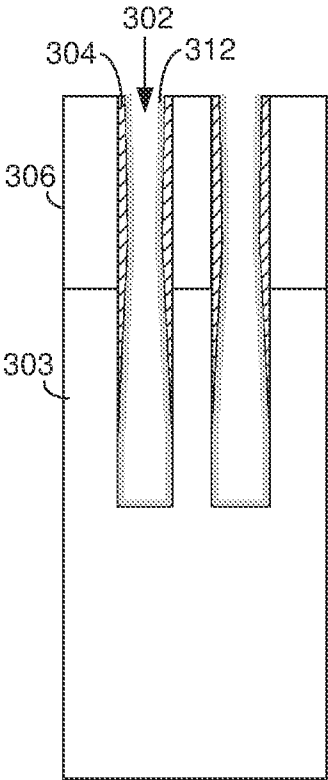


FIG. 3B

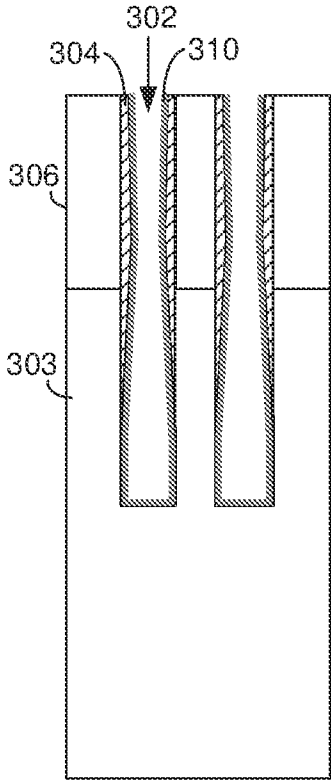


FIG. 3C

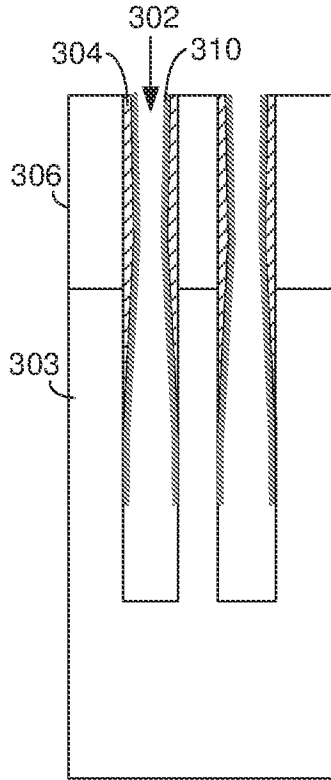


FIG. 3D

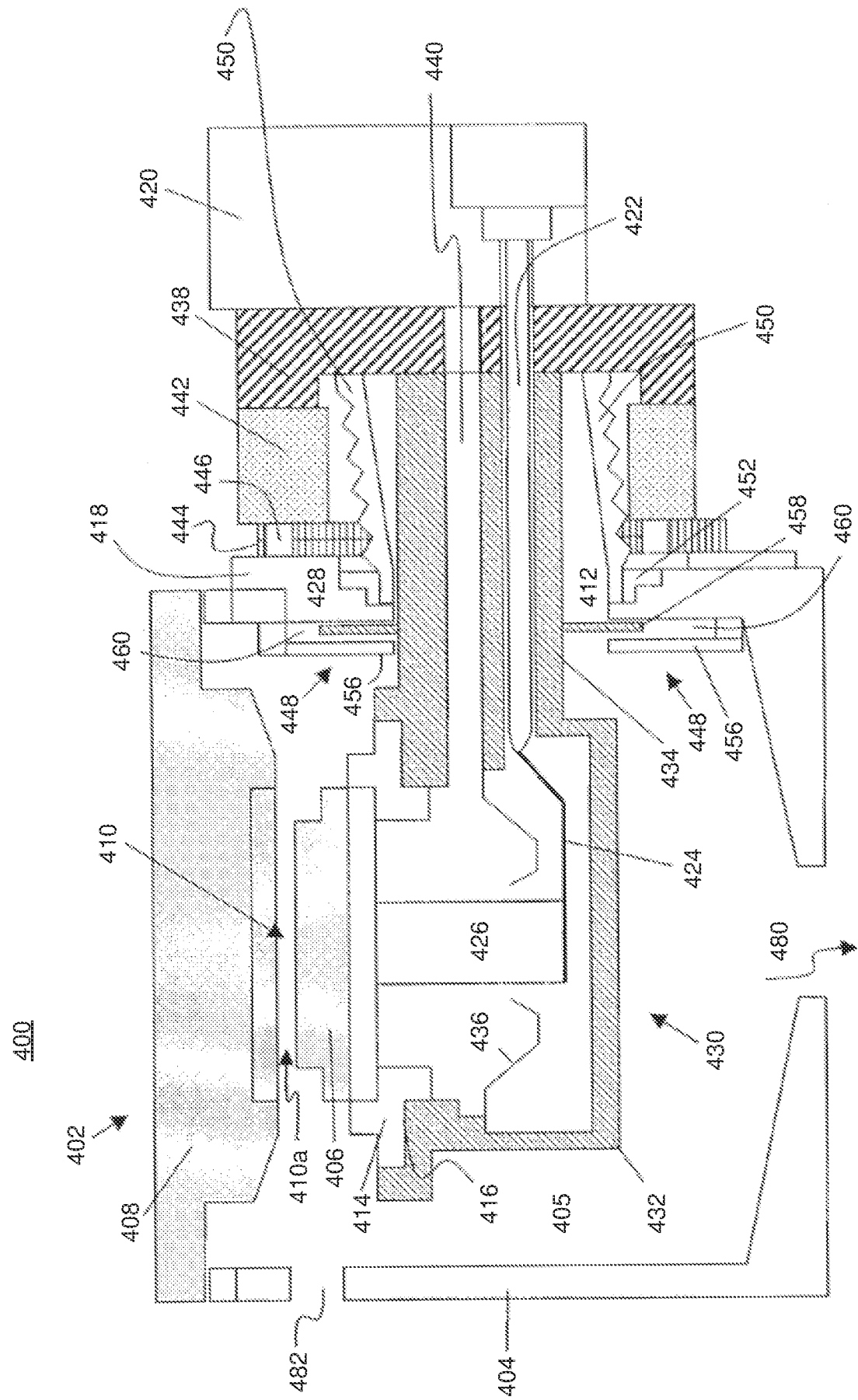


FIG. 4A

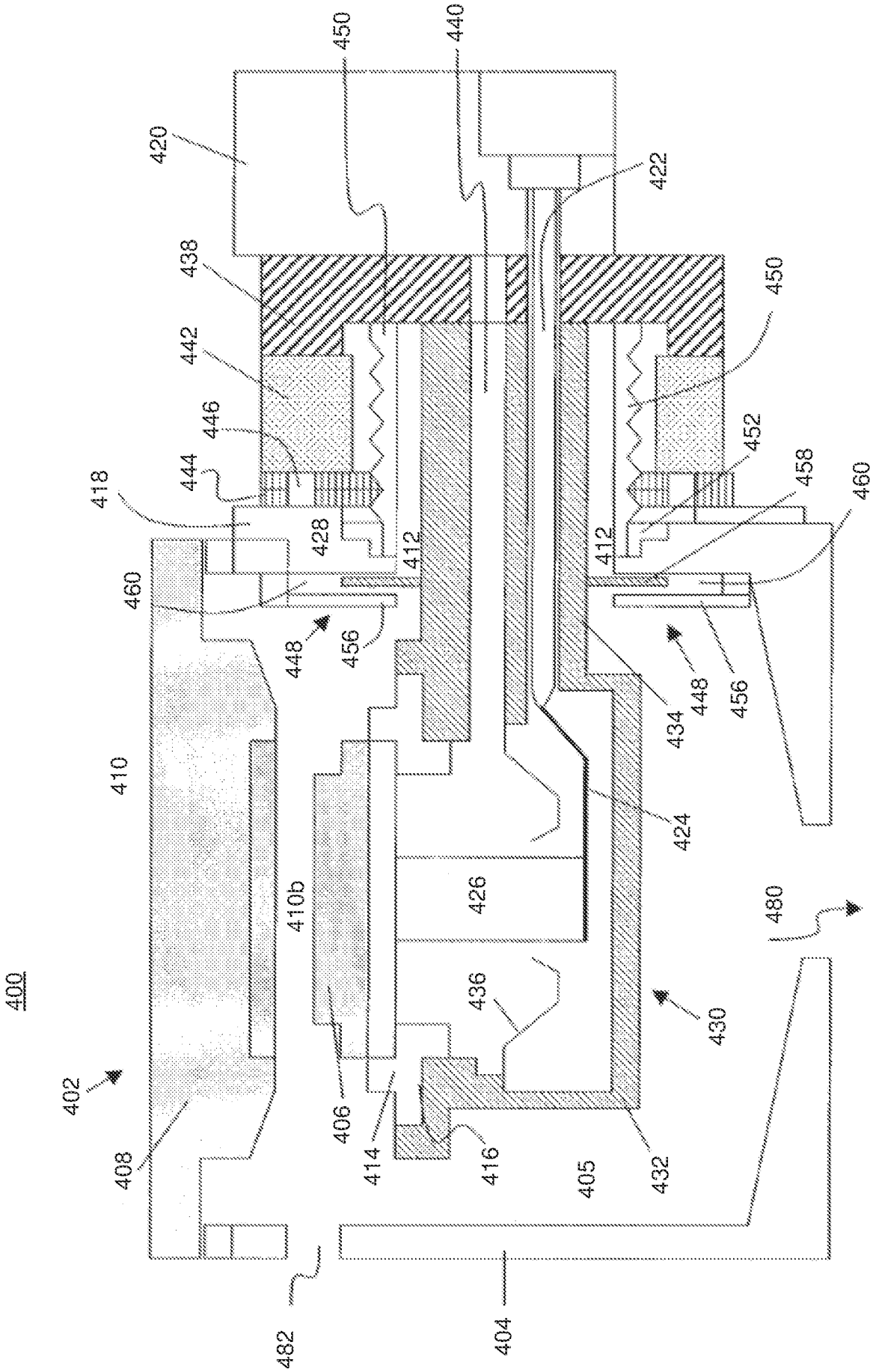


FIG. 4B

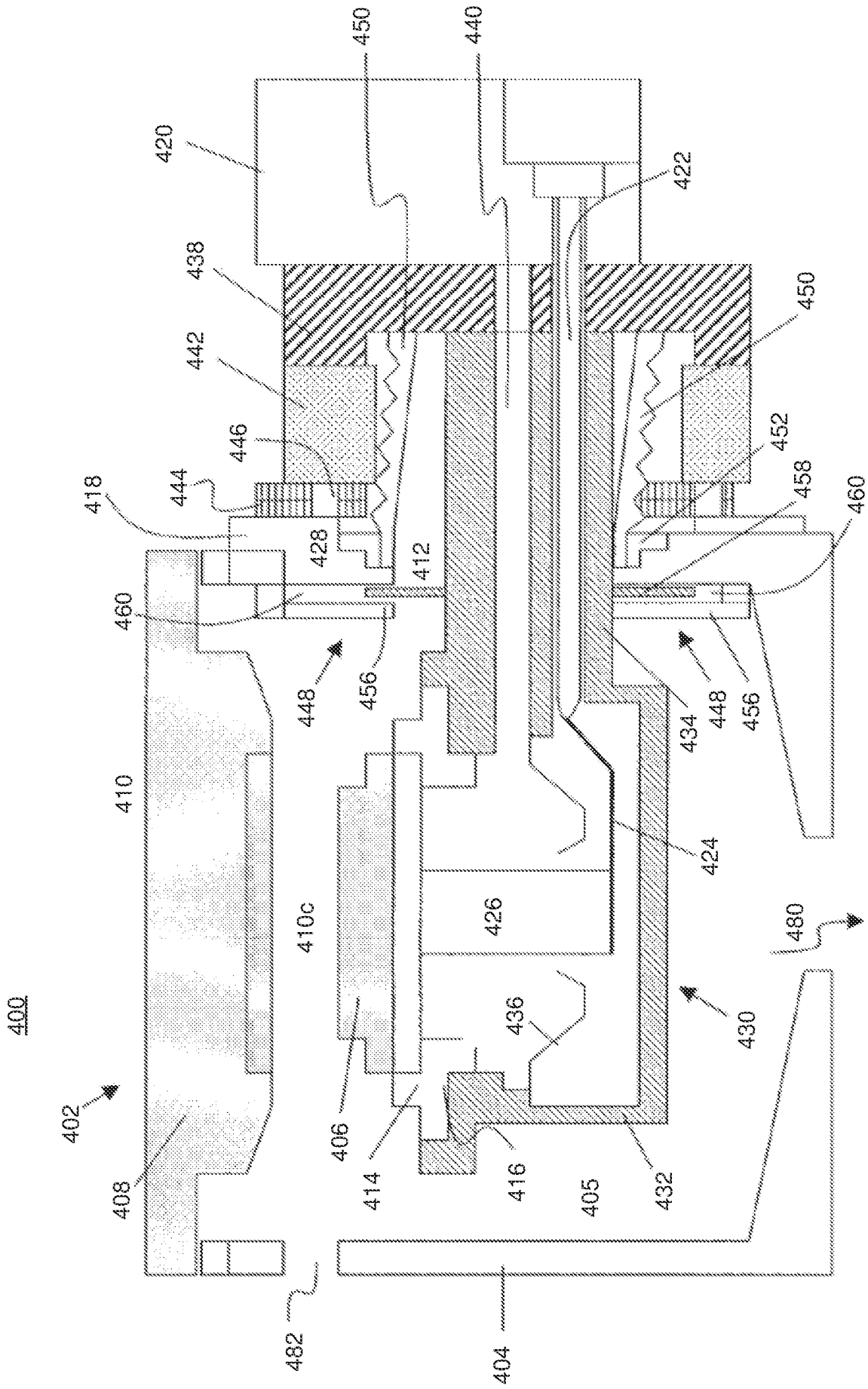


FIG. 4C

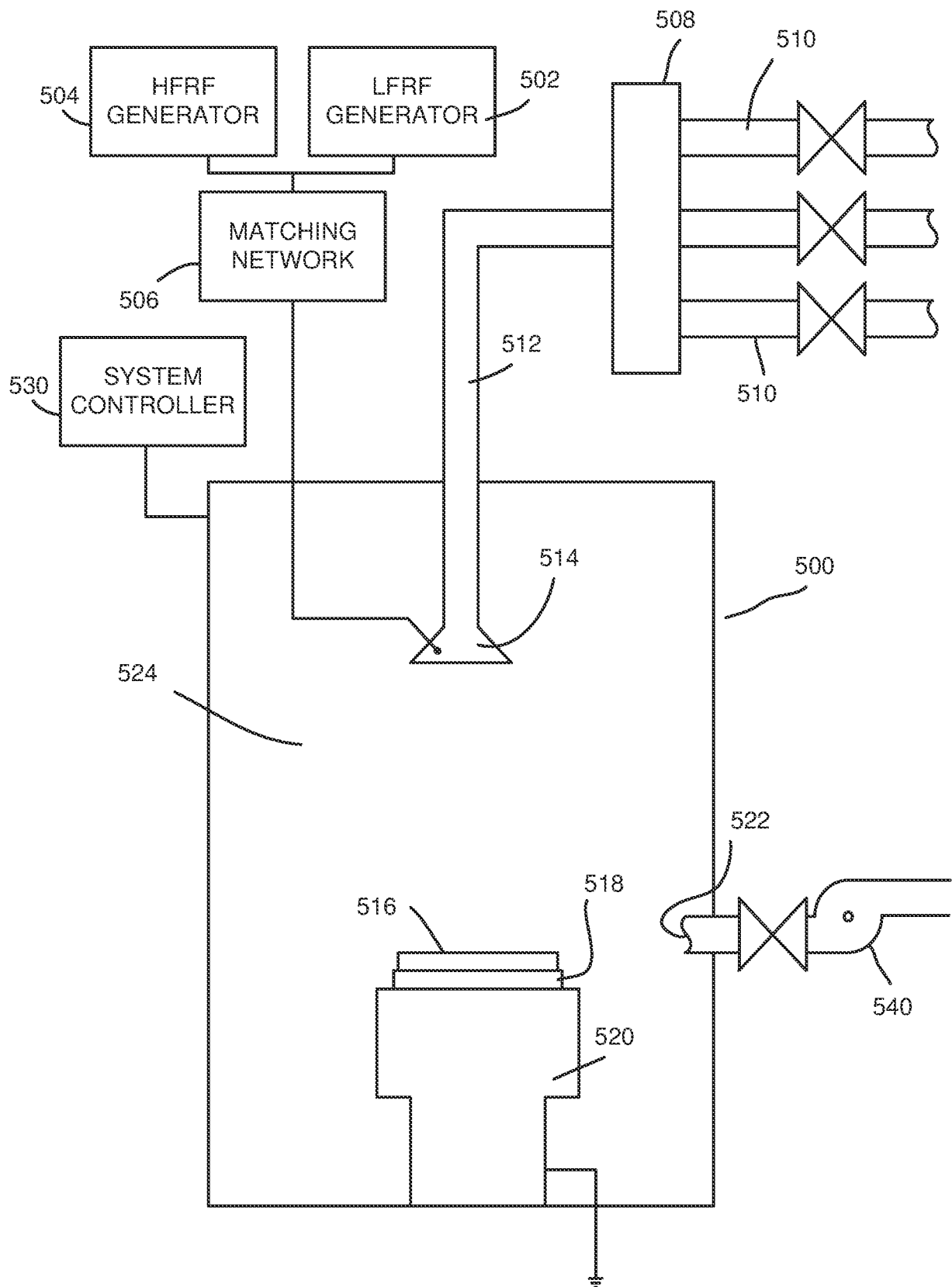


FIG. 5

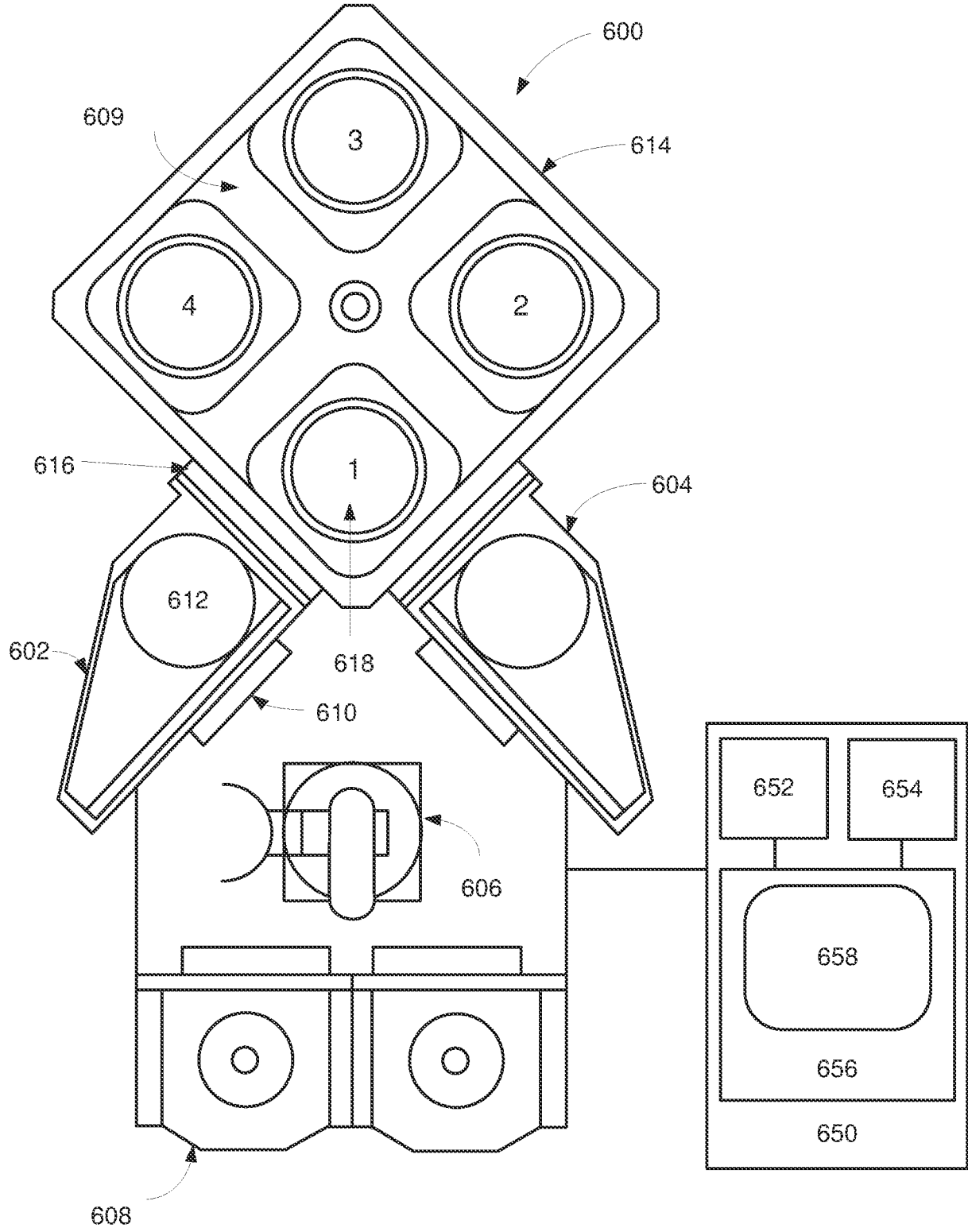


FIG. 6

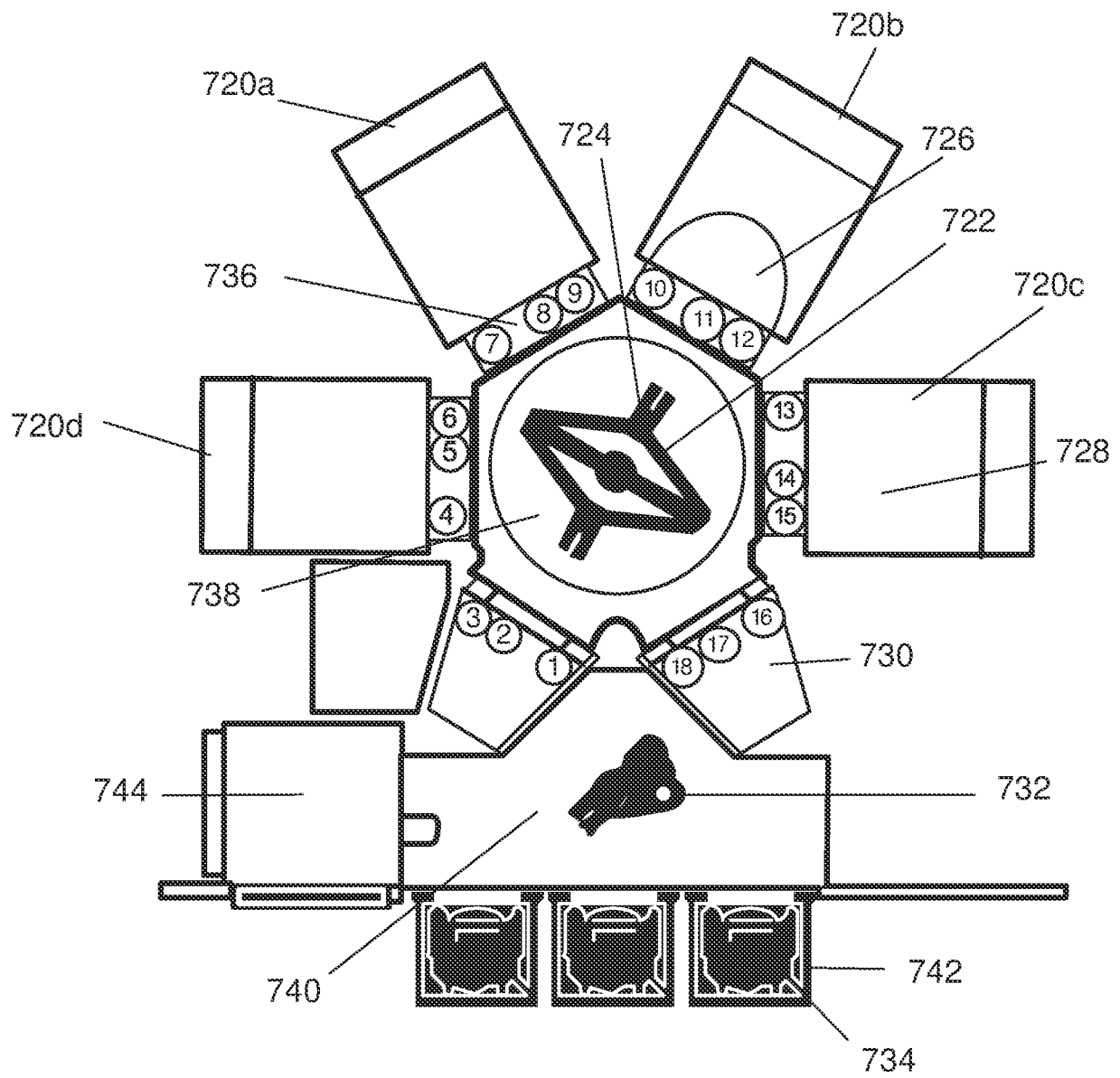


FIG. 7

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US2023/015028

A. CLASSIFICATION OF SUBJECT MATTER

H01L 21/311(2006.01)i; **H01L 21/3065**(2006.01)i; **C23C 16/04**(2006.01)i; **C23C 16/50**(2006.01)i; **C23C 16/52**(2006.01)i;
H01J 37/32(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 21/311(2006.01); C23C 16/04(2006.01); H01J 37/32(2006.01); H01L 21/02(2006.01); H01L 29/51(2006.01);
H01L 29/66(2006.01)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: etched feature, stack, reactant, aldehyde functional group, isocyanate functional group

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2018-0174858 A1 (LAM RESEARCH CORPORATION) 21 June 2018 (2018-06-21) See paragraph [0039] and claims 1-19.	1-22
Y	WO 2021-076746 A1 (LAM RESEARCH CORPORATION) 22 April 2021 (2021-04-22) See paragraphs [0077], [0082].	1-12
Y	US 2021-0082713 A1 (TOKYO ELECTRON LIMITED) 18 March 2021 (2021-03-18) See paragraphs [0071], [0102], [0155]-[0163] and figures 1, 9.	13-22
A	US 2021-0098263 A1 (TOKYO ELECTRON LIMITED) 01 April 2021 (2021-04-01) See paragraphs [0041]-[0228] and figures 1-14.	1-22
A	US 2015-0091075 A1 (KABUSHIKI KAISHA TOSHIBA) 02 April 2015 (2015-04-02) See paragraphs [0030]-[0041] and figures 2A-2F.	1-22

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:

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“X” document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

“Y” document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

“&” document member of the same patent family

Date of the actual completion of the international search

03 July 2023

Date of mailing of the international search report

03 July 2023

Name and mailing address of the ISA/KR

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International application No.

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