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(54) Title: DATA RETENTION SECONDARY VOLTAGE REGULATOR

(57) Abstract: An integrated circuit device has a primary voltage regulator and an ultra-low power secondary voltage regulator. The ultra-low power secondary voltage regulator supplies voltage to certain circuits used for providing data retention and dynamic operation, e.g., a real time clock and calendar (RTCC) when the integrated circuit device is in a low power sleep mode. The primary voltage regulator provides power to these same certain circuits when the integrated circuit is in an operational mode.

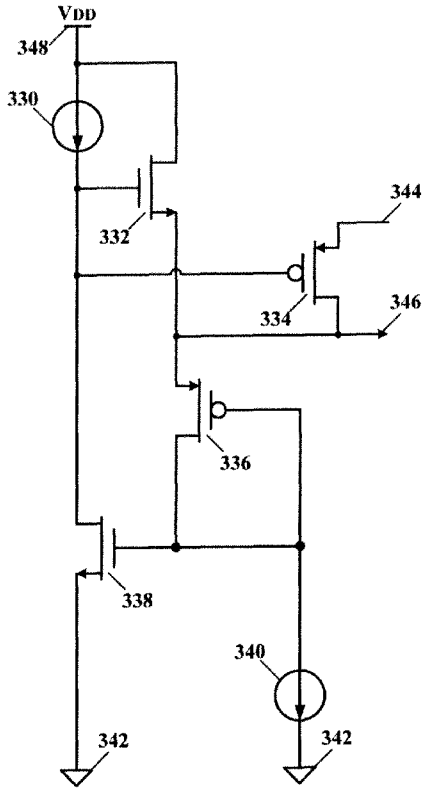

FIGURE 3

WO 2010/144557 A1

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DATA RETENTION SECONDARY VOLTAGE REGULATOR

This application claims priority to commonly owned United States Provisional Patent Applications Serial Number 61/185,627; filed June 10, 2009; entitled "Data Retention Secondary Voltage Regulator," by D.C. Sessions, and is hereby incorporated by reference herein for all purposes.

TECHNICAL FIELD

The present disclosure relates to integrated circuit device voltage regulation, and, more particularly, to a low power secondary voltage regulator in parallel with and functions when a primary voltage regulator is off. The secondary voltage regulator may be used when the integrated circuit device is in a sleep mode and a regulated voltage is needed for circuits that are used to retain information that will be needed when the integrated circuit device returns to an operational mode.

BACKGROUND

Power must be supplied with minimal power consumption to circuits that retain and/or operate on data when an integrated circuit device is in a sleep mode. These circuits are powered so as to retain the data when other circuits of the integrated circuit device are in a low power sleep mode. In addition, minimal dynamic power may be supplied to circuits that operate on data during the sleep mode, *e.g.*, a real time clock and calendar (RTCC), at minimum power consumption.

A primary voltage regulator having precision voltage regulation, *e.g.*, a bandgap voltage reference and associated voltage regulator circuits, requires a significant amount of power that is not desirable when battery operated devices go into a low power sleep mode yet still have to maintain voltage(s) on some circuits in order to retain/operate on data.

SUMMARY

What is needed is a way to supply necessary regulated voltage(s) to those circuits in an integrated circuit device requiring power for data retention and/or minimal dynamic power for continuous operation such as, for example but not limited to, a real time clock and calendar (RTCC) when other circuits of the integrated circuit device are in a sleep mode.

According to a specific example embodiment of this disclosure, a low power voltage regulator for supplying operating voltage to circuits required to maintain data and/or be operational during an integrated circuit device low power sleep mode comprises: a first constant current source connected to a supply voltage source; a first N-channel field effect transistor (FET) having a source, a drain and a gate, wherein the drain of the first N-channel FET is connected to the supply voltage, the gate of the first N-channel FET is connected to the first constant current source and the first constant current source is connected between the gate and drain of the first N-channel FET; a second N-channel FET having a source, a drain and a gate, wherein the drain of the second N-channel FET is connected to the gate of the first N-channel FET and the first constant current source, and the source of the second N-channel FET is connected to a supply voltage common; a second constant current source connected to the supply voltage common and the gate of the second N-channel FET; a first P-channel FET having a source, a drain and a gate, wherein the drain and gate of the first P-channel FET are connected to the gate of the second N-channel FET and the second constant current source, and the source of the first P-channel FET is connected to the source of the first N-channel FET; the first and second N-Channel FETs, the first P-channel FET and the first and second constant current sources comprise a low power secondary voltage regulator having an output, wherein the output is the connected sources of the first P-channel FET and the first N-channel FET; and a maintained voltage core logic of an integrated circuit device connected to the output of the low power secondary voltage regulator. The low power voltage regulator may further comprise: a second P-channel FET having a source, a drain and a gate, wherein the drain of the second P-channel FET is connected to the sources of the first N-channel and first P-channel FETs, the gate of the second P-channel FET is connected to the drain of the second N-channel FET and the first constant current source, and the source of the second P-channel FET is connected to an output from a primary voltage regulator; wherein the maintained voltage core logic is coupled to and receives its operating voltage from the primary voltage regulator through the second P-channel FET when the integrated circuit device is in an operational mode; and wherein the maintained voltage core logic receives its operating voltage from the output of the low power secondary voltage regulator when the integrated circuit device is in a low power standby sleep mode.

According to another specific example embodiment of this disclosure, a low power voltage regulator for supplying back-up voltage to circuits required to maintain data and/or be operational during an integrated circuit device low power sleep mode comprises: a first constant current source connected to a supply voltage source; a first N-channel field effect transistor (FET) having a source, a drain and a gate, wherein the drain of the first N-channel FET is connected to the supply voltage, the gate of the first N-channel FET is connected to the first constant current source and the first constant current source is connected between the gate and drain of the first N-channel FET; a second N-channel FET having a source, a drain and a gate, wherein the drain of the second N-channel FET is connected to the gate of the first N-channel FET and the first constant current source, and the source of the second N-channel FET is connected to a supply voltage common; a second constant current source connected to the supply voltage common and the gate of the second N-channel FET; a first P-channel FET having a source, a drain and a gate, wherein the drain and gate of the first P-channel FET are connected to the gate of the second N-channel FET and the second constant current source, and the source of the first P-channel FET is connected to the source of the first N-channel FET; a second P-channel FET having a source, a drain and a gate, wherein the drain of the second P-channel FET is connected to the sources of the first N-channel and first P-channel FETs, the gate of the second P-channel FET is connected to the drain of the second N-channel FET and the first constant current source, and the source of the second P-channel FET is connected to an output from a primary voltage regulator; the first and second N-Channel FETs, the first P-channel FET and the first and second constant current sources comprise a low power secondary voltage regulator having an output, the output is the connected sources of the first P-channel FET and the first N-channel FET; and a maintained voltage core logic of an integrated circuit device, wherein the maintained voltage core logic is coupled to and receives its operating voltage from the primary voltage regulator through the second P-channel FET when the integrated circuit device is in an operational mode; and the maintained voltage core logic receives its operating voltage from the output of the low power secondary voltage regulator when the integrated circuit device is in a low power standby sleep mode.

According to yet another specific example embodiment of this disclosure, a low power voltage regulator for supplying operating voltage to circuits required to maintain data and/or be

operational during an integrated circuit device low power sleep mode, comprises: an amplifier having a non-inverting input, an inverting input, and an output; an N-channel field effect transistor (FET) having a source, a drain and a gate, wherein the drain of the N-channel FET is connected to a supply voltage source, and the gate of the N-channel FET is connected to the output of the amplifier; the non-inverting input of the amplifier is connected to a voltage approximately equal to a threshold voltage of the N-channel FET; a constant current source connected to a supply voltage common; a first P-channel FET having a source, a drain and a gate, wherein the drain and gate of the first P-channel FET are connected to the inverting input of the amplifier and the constant current source, and the source of the first P-channel FET is connected to the source of the N-channel FET; the amplifier, the N-Channel FET, the first P-channel FET, and the constant current source comprise a low power secondary voltage regulator having an output, wherein the output is the connected sources of the first P-channel FET and the N-channel FET; and a maintained voltage core logic of an integrated circuit device connected to the output of the low power secondary voltage regulator. The low power voltage regulator may further comprise: a second P-channel FET having a source, a drain and a gate, wherein the drain of the second P-channel FET is connected to the sources of the N-channel and first P-channel FETs, the gate of the second P-channel FET is connected to the output of the amplifier and the gate of the N-channel FET, and the source of the second P-channel FET is connected to an output from a primary voltage regulator; wherein the maintained voltage core logic is coupled to and receives its operating voltage from the primary voltage regulator through the second P-channel FET when the integrated circuit device is in an operational mode; and wherein the maintained voltage core logic receives its operating voltage from the output of the low power secondary voltage regulator when the integrated circuit device is in a low power standby sleep mode.

According to still another specific example embodiment of this disclosure, a low power voltage regulator for supplying back-up voltage to circuits required to maintain data and/or be operational during an integrated circuit device low power sleep mode comprises: an amplifier having a non-inverting input, an inverting input, and an output; a N-channel field effect transistor (FET) having a source, a drain and a gate, wherein the drain of the N-channel FET is connected to a supply voltage source, the gate of the N-channel FET is connected to the first constant current source and the first constant current source is connected to the

output of the amplifier; the non-inverting input of the amplifier is connected to a voltage approximately equal to a threshold voltage of the N-channel FET; a constant current source connected to a supply voltage common; a first P-channel FET having a source, a drain and a gate, wherein the drain and gate of the first P-channel FET are connected to the inverting input of the amplifier and the constant current source, and the source of the first P-channel FET is connected to the source of the N-channel FET; the amplifier, the N-Channel FET, the first P-channel FET, and the constant current source comprise a low power secondary voltage regulator having an output, wherein the output is the connected sources of the first P-channel FET and the N-channel FET; a maintained voltage core logic of an integrated circuit device connected to the output of the low power secondary voltage regulator; and a second P-channel FET having a source, a drain and a gate, wherein the drain of the second P-channel FET is connected to the sources of the N-channel and first P-channel FETs, the gate of the second P-channel FET is connected to the output of the amplifier and the gate of the N-channel FET, and the source of the second P-channel FET is connected to an output from a primary voltage regulator; wherein the maintained voltage core logic is coupled to and receives its operating voltage from the primary voltage regulator through the second P-channel FET when the integrated circuit device is in an operational mode; and wherein the maintained voltage core logic receives its operating voltage from the output of the low power secondary voltage regulator when the integrated circuit device is in a low power standby sleep mode.

BRIEF DESCRIPTION OF THE DRAWINGS

A more complete understanding of the present disclosure thereof may be acquired by referring to the following description taken in conjunction with the accompanying drawings wherein:

Figure 1 illustrates a schematic block diagram of an integrated circuit device having a primary voltage regulator and an ultra-low power secondary voltage regulator for providing data retention and dynamic power for continuous operation of certain circuits when the integrated circuit device is in a low power sleep mode, according to the teachings of this disclosure;

Figure 2 illustrates a schematic block diagram of an integrated circuit device having a primary voltage regulator and an ultra-low power secondary voltage regulator connected to independent voltage sources and providing for data retention and dynamic power for continuous operation of certain circuits when the integrated circuit device is in a low power sleep mode, according to the teachings of this disclosure;

Figure 3 illustrates a schematic diagram of an ultra-low power secondary voltage regulator of Figures 1 and 2, according to a specific example embodiment of this disclosure; and

Figure 4 illustrates a schematic diagram of an ultra-low power secondary voltage regulator of Figures 1 and 2, according to another specific example embodiment of this disclosure.

While the present disclosure is susceptible to various modifications and alternative forms, specific example embodiments thereof have been shown in the drawings and are herein described in detail. It should be understood, however, that the description herein of specific example embodiments is not intended to limit the disclosure to the particular forms disclosed herein, but on the contrary, this disclosure is to cover all modifications and equivalents as defined by the appended claims.

DETAILED DESCRIPTION

Referring now to the drawing, the details of specific example embodiments are schematically illustrated. Like elements in the drawings will be represented by like numbers, and similar elements will be represented by like numbers with a different lower case letter suffix.

Referring to Figure 1, depicted is a schematic block diagram of an integrated circuit device having a primary voltage regulator and an ultra-low power secondary voltage regulator for providing data retention and dynamic power for continuous operation of certain circuits when the integrated circuit device is in a low power sleep mode, according to the teachings of this disclosure. An integrated circuit device 100 comprises digital logic 108 (and possibly analog circuits *e.g.*, a mixed signal device), core logic 106 that remains active

even when the integrated circuit device 100 is in a low power sleep mode, a primary voltage regulator 102, and an ultra-low power secondary voltage regulator 104.

Both voltage regulators 102 and 104 are powered from an external power source, VDD, connected at node 110, *e.g.*, a battery. When the integrated circuit device 100 is in an operational mode the primary voltage regulator 102 supplies operating voltage to the core logic 106 among other circuits within the device 100. However, when the integrated circuit device 100 goes into a low power sleep mode most current consuming logic circuits and the primary voltage regulator 102 generally will be inhibited (shutdown) so as to substantially reduce current consumption within the device 100. The core logic 106 (*e.g.*, back-up domain) must remain operational during the low sleep mode of the device 100, *e.g.*, a real time clock and calendar (RTCC), *etc.*

External connection nodes of the integrated circuit device 100 may be for example but are not limited to a supply voltage node 110, VDD, a supply common node 116, Vss, and a regulator stabilization capacitor node 112.

Referring to Figure 2, depicted is a schematic block diagram of an integrated circuit device having a primary voltage regulator and an ultra-low power secondary voltage regulator connected to independent voltage sources and providing for data retention and dynamic power for continuous operation of certain circuits when the integrated circuit device is in a low power sleep mode, according to the teachings of this disclosure. An integrated circuit device 200 comprises digital logic 108 (and possibly analog circuits *e.g.*, a mixed signal device), core logic 106 that remains active even when the integrated circuit device 200 is in a low power sleep mode, a primary voltage regulator 102, and an ultra-low power secondary voltage regulator 104.

Voltage regulator 102 is powered from a first external power source, VDD-1, and voltage regulator 104 is powered from a second external power source, VDD-2, *e.g.*, a battery. When the integrated circuit device 200 is in an operational mode the primary voltage regulator 102 supplies operating voltage to the core logic 106 among other circuits within the device 200. However, when the integrated circuit device 200 goes into a low power sleep mode most current consuming logic circuits and the primary voltage regulator 102 generally will be inhibited (shutdown) so as to substantially reduce current consumption within the

device 200. The core logic 106 (*e.g.*, back-up domain) must remain operational during the sleep mode of the device 200, *e.g.*, a real time clock and calendar (RTCC), *etc.*

External connection nodes of the integrated circuit device 100 may be for example but are not limited to a main supply voltage node 210, VDD-1, a secondary supply voltage node 211, VDD-2, a supply common node 116, Vss, and a regulator stabilization capacitor node 112.

Referring to Figure 3, depicted is a schematic diagram of an ultra-low power secondary voltage regulator of Figures 1 and 2, according to a specific example embodiment of this disclosure. A primary power source, VDD, is coupled at node 348 and an output node 346 is approximately the sum of the threshold voltages, Vt, of transistors 336 and 338. The drain current of transistor 338 equals the current supplied by a constant current source 330. This arrangement turns off transistor 334 and biases transistor 332 at a level sufficient to provide a required amount of current to the output node 346. The feedback from this closed-loop system maintains the output node 346 at the desired voltage operating point for the voltage maintained core logic 106.

When a voltage from the primary voltage regulator 102 is applied to node 344, transistor 334 passes current to the output node 346 and raises the gate of transistor 338 above its threshold. As a result, the drain of transistor 338 is pulled lower, turning off transistor 332 and turning transistor 334 on hard. The result is an ultra-low power standby voltage regulator 104 that provides state-retention power to the core logic 106 when no power is available from the normal operational primary voltage regulator 102, and optionally may use the voltage from the primary voltage regulator 102 when power from it becomes available. Transistors 332 and 338 may be N-channel insulated gate (IG) metal oxide semiconductor (MOS) field effect transistors (FETs), and transistors 334 and 336 may be P-channel IG MOS FETs.

Referring to Figure 4, depicted is a schematic diagram of an ultra-low power secondary voltage regulator of Figures 1 and 2, according to another specific example embodiment of this disclosure. A primary power source, VDD, is couple at node 348 and an output node 346 is approximately the sum of the threshold voltages, Vt, of transistors 436 and 432. An inverting amplifier 450 has a negative input connected to the drain and gate of

the transistor 436 and the current sink 440. A positive input of the inverting amplifier 450 is set to a voltage, V_{TN}, that is appropriate for the needs of the load. The output of the inverting amplifier 450 is connected to the gates of the transistors 432 and 434.

This arrangement turns off transistor 434 and biases transistor 432 at a level sufficient to provide a required amount of current to the output node 346. The feedback from this closed-loop system maintains the output node 346 at the desired voltage operating point for the voltage maintained core logic 106.

When a voltage from the primary voltage regulator 102 is applied to node 344, transistor 434 passes current to the output node 346 and raises the gate of transistor 432 above its threshold. As a result, the drain of transistor 432 is pulled lower, turning off transistor 432 and turning transistor 434 on hard. The result is an ultra-low power standby voltage regulator 104 that provides state-retention power to the core logic 106 when no power is available from the normal operational primary voltage regulator 102, and optionally may use the voltage from the primary voltage regulator 102 when power from it becomes available. Transistor 432 may be an N-channel insulated gate (IG) metal oxide semiconductor (MOS) field effect transistor (FET), and transistors 434 and 436 may be P-channel IG MOS FETs.

While embodiments of this disclosure have been depicted, described, and are defined by reference to example embodiments of the disclosure, such references do not imply a limitation on the disclosure, and no such limitation is to be inferred. The subject matter disclosed is capable of considerable modification, alteration, and equivalents in form and function, as will occur to those ordinarily skilled in the pertinent art and having the benefit of this disclosure. The depicted and described embodiments of this disclosure are examples only, and are not exhaustive of the scope of the disclosure.

CLAIMS

What is claimed is:

1. A low power voltage regulator for supplying operating voltage to circuits required to maintain data and/or be operational during an integrated circuit device low power sleep mode, comprising:

a first constant current source connected to a supply voltage source;

a first N-channel field effect transistor (FET) having a source, a drain and a gate,

wherein the drain of the first N-channel FET is connected to the supply voltage, the gate of the first N-channel FET is connected to the first constant current source and the first constant current source is connected between the gate and drain of the first N-channel FET;

a second N-channel FET having a source, a drain and a gate,

wherein the drain of the second N-channel FET is connected to the gate of the first N-channel FET and the first constant current source, and the source of the second N-channel FET is connected to a supply voltage common;

a second constant current source connected to the supply voltage common and the gate of the second N-channel FET;

a first P-channel FET having a source, a drain and a gate,

wherein the drain and gate of the first P-channel FET are connected to the gate of the second N-channel FET and the second constant current source, and the source of the first P-channel FET is connected to the source of the first N-channel FET;

the first and second N-Channel FETs, the first P-channel FET and the first and second constant current sources comprise a low power secondary voltage regulator having an output, wherein the output is the connected sources of the first P-channel FET and the first N-channel FET; and

a maintained voltage core logic of an integrated circuit device connected to the output of the low power secondary voltage regulator.

2. The low power voltage regulator according to claim 1, further comprising:

a second P-channel FET having a source, a drain and a gate,

wherein the drain of the second P-channel FET is connected to the sources of the first N-channel and first P-channel FETs, the gate of the second P-channel FET is connected to the drain of the second N-channel FET and the first constant current source, and the source of the second P-channel FET is connected to an output from a primary voltage regulator;

wherein the maintained voltage core logic is coupled to and receives its operating voltage from the primary voltage regulator through the second P-channel FET when the integrated circuit device is in an operational mode; and

wherein the maintained voltage core logic receives its operating voltage from the output of the low power secondary voltage regulator when the integrated circuit device is in a low power standby sleep mode.

3. The low power voltage regulator according to claim 1, wherein a voltage supplied to the maintained voltage core logic is a sum of threshold voltages of the first P-channel FET and the second N-channel FET.

4. The low power voltage regulator according to claim 2, wherein a voltage supplied to the maintained voltage core logic when the integrated circuit device is in the low power standby sleep mode is a sum of threshold voltages of the first P-channel FET and the second N-channel FET.

5. The low power voltage regulator according to claim 2, wherein current through the second N-channel FET is substantially equal to current from the first constant current source when the integrated circuit device is in the low power standby sleep mode and no voltage is being supplied from the primary voltage regulator.

6. The low power voltage regulator according to claim 5, wherein when no voltage is being supplied from the primary voltage regulator the second P-channel FET is turned off and the first N-channel FET supplies operating current to the maintained voltage core logic.

7. A low power voltage regulator for supplying back-up voltage to circuits required to maintain data and/or be operational during an integrated circuit device low power sleep mode, comprising:

a first constant current source connected to a supply voltage source;

a first N-channel field effect transistor (FET) having a source, a drain and a gate,

wherein the drain of the first N-channel FET is connected to the supply voltage, the gate of the first N-channel FET is connected to the first constant current source and the first constant current source is connected between the gate and drain of the first N-channel FET;

a second N-channel FET having a source, a drain and a gate,

wherein the drain of the second N-channel FET is connected to the gate of the first N-channel FET and the first constant current source, and the source of the second N-channel FET is connected to a supply voltage common;

a second constant current source connected to the supply voltage common and the gate of the second N-channel FET;

a first P-channel FET having a source, a drain and a gate,

wherein the drain and gate of the first P-channel FET are connected to the gate of the second N-channel FET and the second constant current source, and the source of the first P-channel FET is connected to the source of the first N-channel FET;

a second P-channel FET having a source, a drain and a gate,

wherein the drain of the second P-channel FET is connected to the sources of the first N-channel and first P-channel FETs, the gate of the second P-channel FET is connected to the drain of the second N-channel FET and the first constant current source, and the source of the second P-channel FET is connected to an output from a primary voltage regulator;

the first and second N-Channel FETs, the first P-channel FET and the first and second constant current sources comprise a low power secondary voltage regulator having an output, the output is the connected sources of the first P-channel FET and the first N-channel FET; and

a maintained voltage core logic of an integrated circuit device, wherein

the maintained voltage core logic is coupled to and receives its operating voltage from the primary voltage regulator through the second P-channel FET when the integrated circuit device is in an operational mode; and

the maintained voltage core logic receives its operating voltage from the output of the low power secondary voltage regulator when the integrated circuit device is in a low power standby sleep mode.

8. The low power voltage regulator according to claim 7, wherein a voltage supplied to the maintained voltage core logic when the integrated circuit device is in the low power standby sleep mode is a sum of threshold voltages of the first P-channel FET and the second N-channel FET.

9. The low power voltage regulator according to claim 7, wherein current through the second N-channel FET is substantially equal to current from the first constant current source when the integrated circuit device is in the low power standby sleep mode and no voltage is being supplied from the primary voltage regulator.

10. The low power voltage regulator according to claim 9, wherein when no voltage is being supplied from the primary voltage regulator the second P-channel FET is turned off and the first N-channel FET supplies operating current to the maintained voltage core logic.

11. A low power voltage regulator for supplying operating voltage to circuits required to maintain data and/or be operational during an integrated circuit device low power sleep mode, comprising:

an amplifier having a non-inverting input, an inverting input, and an output;

an N-channel field effect transistor (FET) having a source, a drain and a gate,

wherein the drain of the N-channel FET is connected to a supply voltage source, and the gate of the N-channel FET is connected to the output of the amplifier;

the non-inverting input of the amplifier is connected to a voltage approximately equal to a threshold voltage of the N-channel FET;

a constant current source connected to a supply voltage common;

a first P-channel FET having a source, a drain and a gate,

wherein the drain and gate of the first P-channel FET are connected to the inverting input of the amplifier and the constant current source, and the source of the first P-channel FET is connected to the source of the N-channel FET;

the amplifier, the N-Channel FET, the first P-channel FET, and the constant current source comprise a low power secondary voltage regulator having an output, wherein the output is the connected sources of the first P-channel FET and the N-channel FET; and

a maintained voltage core logic of an integrated circuit device connected to the output of the low power secondary voltage regulator.

12. The low power voltage regulator according to claim 11, further comprising:

a second P-channel FET having a source, a drain and a gate,

wherein the drain of the second P-channel FET is connected to the sources of the N-channel and first P-channel FETs, the gate of the second P-channel FET is connected to the output of the amplifier and the gate of the N-channel FET, and the source of the second P-channel FET is connected to an output from a primary voltage regulator;

wherein the maintained voltage core logic is coupled to and receives its operating voltage from the primary voltage regulator through the second P-channel FET when the integrated circuit device is in an operational mode; and

wherein the maintained voltage core logic receives its operating voltage from the output of the low power secondary voltage regulator when the integrated circuit device is in a low power standby sleep mode.

13. The low power voltage regulator according to claim 12, wherein when no voltage is being supplied from the primary voltage regulator the second P-channel FET is turned off and the N-channel FET supplies operating current to the maintained voltage core logic.

14. A low power voltage regulator for supplying back-up voltage to circuits required to maintain data and/or be operational during an integrated circuit device low power sleep mode, comprising:

an amplifier having a non-inverting input, an inverting input, and an output;

a N-channel field effect transistor (FET) having a source, a drain and a gate,

wherein the drain of the N-channel FET is connected to a supply voltage source, the gate of the N-channel FET is connected to the first constant current source and the first constant current source is connected to the output of the amplifier;

the non-inverting input of the amplifier is connected to a voltage approximately equal to a threshold voltage of the N-channel FET;

a constant current source connected to a supply voltage common;

a first P-channel FET having a source, a drain and a gate,

wherein the drain and gate of the first P-channel FET are connected to the inverting input of the amplifier and the constant current source, and the source of the first P-channel FET is connected to the source of the N-channel FET;

the amplifier, the N-Channel FET, the first P-channel FET, and the constant current source comprise a low power secondary voltage regulator having an output, wherein the output is the connected sources of the first P-channel FET and the N-channel FET;

a maintained voltage core logic of an integrated circuit device connected to the output of the low power secondary voltage regulator; and

a second P-channel FET having a source, a drain and a gate,

wherein the drain of the second P-channel FET is connected to the sources of the N-channel and first P-channel FETs, the gate of the second P-channel FET is connected to the output of the amplifier and the gate of the N-channel FET, and the source of the second P-channel FET is connected to an output from a primary voltage regulator;

wherein the maintained voltage core logic is coupled to and receives its operating voltage from the primary voltage regulator through the second P-channel FET when the integrated circuit device is in an operational mode; and

wherein the maintained voltage core logic receives its operating voltage from the output of the low power secondary voltage regulator when the integrated circuit device is in a low power standby sleep mode.

15. The low power voltage regulator according to claim 14, wherein when no voltage is being supplied from the primary voltage regulator the second P-channel FET is turned off and the N-channel FET supplies operating current to the maintained voltage core logic.

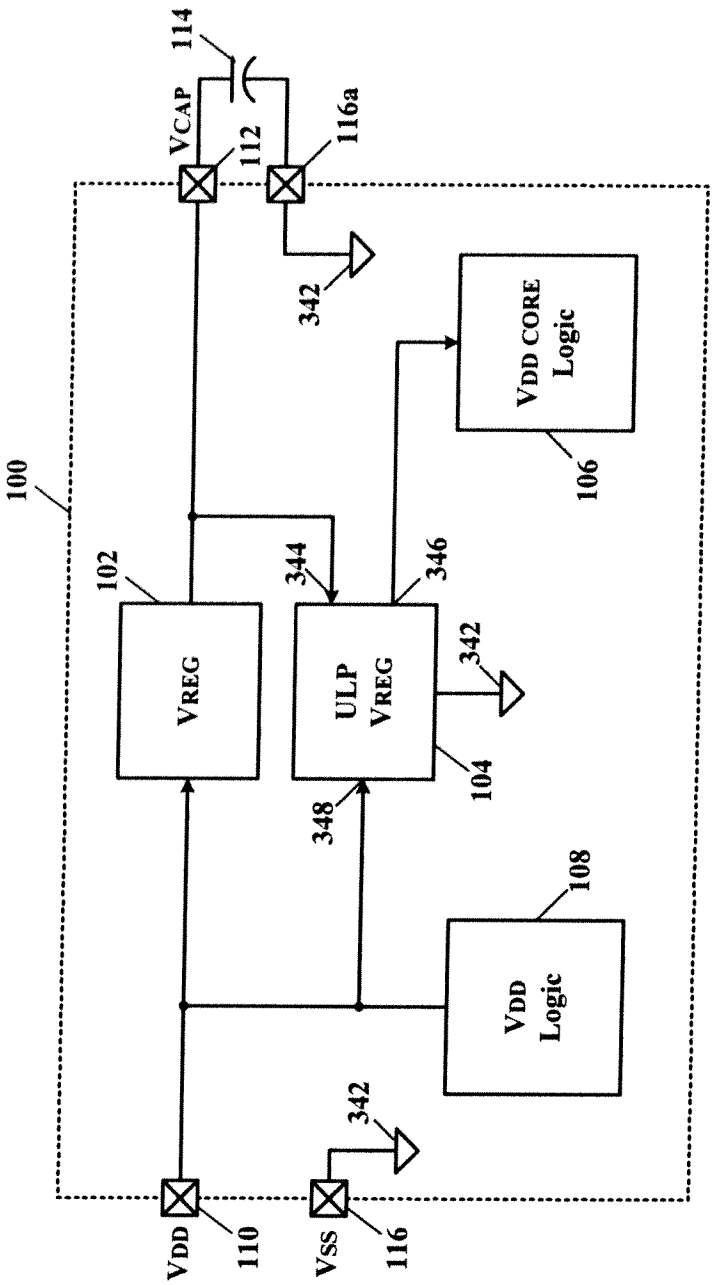
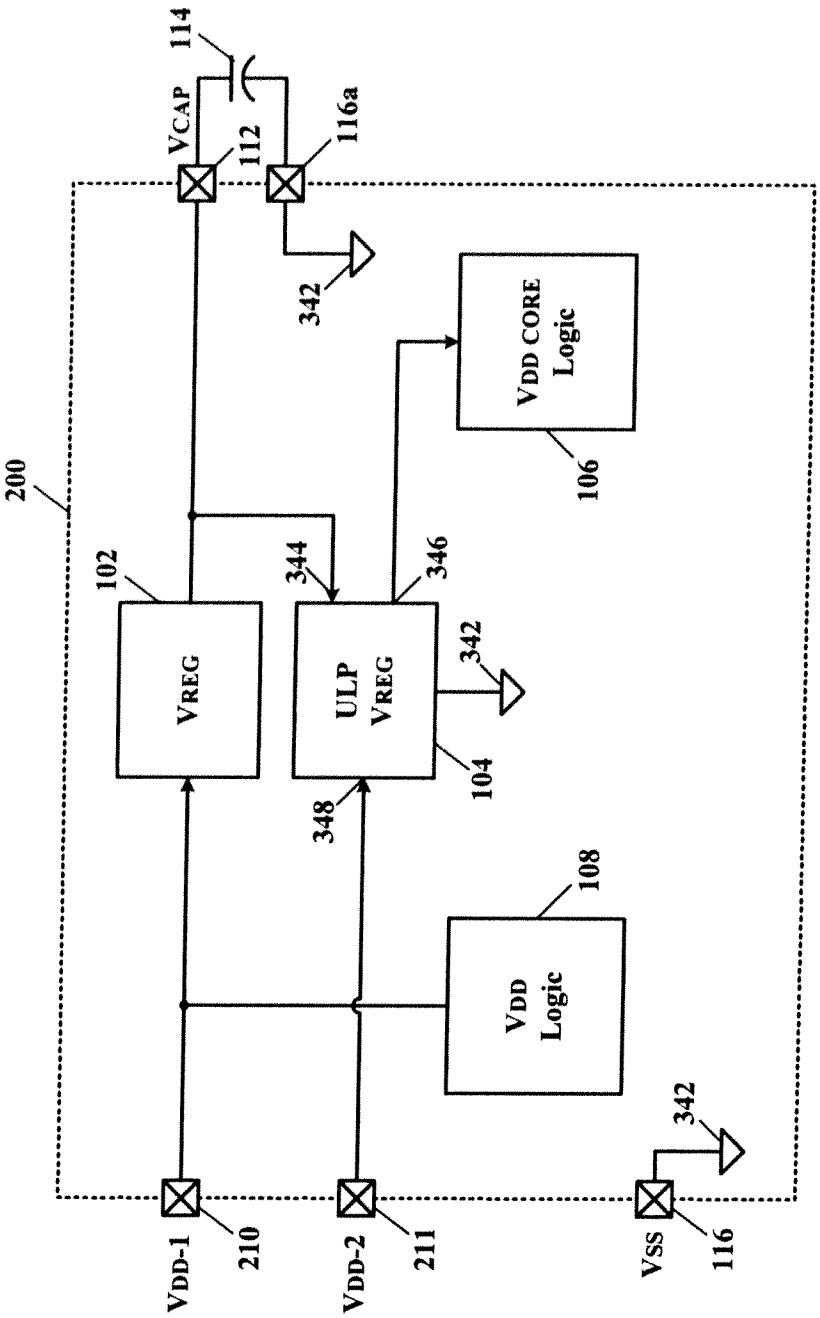

114
VCAP
112
116a
342
VDD CORE Logic
106
100
102
344
346
VREG
ULP VREG
342
104
348
108
VDD Logic
342
VDD
110
VSS
116

FIGURE 1


114
VCAP
112
116a
342
VDD CORE Logic
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102
344
346
VREG
ULP VREG
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104
348
108
VDD Logic
342
VDD-1
210
VDD-2
211
VSS
116

FIGURE 2

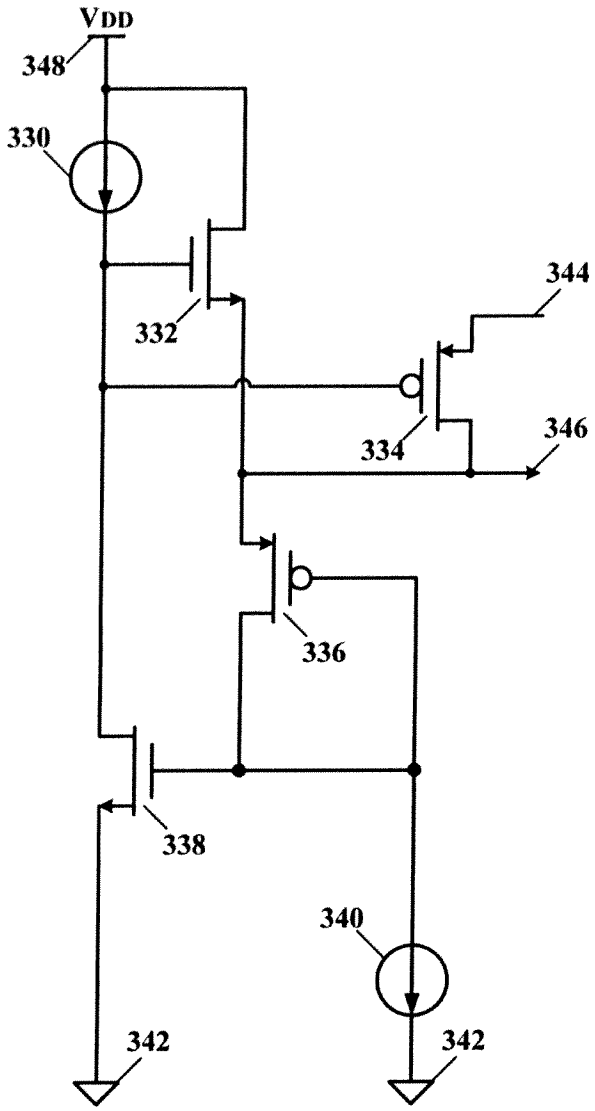

FIGURE 3

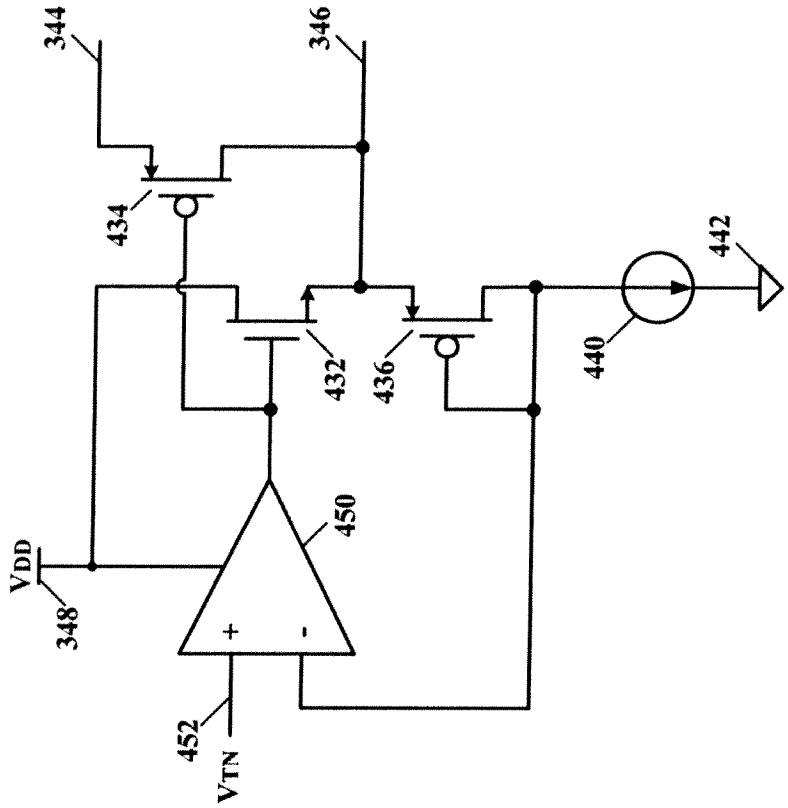

FIGURE 4

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2010/037945

A. CLASSIFICATION OF SUBJECT MATTER
INV. G05F1/575 G05F3/24
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G05F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	JP 3 131916 A (SEIKO EPSON CORP) 5 June 1991 (1991-06-05)	1,11
A	the whole document	2-10, 12-15
A	US 2008/116862 A1 (YANG TA-YUNG [US] ET AL) 22 May 2008 (2008-05-22) paragraph [0001] - paragraph [0012]; figures 1,2	1-15
X	US 6 043 638 A (TOBITA YOUICHI [JP]) 28 March 2000 (2000-03-28)	1,11
A	the whole document	2-10, 12-15
A	WO 02/19074 A2 (PRIMARION INC [US]) 7 March 2002 (2002-03-07) * abstract; figure 6	1-15

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[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
1 October 2010	08/10/2010

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Fax: (+31–70) 340–3016	Arias Pérez, Jagoba

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INTERNATIONAL SEARCH REPORT

International application No
PCT/US2010/037945

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

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A	WO 2004/061830 A2 (INFINITE DATA STORAGE LTD [GB]; LOCKWOOD DAVID [GB]; PERROTT CHRISTOPH) 22 July 2004 (2004-07-22) * abstract; figure 3 -----	1-15

1

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