

- [54] CONTROL SYSTEM FOR HIGH-SPEED
PRINTING MACHINES

- [75] Inventor: **Aleardo Giani**, Milano, Italy

- [73] Assignee: **Honeywell Information Systems
Italia, Caluso, Italy**

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- [30] Foreign Application Priority Data

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- [51] Int. Cl. B41j 1/20, B41j 5/30

- [58] **Field of Search**..... 101/93 C, 90, 111;
340/172.5

- [56]
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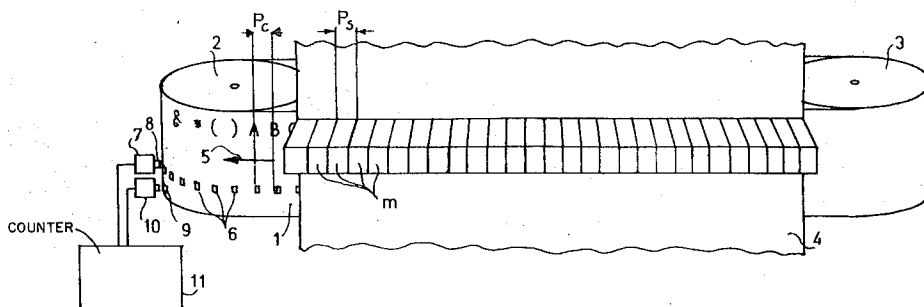
Primary Examiner—William B. Penn

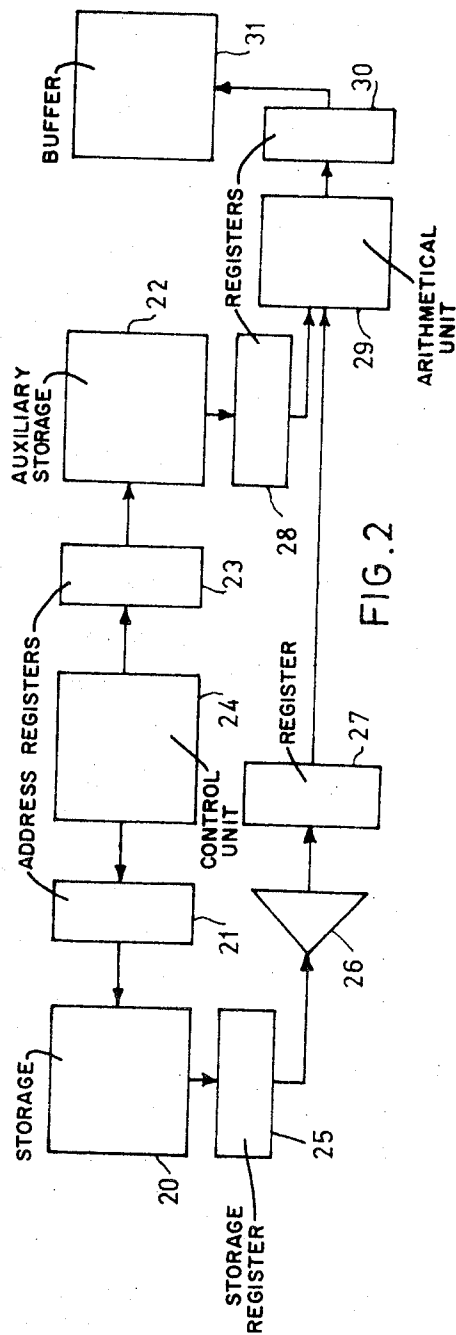
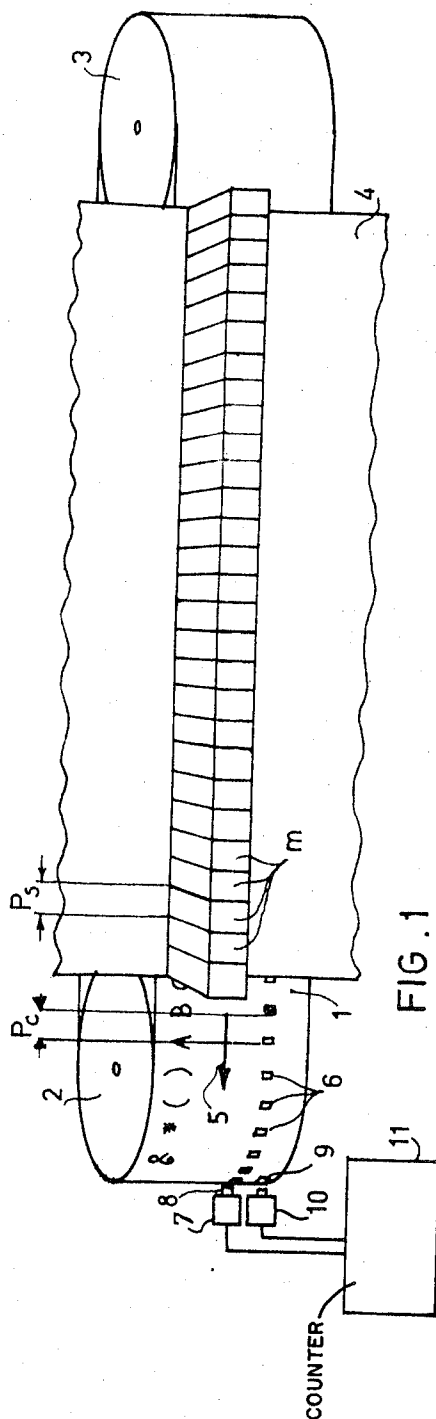
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[57] **ABSTRACT**

A high speed printer is provided with a control circuit wherein each binary code representing a character to be printed in an assigned printing position is linked to one or more recognition bits which serve to determine if such character belongs to that group or groups in a set which are repeated with greater frequency.

13 Claims, 20 Drawing Figures



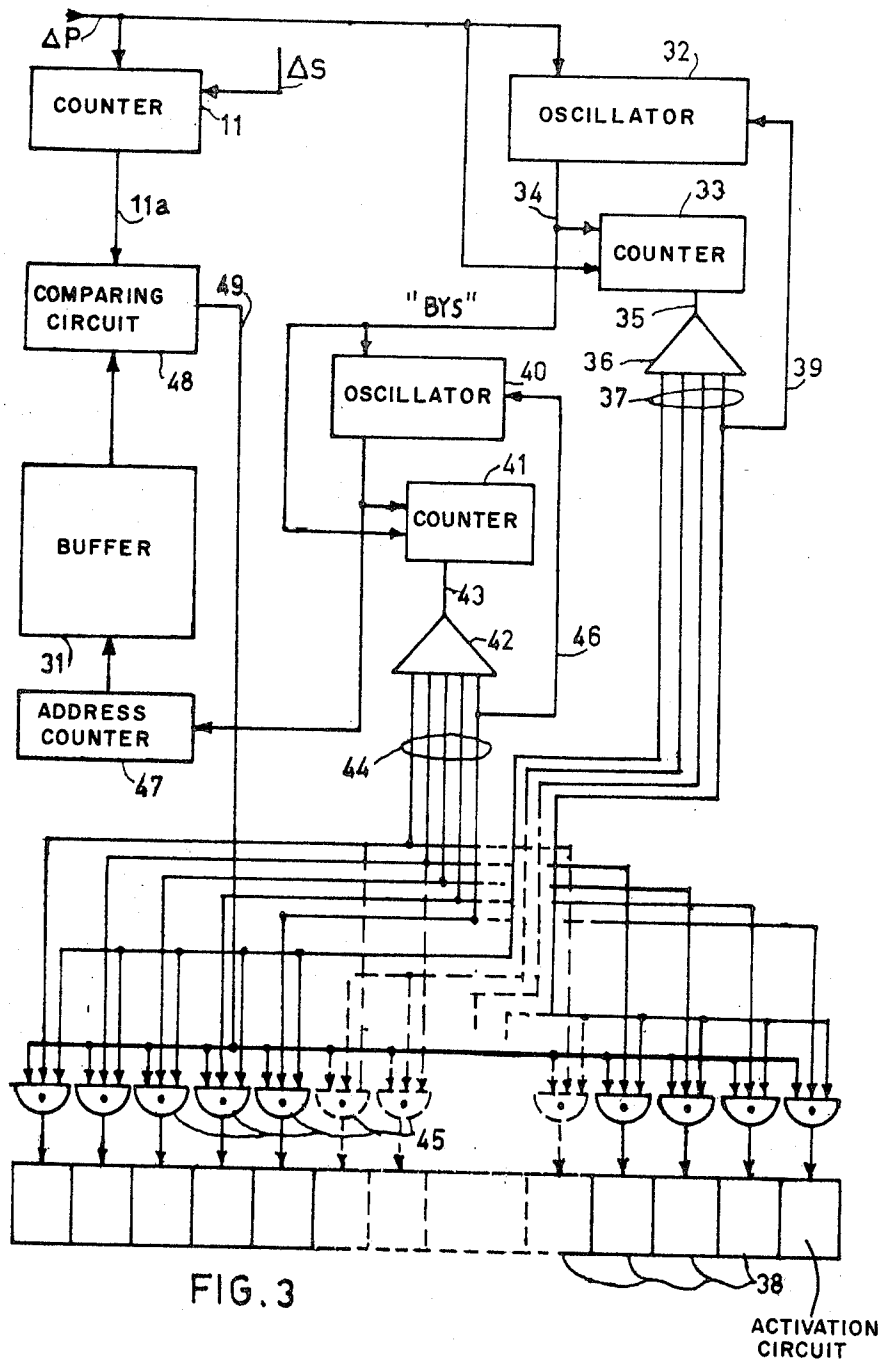


Aleardo GIANI

INVENTOR.

By *Robert Blum*

ATTORNEY.

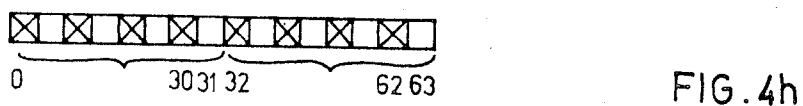
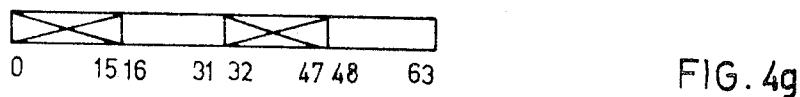
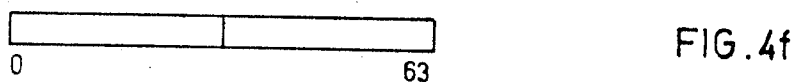
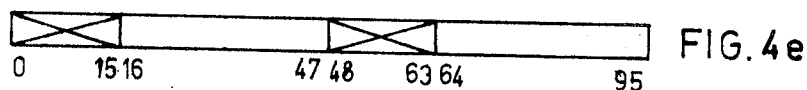
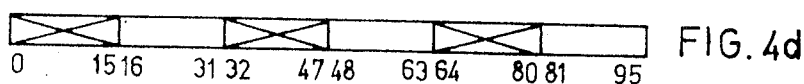
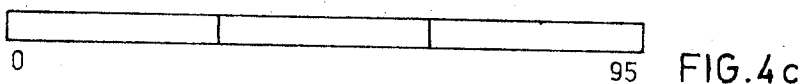
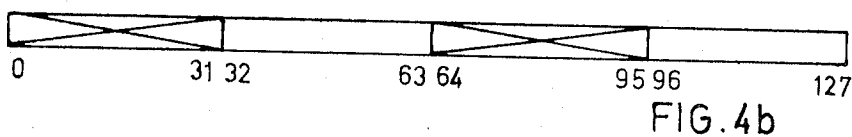
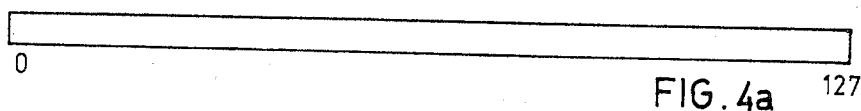


Aleardo GIANI

INVENTOR.

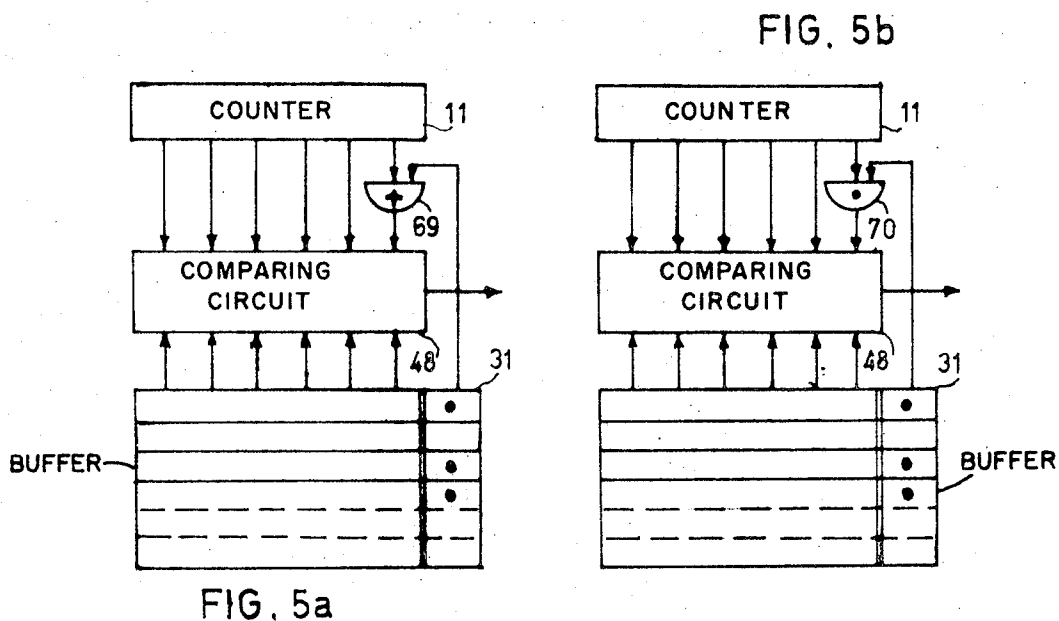
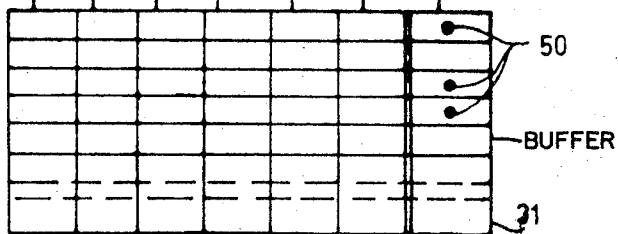
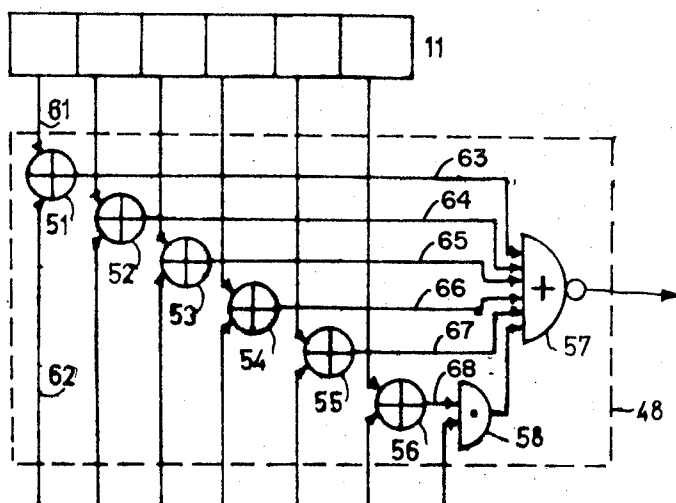
By *Anthony C. Blinn*

ATTORNEY.



Aleardo GIANI
INVENTOR.

By *Hubert Blum*
ATTORNEY.



Aleardo GIANI
INVENTOR.

By Hubert P. Blinn
ATTORNEY.

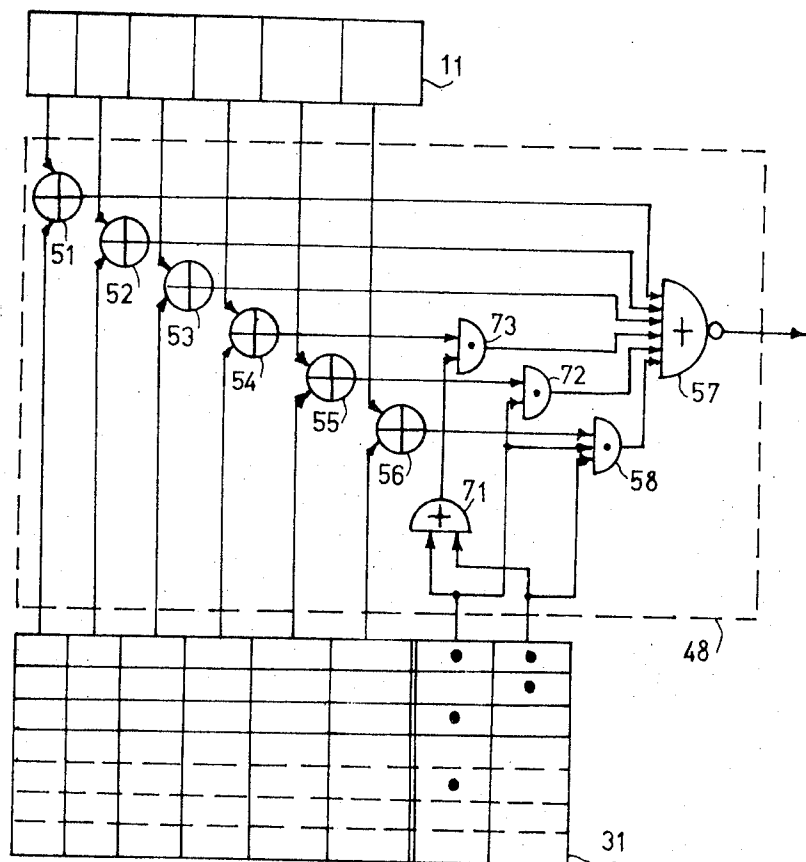
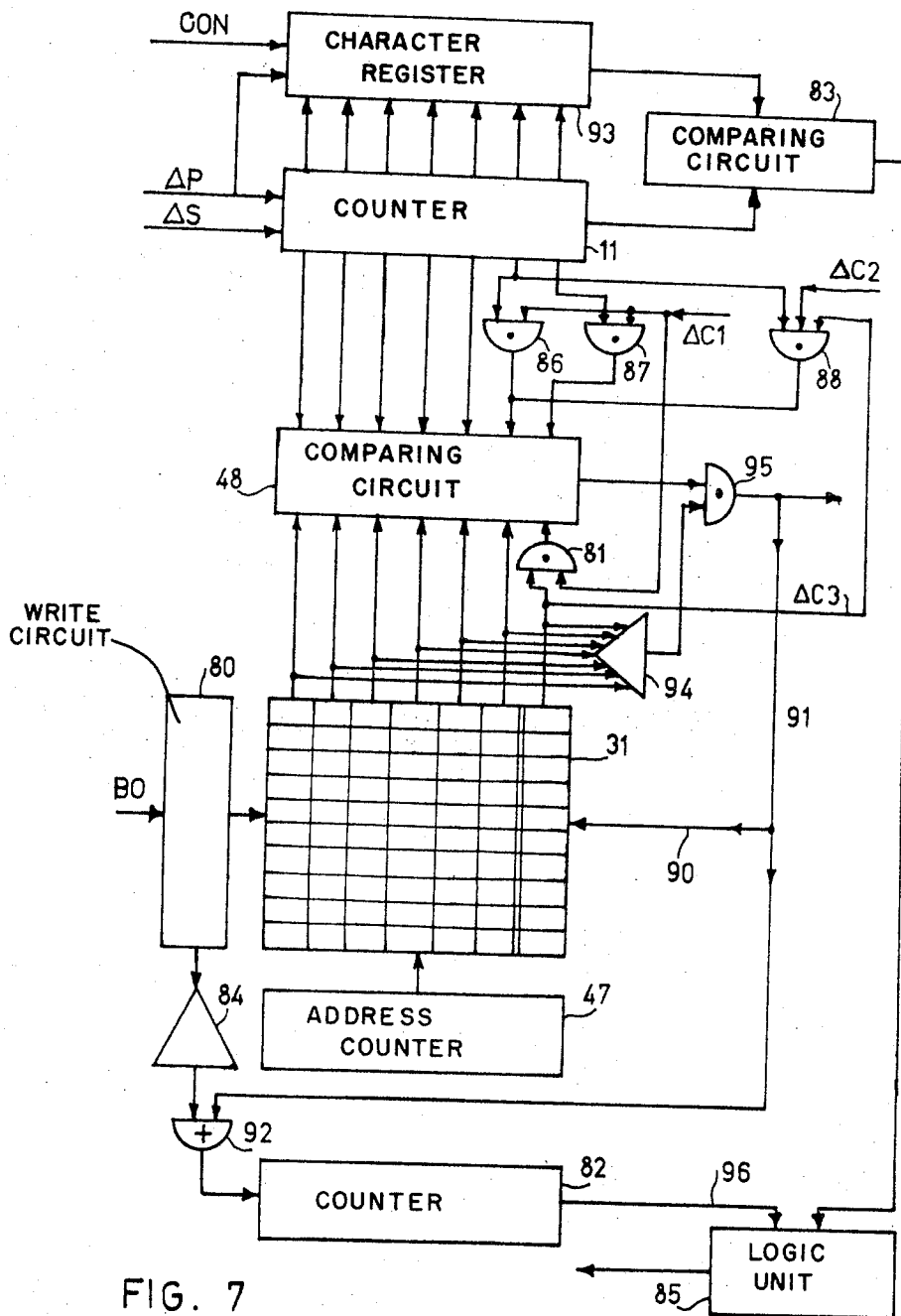


FIG. 6

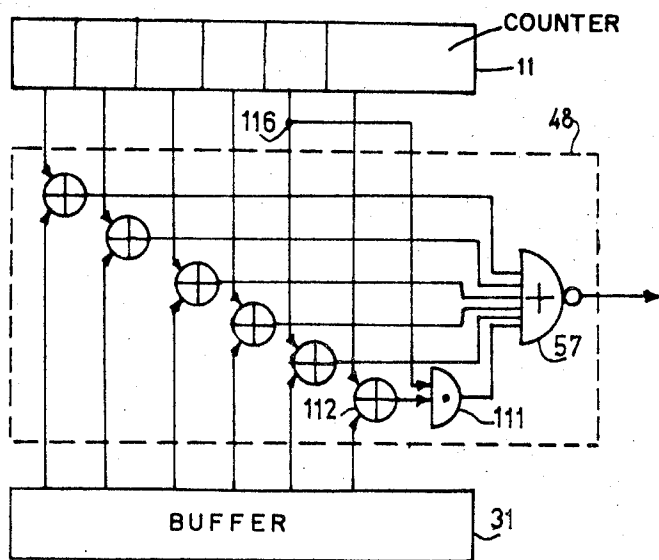
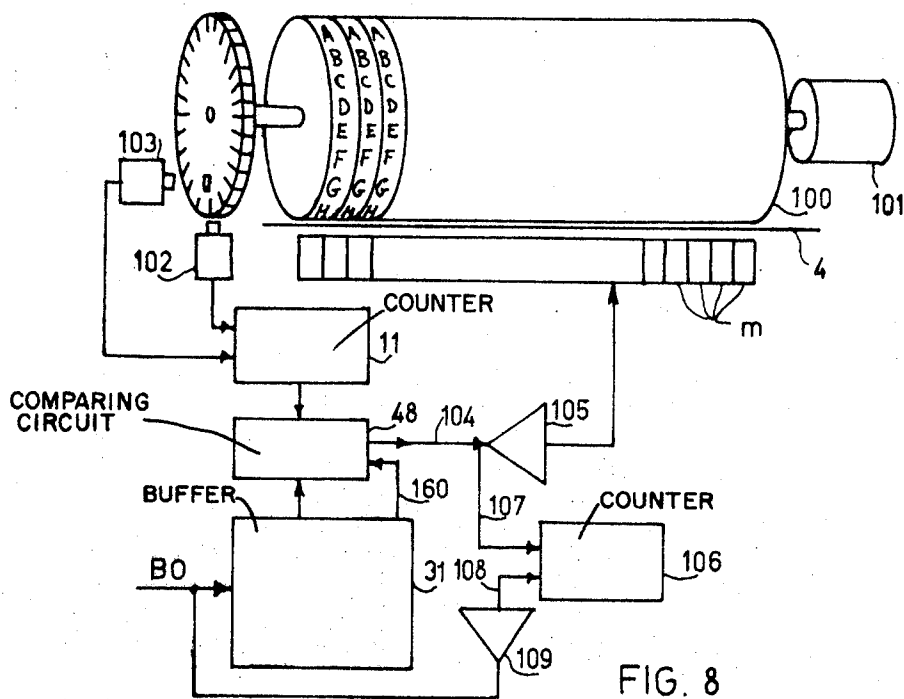
Aleardo GIANI
INVENTOR.

By *Hubert Blime*
ATTORNEY.



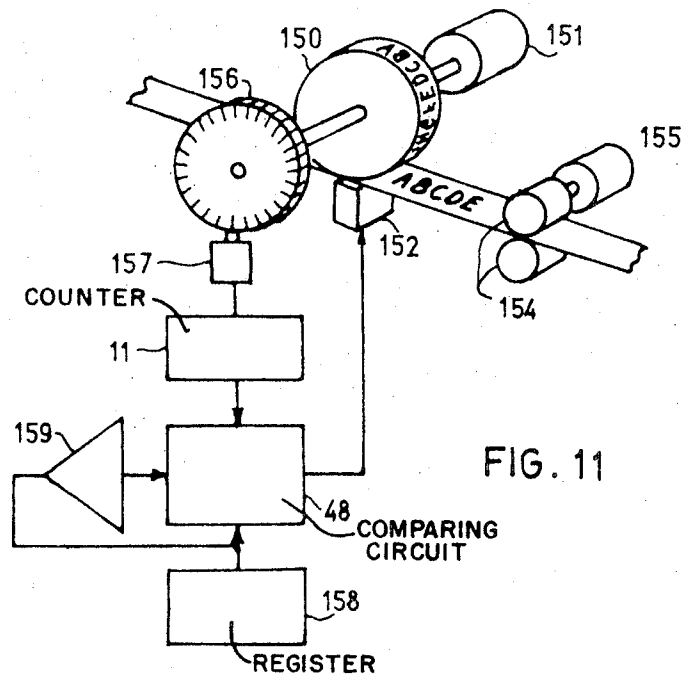
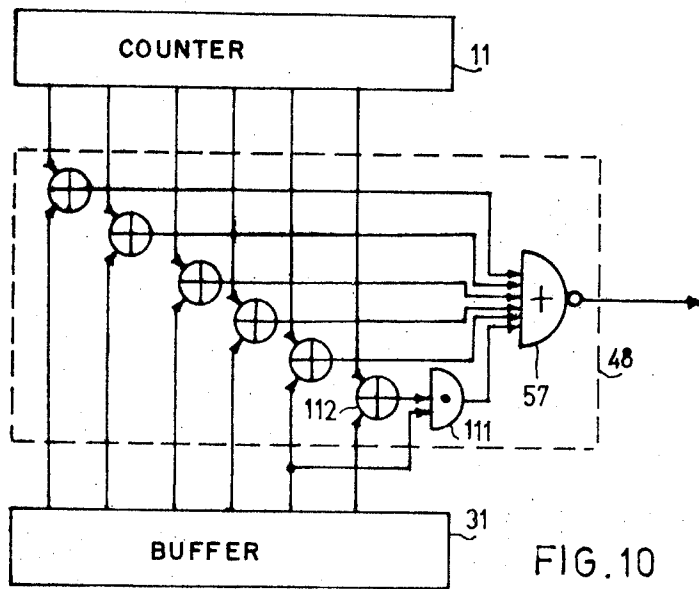
Aleardo GIANI
INVENTOR.

By Richard Blum
ATTORNEY.



Aleardo GIANI
INVENTOR.

By *Robert E. Bine*
ATTORNEY



Aleardo GIANI
INVENTOR.

By *Anthony J. Brine*
ATTORNEY.

CONTROL SYSTEM FOR HIGH-SPEED PRINTING MACHINES

BACKGROUND OF THE INVENTION

The present invention concerns on-the-fly-by high-speed printers, used in data processing systems, particularly printers known as parallel chain printers, belt, or bar printers, and insofar as the invention is also applicable, to other parallel high-speed drum or serial printers.

Parallel chain printers are well known in the art, and generally consist of a type-holder unit in the form of a belt on which are arranged in sequence the various types of an appropriate alpha-numerical set of figures, alphabetical letters and special symbols. The belt or chain is kept in tension close to a printing support and defines on said support a printing line.

Corresponding with this printing line on the same side or on the opposite side of the printing support, as the case may be, printing media are positioned, for example printing hammers in the case of impact printers, electrodes in the case of electrostatic printers, radiation sources in the case of optical printers, etc., one for each printing position. The type-holding belt is kept in motion along the printing line and moves facing the latter at a constant speed.

For each predetermined printing position, when due to the transport effect of the type-holding unit the types of the type-holding unit which have reached the printing position coincide with the characters to be printed in these positions, the corresponding printing devices receive an order and the printing is carried out. When all characters of a line are printed, the printing support is made to move on in a transverse direction to the printing line for an appropriate distance (space between the lines), and the printing of the next line begins.

It is apparent that the printing time of a line consists of the total time needed for the spacing between lines plus the time required for the type-holding unit to pass over all the printing positions. It is known that this printing time may be reduced if the characters printed along a printing line are counted and then as a result of this calculation the spacing between lines is completed after the entire line is actually printed, irrespective of the fact that all types of the type-holding unit have passed along all the printing positions. It is known, furthermore, that as farther reduction of the printing time may be accomplished if in the type-holding units in which certain types, for example numbers, are used more frequently they are repeated with greater frequency, when such units are used together with the previously described device.

The result of the above, however, is that some simplified logic for the control of the device, known in the field, cannot be applied, hence the control system of the printer becomes both expensive and complex.

SUMMARY OF THE INVENTION

Such drawbacks are overcome by the present invention which permits the use of simplified circuits of known construction, in the case where the frequency of the character repetition in the set is different. These advantages are achieved according to the invention by linking to each binary code representing a character to be printed in an assigned printing position one or more recognition bits which indicate if such a character belongs to that group or groups in the set which are re-

peated with greater frequency. Such a recognition bit furnishes the means of appropriately modifying the control logic of the printing apparatus which evolves to be extremely simple and economical.

Other advantages of the invention will become clear in the following description, presented for exemplary purposes which are not limitative, and from the attached drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 represents schematically the structure of a parallel belt printer.

FIG. 2 illustrates in the form of a logical block diagram the structure of an electronic apparatus which performs some logical operations preliminary to the printing.

FIG. 3 shows in the form of a logical block diagram a timing and control circuit which controls the printing operations in a belt printer.

FIGS. 4a, b, c, d, e, f, g, and h represent schematically in strip form several possible type arrangements with various repetition frequencies on type-holding units of the belt-kind, which are applicable in the present invention.

FIGS. 5, 5a, 5b and 6 illustrate in the form of a logical block diagram some of the possible modifications of the control circuit which controls the printing operations according to the invention.

FIG. 7 shows in the form of a logical block diagram a preferred embodiment of a control circuit for a belt printer according to the invention.

FIG. 8 illustrates in the form of a logical block diagram a parallel drum printer as an alternate embodiment of the present invention.

FIGS. 9 and 10 show in schematic form several versions of the invention for possible application in a drum printer.

FIG. 11 represents in schematic block form a serial printer as an embodiment of the present invention.

GENERAL DISCUSSION

For a better understanding of the invention some general remarks on the operation of chain- and belt-printers are considered to be in order.

FIG. 1 represents schematically the electromechanical structure of this type of printer. A belt 1 stretched over two motor-driven pulleys 2 and 3 carries evenly distributed a number of embossed types. The types are uniformly spaced from each other at a suitable pitch P_c . The belt 1 is kept in motion at a constant speed by the motor-driven pulleys 2, 3 driven in turn by a motor (not shown), in such a manner that all the types distributed on it pass along a straight-line path close to the printing support 4. The direction of this motion is, for example the one indicated by the arrow 5. Aligned close to the printing support 4 and opposite the type-holder belt 1, a number of printing hammers m is arranged which hammers are uniformly positioned at a suitable pitch P_2 .

In an optical version for frontal printers, the hammers m may be placed on the same side as the belt 1 relative to the printing support 4.

The impression is performed by action of the various hammers at the proper moments when the types which are to be printed in the various printing positions are, due to the movement of the belt, in the corresponding predetermined printing positions. The printing support

is compressed by the imprint operation between the types and the printing hammers along with an ink rub-bon (if not other means of inking are provided) so that the impression of the type is transferred to the printing support. This is then printing on-the-fly-by and suitable timing devices are necessary.

It is, for example, assumed in FIG. 1 that corresponding with each type the type-holding belt 1 carries an index 6 which may be sensed by a pickup device 7 which emits an electric pulse each time an index 6 passes by its corresponding detection head 8. An additional index 9 may be placed on a second track of the type-holding belt 1 and may be detected by a second pickup 10. The pickup 7 may emit a timing pulse which signals when a type comes into alignment with the first printing position, while the pickup 10 may supply a timing pulse which indicated what the pulse of the immediately following types is in relation to the first type of the printing set.

Such a pulse may be considered an initial pulse and may, for example place a binary counter 11 in a reset condition which evolves with the successive pulses of the types and which then emits a sequence of binary codes each of which corresponds with a character and indicates the order number beginning with the initial character, linked with the pulse generated by the additional index 9. To each type that comes successively into the first printing position, the counter 11 assigns a binary code which permits its identification. This code will henceforth be designated for the sake of clarity as the order number of the type.

The printing of a character in the first printing position is relatively simple. When the order number of the type which is in printing position coincides with the code of the type to be printed, a print order is issued. As for the printing of the characters in the following positions the operation is more complicated.

The pitch of the types P_c is in fact usually different and wider than the printing pitch P_s . When a type is aligned with the first printing position, other types will be aligned with other printing positions in equal successive distances L . By measuring this distance L by the number of types the definition of "pitch of type alignment" Pac follows, such as $Pac \cdot P_c = L$; and by measuring the same distance by the number of printing positions the definition of a "pitch of printing alignment" Pas ensues, such as $Pas \cdot P_s = L$.

Generally, when a given character whose position on the type-holder unit is defined by an order number C , generated by the counter 11, is aligned in a generic printing position S , then also the types of the order number $C \pm KPas$ will align with the printing positions $S \pm KPas$ in which K is an integer.

To offer an example, assume that $Pac = 13$ and $Pas = 20$. This means that if the first type (or the one with the order number $C = 1$) is aligned with the first printing position then also the types 14, 27, 40, 53 . . . will be aligned with the 21st, 41st, 51st, 61st printing positions. In the assumption that there are 160 printing positions the number of types which will be aligned at the same time with the printing positions will be eight.

In a following moment, eight other types will be aligned with eight other printing positions, and so successively for subsets of eight characters each, until, after Pas (in the example 20) basic intervals the second type will be aligned with the first printing position, and the 15, 28, 41 . . . type will align with the 21st, 41st,

etc., printing position, respectively. The types of the printing set consequently come into alignment in the various printing positions for the successive subsets.

The order in which the various types comprised between a type-alignment pitch and subsets to which these belong come successively into alignment with the printing positions contained between a printing-alignment pitch, may be determined as follows.

It is obvious that of the different non aligned types the first to come into alignment will be the one whose disalignment is the least, disalignment being the distance of the printing position which lies in the same direction as the movement of the type-holder unit and which is then reached due to this movement. Since the distance of each type from each generic character C aligned in a generic instant with the generic printing position S is measured by $P'as \cdot Pc$ and the distance of each printing position from the position S by $P'as \cdot Ps$ in which $P'as$ and $P'ac$ are generic integers, smaller than Pas and Pac , respectively, the various disalignment distances between a type and a printing position will be given by all possible combinations for which $D = P'ac \cdot Pc - P'as \cdot Ps$ is larger than zero. The alignment, therefore is determined in that printing position, and for that type, identified by the number pair $P'as$ and $P'ac$, for which D is a minimum. It is easy to show that this occurs for the values $P'as$ and $P'ac$ for which the difference between $P'as/P'as$ and Pac/Pas is the smallest.

The intergers $P'ac$ and $P'as$, thus determined, define "a realignment pitch," measured in the number of characters and in the number of printing positions, respectively, which determine the order in which within each Pas and each Pac the successive types come into alignment with the respective printing positions.

In the case of the example in which $Pac = 13$ and $Pas = 20$, the appropriate fraction with numerator and denominator less than 13 and 20, respectively, results in a minimum value in excess of 13/20 which is two-thirds. Thus $P'ac = 2$ and $P'as = 3$. The order in which the types will align with the printing positions will be: 1, 3, 5, 7, 9, 11, 13, 2, 4, 6, 8, 10, 12, and the order of the printing positions will be: 1, 4, 7, 10, 13, 16, 19, 2, 5, 8, 11, 14, 20, 3, 6, 9, 12, 15, 18. Thus during the interval of one character pulse and the next, i.e., during the interval necessary for the successive characters of the type-holding unit to come into alignment with the same printing position, 20 or generally subcyclical Pas of equal duration may be identified corresponding with which there is a sequential alignment of the characters corresponding with the different subsets of printing positions, according to a pre-established order.

It should be noted that the pitch of the type P_c and that of the printing P_s (or the respective alignment pitches), the conditions and the moment at which the alignment between the printing positions and the types is ascertained are fully identified.

It will now be examined as to how the order number of a type whose function is the identification of the type aligned in the first printing position may be used to also identify the aligned types in other printing positions. This objective is accomplished by linking with each type that is to be printed in a printing position different from the first position a correct code C_c unequivocally correlated to this type, and to the printing position in which it is to be printed, and to compare this correct code with the order number of the type C supplied by the binary counter 11. The order number of the type C

is thus not only compared with the code representing the type to be printed in the first printing position, but also with the correct codes assigned to the types to be printed in the successive printing positions. The comparison occurs of course according to an appropriate order, or by groups of simultaneously aligned characters, taken in a definite order from the alignment pitch of the groups P_{ac} .

The correct code which is linked with the types to be printed is given by the relation:

$$C_c = C - K P_{ac} + K_1 N \text{ in which} \quad (1)$$

C is the code representing the type which is chosen as equal to the order number linked with each type of the counter belt,

P_{ac} is the alignment pitch measured in number of characters,

K is the integer which together with P_{ac} defines the various printing positions in the same group,

N is the number of characters which make up the total of the printing types,

K_1 is an integer, or zero.

The additional term $K_1 N$ is introduced to take into consideration the cyclicity with which the totality of the types appear along the printing line.

The correlation formula (1) is obviously applicable in the case where the movement of the type-holding belt is contrary to the order in which the printing positions are considered, or if it occurs in the direction indicated by the arrow 5. If the movement of the belt runs in the opposite direction the following relation, as may be easily inferred, holds, however;

$$C_c = C + K P_{ac} - K_1 N. \quad (2)$$

A description of the arithmetic network could be used to carry out the correction operation would go beyond the objectives of the invention. Information in this respect may be found in any manual which deals with the technology of the digital computer, i.e., in the authoritative text "Digital Computer and Control Engineering" by Robert Steven Ledley, McGraw-Hill, 1960. A specific feasible solution for application in a printer of the described type is also offered in logical block form in U.S. Pat. No. 3,314,360 issued Apr. 18, 1967 in the name of W. P. Foster.

No doubt other feasible solutions may be used to perform the indicated correction. For instance the various corrective coefficients, $\pm K P_{ac} \mp K_1 N$, may be stored in an auxiliary memory for reading only, also known by the experts of the field under the acronym ROS (read only storage) and from there retrieved in a suitable sequence and summed up in a computer network with the code of type C .

FIG. 2 represents in schematic block form such a solution and represents in a generic way the part of a structure of an electronic computer which may be used to perform the different required operations. The data to be printed is contained in a data storage 20 where each character is represented by a predetermined binary code which may be completely arbitrary, or taken from standardized codes (ISO - ECMA, etc.). The corrective coefficients are contained in an auxiliary storage 22. The address registers 21 and 23 provide for retrieval from the storages 20 and 22, respectively, of the characters and the correction coefficients one by one

in the most convenient sequence (for example, notably by successive subsets).

A control unit 24 controls the read operation of the storages 20, 22 and, generally, all operations of the computer.

The corrective operation is conducted as follows:

First, the characters to be printed are retrieved one by one from the storage 20 and stored one at a time in a storage register 25.

From the register 25 they are transmitted to a decoder network 26 which converts the binary representation of the characters into order number C used in the printing installation for the identification of each character. The order number C is sent to a register 27. Simultaneously, the control unit 24 retrieves from the storage 22 the corrective coefficient, corresponding with the printing position in which the character is to be printed whose code is contained in a register 27, and stores it in a register 28. The content of the two registers 27 and 28 are then added in the arithmetical unit 29 and the result is stored in a register 30 which thus, now contains a correct code C_c .

The operation is repeated for all characters to be printed in a printing line and the corresponding corrected codes are progressively stored in an auxiliary memory of the printer or "buffer" 31.

FIG. 3 represents in schematic block form the control logic of a parallel chain printer of the described type. The "buffer" 31 contains the correct character codes of a complete printing line and is stored in a data processing unit, such as already described with reference to FIG. 2. The binary counter 11 of FIG. 3 receives pulses of character synchronization ΔP and reset pulses or revolving pulses ΔS corresponding with the pulses originating from the pickups 7 and 10 already shown in FIG. 1. As already mentioned, the binary counter 11 presents at its outputs, symbolized for the sake of simplicity by a single wire 11a, a binary code (which changes with the time) and which corresponds with the code of the character which was located in successive moments corresponding with the first printing position. The synchronization pulses of the character ΔP are, moreover, applied to an oscillator 32 from which they elicit the go signal and to a binary counter 33 from which they elicit the reset. The oscillator 32 emits from its output on wire 34 BYS pulses which are uniformly distributed along the entire interval between two synchronization pulses ΔP , equal in number to P_{as} .

To refer to a specific case, let it be assumed that $P_{as} = 20$. The pulses BYS originating in the oscillator 32 are applied to the binary counter 33, having a counting capacity equal at least to P_{as} , and cause it to produce the count progressively. The outputs of the counter 33, denoted for the sake of simplicity by a single wire 35, feed a decoder circuit 36 which presents suitable electric signals one at a time on the P_{as} wires of the output 37. The electric signal, present sequentially on each of the wires 37, selects P_{as} groups of activation circuits, one for each printing electromagnet. The activation circuits are symbolized by the blocks 38. When the counter 33 has completed the count of P_{as} number of BYS pulses, the electric signal appearing at the output of the decoder circuit 36 is applied to the P_{as} -th wire of the output from which it is derived via wire 39 and applied to the oscillator 32 functioning as a stop signal. Due to this signal, the oscillator 32 produces P_{as} pulses and then stops waiting for a new go order.

The PYS pulses produced by the oscillator 32 besides being applied to the counter 33 are also applied to a second oscillator 40 which generates pulses, and to a binary counter 41 from which they elicit the reset. The oscillation frequency of the oscillator 40 is higher than that of the oscillator 32, so that between a BYS pulse and the following one the oscillator 40 is able to produce a certain number of pulses, equal at least to the number N_c of the printing columns of the printer divided by P_{as} . Thus, when the number of the printing columns is 160 and $P_{as} = 20$ the oscillator 40 produces at least eight pulses.

Similarly to the counter 33, the counter 41 applies to a decoder circuit 42 a combination of signals over the output wires (represented for the sake of simplicity by a single wire 43), and the decoder circuit supplies electric signals one at a time on the N_c/P_{as} wires of the output 44. The electrical signal successively appearing on each of the wires 44 selects N_c/P_{as} groups of activation circuits, precisely an activation circuit within the range of each of the P_{as} groups chosen by the wires 37. This means that the electric signal originating from the decoder 42 and that stemming from the decoder 36, select one activation circuit at a time.

The selection is achieved by means of AND circuits 45, having three inputs, one AND circuit for each activation circuit. To the third input of each AND circuit a print order is applied. Each activation circuit receives a print order, therefore, only when there is simultaneously applied to the inputs of the corresponding AND circuit the print order, the group-selection signal originating from the decoder 36, and the selection signal originating from the decoder 42.

As soon as the counter 41 has completed the count of 8 pulses the electrical signal present at the output of the decoder circuit 36 is applied to the N_c/P_{as} -th wire of the output from which it is derived via the wire 46 and applied to the oscillator 40 functioning as a stop signal. Due to this signal, the oscillator 40 produces N_c/P_{as} pulses and then stops, awaiting a new go signal.

The pulses produced by the oscillator 40 in addition to being applied to the counter 41, are also applied to an address counter 47 whose function is to address various storage positions of the buffer 31 consecutively and to retrieve from it one by one the correct codes there contained. The retrieved correct codes are applied to the comparing circuit 48 to which is also applied the order number produced by the counter 11. If the two codes agree, a positive comparing signal is generated on the wire 49 and applied to the third input of all AND circuits 45 with the function of a print order. Only the selected AND circuit issues the order of course, to the activation circuit 38 linked with it.

It must be pointed out here that the order number produced by the counter 11 is modified at the receipt of any pulses Δp from the counter, while during the interval between two pulses Δp the two oscillators 32 and 40 in cascade generate as many pulses as there are printing columns, and the counter 47, therefore, addresses all the storage positions of the buffer 31.

Each order number of a character is thus compared with all correct codes which define a printing line and the printing operation is carried out character by character in those printing positions where the alignment conditions and those of coincidence between the characters actually present in the printing positions, and the characters to be printed, are met. It should also be

noted that for the N_c/P_{as} printing positions chosen by the counter 41 sequentially the printing should be performed simultaneously, for, in fact, the character alignment occurs simultaneously for these printing positions.

The sequential printing is, however, not such as to produce significant disalignments since it is in every case contained between a P_{as} -th of the printing pitch and it is, moreover, possible to achieve a "realignment" of the printing times by suitable delay circuits. Also, other auxiliary circuits are associated with this logical structure of the belt printers, as for example circuits signalling printing errors or counters keeping track of the operations carried out along the printing line so as to initiate a lead operation or an advancing of the paper as soon as the printing of a line is concluded.

THE INVENTION

The preceding description makes it clear that the character code generated by the counter of the timing pulses permits the control of all printing operations along the printing line if provisions are made for the correction of the codes of the characters to be printed as a function of the position in which they are to be printed.

The above described system, however, does not permit the use of a type-holder unit on which the types are distributed with a varying frequency, for it links reciprocally the types, and the printing positions occupied by them on the type-holding unit. The system, however, makes it possible to remove this limitation by application of some expedients.

As already indicated, this is obtained according to the invention, by linking to the correct codes stored in the auxiliary memory, one or several added units of data which provide for distinguishing the frequency of repetition of each character on the type-holding unit. This is especially advantageous for the characters to be printed, each different from the other, are known not to exceed in general 128, and may thus be represented by binary codes of 7 bits. Yet, the memory banks for building auxiliary storages and buffers are generally used to store data of 8 or 9 bits. 2 or 3 bits remain available, therefore, to which this specific function may be assigned. The following description shows how this may be accomplished.

FIG. 4a represents schematically, in the form of strips, an alpha-numerical set distributed on a type-holding unit. All the types, a total of 128, are distributed with the same frequency in the set once, and each type may be represented by a binary code of 7 bits from 0000000 to 1111111 inclusive.

FIG. 4b represents in the same form an alpha-numerical set in which the characters are distributed with a different frequency; the first group of characters (from 0 to 31) is identical with the third group of characters (from 64 to 95) which thus are represented twice in the set, while the remaining characters are represented only once.

FIG. 4c represents another alpha-numerical set in which the characters are distributed with the same frequency and the set comprises 96 characters.

FIG. 4d represents an alpha-numerical set of 96 characters in which the characters are distributed with a different frequency: the first group of characters (from 0 to 15) is identical with the third (from 32 to 47) and with the fifth group of characters (from 64 to 80)

which thus are presented three times in the set, while the remaining characters, distributed in the second, fourth, and sixth group, are present only once.

FIG. 4e illustrates another alpha-numerical set in which the characters are distributed with a different frequency: the first group of characters (from 0 to 15) is identical with the third group of characters (from 48 to 63) which thus are presented twice in the set, while the remaining characters, distributed in the second and in the fourth group, are present only once.

FIG. 4f represents another set of 64 characters distributed with the same frequency.

FIG. 4g symbolizes another set of 64 characters, distributed with a different frequency: the first group of characters (from 0 to 15) is identical with the third group of characters (from 32 to 47) which thus are present twice in the set, while the remaining characters, distributed in the second and in the fourth group, are present only once.

The sets shown in the described illustrations are only some examples of the innumerable arrangements of characters in a set, with different or equal frequencies, which may be suitably applied in the belt printers. In FIG. 4h if for example, another case represented in which the repeated characters are not gathered in two adjacent groups, but are placed in equal positions, from 0 to 30, and repeated in the same positions from 32 to 62. The characters arranged in unequal positions are, however, only present once in the set.

The requirement, common to all the illustrated sets and necessary to put the invention into effect, consists in that the order numbers representative of the characters repeated with a greater frequency in the set, such as generated by the counter 11 of FIG. 1, differ among each other only by one or a few specified bits. In other words, if with a pre-established character an order number determined by the counter 11 is linked and if subsequently the same character is represented in the printing set, it is necessary that the counter 11 link to that character which is identical with the first an order number which differs from the first only by one or a few specified bits. This is achieved by placing the characters on the type-holder unit in order according to the criteria of the type of the illustrated characters. To clarify this concept further, we shall consider the set of characters shown schematically in FIG. 4g.

This may for example, consist of the following 16 characters: 0 1 2 3 4 5 6 7 8 9 + - . , ; repeated twice in the set and of 32 characters A B C D E F G H I J K L M N O P Q R S T U V W X Y Z & ' * ° () repeated once. The following Table 1 assigns to each character of the set a sequential numerical rank, and links with it a binary code representative of this rank:

TABLE 1

0	0	000000	32	0	100000
1	1	000001	33	1	100001
2	2	000010	34	2	100010
3	3	000011	35	3	100011
4	4	000100	36	4	100100
5	5	000101	37	5	100101
6	6	000110	38	6	100110
7	7	000111	39	7	100111
8	8	001000	40	8	101000
9	9	001001	41	9	101001
10	+	001010	42	+	101010
11	-	001011	43	-	101011
12	.	001100	44	.	101100
13	,	001101	45	,	101101
14	;	001110	46	;	101110
15	;	001111	47	;	101111
16	A	010000	48	Q	110000

17	B	010001	49	R	110001
18	C	010010	50	S	110010
19	D	010011	51	T	110011
20	E	010100	52	U	110100
21	F	010101	53	V	110101
22	G	010110	54	W	110110
23	H	010111	55	X	110111
24	I	011000	56	Y	111000
25	J	011001	57	Z	111001
26	K	011010	58	&	111010
27	L	011011	59	,	111011
28	M	011100	60	*	111100
29	N	011101	61	°	111101
30	O	011110	62	(	111110
31	P	011111	63	)	111111

It may be noted that the binary codes or order numbers, corresponding with the ranks 32 . . . 47, differ from the order numbers corresponding with the ranks 0 . . . 15 only by the more significant bit, the sixth. Two different codes are assigned to the twice repeated characters, different by the more significant bit. This is explained by the fact that the counter 11 that generates the order numbers is totally unconcerned about the arrangement of the types on the type-holder unit, but correlates bi-reciprocally the various positions which the type-holder unit may occupy in a pre-established code (exactly the order number).

Vice versa, the logical system which controls the printing and sees to it that a specified code is assigned, to each type and that it is corrected according to the printing position, assigns a unique code to each type. If, therefore, codes assigned by the logic system to the twice repeated characters are those included between 000000 and 010000, an agreement these codes and the codes of the characters from 100000 to 110000 which represent on the type-holder unit the same types, is never verified. If, however, the codes assigned by the logic system to the twice repeated are those from 100000 to 110000 an agreement between these codes and the codes of the characters from 100000 to 010000 will never be verified. It happens, therefore, that to the characters appearing with a frequency of more than once on the type-holding unit more representative codes are assigned and all are compared with the character code produced by the counter 11. This may simply be achieved with a single comparing operation by confining the comparison in these instances to that part of the code which is significant and by disregarding those bit of the code which may be different. For example, the order number, with reference to the preceding table, assigned to the number 6 is 000110 or 100110, or a symbol used in Boolean algebra: 0 00111. The comparison in this case must only be made for the 5 less significant bits. This condition is imposed on the comparison circuit in a very simple way, namely by linking with the code representative of the character, chosen of any of the various order numbers representative of the same character, an identification code in the form of an additional bit which specifies that the character is repeated several times in the set and that it is applied to adopt the comparison logic.

FIG. 5 represents in logical block form the part of the control system already described in FIG. 3 which is concerned with the indicated modification, according to the invention. In FIG. 5 are shown the counter 11 for generating the order numbers, divided into binary cells, the comparison circuit 48 and the auxiliary storage or buffer 31 which for better clarity is subdivided into lines and columns which stand for binary storage cells. On each line of the storage 31 a character code with 6 bits (not shown) is stored. In the seventh columns there

is stored for each character, an information bit for those character which are repeated several times. Such a bit is denoted by the dots 50.

The characters stored in the storage 31 are retrieved one by one, together with the identification bit 50, when present, and applied to the comparison circuit 48. Such a comparison circuit consists, for example of six logical elements 51, 52, 53, 54, 55, 56 which perform the logical function exclusive or, of an element 57 that performs the logical function NOR, and of a circuit AND 58. To the two inputs of the logical element 51 the less significant bits of the order number (originating from the counter 11 over the wire 61) and of the code retrieved from the memory 31 (stemming from the memory over wire 62), respectively are applied.

The procedure is similar for the bits of greater weight which are applied to the inputs of the logical elements 52, 53, 54, 55, 56. It is apparent that the output of each logical element 51 . . . 56 takes on the logical level of 0 every time that the logical levels at the two inputs coincide. When, therefore, the order number and the code retrieved from the memory 31 coincide, the outputs of all logical elements 51 . . . 56 are at the logical level 0. These outputs 63, 64, 65, 66, 67, with the exception of the output of the logical element 56, are connected with the inputs of the element NOR 57.

The output 68 of the logical element 56 is instead linked with NOR 57 across the AND gate 58 having two inputs. To the second input of the AND gate 58 the bit of a character identifiable as a repeated character is applied. For reasons of convenience it may be assumed that this bit has the logic level 0, when present, and the logic level 1, when absent. Thus when the code retrieved from the storage 31 corresponds with a character which is not repeated several times (and, therefore, the information bit is absent) the output of the circuit 56 is applied to the NOR 57 and has a level which depends on the result of the comparison of the two more significant bits of the order number and of the code retrieved from the storage 31, respectively. When the outputs of all circuits 51 . . . 56 have the logic level 0 this means that the two codes agree and that the output of NOR 57 is at the logic level 1. In other words, under these conditions the two codes are compared in their entirety. On the contrary, when the code retrieved from the memory 31 corresponds with a character which is repeated several times (and, therefore the identification bit is present) the output of circuit 58 remains at the level 0, irrespective of the result of the comparison effected by the circuit 56, i.e., the comparison of the two codes is performed partially, under the exclusion of the more significant bit.

The desired result is thus obtained. Obviously the same result may be accomplished by application of other circuit solutions. FIG. 5a, for example illustrates another solution.

In FIG. 5a the comparison circuit 48 does not constitute any modification and, on the contrary, the order number assigned to in this circuit is modified by the logical circuit OR 69. The operation is as follows.

In the storage 31 are stored the correct codes C_c , derived from the already cited formulas, and stemming from a code representative of the character C which for the characters having a repetition frequency of more than one is selected as order number C of greater weight from the codes of characters representative of the same character.

Thus, with reference to the preceding table, the representative code 100111 is made to correspond with the numerical character 7 with which the character codes 000111 and 100111 correspond. This, of course, is done by the decoder matrix 26 shown in FIG. 2. Also, in this case, an identification bit which we assume for the sake of simplicity to have the logic level 1, when present, is linked to the code of characters which are repeated several times on the type-holder unit. Such information bit is applied during the comparison of the order number and code drawn from the memory 31 to an input of the circuit OR 69. As may be seen from FIG. 5a, the more significant bit of the order number is not directly applied to the comparison circuit, but over the circuit OR 69. When the identification bit is at the logic level 1, the more significant bit which was applied to the comparison circuit as an order-number bit takes on the logical level 1 in each case, and thus coincides necessarily with the more significant bit of the code derived from the storage. In this case, the comparison circuit is adapted to one of the inputs rather than to its output.

A similar solution is presented in FIG. 5b. In this case, the correct codes C_c , derived from a code representing the character C which for the characters of a repetition frequency of more than one is the order number of lesser weight among the order numbers representative of the same character, are stored in memory 31. When in this case the identification bit, which we shall assume to have the logic level 0, when present, is present the circuit AND 70 prevents the application of the less significant bit of the order number to the comparison circuit and applies instead a bit having the logic level 0 which coincides thus with the more significant bit of the code extracted from the memory 31.

In the preceding examples, reference was made to the utilization of a single bit of identification, but clearly the described inventive concept may be extended to the application of more identification bits, by which the flexibility of the use of the invention may be broadened.

We may, for example, consider the following table (Table 2):

TABLE 2

0	0	000000**	32	0	100000**
1	1	000001*	33	1	100001*
2	2	000010*	34	2	100010*
3	3	000011*	35	3	100011*
4	4	000100*	36	4	100100*
5	5	000101*	37	5	100101*
6	6	000110*	38	6	100110*
7	7	000111*	39	7	100111*
8	0	001000**	40	0	101000**
9	8	001001*	41	8	101001*
10	9	001010*	42	9	101010*
11	A	001011	43	S	101011
12	B	001100	44	T	101100
13	C	001101	45	U	101101
14	D	001110	46	V	101110
15	E	001111	47	W	101111
16	O	010000*	48	O	100000**
17	F	010001	49	X	110001
18	G	010010	50	Y	110010
19	H	010011	51	Z	110011
20	I	010100	52	.	110100*
21	S	010101*	53	5	110101
22	J	010110	54	.	110110
23	K	010111	55	-	110111
24	O	011000**	56	O	111000**
25	L	011001	57	+	111001
26	M	011010	58	&	111010
27	N	011011	59	.	111011
28	O	011100	60	.	111100
29	P	011101	61	.	111101
30	Q	011110	62	(	111110
31	R	011111	63	)	111111

Table 2 illustrates a set of characters distributed on a type-holding unit with variable frequency. The character 0 is repeated eight times and is identified by the character codes:

000000
001000
010000
011000
111000

The character 5 is repeated four times and identified by the character code:

000101
010101
100101
110101

The characters 2 3 4 6 7 8 9 are repeated twice and the corresponding codes differ for each character in the more significant bit.

Finally, the remaining characters are repeated only once. It is thus apparent that for the character 0 the comparison between the representing codes must be confined to the three less significant bits. For the character 5, the two more significant bits must be excluded and for the characters 2 3 4 6 7 8 9 the more significant bit is to be excluded.

Hence, two identification bits are linked with the character 0, as shown in Table 2, one identification bit of weight 2 with the character 5, and one identification bit of weight 1 with the characters 2 3 4 6 7 8 9.

FIG. 6 demonstrates how such identification bits are used to modify the comparison conditions of the comparison circuit 48. In this case the comparison circuit 48 comprises the elements OR 71, AND 72, and AND 73 in addition to the elements 51, 52, 53, 54, 55, 56 which perform the logical function exclusive or, and the element NOR 57 and AND 58. The two identification bits of the character 0, when present, are applied to the two inputs of the circuit OR 71 and, since they are assumed to have the logical level 0, when present, the output of the element OR 71 will have the logical level 0 only, if both bits are present. The output of the element OR 71 is, however, applied to the input of the circuit AND 73 which conditions the application of the result of the comparison carried out by the circuit 54 to circuit NOR 57. Similarly, the circuits AND 58 and 72 receive the identification bit of weight 1 and of weight 2, respectively, and as a function of the logical value of these, they prepare the application of the result of the comparison performed by the circuits 56 and 55 to the circuit NOR 57, respectively. Hence, when the two identification bits are present, only the three less significant bits of the order number of the code derived from the memory are compared. When the bit of weight 1 is present the comparison of the more significant bit is excluded and when the bit of weight 2 is present the comparison of the two more significant bits is excluded.

After the general description of the prominent aspects of the invention it behooves one to emphasize that the technical solutions by which the invention may be implemented are of a great variety. The versions and

modifications of the invention are in fact so varied that they render it adaptable to different requirements, as for example to the application to bar printers or parallel serial printers having interchangeable type-holding units. To complete the description, we shall mention for exemplifying purposes the logic organization of a chain printer with interchangeable units of type-holders and, most advanced in the application of the invention, of a drum printer and a serial printer.

FIG. 7 illustrates schematically the control logic of the first mentioned of these printers. It is assumed that the chain printer applies type-holding units of 128, 96, 64, 48, 16 characters which are interchangeable, let alone the fact that a type-holding unit with a set of characters repeated is exactly $48 + 16$, hence of the type represented in FIG. 4g.

The logic includes: a counter 11 for generating order numbers of 7 bits and thereby having the capacity of binary counting from 0 to 127, a logic write circuit 80 which receives from the data processing system the print information over a data transmission channel BO and stores it in the buffer 31, which has a capacity of 160 characters of 7 bits each, an address counter 47 of the storage, a comparator circuit 48 with 7 bits, the oscillators and counters already illustrated in FIG. 3 and there marked with the reference numbers 32, 40, 33, 41 along with their respective decoders, and the selection and control network of the various activation circuits which are not shown in FIG. 7 for the sake of the simplicity of design.

The logic includes furthermore: a conditioning network of the comparator circuits, a counter 82 of the performed printings having a capacity of counting to 160, a second comparing circuit 83 of 7 bits, a first decoder 84 of the "space" code, a logic unit 85 for printing termination and errors, a character register 93, a second decoder 94 of the space code, and a circuit 95 for the preparation of the print orders. The conditioning network consists of four AND gate circuits 81, 86, 87, and 88.

The circuits AND 81, 86, and 87 are of the type having two inputs. To the first input of these circuits a signal ΔC_1 is applied whose function it is to indicate that the installed type-holding unit is of the kind in which the characters are repeated with the same frequency. This signal may be applied automatically since the type-holding unit is built so as to close a signalling circuit, though it may be applied by the data processing unit which monitors the printing operations, or it may be applied by a manual presetting which closes a suitable switch and connects this input with an appropriate voltage source.

The circuit AND 88 is of the three input type. A signal ΔC_2 whose function it is to indicate that the installed type-holding unit is of the kind in which the characters are repeated with a different frequency is applied to an input of the circuit AND 88. This signal which alternates with ΔC_2 and excludes it may be applied in the forms already mentioned for the signal ΔC_1 , or one of the two may be derived from the other by a single logical inversion. A signal ΔC_3 whose function it is to indicate that the character whose correct code was presented to the comparison circuit is not repeated is applied to a second input. The signal consists of one of the bits retrieved from the buffer 31 which under these circumstances takes on the role of an identification or discrimination bit among the repeated and not re-

peated characters, and in the example represents the more significant bit. In fact, when the characters are repeated the type-holding unit in the given example contains only 64 characters, hence 6 bits are sufficient for their identification. The weighted bit 32 of the order number generated by the counter 11 is applied to the third input. The same bit is also applied to the second output of the circuit AND 86. The more significant bit of the order number generated by the counter 11, however, is applied to the second input of the circuit AND 87.

Finally, the more significant bit of the character code, thus corresponding with the signal ΔC_3 , is applied to the second input of the circuit AND 81. The outputs of the two circuits AND 86 and 88 are applied in parallel to the comparison circuit corresponding with the input of the weighted bit 32, and the output of the circuits AND 87 and 81 is applied to the comparison circuit corresponding with the input of the more significant bit, on the one hand, of the input of the order number and, on the other hand, of the character code.

The operation of the described logic system and the printer controlled by it is as follows.

First of all, the conditioning network is arranged with the signals ΔC_1 or ΔC_2 according to the type of type-holding unit which is installed on the printer. The data to be printed is then stored, over the transmission channel BO and the logical write circuit 80, in the buffer 31. Parallel with this phase, all space signals, identified by a pre-established representative code, which is not subjected to corrections as a function of the printing position, so that it remains unchanged and, therefore, easily discernible by means of a decoder circuit, are recognized by the circuit 84 and for each of these a pulse is transmitted to the counter 82 over the circuit OR 92. The space code may for example consist of the code of 7 bits 1111111.

The counter 82, preadjusted in the condition "reset" at the start of the loading of the buffer 31, performs the counting of all pulses corresponding with the spaces available in the printing line.

Parallel with the loading phase of the buffer 31, the counter 11 always evolves in like manner to provide at any moment over the order numbers information of the position of the type-holder unit. As soon as the loading of the buffer 31 is completed the printing operations begin.

First of all, simultaneously with the application of a timing signal ΔP and due to a go signal CON originating from the data processing system the order number C present at the start of the printing operations in the counter 11 is stored in the register 93. Then the go signal is given to the read operations of the buffer, timed by the already described oscillator circuits. If the signal ΔC_1 is present the comparison between the order number and the codes retrieved from the buffer is carried out completely, in fact, the circuits AND 81, 86, 87 are now enabled to transfer bits applied to their second input. But, when the signal ΔC_1 is absent the signal ΔC_2 will be present, the comparison of the more significant bit will be excluded, while the one of the weighted bit 32 will only be permitted when the signal ΔC_3 is also present or only for characters of a single repetition. The comparison operation is repeated for each order number C produced by the counter with all codes stored in the buffer 31.

Whenever the result of the comparison is positive, a print order is issued over the circuit AND 95 (which is now assumed to be capable of signal transmission) and this order is applied over the wire 91 and the circuit OR 92 to the counter 82 which adds to the already performed count of the spaces, the count of the already performed impressions. To prevent the space code from giving use to a print order following a positive comparison with the corresponding order number, this code is decoded by the decoder circuit 94 which blocks the circuit AND 95 thereby inhibiting the eventual print order to be transmitted downstream.

The presence of the conditioning circuit is also important to prevent the repeated printing in the same printing position of the same character which may be ascertained by the effect of the repetition on the type-holding unit of the same character. To avoid this inadequacy it must be realized that the print orders are sent over the wire 90 to the auxiliary storage 31 where they cancel the character code as soon as it has been compared, and replace it with the registration in the corresponding storage position of the code representative of one space. Therefore, when the comparing operation is subsequently repeated between the content of the same storage position and the successive order numbers the printing of an already printed character cannot be repeated again.

When all printings of a printing line are completed the counter 82 finishes its count up to 160 and emits on wire 96 a print termination signal which is received by the print termination logic circuit 85 and is transmitted to the data processing system to inform it that the printing has been correctly accomplished. After this signal, the printing of a new printing line may be ordered. In the meantime, the various order numbers C produced by the counter 11 are compared in the comparing circuit 83 with the character code stored in register 93. The counter 11 develops, in a cyclical fashion, a period which depends on the number of characters present on the type-holder unit, irrespective of its counting capacity. In fact, the reset signal ΔS modifies the length of the counting cycle, adapting it to different cases.

It is, therefore apparent that when the counter 11 generates an order number C which agrees with the one stored in the register 93 the type-holding unit has presented all characters of the set in all printing positions and that the printing of the printing line should be completed. The positive result of the comparison carried out by the circuit 83 is thus transmitted to the completion of print logical circuit 85 where it is used to generate an error signal. This kind of positive result is obviously verified only in conditions of malfunctioning in that, as already mentioned, the end-of-print signal is given by the counter 82 before or, at the latest, at the completion of a counting cycle of the counter 11.

We may now consider briefly a parallel drum printer in which the invention is applied.

FIG. 8 illustrates schematically a drum printer and its logic organization. Only elements essential for an understanding of the printer are shown.

The mechanics of the printer consist of a rotating drum 100 on whose circumference are as many sets of types arranged as there are printing columns. Close to the drum and linked with its generator are the printing hammers m positioned, one for each column of print. Between the hammers and the type-holder drum, the printing support is inserted and possibly the ink ribbon.

The drum is kept in rotation by a motor 101 so that the various types place themselves sequentially along the printing line.

Along with the drum an indented or perforated timing disk revolves linked with a photo-sensitive magnetic pickup or firmly attached equivalent. The pick-up 102 fills the same function as the pickup 10 of FIG. 7, i.e., emits a pulse each time the characters are aligned in printing position. These pulses are applied to a counter 11 which creates and sends out an order number which permits the identification of the types aligned in printing position. In this case too, a pickup 103 is provided which issues a reset pulse to the counter 11 to identify the start of the type set.

The codes of the characters to be printed in a printing line are stored over a data input channel BO in a storage buffer 31 from which they are retrieved singly and compared with the order number produced by the counter 11 in the comparison circuit 48. When the comparison is positive, the printing in the assigned printing position is ordered over the wire 104 and the selection network 105 of the hammers. Also in this instance the printing speed is known to increase when forward movement of the printing support is ordered and printing the next line is started as soon as the printing of a line is completed, without waiting for the completion of a complete rotation of the type-holding unit.

From this follows, as already described for chain printers, the count of the printing orders and the order of the count of blank spaces in a line. The count is performed by the counter 106 which receives pulses corresponding with the printing orders over the wire 107, and over wire 108 pulses derived from the signals present in the input channel BO, by means of the completed decodification in the decoder 109, each corresponding with a space of the printing line. When the count of the counter 106 attains the equivalent of the printing positions of a line, this means that the printing of the line has been completed. The printing support may now be moved ahead and, as soon as possible, the printing of the subsequent line may begin.

A further increase in speed may be achieved if certain characters are repeated within a set of characters with a higher frequency. When for example, an alpha-numerical printer has to print only numeric characters, it is useful if the numerical characters are repeated in the set with a higher frequency. In this case the counter 11 will associate a plurality of various order numbers with the same numeric character, while the code representative of the character will only be one. In this case, too, then the described invention may be applied or one may provide an additional recognition index for each character code which is used to modify the comparing conditions of the comparator circuit 48.

Into the schematic drawing of FIG. 8 must be introduced the parts and variants, already illustrated in FIGS. 5, 5a, 5b, and the obvious modifications of the latter, which are schematically drawn in FIG. 8 from the added buffer column for the identification indices and from the conditioning wire 160 of the comparing circuit 48. It must be noted, moreover, that in this case the character code is not corrected to keep count of the printing position and that the order number assigned to a character on the type-holder unit is not used for the printing of different characters, but only for the specific character represented by it. In this case, therefore, for the recognition of the repetition frequency of char-

acters one may indiscriminately use either an additional recognition code, such as the order numbers, or the character codes.

Let us consider for example Table 1. In this table the characters of a double repetition frequency are linked with binary order numbers which differ for the same character, only by the more significant bit. These characters, moreover, are distinguished from those of a simple repetition frequency by the fact that they are the only ones having the weighted bit 16 equal to 0. Such a discrimination element may be used to prevent the comparison of the more significant bit, and this condition may be imposed equally by the counter 11 and by the buffer 31.

The first solution is shown in FIG. 9. The counter 11 is broken up in its binary cells: the wire 116 which applied the weighted bit 16 stemming from the counter 11 to the comparison circuit 48 also initiates transmission of the signal of the output of the circuit exclusive or 112 to the circuit NOR 57 over the circuit AND 111. Therefore, when the weighted bit 16 is 0 the comparison circuit 48 behaves as if the more significant bits had not been compared.

The same result is obtained with the logical scheme of FIG. 10. In this case, it may be observed that the comparison circuit 48 is modified by the weighted bit 16 originating from the buffer 31. It is evident that rather than modifying the comparison circuit in the described manner, one may use circuits similar to those shown in FIGS. 5a and 5b, or modify, if so desired, the character codes, or the order numbers applied to the comparison circuit.

To conclude the exemplified review of the possible applications of the invention, we may consider a serial printer, schematically illustrated in FIG. 11. The illustrated form of construction was chosen because of its simplicity of representation. It should not be deemed — this is repeated — limitative of the objectives of the invention.

In FIG. 11 a type-holding unit 150 in the shape of a cylindrical drum having the types arranged on its circumferential rim, is rotated by a motor 151 and sequentially presents the various types corresponding to a printing position identified by the printing hammer 152. Between the type-holding unit 150 and the printing hammer 152 is inserted the printing support 153, for example in the form of a tape. Whenever an impression has been made, the tape is made to advance one printing position, for example by the action of small advancing rollers 154 one of which is intermittently activated by a motor 155.

It is apparent that in other versions it could be the type-holding unit which moves together with the printing hammer, both being installed on one or several printing carriages.

Generally, a timing wheel 156 with a respective pickup 157 is linked to the type-holding unit 150. The pulses produced by the pickup 157 are applied to the counter 11 whose output is compared in the comparison circuit 48 with the content of the storage 158, which is the code representing the character to be printed. When the comparison is positive, or when the type-holding unit presents the character to be printed in printing position, the impression is ordered.

It is evident also that the considerations already discussed may be applied in this case, or an increase of the printing speed may be achieved in many other cases by

repetition of the types on the type-holder unit having a varying frequency and it is, moreover, clear that provision may be made for their recognition with the devices which have been illustrated. Such devices are shown in general by a decoder network 159 which decodes the character code stored in a register 158 and conditions the comparing network 28 in a suitable manner.

What is claimed is:

1. A high speed printer comprising:
 - a mobile type-holding unit having a plurality of different type characters, each of said characters identified by a binary code and at least one of said type characters being represented more than once,
 - printing means for printing said type characters in different printing positions along a print line,
 - timing means for generating a plurality of signals to control operation of said high speed printer,
 - counter means, responsive to one of said plurality of signals of said timing means, for supplying an order number indicating the position at which one of said type characters is arranged on said type-holding unit,
 - storage means for storing a plurality of binary codes representative of said plurality of characters in addition to an information bit indicating said one character represented more than once, said storage means supplying one of said binary codes, in response to a second of said plurality of signals of said timing means,
 - comparing means, responsive to said order number of said counter means and said one binary code of said storage means, for providing a signal enabling said printer means to print a type character corresponding to said one binary code, and
 - conditioning means coupled to said storage means for inhibiting a predetermined portion of said binary code in response to said information bit provided by said storage means, said comparing means in response to said conditioning means enabling a signal corresponding to either of said binary codes of said one type character to be provided to said print means.
2. The printer as defined in claim 1 wherein said conditioning means further includes:
 - means responsive to said storage means for preventing a repetition of said one character in the same printing position.
3. A high speed printer comprising:
 - a mobile type-holding unit having a plurality of different type characters, each of said type characters identified by a binary code,
 - printing means for printing said type characters in different printing positions along a print line,
 - timing means for generating control signals,
 - counter means, responsive to one of said control signals, for supplying an order number indicating the position at which one of said type characters is arranged on said type-holding unit,
 - storage means for storing a plurality of binary codes representative of said plurality of type characters in addition to at least one information bit indicating type characters provided on said type-holding unit more than once, said storage means supplying one of said plurality of binary codes, in response to a second control signal of said timing means,
 - comparing means, responsive to said order number of said counter means and said binary code sup-

plied by said storage means, for providing a signal enabling said printer means to print a type character corresponding to said one binary code,

conditioning means, coupled to said storage means and responsive to said at least one information bit, for inhibiting a portion of said binary code determined by said at least one information bit, said comparing means in response to said conditioning means comparing only the remaining portion of said one binary code.

4. The printer as defined in claim 3 wherein said remaining portion of said one binary code corresponds to remaining portions in others of said binary codes, and wherein said remaining portions identify identical type characters.

5. The printer as defined in claim 3 wherein one information bit indicates a type character represented twice on said holding unit and wherein more than one information bit indicates the repetition frequency of the type characters on said type-holding unit.

6. The printer as defined in claim 5 wherein said conditioning means includes:

means responsive to said storage means for preventing said type characters represented more than once to be supplied to a same printing position.

7. A high speed printer comprising:

a mobile type-holding unit having a plurality of different type characters, each of said type characters identified by a binary code,

printing means for printing said plurality of type characters in different printing positions along a print line,

timing means for generating control signals,

counter means, responsive to one of said control signals, for supplying an order number indicating the position of said plurality of type characters on said type-holding unit,

storage means for storing a plurality of binary codes representative of said plurality of type characters in addition to at least one information bit indicating type characters provided on said type-holding unit more than once, said storage means supplying one of said plurality of binary codes in response to a second control signal of said timing means,

comparing means, responsive to said order number of said counter means and said binary code supplied by said storage means, for providing a signal enabling said printer means to print a type character corresponding to said one binary code, and

conditioning means, coupled to said storage means, for modifying a predetermined portion of said order number in response to said information bit, said comparing means in response to said conditioning means comparing only the remaining portion of said order number.

8. The printer as defined in claim 7 wherein said remaining portion of said order number corresponds to identical type characters provided by said type-holding unit.

9. A parallel printer for printing a line of characters along a printing line, said printer comprising:

a drum type holder unit having an axis parallel to said printing line, said drum unit having a plurality of type characters distributed on cylindrical rings with a variable frequency,

timing means for generating control signals indicating the movement of said type-holding unit,

counter means, responsive to said control signals, for supplying an order number indicating the position of said type-holding unit and the position of said plurality of type characters arranged on said type-holding unit,

storage means for storing a plurality of binary codes representative of said plurality of type characters in addition to an information bit indicating type characters provided on said drum unit more than once, said storage means supplying one of said plurality of binary codes, in response to a second control signal of said timing means,

comparing means, responsive to said order number of said counter means and said binary code supplied by said storage means, for providing a signal enabling said printer means to print a type character corresponding to said one binary code, and conditioning means, coupled to said storage means, for inhibiting a predetermined portion of said binary code in response to said information bit, said comparing means in response to said conditioning means comparing only the remaining portion of said one binary code.

10. A high speed printer comprising:

a continuously moving type-holding unit having a plurality of different type characters distributed with a variable frequency attached thereto, said type-holding unit presenting sequentially in at least one printing position said type characters arranged on said type-holding unit,

timing means for generating control signals,

counter means, responsive to one of said control signals, for supplying an order number indicating the position of said type characters on said type-holding unit,

storage means for storing a plurality of binary codes representative of said type characters in addition to at least one information bit indicating type characters provided on said type-holding unit more than once, said storage means supplying one of said plurality of binary codes, in response to a second control signal of said timing means,

comparing means, responsive to said order number of said counter means and said binary code supplied by said storage means, for providing a signal enabling said printer means to print a type character corresponding to said one binary code, and

conditioning means, coupled to said storage means, for modifying a predetermined portion of said binary code in response to said information bit, said comparing means in response to said conditioning means comparing the remaining portion of said one binary code.

11. A control circuit for a high speed printer having a moveable type carrier including a plurality of different type characters distributed with variable frequency and printing means for printing said type characters on a print line, said circuit comprising:

timing means for generating signals indicating the movement of said type carrier,

counting means responsive to said signals of said timing means for providing an order number indicative of the position of said type carrier and the position of said type characters thereon,

means for comparing said order number with coded representations of various type characters to be printed in different printing positions,

storage means for storing at least one of said coded representations and for transmitting one of said coded representations to said comparing means, discriminating means for distinguishing between various type characters in accordance with the type character's repetition on the type carrier, and conditioning means responsive to said discriminating means, for modifying said comparing means as a function of the repetition frequency of a type character on the type carrier.

12. The control circuit as defined in claim 11 and further including:

means responsive to said discriminating means for modifying said coded representation of said type characters, and

means responsive to said storage means for preventing a repetition of the printing of the same type character in the same position.

13. The control circuit as defined in claim 11 wherein said discriminating means is responsive to at least one information bit linked with said coded representations of said storage means, and

wherein said condition means comprises logic circuits operating selectively on a portion of said comparing means for inhibiting the comparison.

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