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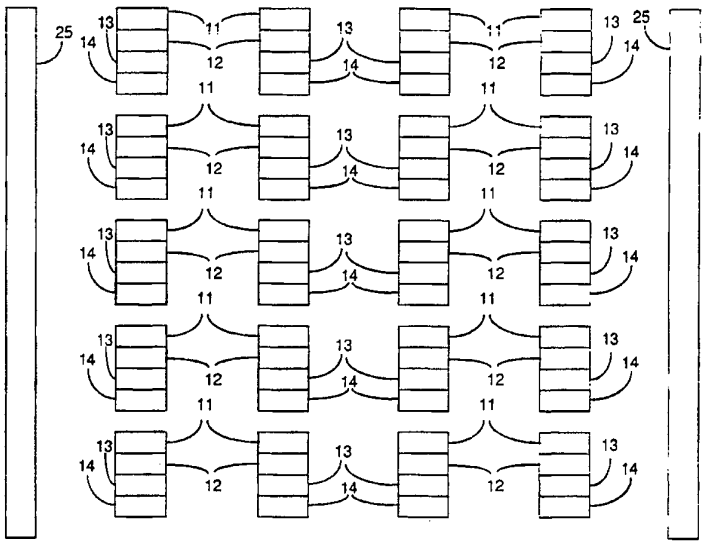
(54) Title: BRIGHT FIELD WAFER TARGET



(57) Abstract

A composite target used in alignment of layers (22-26) on a wafer uses alignment marks placed in a target area (9, 10). First alignment marks (11) are composed of material from a first layer (22) placed on the wafer. As subsequent layers (22-26) are placed on the wafer, alignment marks composed of material from the subsequent layers (23-26) are placed within the target area (9, 10). For example, alignment marks (12) composed of material from a second layer (23) are each placed adjacent to one of the alignment marks composed of material from the first layer (22). Alignment marks (13) composed of material from a third layer (24) are each placed adjacent to one of the alignment marks composed of material from the second layer (23). Alignment marks (14) composed of material from a fourth layer (25) are each placed adjacent to the alignment marks composed of material from the third layer (24). And so on. The alignment marks (11-15) are, for example, each rectangular in shape.

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BRIGHT FIELD WAFER TARGET

Technical Field

This invention relates generally to processing integrated circuits and more particularly to auto alignment marks used to align layer placement during processing of wafers.

Background

When processing wafers, targets are placed to assure each layer is properly aligned with respect to prior layers. Within the targets, alignment marks are placed. Layers placed subsequent to the alignment marks, utilize the alignment marks for proper placement. The subsequent layer can then be aligned to the mark within an alignment error. The alignment error results from the error tolerances of the processing devices. See for example, Canon Reticle Alignment for Canon I-2000/I-2500 Stepper Model, available from Canon U.S.A. having a business address of 2051 Mission College Blvd., Santa Clara, CA 95054.

For example, in a first layer, master marks may be placed in each target. Subsequent layers are all aligned to these first layer master marks. This assures that every layer subsequent to the first layer will be aligned to the first layer within the alignment error. However, one problem with such a master mark alignment system is that the total alignment errors between layers other than the first layer is the square root of two times the alignment error. Thus immediately adjacent layers may be misaligned an amount up to the square root of two times the alignment error. In some processes this amount of error between adjacent layers may be excessive.

Alternately, each layer may include alignment marks for each target. Each layer is aligned using alignment marks composed of material from the immediately prior layer. This guarantees that immediately adjacent layers are misaligned at most an amount equal to the alignment error.

However, use of such a sequential mark alignment system may result in a "walking error" wherein misalignment between layers which are not immediately adjacent to one another can be significantly larger than the alignment error.

Disclosure of the Invention

In accordance with the preferred embodiment of the present invention, a target used in alignment of layers on a wafer is presented. Within a target area, alignment marks are placed. The alignment marks are composed of material from a first layer placed on the wafer. Also within the target area, as subsequent layers are placed on the wafer, alignment marks composed of material from the subsequent layers are placed within the target area. For example, alignment marks composed of material from a second layer are each placed adjacent to one of the alignment marks composed of material from the first layer. Alignment marks composed of material from a third layer are each placed adjacent to one of the alignment marks composed of material from the second layer. Alignment marks composed of material from a fourth layer are each placed adjacent to one of the alignment marks composed of material from the third layer. And so on. In the preferred embodiment of the present invention, the alignment marks are each rectangular in shape.

The resulting composite target utilizes visible alignment marks for a multitude of layers. This combines the advantages inherent in a master mark alignment scheme and a sequential mark alignment scheme. The present invention is advantageous over the sequential mark alignment scheme as the present invention does not require a new target for every layer, thus saving space in the scribe lines.

Brief Description of the Drawings

Figure 1 shows two targets on the scribe lines of the device area on a wafer in accordance with the prior art.

Figure 2 shows alignment marks from a first layer placed on a target in accordance with the preferred embodiment of the present invention.

Figure 3 shows alignment marks from a second layer added to the target shown in Figure 1 in accordance with the preferred embodiment of the present invention.

Figure 4 shows alignment marks from a third layer added to the target shown in Figure 1 in accordance with the preferred embodiment of the present invention.

Figure 5 shows alignment marks from a fourth layer added to the target shown in Figure 1 in accordance with the preferred embodiment of the present invention.

Figure 6 shows alignment marks from a fifth layer added to the target shown in Figure 1 in accordance with the preferred embodiment of the present invention.

Description of the Preferred Embodiment

Figure 1 shows a target 9 and a target 10 on the scribe line of device area 8 of a wafer being processed in accordance with the prior art. Each of target 9 and target 10 are, for example, 120 micrometers by 50 micrometers.

In the preferred embodiment, a composite wafer target is partially built at each layer where an etch is performed. For example the layers may be composed of oxide, polysilicon, metal or some other material used in processing wafers. Figures 2 through 6 show processing stages of the composite wafer target in accordance with the preferred embodiment of the

present invention. The particular composite wafer target shown being processed is for a process in which five layers are etched.

Figure 2 shows target area 10 after a first layer is etched. After etching the first layer, alignment marks 11 are exposed within target area 10. Outside lines 22 from the first layer are also exposed. Each of alignment marks 11, for example, has a width of 1.2 micrometers and a height of 4 micrometers. In the shown example, Alignment marks 11 are separated from each other by a distance of, for example, 20 micrometers. While only 20 of alignment marks 11 are shown, a typical target may have, for example, more (or less) than twenty alignment marks for each layer.

Figure 3 shows target area 10 after a second layer is etched. After etching the second layer, alignment marks 12 are exposed within target area 10. Outside lines 23 from the second layer are also exposed. Outside lines 23 are placed directly over outside lines 22. Each of alignment marks 12, for example, has a width of 1.2 micrometers and a height of 4 micrometers. In the shown example, each of alignment marks 12 is immediately adjacent to one of alignment marks 11.

Figure 4 shows target area 10 after a third layer is etched. After etching the third layer, alignment marks 13 are exposed within target area 10. Outside lines 24 from the second layer are also exposed. Outside lines 24 are placed directly over outside lines 23. Each of alignment marks 13, for example, has a width of 1.2 micrometers and a height of 4 micrometers. In the shown example, each of alignment marks 13 is immediately adjacent to one of alignment marks 12.

Figure 5 shows target area 10 after a fourth layer is etched. After etching the fourth layer, alignment marks 14 are exposed within target area 10. Outside lines 25 from the second layer are also exposed. Outside lines 25 are placed directly over outside lines 24. Each of alignment marks 14, for

example, has a width of 1.2 micrometers and a height of 4 micrometers. In the shown example, each of alignment marks 14 is immediately adjacent to one of alignment marks 13.

Figure 6 shows target area 10 after a fifth layer is etched. After etching the fifth layer, alignment marks 15 are exposed within target area 10. Outside lines 26 from the second layer are also exposed. Outside lines 26 are placed directly over outside lines 25. Each of alignment marks 15, for example, has a width of 1.2 micrometers and a height of 4 micrometers. In the shown example, each of alignment marks 5 is immediately adjacent to one of alignment marks 14.

Embodiments of targets in accordance with the present invention may vary significantly. For example, the exact size of each alignment mark is not significant. Therefore, the height and/or width of alignment marks can vary from layer to layer. Likewise, the distance between the alignment can be varied to account for the addition alignment marks from more than (or less than) five layers.

The outside lines on the left and the right of the alignment marks are used to minimize resist pile up over the target. These all overlap at each masking layer. Even if the lines are broken, this will not impact the alignment of the layers.

The present invention presents a composite target in which alignment marks for each layer are visible for use in the alignment of subsequent layers. This system combines the advantages inherent in a master mark alignment scheme and a sequential mark alignment scheme.

The foregoing discussion discloses and describes merely exemplary methods and embodiments of the present invention. As will be understood by those familiar with the art, the invention may be embodied in other specific forms without departing from the spirit or essential characteristics

thereof. Accordingly, the disclosure of the present invention is intended to be illustrative, but not limiting, of the scope of the invention, which is set forth in the following claims.

Claims

I Claim:

1. A method for producing a target (11-15) used in alignment of layers (22-26) on a wafer, the method comprising the steps of:

(a) placing, within a target area (9,10), first alignment marks (11) composed of material from a first layer (22) placed on the wafer; and,

(b) placing, within the target area (9,10), subsequent alignment marks (12-15) composed of material from layers (22-26) placed on the wafer subsequent to the first layer (22), wherein the subsequent alignment marks (12-15) are placed in locations within the target area (9,10) which are different from locations within the target area (9,10) in which the first alignment marks (11) are placed.

2. A method as in claim 1 wherein step (b) includes the substeps of:

(b.1) placing, within the target area (9,10), second alignment marks (12) composed of material from a second layer (23) placed on the wafer subsequent to the first layer (22), each of the second alignment marks (12) being within the target area (9,10) and adjacent to one of the first alignment marks (11); and,

(b.1) placing, within the target area (9,10), third alignment marks (13) composed of material from a third layer (24) placed on the wafer subsequent to the second layer (23), each of the third alignment marks (13) being within the target area (9,10) and adjacent to one of the second alignment marks (12).

3. A method as in claim 2 wherein step (b) additionally includes the substep of:

(b.3) placing, within the target area (9,10), fourth alignment marks (14) composed of material from a fourth layer (25) placed on the wafer subsequent to the third layer (24), each of the fourth alignment marks (14) being within the target area (9,10) and adjacent to one of the third alignment marks (13).

4. A method as in claim 3 wherein the first alignment marks (11) placed in step (a) and the second, the third and the fourth alignment marks (12-14) placed in step (b) are each rectangular shaped.

5. A target (11-15) used in alignment of layers (22-26) on a wafer, the target (11-15) comprising: the steps of:

first alignment marks (11) composed of material from a first layer (22) placed on the wafer placed within a target area (9,10) in the wafer; and,

subsequent alignment marks (12-15) composed of material from layers (22-26) placed on the wafer subsequent to the first layer (22), the subsequent alignment marks (12-15) being placed in locations within the target area (9,10) which are different from locations within the target area (9,10) in which the first alignment marks (11) are placed.

6. A target (11-15) as in claim 5 wherein the subsequent alignment marks (12-15) include:

second alignment marks (12) composed of material from a second layer (23) placed on the wafer subsequent to the first layer (22), each of the second alignment marks (12) being placed within the target area (9,10) adjacent to one of the first alignment marks (11); and,

third alignment marks (13) composed of material from a third layer (24) placed on the wafer subsequent to the second layer (23), each of the third

alignment marks (13) being placed within the target area (9,10) adjacent to one of the second alignment marks (12).

7. A target (11-15) as in claim 6 wherein the subsequent marks additionally include:

fourth alignment marks (14) composed of material from a fourth layer (25) placed on the wafer subsequent to the third layer (24), each of the fourth alignment marks (14) being placed within the target area (9,10) adjacent to one of the third alignment marks (13).

8. A target (11-15) as in claim 7 wherein the first alignment marks (11), the second alignment marks (12), the third alignment marks (13) and the fourth alignment marks (14) are each rectangular shaped.

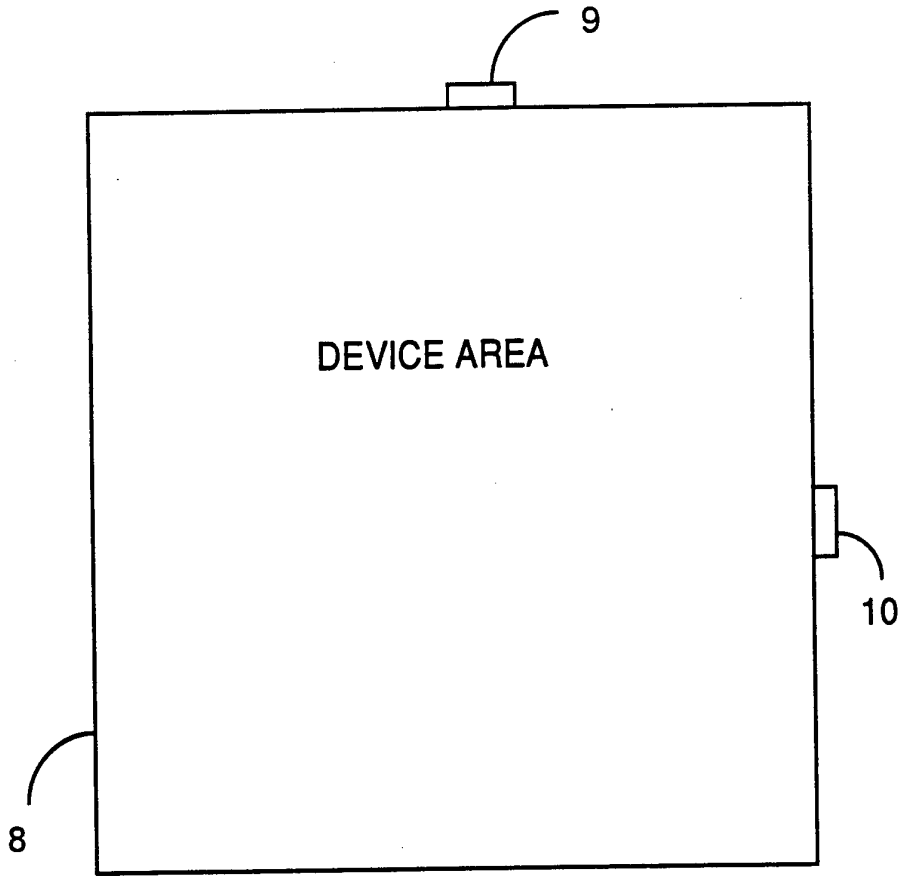


FIG. 1 (PRIOR ART)

FIG. 2

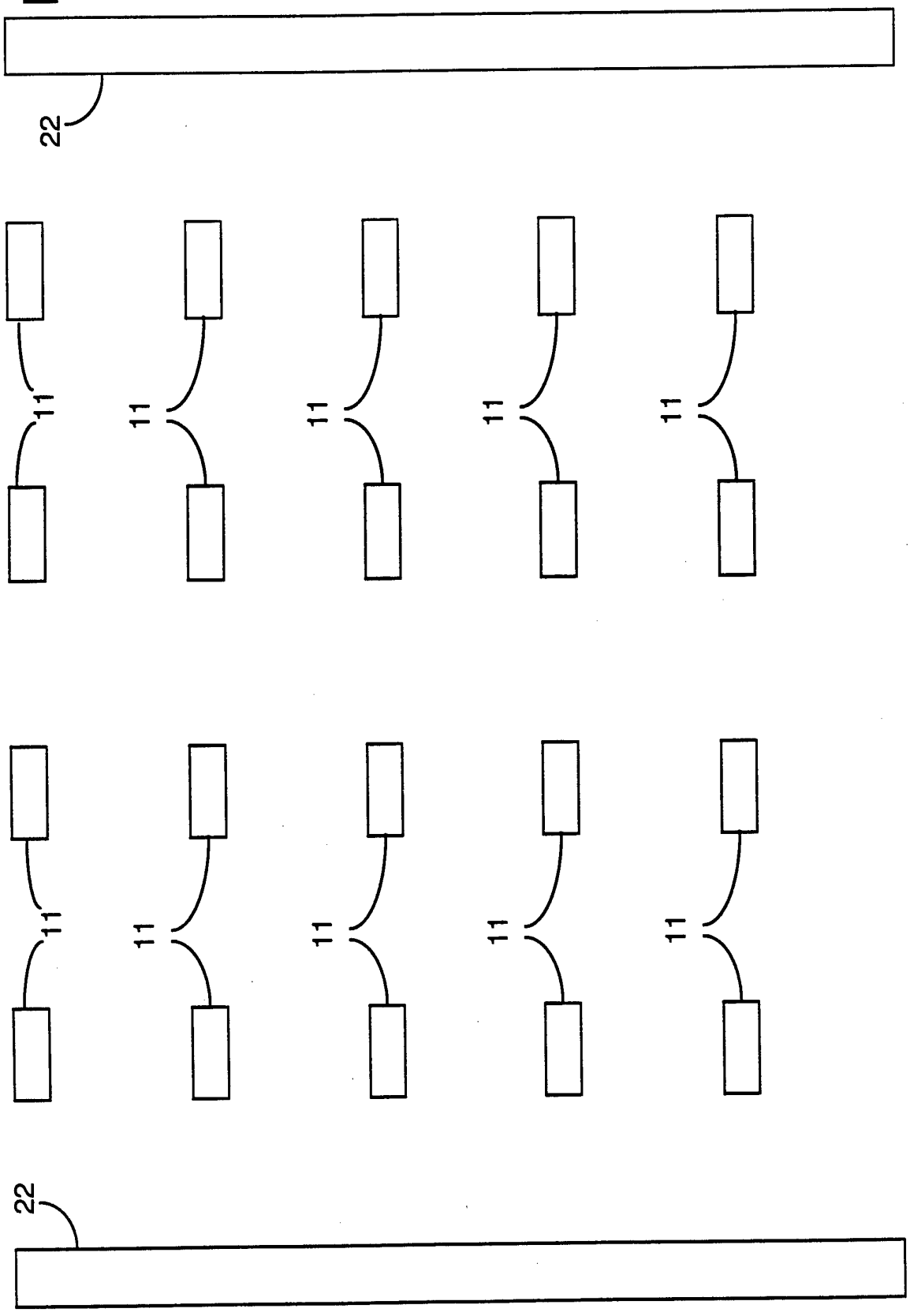


FIG. 3

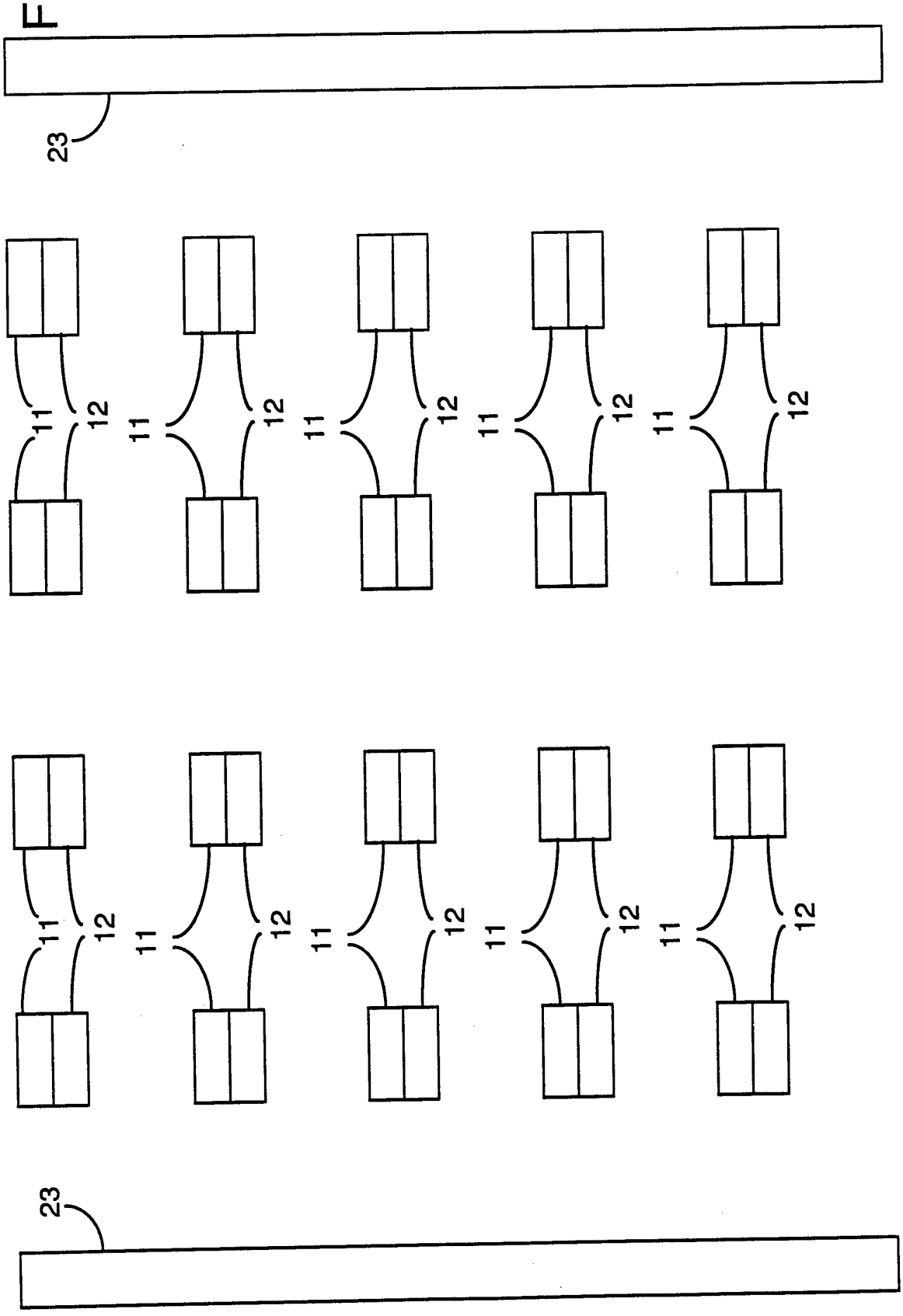


FIG. 4

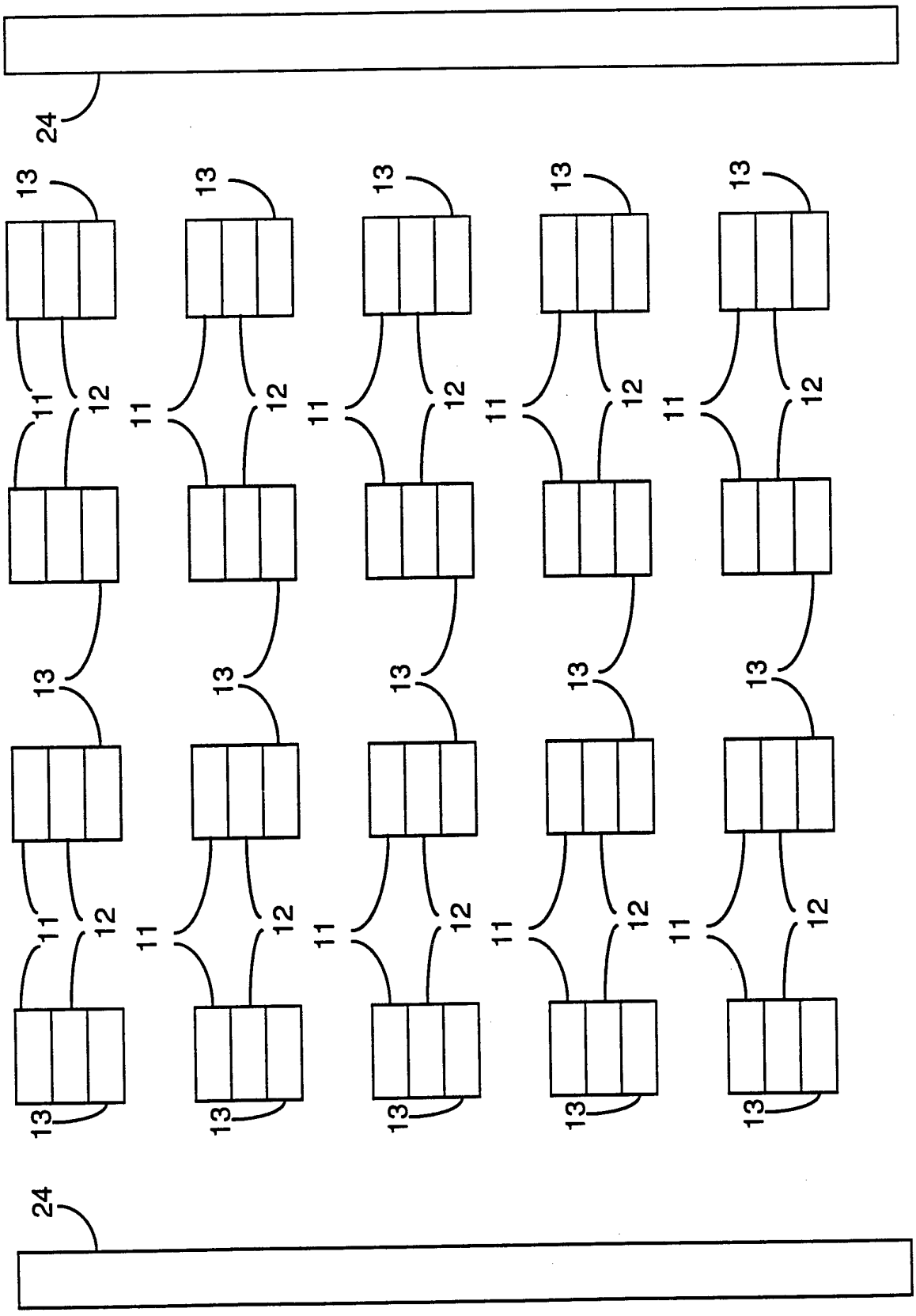


FIG. 5

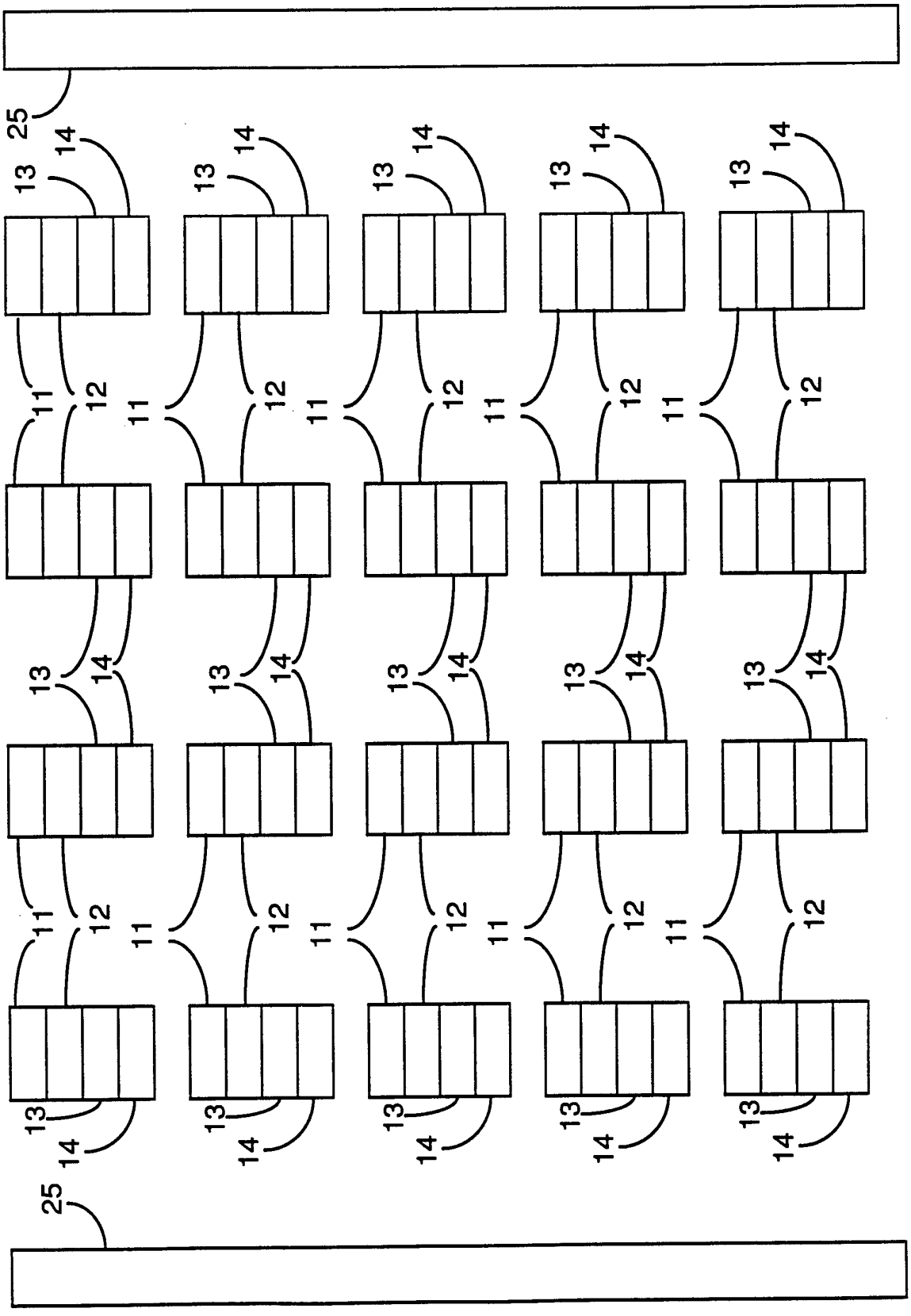
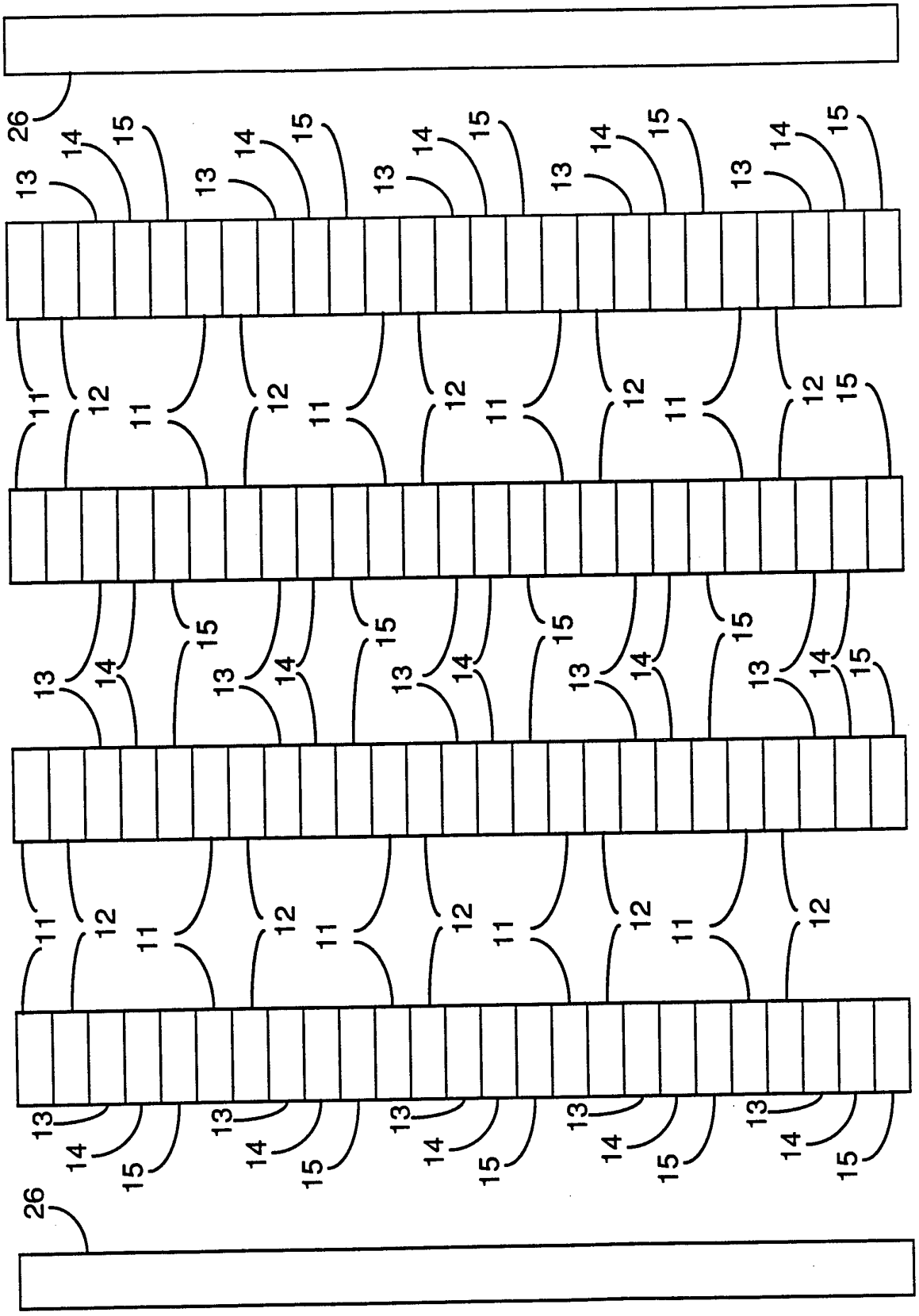


FIG. 6



INTERNATIONAL SEARCH REPORT

Interna l Application No
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A. CLASSIFICATION OF SUBJECT MATTER
IPC 5 H01L23/544

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 5 H01L

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Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US,A,4 343 877 (CHIANG) 10 August 1982 see the whole document ---	1-8
X	IBM TECHNICAL DISCLOSURE BULLETIN. vol. 13, no. 4 , September 1970 , NEW YORK US pages 955 - 956 S. MAGDO 'Registering Marks for Semiconductor Fabrication Masks' see the whole document ---	1-3,5-7
A	EP,A,0 061 536 (FUJITSU LIMITED) 6 October 1982 see abstract; claims; figures --- -/--	1-8

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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3 June 1994	14.06.94

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A	IBM TECHNICAL DISCLOSURE BULLETIN. vol. 18, no. 10 , March 1976 , NEW YORK US page 3306 G.F. DOLAN ET AL. 'Split Field Alignment Marks' see figure 2 -----	1-8

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Information on patent family members

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Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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EP-A-0061536	06-10-82	JP-C- 1369437	25-03-87
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		JP-B- 61035693	14-08-86
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