

[54] **SOLID STATE PHASE CONTROLLED SWITCH**

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[58] Field of Search. 307/252 N, 252 T; 323/18, 19, 323/22 SC, 24, 38, 34

[56] **References Cited**

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Primary Examiner—John Zazworsky

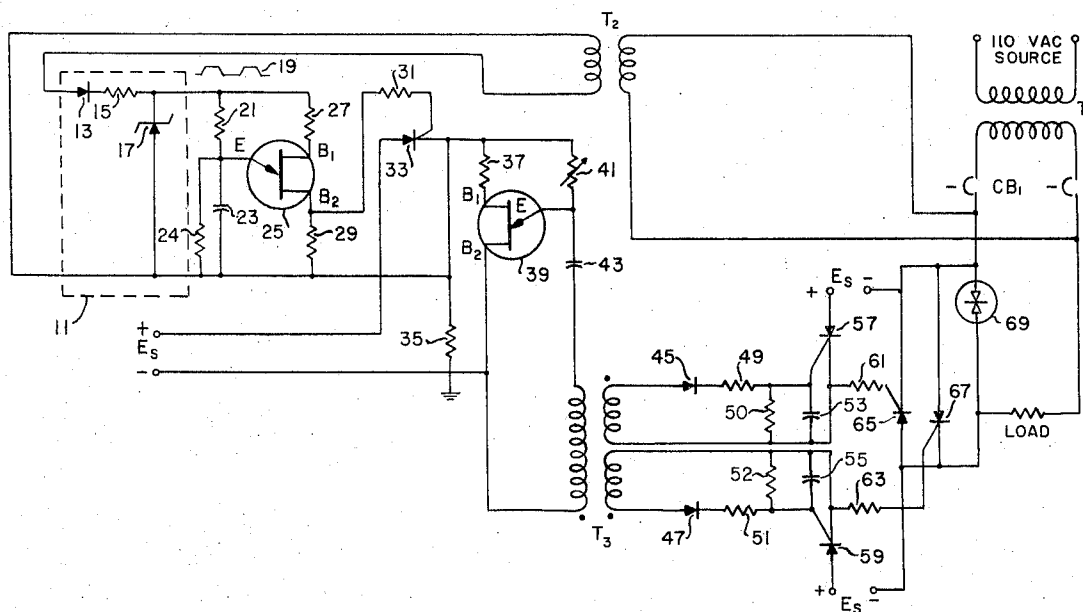
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[57]

ABSTRACT

A phase controlled switch connects a load to an A.C. power source at a particular phase angle of the power source. A first trigger signal referenced to a zero crossing region of the wave form is obtained. This first signal starts a timer which in turn generates a second signal. The variable timer can be preset to produce a delayed signal over a full period of the A.C. wave form. A latching switch system responsive to the timing signal connects the load to the power supply and holds the load connected until the power supply is physically disconnected from the load.

9 Claims, 2 Drawing Figures



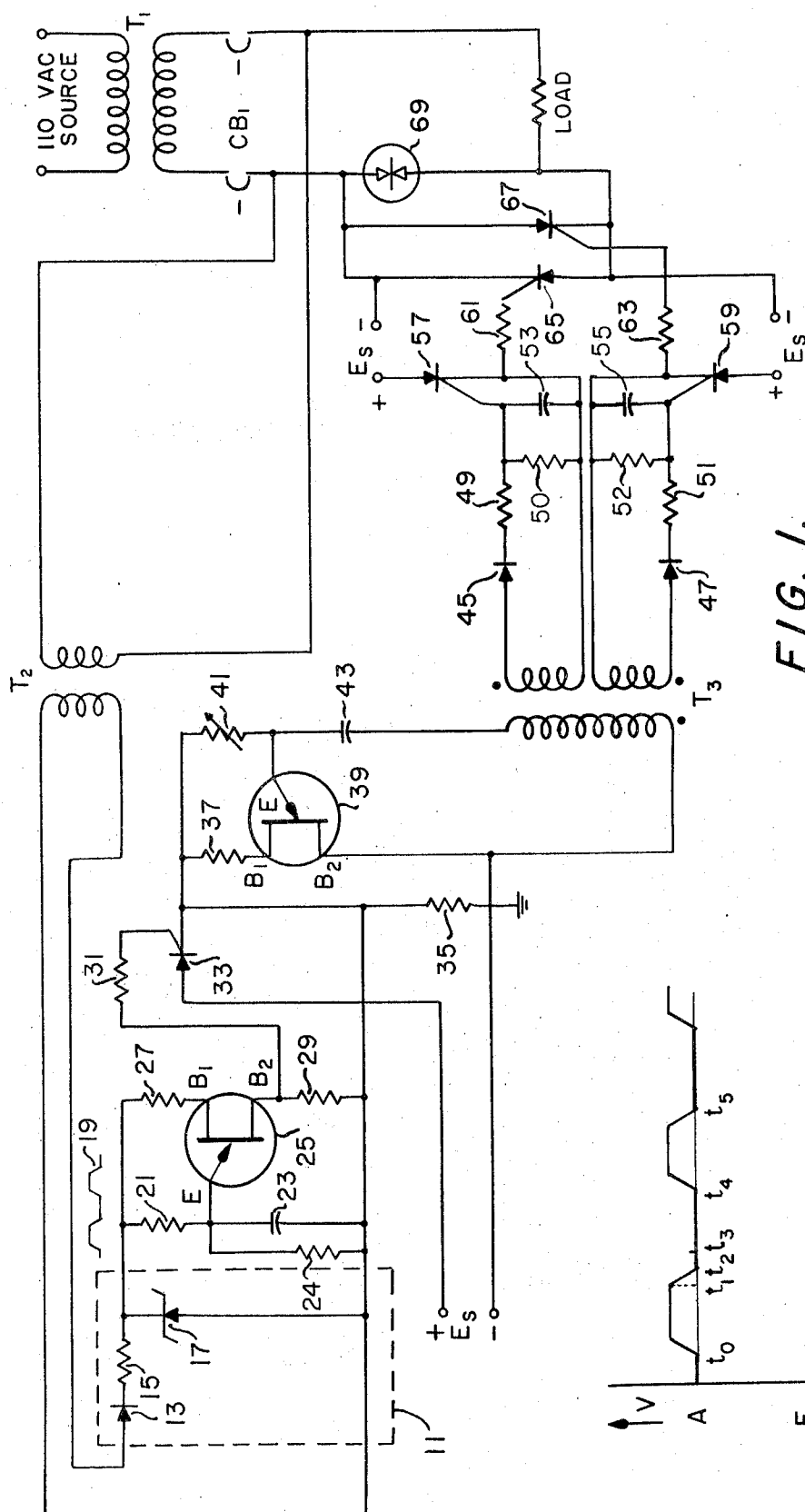


FIG. 1.

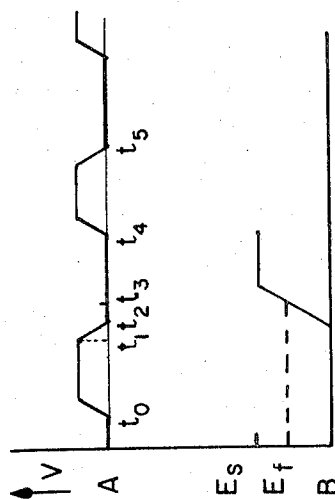


FIG. 2.

SOLID STATE PHASE CONTROLLED SWITCH

The invention described herein may be manufactured and used by or for the Government of the United States of America for Governmental purposes without the payment of any royalties thereon or therefor.

BACKGROUND OF THE INVENTION

The prior art includes a number of devices for switching a load to an A.C. source at a particular phase angle of the source. These devices commonly use pulsing triggers requiring multivibrators, differential amplifiers, or other comparator means and function generators. This invention accomplishes substantially the same result as other prior art devices but with smaller and more efficient circuits. The workings of the switch are digital in nature in that voltages are not compared but are seen by the subsystems within the switch as a substantially either "off" or "on" condition. This digital approach increases the reliability of the switch over the prior art as it is not as dependent upon tolerances within operating ranges of the components.

SUMMARY OF THE INVENTION

The switch is built of three basic blocks. The first block is a half wave rectifier and clipper which produces a half wave rectified wave form from the A.C. power source and then clips the positive portion of the rectified wave form to approximately 25 percent of its peak value. The resultant half wave clipped wave form is then substantially a squared wave form. By clipping the wave form at a low value, relative to the power source's peak value, the ascending and descending slopes of the wave form are kept at a maximum and are therefore substantially vertical, giving the clipped wave form the appearance of a square wave.

The clipped wave form is connected to the emitter of a unijunction transistor and to a capacitor connected from the base of the unijunction transistor to ground. The time interval corresponding to the descending edge of the clipped wave form is instantaneous relative to the period of the A.C. wave form. At this interval, the base to base voltage across the unijunction transistor drops so that the voltage stored at the emitter fires the unijunction transistor causing it to generate a turn on or first trigger signal to an SCR.

The "turned on" SCR then applies a D.C. voltage to a timer circuit which in turn triggers a switch connecting the load to the A.C. source at a predetermined time subsequent to and delayed from the trigger signal of the first unijunction transistor.

The trigger pulse of the first unijunction transistor is a reference pulse which always occurs at the descending edge of the clipped wave form and substantially at the zero crossing point of the A.C. wave form corresponding to the descending edge. The time delay signal then represents a predetermined interval of time subsequent to the first trigger pulse. The time delay circuit may be set to produce a signal immediately following the reference first trigger signal or at the end of a full period of the A.C. wave form. In this manner, a time delay signal may be generated at any point in time over a full period of the A.C. wave form and, if reason demands it, may even be extended beyond one full period to a number of periods of the A.C. wave form.

The switching circuit includes a transformer having one primary and two secondary windings so that two

voltages may be independently generated for closing respective SCR switches on each side of the load. Latching SCRs are provided in the switches so a switch is closed and held closed after the latching SCRs are turned on and independent of the subsequent excursions of the A.C. wave form or the pulses generated by the time delay circuit.

BRIEF DESCRIPTION OF THE DRAWING

FIG. 1 shows the phase controlled switch in schematic form.

FIG. 2 is a time diagram of the rectified and clipped wave form, numeral 19 of FIG. 1.

DESCRIPTION OF THE INVENTION

A power source, in this case, a 110 volt A.C. source, is connected to a load through a transformer T1, circuit breaker CB1, and SCRs 65 and 67. The phase controlled switch, turning on SCRs 65 and 67 and connecting the power source to the load, is energized from the power source through transformer T2.

A first block of the switch is the half wave clipper represented by the box in dashed lines marked 11. It includes a diode 13 with its anode connected to the transformer T2 and is in series with a resistor 15. Connected across the output of the half wave rectifier is a zener diode 17 which clips the output of the half wave rectifier approximately 25 percent of its peak value. The output of the half wave rectifier and clipper is wave form 19.

The second block of the switch comprises unijunction transistor 25 and 39 for generating a first trigger signal referenced to a particular phase angle of the wave form 19 and for generating a delayed signal subsequent to the trigger signal of unijunction transistor 25. A resistor 21 is connected between the output of the half wave rectifier and the emitter of the unijunction transistor 25 and a capacitor is connected between the emitter and a common junction point at one side of resistor 35. The unijunction transistor base B1 is connected to the half wave rectifier through dropping resistor 27 and the base B2 is connected to the common junction point of resistor 35 through a second dropping resistor 29. The gate of SCR 33 is connected to B2 of unijunction transistor 25 by resistor 31. SCR 33, when in an "on" condition connects the D.C. source Es to resistors 41 and 37 of the timer unijunction transistor 39.

Resistor 35 acts as a dummy load maintaining the holding current of SCR 33 to prevent its turn off. Base B1 of unijunction transistor 39 is connected to SCR 33 by resistor 37 and base B2 is connected to ground. The emitter E of unijunction transistor 39 is connected to ground through a capacitor 43 connected in series with the primary winding of transformer T3.

The third block is the switch connecting the load to the source. It comprises transformer T3 having a single primary and two secondary windings for generating two secondary voltages with their polarities arranged to render diodes 45 and 47 conductive. Resistor 50 and capacitor 53 are connected to diode 45 and resistor 52 and capacitor 55 are connected to diode 47 to minimize switch closings due to transients. The output of diodes 45 and 47 are connected to the gates of SCRs 57 and 59 respectively. Each of these SCRs is connected to source Es and the cathodes of each of these SCRs are connected through resistors 61 and 63 re-

spectively to the gates of switching SCRs 65 and 67. A surge protector 69 is connected across the switching SCRs 65 and 67 to protect them from surges in the load.

OPERATION OF THE INVENTION

Closing of circuit breaker CB1 connects the 110 volt power source to the switch through isolation transformers T1 and T2. The half wave rectifier consisting of diode 13 and resistor 15 produces a half wave rectified wave which is then clipped by zener diode 17 to produce the wave form 19 shown in FIG. 1 and line A of FIG. 2. The period of the source is the time interval t_0 to t_4 . In the interval t_0 to t_1 , capacitor 23 charges to its maximum value through charging resistor 21. Also, within the interval t_0 to t_1 , unijunction transistor 25 is held "off" by the interbase voltage. The voltage drops across resistor 27, the unijunction transistor interbase resistance, and resistor 29 are such that the stored voltage across capacitor 23 is less than the intrinsic stand-off ratio of unijunction transistor 25 multiplied by the voltage drop across B1 and B2. Under this condition, the emitter E is reverse biased and only a small leakage current will flow. At the descending edge of the clipped wave form between t_1 and t_2 , the voltage across resistor 29 drops while the voltage at the emitter E will be temporarily held by capacitor 23. At this point, the voltage across the unijunction transistor base B2 multiplied by the intrinsic stand-off ratio is less than the stored voltage at capacitor 23 and unijunction transistor 25 is forward biased. Current then flows through resistor 29. The voltage generated across resistor 29 is the first trigger signal which is connected to the gate of SCR 33, turning on SCR 33 and so causing current to flow into the R-C charging circuit comprising variable resistor 41, capacitor 43 and the primary transformer T3. In addition, the voltage E_s applied to SCR 33 is impressed across the base of the unijunction transistor 39 through resistor 37, establishing an interbase voltage across B1 and B2 and reverse biasing the unijunction transistor. The voltage across capacitor 43 will be a ramp with respect to time as shown in line B of FIG. 2, having a maximum value substantially that of source E_s diminished by the voltage drop through SCR 33.

When the voltage across the capacitor 43 reaches a firing voltage E_s (the voltage across the bases B1 and B2 multiplied by the intrinsic stand-off ratio of unijunction transistor 39), unijunction transistor 39 will be forward biased and is turned on causing current to flow through the primary of transformer T3 and forward biasing at diodes 45 and 47.

These voltages at diodes 45 and 47 are applied through resistors 49 and 51 to the gates of SCRs 57 and 59 respectively. With SCRs 57 and 59 "turned on", a D.C. voltage from source E_s is applied to the gates of SCRs 65 and 67 through resistors 61 and 63 respectively. The operation of SCRs 57 and 59 is latching and once each of these SCRs are turned on, each will be held on, turning "on" and holding "on" SCRs 65 and 67 and holding them "on" as the A.C. wave form reverses polarity.

As shown in FIG. 2, line A, which is not to scale, the descending edge of the clipped wave form is substantially vertical and the wave form is substantially square. The time interval between t_1 and t_2 embracing the descending edge is instantaneous with respect to the total period of the A.C. wave form. The first trigger pulse

seen by SCR 33 is digital and it represents the instant in time when the clipped wave form 19 drops from its peak value to zero and provides references to the phase of the wave form at that point.

As the interval corresponding to the descending edge is substantially instantaneous, any variation in this interval or at the point in time when unijunction 25 is turned on, will be negligible with respect to the time delay interval subsequent to the first trigger signal.

Resistor 41 is adjusted to produce a ramp voltage at the emitter E of unijunction transistor 39 through the R-C timing circuit so that unijunction transistor 39 fires at voltage E_r appearing at the emitter E at a predetermined phase angle of the clipped wave between times t_2 and t_5 . The reaction of the latching at SCRs 57 and 59 and switching SCRs 65 and 69 is instantaneous with respect to the appearance of the time delay signal from unijunction transistor 39. The load then is connected to the source at a phase angle of the source corresponding to the predetermined delay signal appearing subsequent to the descending edge of the clipped wave 19.

What is claimed is:

1. A phase controlled switch comprising:

first means connected to an A.C. power source for generating a first signal coincident with a first predetermined phase angle of said A.C. source;

a second means connected to said first means for generating a signal responsive to said first signal and delayed in time with respect to said first signal; and

a switch means connected to said second means and responsive to said second signal for connecting a load to the A.C. source coincident with a second predetermined phase angle of said A.C. source and for holding said load connected to said A.C. source until and only until said A.C. source is physically disconnected from said load;

wherein said first and second predetermined phase angles are independent of the amplitude of said A.C. source and are predetermined before the switching on of said A.C. source.

2. The switch of claim 1, wherein:

said first means includes a half wave rectifier and a clipper for producing a half wave rectified and clipped wave form from said A.C. source.

3. The switch of claim 2 wherein:

said first signal generated by said first means is coincident with the phase angle defined by the zero cross of the descending edge of said clipped wave form; and

said wave form is clipped to produce a substantially squared wave form.

4. The switch of claim 3, wherein:

said second means is a variable timing circuit for producing said second signal delayed over a time range encompassing a period of said A.C. source.

5. The switch of claim 4, wherein:

said first means includes a first unijunction transistor;

a storage means connected between the emitter of said first unijunction transistor and ground for temporarily holding the voltage of the clipped wave form to fire said first unijunction transistor; and means for generating a first trigger signal responsive to said first unijunction transistor being fired.

6. The switch of claim 5, wherein:

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said timing means is a second unijunction transistor;

a variable resistor connected at one end to the emitter of said second unijunction transistor and connected at its other end to receive said triggering signal;

a storage means connected between the emitter of said second unijunction transistor and ground; and

said timing unijunction transistor being triggered and generating said delayed signal when said storage means connected to the emitter at said second unijunction transistor reaches the said second unijunction transistor firing voltage.

7. The switch of claim 6, wherein:

said switch means includes means responsive to said delayed signal for producing two switching signals;

each of said two switching signals being connected to respective latching gates; and

said latching gates being turned on in response to said switching signals and being held on independent of said A.C. wave form for connecting said power

source to the load.

8. The switch of claim 7, wherein:

said means for generating a first trigger signal is a SCR connected to said first unijunction transistor; and

said SCR connecting said variable resistor to a D.C. voltage source for triggering said second unijunction transistor in response to said firing signal from said first unijunction transistor.

9. The switch of claim 8, wherein:

said latching gates are a first pair of SCRs; and said switch means further including:

a second pair of SCRs, the anodes of each of said second pair of SCRs being connected between a respective side of said power source and the cathodes of each of said second pair of SCRs being connected to one side of said load for connecting said load to said power source; and

said second pair of SCRs being turned on and connecting said load to said source in response to said first pair of latching SCRs being turned on.

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