Abstract: Methods and apparatus are provided for modulating a data rate of a clock signal. A method of transmitting a binary signal is provided comprising the steps of generating (105) random bit periods for each of a first plurality of bits in the binary signal, complementing each bit period of the first plurality of bits in the binary signal with a different bit period in a second plurality of bits in the binary signal to produce complemented pairs, and transmitting (115) the binary signal having a data rate varying with the bit periods of the binary signal. Each of the complemented pairs has a total period substantially equal to a pre-determined period. A timing apparatus for modulating a data rate of a binary signal comprises a binary sequence generator (30) configured to randomly generate a binary sequence indicating a value for modulating a bit rate of each bit in the binary signal while maintaining a signal period of the binary signal, a digital-to-analog converter (DAC) (32) having an input coupled to the binary sequence generator and having an output, and a voltage controlled oscillator (VCO) (34) having an input coupled to the output of the DAC. The DAC is configured to produce a voltage in response to the value of the binary sequence. The VCO is configured to generate a modulated binary signal having a period varying linearly with the voltage.
SPREAD SPECTRUM CLOCK AND METHOD FOR MESSAGE TIMING IN A COMMUNICATION SYSTEM

FIELD OF THE INVENTION

[0001] The present invention generally relates to message timing in communication systems, and more particularly relates to methods and timing circuits for maintaining a constant message time in a communication system.

BACKGROUND OF THE INVENTION

[0002] Serial communication systems are generally simple to implement and thus popular for a variety of applications. One example of a serial communication system is a Master Control Unit (MCU) coupled in series with one or more slave devices, such as via a two wire bus. The MCU supplies power to the slave devices and also communicates with the slave devices via the two wire bus. In one example, the MCU and the slave devices interact sequentially in two phases. During the first phase, the MCU supplies power to all of the slave devices. During the second phase, the MCU communicates with one of the slave devices. Typically, the MCU communicates using a voltage based signal, and the slave devices respond using a current based signal.

[0003] One specific application of a serial communication system is with airbag deployment systems in automobiles. In airbag deployment systems, a master cylinder control unit is connected in series (e.g., via the two wire bus) with multiple accelerometer sensors placed around a vehicle. Each of the sensors is generally a low power device and typically bus powered by the master cylinder control unit. Despite the relatively low power provided along the two wire bus, one concern with communications between the master cylinder control unit and the sensors is with maintaining an adequate signal-to-noise ratio.

[0004] Interference such as electromagnetic radiation from the two wire bus may decrease the signal-to-noise ratio, in addition to electromagnetic radiation from other equipment residing in the vehicle, and thus a design consideration is to minimize the amount of energy radiated by the two wire bus. Serial communication systems include clocking circuitry to maintain synchronization of serial data, and the clocking circuitry may generate
interference. The clocking circuitry includes a driver that typically produces trapezoidal shaped pulses. These trapezoidal shaped pulses commonly generate impulse shaped spectral components at harmonics of the fundamental frequency (e.g., the bit rate of the serial data), and greater amplitudes of these spectral components may decrease the signal-to-noise ratio.

[0005] Apart from shielding the two wire bus, low radiation signaling methods and data whitening have been used to reduce the amount of energy radiated by the two wire bus. Low radiation signaling methods include current mode signaling, instead of voltage mode signaling, loop cancellation with twisted wires, and differential signaling. Data whitening refers to addressing data content to randomize the presence of zeros and ones and to suggest a resemblance to white noise. Both of these approaches may require additional complex circuitry to implement.

[0006] Accordingly, a method for randomizing the data rate in a communication system is desired that reduces the interference to the communication system. In addition, a circuit for modulating a data rate in a communication system is desired that reduces the interference to the communication system. Furthermore, other desirable features and characteristics of the present invention will become apparent from the subsequent detailed description of the invention and the appended claims, taken in conjunction with the accompanying drawings and this background of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] The present invention will hereinafter be described in conjunction with the following drawing figures, wherein like numerals denote like elements, and

[0008] FIG. 1 is a schematic diagram of a spread spectrum bus based communications system;

[0009] FIG. 2 is a schematic diagram of the timing circuit shown in FIG. 1;

[0010] FIG. 3 is a schematic diagram of an exemplary embodiment of a binary sequence; and
FIG. 4 is a flow diagram of a method for transmitting a binary message.

DETAILED DESCRIPTION

The following detailed description of the invention is merely exemplary in nature and is not intended to limit the invention or the application and uses of the invention. Furthermore, there is no intention to be bound by any theory presented in the preceding background of the invention or the following detailed description.

Referring to the drawings, FIG. 1 is a schematic diagram of a spread spectrum bus based communication system 10. The spread spectrum bus based communication system 10 comprises a Master Control Unit (MCU) 12 (e.g., a master cylinder control unit), a driver 14 having a first input coupled to MCU 12, a timing circuit 16 coupled to a second input of driver 14, and one or more slave devices 18, 20 coupled to an output of driver 14 via a communication bus 22 (e.g., a twisted wire pair). Spread spectrum bus based communication system 10 provides communication between MCU 12 to slave devices 18, 20 via communication bus 22 that is well-suited for implementation in various automotive control systems as well as other control systems. Each of slave devices 18, 20 may be coupled with a sensor 24, 26, respectively (e.g., an impact sensor for a vehicle), although other devices may be coupled with slave devices 18, 20 for communicating with MCU 12. MCU 12 communicates with and supplies power to slave devices 18, 20 via communication bus 22. During a communication phase, binary messages are transmitted between MCU 12 and slave devices 18, 20. Timing circuit 16 modulates a binary sequence to produce the binary messages in a signal transmitted at the output of driver 14. Slave devices 18, 20 extract the binary messages from this signal and communicate the content of the binary messages to sensors 24, 26. Although timing circuit 16 is described with regard to spread spectrum bus based communication system 10, timing circuit 16 may be implemented with a variety of communication systems using pulse width modulated communication.

FIG. 2 is a schematic diagram of an exemplary embodiment of timing circuit 16 shown in FIG. 1. Timing circuit 16 comprises a binary sequence generator 30 having an input configured to receive a clock signal, a Digital-to-Analog Converter (DAC) 32 having an output and having an input coupled to an output of binary sequence generator 30, and a Voltage Controlled Oscillator (VCO) 34 having an input coupled to the output of DAC 32, a
first output coupled to binary sequence generator 30, and a second output configured to couple with a variety of serial communications devices, such as slave devices 18, 20 via communications bus 22 shown in FIG. 1. Timing circuit 10 produces a signal at the second output of VCO 34 carrying a binary message. In an exemplary embodiment, timing circuit 16 is incorporated with a central communications control unit (e.g., MCU 12 shown in FIG. 1) that both supplies power to and communicates with other devices (e.g., slave devices 18, 20 shown in FIG. 1).

[0015] FIG. 3 is a schematic diagram of an exemplary embodiment of a binary sequence 40 for modulation by timing circuit 16 shown in FIG. 1. Binary sequence 40 comprises a sequence of bits (e.g., B1, B2, ... B12), and each bit has a time period (e.g., T1, T2, ...T12). Although binary sequence 40 is described as twelve (12) bits and twelve (12) corresponding time periods, binary sequence 40 may have any even number of bits and even number of corresponding time periods. Binary sequence 40 contains data for communication with the slave devices. For example, binary sequence 40 may contain a command from MCU 12 shown in FIG. 1 for extraction by slave devices 18, 20 shown in FIG. 1.

[0016] Referring to FIGS. 2 and 3, binary sequence generator 30 (e.g., a pseudo-random binary sequence generator) randomly generates the time periods for each of the bits of binary sequence 40 to produce a modulated binary sequence. In an exemplary embodiment, binary sequence 40 has a total time period, or signal period, that is pre-determined by a cyclical communication phase (e.g., between MCU 12 and slave devices 18, 20 shown in FIG. 1). This total time period is maintained in the modulated binary sequence for recovery of a relatively stable clock frequency by components of communications system 10 (FIG. 1). For convenience of explanation, binary sequence 40 is divided into a first half (e.g., low byte) and a second half (e.g., high byte). Binary sequence generator 30 randomly generates time periods for each of the bits in the first half of binary sequence 40, and each of these time periods is less than the total time period of binary sequence 40. In an exemplary embodiment, binary sequence generator 30 randomly generates a separate binary sequence, having a pre-determined value associated therewith, for each of the bits in the first half of binary sequence 40. While the random generation of time periods is described in the context of the first half, binary sequence generator 30 may also randomly generate the time periods for each of the bits in a first plurality of bits of binary sequence 40 regardless of the position of each of the bits in the first plurality in binary sequence 40. In this case, binary sequence 40 is grouped into the first plurality of bits and a second plurality of bits having an
equal number of bits as the first plurality of bits while occupying a different position in binary sequence 40.

[0017] After establishing the time periods for the bits in the first half of binary sequence 40, or first plurality of bits, binary sequence generator 30 then generates time periods for each of the bits in the second half of binary sequence 40 such that each time period in the first half of binary sequence 40 is complemented by a time period for a different bit in the second half of binary sequence 40. For example, binary sequence generator 30 randomly generates time periods (T1, T2, ... T6) for the first half of binary sequence 40, then selects time periods (T7, T8, ... T12) for the second half of binary sequence 40 such that T1+T7 = T2+T8 = T3+T9 = T4+T10 = T5+T11 = T6+T12 = a pre-determined constant time period. Although the time periods of the first half of binary sequence 40 are described as sequentially complementing the time periods of the second half of binary sequence 40, a variety of sequences (e.g., more random sequences) for complementing the time periods of the second half of binary sequence 40 may be used while maintaining the relationship of the complemented time periods (e.g., the sum of the time period for a bit in the first half of binary sequence 40 with the time period for a complementing bit in the second half of binary sequence 40 remains the pre-determined constant).

[0018] In an alternative embodiment, binary sequence generator 30 randomly generates bit rates for each of the bits in the first half of binary sequence 40 then generates bit rates for each of the bits in the second half of binary sequence 40 such that each bit rate in the first half of binary sequence 40 is complemented by a bit rate in the second half of binary sequence 40. When complementing each bit in the first half of binary sequence 40, binary sequence generator 30 maintains the sum of the bit rates (e.g., for a bit in the first half of binary sequence 40 with a complementing bit in the second half of binary sequence 40) at a pre-determined constant (e.g., the inverse of the pre-determined constant time period).

[0019] DAC 32 converts the value of each binary sequence generated by binary sequence generator 30 to a voltage. In an exemplary embodiment, DAC 32 has a transfer function for converting the value of each binary sequence to a pre-determined voltage. VCO 34 outputs a clock signal via the first output and a modulation signal via the second output. The modulation signal has a period that varies linearly with the voltage received from DAC 32. The modulation signal is combined with communication signals at driver 14 (FIG. 1) to produce a modulated communication signal such as a Pulse Width Modulated (PWM)
signal. For example, VCO 34 generates a square wave clock signal that is PWM based on the voltage from DAC 32. For PWM bus coding convention, VCO 34 outputs a logic one signal with a two-third (2/3) duty cycle pulse and outputs a logic zero signal with a one-third (1/3) duty cycle pulse.

[0020] FIG. 4 is a flow diagram of a method for transmitting a binary message (e.g., a PWM message). The method begins at 100. Referring to FIGS. 2 and 4, binary sequence generator 30 generates random bit rates for each bit in a first half of the PWM message at step 105. Alternatively, binary sequence generator 30 generates random time periods for each bit in the first half of the PWM message. The PWM message has a total time period, and binary sequence generator 30 generates the random time periods such that each of the generated time periods is less than the total time period. In an exemplary embodiment, binary sequence generator 30 randomly generates a binary sequence for each bit in the first half of the PWM message. Each randomly generated binary sequence indicates a value.

[0021] Binary sequence generator 30 then selects bit rates, or time periods, for each bit in a second half of the PWM message at step 110. Each of the bit rates, or time periods, in the second half of the PWM message complements a different bit rate, or time period, in the first half of the PWM message. In one exemplary embodiment, binary sequence generator 30 selects complementary bit rates, or time periods, for each bit in the second half of the PWM message in order of the sequence of bits in the second half of the PWM message. In another exemplary embodiment, binary sequence generator 30 selects complementary bit rates in the second half of the PWM message such that the sum of each pair of complemented bit rates, or complemented time periods, is substantially equal to a pre-determined constant.

[0022] VCO 34 transmits a signal having the PWM message at step 115. The signal has a data rate varying with the bit rates, or time periods, of the PWM message. In one exemplary embodiment, DAC 32 converts the value of the binary sequence for each bit in the PWM message to a voltage, and VCO 34 transmits a signal having a period varying linearly with the voltage from DAC 32.

[0023] By randomly generating bit rates for consecutive bits in the binary message, the spectrum of the binary message is spread over a larger bandwidth and generally reduces interference to radio equipment operating within the proximity of the communication bus,
and thus the timing circuit 16 (FIG. 2) provides low power and low radiation data communication that is ideally suited to pulse width modulation based communication systems. Additionally, the binary message produced by the timing circuit 16 (FIG. 2) has a relatively stable time reference such that detection of the message time of the binary message provides a stable clock signal for sampling signals.

[0024] In an exemplary embodiment, a method is provided for transmitting a binary signal. The method comprises the steps of generating random bit periods for each bit in a first plurality of bits in the binary signal, complementing each bit period of the first plurality of bits in the binary signal with a different bit period in a second plurality of bits in the biliary message to produce complemented pairs, and transmitting the binary signal having a data rate varying with the bit periods of the binary signal. Each of the complemented pairs has a total period substantially equal to a pre-determined period. The first plurality of bits in the binary signal is a first half of the binary signal having a sequence, and the complementing step comprises complementing the bit periods of a second half of the binary signal with the bit periods of the first half of the binary signal based on the sequence of the first half of in the binary signal. The binary signal has a signal period, and the bit periods for each bit in the first plurality of bits in the binary signal is less than the signal period. The generating step comprises randomly generating a binary sequence for each bit in the first plurality of bits in the binary signal, the binary sequence indicating a value. The method for transmitting a binary signal may further comprise the step of converting the value of the binary sequence to a voltage, and the transmitting step may comprise transmitting the binary signal having a period varying linearly with the voltage.

[0025] In another exemplary embodiment, a method is provided for transmitting a message signal. The method comprises the steps of generating random bit rates for each bit in a first half of the message signal, selecting bit rates for each bit in a second half of the message signal, and transmitting a signal having the message signal and having a data rate varying with the bit rates of the message signal. Each of the bit rates in the second half of the message signal complements a different bit rate in the first half of the message signal. The message signal comprises a pulse width modulate (PWM) message. The generating step comprises randomly generating a binary sequence, and the binary sequence indicates a value. The method may further comprise the steps of converting the binary sequence to a voltage and producing the signal to have a period varying linearly with the voltage. The
first half of the message signal has a sequence, and the selecting step comprises selecting the bit rates of the second half of the message signal with the bit rates of the first half of the message signal based on the sequence of the first half of the message signal. The PWM message has a message time period, and the generating step comprises randomly generating a time period for each bit in the first half of the PWM message, the time period for each bit in the first half of the PWM message less than the message time period. Each bit in the second half of the PWM message has a time period, and the bit rate selecting step comprises pairing each bit in the first half of the PWM message with a different bit in the second half of the PWM message to produce a plurality of paired bits, a sum of the time periods for each of the paired bits being constant.

[0026] In yet another exemplary embodiment, a timing apparatus is provided for modulating a data rate of a binary signal having a signal period. The timing apparatus comprises a binary sequence generator configured to randomly generate a binary sequence indicating a value for modulating a bit rate of each bit in the binary signal while maintaining the signal period, a digital-to-analog converter (DAC) having an input coupled to the binary sequence generator and having an output, and a voltage controlled oscillator (VCO) having an input coupled to the output of the DAC. The DAC is configured to produce a voltage in response to the value of the binary sequence. The VCO is configured to produce a modulated binary signal having a period varying linearly with the voltage. The binary sequence generator comprises a pseudo-random binary sequence generator configured to randomly generate the binary sequence. The pseudo-random binary sequence generator is configured to randomly generate a binary sequence for each bit of a first plurality of bits in the binary signal, each of the binary sequence indicating a random bit rate. The pseudo-random binary sequence generator is further configured to select bit rates for each bit of a second plurality of bits in the binary signal, each of the bit rates in the second plurality of bits complementing a different bit rate in the first plurality of bits. The binary sequence generator comprises a pseudo-random binary sequence generator configured to randomly generate a binary sequence for each bit of a first plurality of bits in the binary signal, each of the binary sequence indicating a random time period. The pseudo-random binary sequence generator is further configured to select bit periods for each bit of a second plurality of bits in the binary signal to produce a plurality of pairs, each bit period of the first plurality of bits complementing a different bit period of the second plurality of bits to produce a predetermined total period. Each bit period in the first plurality of bits is less than the pre-
determined total period. The first plurality of bits is a first half of the binary signal having an order and the second plurality of bits is a second half of the binary signal, and the pseudo-random binary sequence generator is further configured to sequentially select the bit period for each bit in the second half based on the order.

[0027] While at least one exemplary embodiment has been presented in the foregoing detailed description, it should be appreciated that a vast number of variations exist. It should also be appreciated that the exemplary embodiment or exemplary embodiments are only examples, and are not intended to limit the scope, applicability, or configuration of the invention in any way. Rather, the foregoing detailed description will provide those skilled in the art with a convenient road map for implementing the exemplary embodiment or exemplary embodiments. It should be understood that various changes can be made in the function and arrangement of elements without departing from the scope of the invention as set forth in the appended claims and the legal equivalents thereof.
CLAIMS

What is claimed is:

1. A method of transmitting a binary signal, the method comprising the steps of:
   generating (105) random bit periods for each of a first plurality of bits in the binary signal;
   complementing each bit period of the first plurality of bits in the binary signal with a different bit period in a second plurality of bits in the binary signal to produce complemented pairs, each of the complemented pairs having a total period substantially equal to a pre-determined period; and
   transmitting (115) the binary signal having a data rate varying with the bit periods of the binary signal.

2. A method of transmitting a binary signal according to claim 1, wherein the first plurality of bits is a first half of the binary signal having a sequence, wherein the second plurality of bits is a second half of the binary signal, and wherein said complementing step comprises complementing the bit periods of the second half of the binary signal with the bit periods of the first half of the binary signal based on the sequence of the first half of the binary signal.

3. A method for transmitting a binary signal according to claim 1, wherein the binary signal has a signal period, and wherein the bit periods for each bit in the first plurality of bits is less than the signal period.

4. A method for transmitting a binary signal according to claim 1, wherein said generating step comprises randomly generating a binary sequence for each bit in the first plurality of bits, the binary sequence indicating a value.

5. A method for transmitting a binary signal according to claim 4 further comprising the step of converting value of the binary sequence to a voltage, and wherein said transmitting step comprises transmitting the binary signal with a period varying linearly with the voltage.
6. A method for transmitting a binary signal according to claim 1, wherein said transmitting step comprises transmitting the binary signal from a master cylinder control unit to at least one slave device.

7. A method for transmitting a binary signal according to claim 1, wherein said transmitting step comprises transmitting the binary signal along an automotive communications bus.

8. A method for transmitting a message signal, the method comprising the steps of:
   generating (105) random bit rates for each bit in a first half of the message signal;
   selecting (110) bit rates for each bit in a second half of the message signal, each of the bit rates of the second half of the message signal complementing a different bit rate in the first half of the message signal; and
   transmitting (115) a signal having the message signal, the signal having a data rate varying with the bit rates of the message signal.

9. A method according to claim 8, wherein the message signal comprises a pulse width modulated (PWM) message.

10. A method according to claim 8, wherein said generating step comprises randomly generating a binary sequence for each bit in the first half of the message signal, the binary sequence indicating a value.

11. A method according to claim 10 further comprising the steps of:
   converting the binary sequence to a voltage; and
   producing the signal having a period varying linearly with the voltage.

12. A method according to claim 8, wherein the first half of the message signal has a sequence, and wherein said selecting step comprises selecting the bit rates of the second half of the message signal with the bit rates of the first half of the message signal based on the sequence of the first half of the message signal.
13. A method according to claim 9, wherein the PWM message has a message time period, wherein said generating step comprises randomly generating a time period for each bit in the first half of the PWM message, the time period for each bit in the first half of the PWM message less than the message time period, wherein each bit in the second half of the PWM message has a time period, and wherein said bit rate selecting step comprises pairing each bit in the first half of the PWM message with a different bit in the second half of the PWM message to produce a plurality of paired bits, a sum of the time periods for each of the paired bits being constant.

14. A timing apparatus for modulating a data rate of a binary signal having a signal period, the timing apparatus comprising:
a binary sequence generator (30) configured to randomly generate a binary sequence indicating a value for modulating a bit rate of each bit in the binary signal while maintaining the signal period;
a digital-to-analog converter (DAC) (32) having an input coupled to said binary sequence generator and having an output, said DAC producing a voltage in response to said value of said binary sequence; and
a voltage controlled oscillator (VCO) (34) having an input coupled to said output of said DAC, said VCO configured to produce a modulated binary signal having a period varying linearly with said voltage.

15. An apparatus according to claim 14, wherein said binary sequence generator comprises a pseudo-random binary sequence generator configured to randomly generate said binary sequence.

16. An apparatus according to claim 15, wherein said pseudo-random binary sequence generator is configured to randomly generate a binary sequence for each bit of a first plurality of bits in the binary signal, each of said binary sequence indicating a random bit rate.

17. An apparatus according to claim 16, wherein said pseudo-random binary sequence generator is further configured to select bit rates for each bit of a second plurality of bits in the binary signal, each of said bit rates in said second plurality of bits complementing a different bit rate in said first plurality of bits.
18. An apparatus according to claim 14, wherein said binary sequence generator comprises a pseudo-random binary sequence generator configured to randomly generate a binary sequence for each bit of a first plurality of bits in the binary signal, each of said binary sequence indicating a random time period.

19. An apparatus according to claim 18, wherein said pseudo-random binary sequence generator is further configured to select bit periods for each bit in a second plurality of bits of the binary signal to produce a plurality of pairs, each bit period of said first plurality of bits complementing a different bit period of said second plurality of bits to produce a pre-determined total period.

20. An apparatus according to claim 19, wherein said first plurality of bits is a first half of the binary signal having an order and said second plurality of bits is a second half of the binary signal, and wherein said pseudo-random binary sequence generator is further configured to sequentially select said bit period for each bit in said second half based on said order.
BEGIN

100

GENERATE RANDOM BIT RATES FOR EACH BIT IN A FIRST HALF OF A PWM MESSAGE

105

SELECT BIT RATES FOR EACH BIT IN A SECOND HALF OF THE PWM MESSAGE, EACH BIT RATE OF THE SECOND HALF COMPLEMENTING A DIFFERENT BIT RATE IN THE FIRST HALF

110

TRANSMITTING A SIGNAL HAVING THE PWM MESSAGE, THE SIGNAL HAVING A DATA RATE VARYING WITH THE BIT RATES OF THE PWM MESSAGE

115

END

FIG. 3

FIG. 4
INTERNATIONAL SEARCH REPORT

A. CLASSIFICATION

H04B14/02  H04B15/04

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H04B  H04L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and where practical search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

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<th>Citation of document, with indication, where appropriate, of the relevant passages</th>
<th>Relevant to claim No</th>
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D

Further documents are listed in the continuation of box C

X Patent family members are listed in annex

0 Special categories of cited documents

'A' document defining the general state of the art which is not considered to be of particular relevance

'E' earlier document but published on or after the international filing date

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'X' document of particular relevance, the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

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Date of the actual completion of the international search

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Date of mailing of the international search report

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Name and mailing address of the ISA

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Amorotti, M
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