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(54) **Title**: CONTROL METHOD AND APPARATUS FOR A DUAL-CHANNEL WEIGHTED LPOS COMBINING SCHEME

FIG. 3
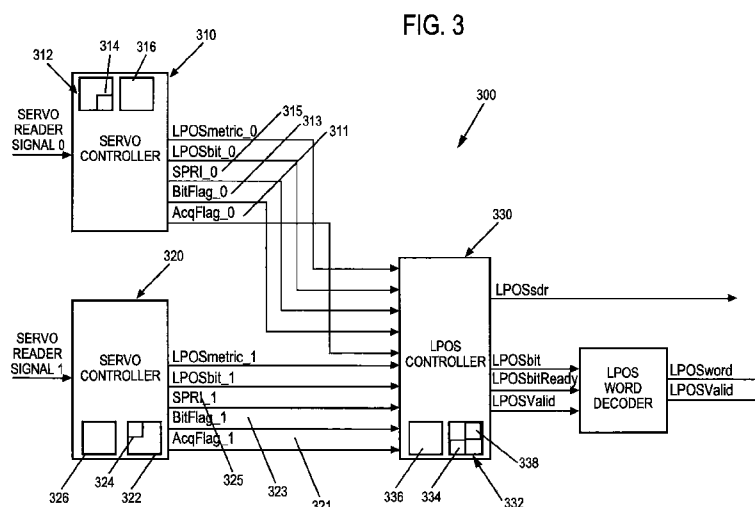
(57) **Abstract**: A method for monitoring a plurality of servo channels, providing a finite state machine ("FSM") comprising a single servo channel mode and a combined servo channel mode, and moving a sequential information storage medium comprising a plurality of servo bands across a read/write head comprising a corresponding plurality of servo sensors. The method further asserts an acquisition flag by a servo channel if that servo channel is tracking a servo pattern, and asserts a bit flag by a servo channel if a new LPOS bit is decoded. If at least one acquisition flag is asserted, the method determines if a bit flag is asserted by a servo channel associated with said asserted acquisition flag, and if an acquisition flag and a bit flag are asserted by a servo channel, the method determines a relative positioning of each servo sensor with respect to an associated servo pattern.

CONTROL METHOD AND APPARATUS FOR A DUAL-CHANNEL WEIGHTED LPOS COMBINING SCHEME

Field Of The Invention

5   Applicants' invention relates generally to a method to monitor multiple servo channels, where a control scheme switches between a single servo channel mode and a combined servo channel mode.

Background Of The Invention

10   Timing-based servo ("TBS") is a technology developed for linear tape drives. In TBS systems, recorded servo patterns consist of transitions with two different azimuthal slopes. Lateral read/write head position is derived from the relative timing of detected pulses, or dibits, sensed by a plurality of servo sensors disposed on the read/write head. TBS patterns also allow the encoding of additional longitudinal position ("LPOS") information

15   without affecting the generation of the transversal position error signals ("PES"). This is obtained by shifting transitions from their nominal pattern position using pulse-position modulation ("PPM"). A specification for the servo format in current midrange tape drives is provided by the linear tape-open ("LTO") format. The complete format for LTO drives of generation 1 (LTO-1) was standardized by the European Computer Manufacturers

20   Association ("ECMA") in 2001 as ECMA-319.

         In tape drives, two dedicated servo channels are normally available from which LPOS information and PES can be derived. A signal from one servo channel may occasionally fade while the other signal from the other servo channel might not be detected.

25   In such an event, the servo channel affected by fading loses timing and needs to undergo re-acquisition. Consequently, additional latency and loss of information is experienced.

Summary Of The Invention

         There is a need for a method to control servo channel combining operations based on

30   the status of the individual servo channels and a timing relationship (skew) between the servo signals. In one embodiment, a method for monitoring a plurality of servo signals, where a control scheme switches between a single servo channel mode and a combined

servo channel mode, is presented. Initially, a sequential information storage medium having multiple servo bands is moved past a read/write head having corresponding servo sensors. Next, the method detects whether one or more acquisition flags are asserted, where each asserted acquisition flag indicates that an associated servo channel is tracking a servo pattern. If at least one acquisition flag is asserted, the method detects whether a bit flag is asserted for the servo channel associated with the asserted acquisition flag, where each bit flag indicates the availability of a new LPOS bit. Finally, if at least one bit flag is asserted, a relative positioning for each servo sensor is determined with respect to an associated servo pattern.

In another embodiment an article of manufacture having a computer readable medium having computer readable program code disposed therein to monitor multiple servo signals, where a control scheme switches between a single servo channel mode and a combined servo channel mode, is presented. The computer readable program code includes a series of computer readable program steps to effect moving a sequential information storage medium having multiple servo bands past a read/write head having corresponding servo sensors, detecting if one or more acquisition flags are asserted, each asserted acquisition flag indicating that an associated servo channel is tracking a servo pattern, if at least one acquisition flag is asserted, detecting if a bit flag is asserted for the servo channel associated with the asserted acquisition flag, each bit flag indicating the availability of a new LPOS bit; and if at least one bit flag is asserted, determining a relative position for each of the servo sensors with respect to an associated servo pattern.

In yet another embodiment, a computer program product encoded in a computer readable medium and useable with a programmable computer processor to monitor a plurality of servo signals, where a control scheme switches between a single servo channel mode and a combined servo channel mode, is presented. The computer program product includes computer readable program code which causes the programmable processor to: move a sequential information storage medium having multiple servo bands past a read/write head having corresponding servo sensors, detect if one or more acquisition flags are asserted, each asserted acquisition flag indicating that an associated servo channel is tracking a servo pattern, if at least one acquisition flag is asserted, detect if a bit flag is asserted for the servo

channel associated with the asserted acquisition flag, each bit flag indicating the availability of a new LPOS bit; and if at least one bit flag is asserted, determine a relative position for each of the servo sensors with respect to an associated servo pattern.

5   In yet another embodiment, a data storage device having multiple servo sensors and corresponding servo controllers is presented. Each servo controller includes an acquisition flag indicating the servo channel has acquired a servo pattern, a bit flag indicating the availability of a new LPOS bit, and a servo sensor position indicator ("SRPI") providing a position of a servo-reader within a servo frame.

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           In yet another embodiment, a data storage library having multiple data storage devices, each data storage device having multiple servo sensors and corresponding servo controllers is presented. Each servo controller includes an acquisition flag indicating the servo channel has acquired a servo pattern, a bit flag indicating the availability of a new
15   LPOS bit, and a servo sensor position indicator ("SRPI") providing a position of a servo-reader within a servo frame.

Brief Description Of The Drawings
           The invention will be better understood from a reading of the following detailed
20   description taken in conjunction with the drawings in which like reference designators are used to designate like elements, and in which:
           FIG. 1A illustrates one embodiment of Applicants' data storage system;
           FIG. 1B is a block diagram of one embodiment of Applicants' data storage device in which the present invention may be implemented;
25   FIG. 1C illustrates elements of Applicants' read/write head;
           FIG. 2 illustrates one embodiment of Applicants' servo pattern comprising four bursts, wherein each of those four bursts comprises a plurality of pulses;
           FIG. 3 is an block diagram illustrating certain elements of Applicants' data storage device;
30   FIG. 4 a block diagram of one embodiment of Applicants' finite state machine;

FIG. 5A illustrates an alignment of servo frames when the second servo channel lags behind the first servo channel by less than fifty (50) percent of the length of the servo frame; and

FIG. 5B illustrates an alignment of servo frames when the second servo channel lags behind the first servo channel by more than fifty (50) percent of the length of the servo frame.

Detailed Description Of The Preferred Embodiments

This invention is described in preferred embodiments in the following description with reference to the Figures, in which like numbers represent the same or similar elements. Reference throughout this specification to "one embodiment," "an embodiment," or similar language means that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one embodiment of the present invention. Thus, appearances of the phrases "in one embodiment," "in an embodiment," and similar language throughout this specification may, but do not necessarily, all refer to the same embodiment.

The described features, structures, or characteristics of the invention may be combined in any suitable manner in one or more embodiments. In the following description, numerous specific details are recited to provide a thorough understanding of embodiments of the invention. One skilled in the relevant art will recognize, however, that the invention may be practiced without one or more of the specific details, or with other methods, components, materials, and so forth. In other instances, well-known structures, materials, or operations are not shown or described in detail to avoid obscuring aspects of the invention.

FIG. 4 is set forth as logical flow diagram. As such, the depicted order and labeled steps are indicative of one embodiment of the presented method. Other steps and methods may be conceived that are equivalent in function, logic, or effect to one or more steps, or portions thereof, of the illustrated method. Additionally, the format and symbols employed are provided to explain the logical steps of the method and are understood not to limit the scope of the method. Although various arrow types and line types may be employed in the flow-chart diagrams, they are understood not to limit the scope of the corresponding method. Indeed, some arrows or other connectors may be used to indicate only the logical flow of the

method. For instance, an arrow may indicate a waiting or monitoring period of unspecified duration between enumerated steps of the depicted method. Additionally, the order in which a particular method occurs may or may not strictly adhere to the order of the corresponding steps shown.

FIG. 1A shows data storage system 100 comprising storage controller 110, data storage devices 112 and 114, and DASD 116. System 100 further includes a plurality of sequential data storage media removeably disposed in a plurality of storage slots disposed in first storage wall 102 and/or second storage wall 104. System 100 also includes at least one robotic accessor 106 / 120 for transporting a specified sequential data storage medium between a storage slot disposed in storage wall 102/104 and data storage device 112 or 114. Accessors are moveably disposed along rail 108.

In the illustrated embodiment of FIG. 1A, host computer 130 comprises a storage management program ("SMP") 132. In certain embodiments, that storage management program, such as for example and without limitation the IBM Data Facility Storage Management Subsystem ("DFSMS") storage management program implemented in the IBM Multiple Virtual Storage ("MVS") operating system, manages the transfer of data to and from a data storage system, such system 100. In the illustrated embodiment of FIG. 1 host computer 130 further comprises a Tape Management System ("TMS") 134. In certain embodiments, the TMS is integral with the storage management program. In certain embodiments, the TMS comprises an IBM REMOVABLE MEDIA MANAGER program.

FIG. 1B is a block diagram showing certain elements of Applicants' data storage device, such as data storage devices 112 and 114 of FIG. 1A. In the illustrated embodiment of FIG. 1A, data storage devices 112 and 114 are in communication with host computer 130. In the illustrated embodiment of FIG. 1B, write processing module 105 and read processing module 115 are in communication with host computer 130 via host interface 103 through which data and commands are communicated. Data to be written is processed in a write processing module 105 and a write channel 107 before being written through write head 109 to a moving sequential data storage medium, such as tape 117. Data is read from tape 117

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by read head 111 and processed by a read channel 113 and a read processing module 115 before being transmitted to the host computer 130 through the host interface 103.

Sequential data storage medium 117 comprises a plurality of parallel data tracks in combination with a plurality of servo patterns encoded in non-data portions of the storage medium. Those servo patterns are used to generate position error signals ("PES") to laterally position a read/write head with respect to the plurality of data tracks, and to determine a longitudinal position ("LPOS") along the length of the medium.

Referring now to FIG. 1C, read/write head 135 consisting of write head 109 and read head 111 (FIG. 1B) comprises multiple elements to read data simultaneously from multiple data tracks. Read/write head 135 further comprises a number of servo elements to detect the servo signals from the servo bands. For example the read/write head may include two servo elements to detect the servo patterns on two servo bands between which are encoded parallel data tracks.

FIG. 1C illustrates surface 114 of a read/write head 135, wherein surface 114 has a facing relationship with sequential data storage medium 117 (FIG. 1B), as medium is moved across read/write head 135. In the illustrated embodiment of FIG. 1C, read/write head 135 comprises (N) read/write head elements (160). In certain embodiments, (N) is selected from the group consisting of 8, 16, 32, and 64. As those skilled in the art will appreciate, read/write head 135 may comprise additional elements not shown in FIG 1C.

In the illustrated embodiment of FIG. 1C, read/write head 135 comprises servo sensor 140, servo sensor 150, and (N) read/write head elements 160 disposed between servo sensor 140 and servo sensor 150. As sequential tape medium 117 (FIG. 1B) is moved across read/write head 135, a read/write head lateral position is derived from the relative timings of pulses detected by servo sensor 140 and/or servo sensor 150.

Referring to FIG. 2, servo pattern 200 comprises transitions comprising one of two different azimuthal slopes. Read/write head lateral position is derived from the relative timing of pulses detected by one or both servo sensors. Servo pattern 200 comprises a first burst 210 comprising five (5) pulses, wherein each of those five (5) pulses comprises a first

azimuthal slope. Servo pattern 200 further comprises a second burst 220 comprising five (5) pulses, wherein each of those five (5) pulses comprises a second azimuthal slope. Servo pattern 200 further comprises a third burst 230 comprising four (4) pulses, wherein each of those four (4) pulses comprises the first azimuthal slope. Servo pattern 200 further

5   comprises a fourth burst 240 comprising four (4) pulses, wherein each of those four (4) pulses comprises the second azimuthal slope.

The present invention provides a control scheme to identify the availability and status of the individual servo channels, and facilitates seamless switching between a single servo

10   channel modes and a combined servo channel mode as the individual servo channels become active or inactive. In certain embodiments, Applicants' control scheme monitors of the status of the two servo channels to provide the correct input to the weighted combining scheme. Applicants' control scheme comprises the components recited in FIG. 3 which implement the finite state machine of FIG. 4.

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Turning to FIG. 3, LPOS controller 330 receives the output of servo controller 310 and servo controller 320. In the illustrated embodiment of FIG. 3, LPOS controller 330 comprises processor 336 and memory 332 having instructions 334 and combining algorithm 338 encoded therein.

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Further in the illustrated embodiment of FIG. 3, servo controller 310 comprises processor 316 and memory 312 having instructions 314 encoded therein. Further in the illustrated embodiment of FIG. 3, servo controller 320 comprises processor 326 and memory 322 having instructions 324 encoded therein.

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Each servo controller can provide to LPOS controller 330 an acquisition flag 311/ 321, a bit flag 313 / 323, and a servo sensor position indicator ("SRPI") 315 / 325. The acquisition flag 311 / 321 indicates that a servo pattern has been acquired. If the acquisition flag is asserted, the servo channel is tracking a servo pattern and is providing frequent servo

30   channel parameter updates (LPOS bit, reliability information, etc.).

The bit flag 313 / 323 indicates the availability of a new and valid LPOS bit and the associated reliability information at the end of each servo frame. A SRPI 315 / 325 indicates a current position of the servo-reader within a servo frame.

5   Acquisition flags 311/ 321, bit flags 313 / 323, and servo sensor position indicators ("SRPI") 315 / 325 are provided to LPOS controller 330. LPOS controller 330 implements a finite state machine ("FSM") having multiple intermediate states dependent upon a change in the status of the servo channels.

10   FIG. 4 illustrates Applicants' FSM 400. Applicants' FSM 400 comprises a finite number of states, transitions between those states, and actions. After reset, FSM 400 is placed in an initial idle state 0. In initial idle state 0 both servo channels, servo channel 0 and servo channel 1, are inactive. In certain embodiments, servo channel 0 comprises signals based upon servo signal detection by servo sensor 140 (FIG. 1C). In certain

15   embodiments, servo channel 1 comprises signals based upon servo signal detection by servo sensor 150 (FIG. 1C).

When an acquisition flag is asserted for one or both servo channels, indicating that the associated servo channel(s) has become active and acquired a valid servo pattern, a

20   transition is performed in the FSM into one of three intermediate states, 6, 7, or 10.

Intermediate state 6 is entered if acquisition flag 311 only is asserted, meaning servo channel 0 has become active but servo channel 1 remains inactive. Similarly, intermediate state 7 is entered if only acquisition flag 321 is asserted for servo channel 1, meaning servo

25   channel 1 has become active while servo channel 0 remains inactive. Finally, intermediate state 10 is entered if acquisitions flag 311 and 321 are asserted for both servo channels, meaning both servo channel 0 and servo channel 1 are active. A transition from initial idle state 0 to intermediate state 10 indicates the absence of channel skew, i.e. that both servo channels simultaneously detect a valid servo pattern. This is likely to occur when the servo

30   patterns encoded in both servo channels are aligned with each other.

FSM 400 will remain in an intermediate state 6, 7, or 10 until a bit flag is asserted and, or status of the servo channels changes. For example, if initially both servo channels become active at the same time and intermediate state 10 is entered, FSM 400 will remain in intermediate state 10 until a bit flag is received or until one of the servo channels becomes inactive. If, by way of example, servo channel 1 becomes inactive, FSM 400 will transition from intermediate state 10 to intermediate state 6. Again, FSM 400 will remain in intermediate state 6 until a change in servo channel status occurs or, as is subsequently discussed, a bit flag is received from the active servo channel, servo channel 0.

If FSM 400 is in either intermediate state 6 or intermediate state 7 and a second servo channel becomes active within a pre-determined time interval, FSM 400 transitions to intermediate state 10. Similarly, if FSM 400 is in either intermediate state 6 or intermediate 7 and the active servo channel becomes inactive, a transition to the initial idle state 0 is made.

If both servo channels are active, the FSM remains in state 10 until one of the servo channels asserts a bit flag, indicating the detection of a new LPOS bit. If both channels indicate the detection of a new LPOS bit simultaneously, combining state 14 is entered and the information from each servo channel can be utilized by LPOS combining algorithm 338 (FIG. 3).

Intermediate states 11 and 12 are entered from intermediate state 10 when a bit flag is asserted for only one of the servo channels when both servo channels are active. For example, if FSM 400 is in state 10 and bit flag 313 is asserted for servo channel 0, intermediate state 11 is entered. Likewise, if bit flag 323 is asserted for servo channel 1, intermediate state 12 is entered. FSM 400 remains in intermediate state 11 or 12 until a bit flag for the second servo channel is detected.

After the detection of the second new LPOS bit, the combining state 14 is entered and the information from each servo channel can be utilized by LPOS combining algorithm 338 (FIG. 3).

When the FSM 400 is in intermediate state 6 or 7, a bit flag cannot be detected from the inactive channel. Therefore, when a bit flag is detected for the active channel, FSM 400 transitions directly to combining state 14. In such a situation, LPOS combining algorithm 338 (FIG. 3) only uses LPOS bit information from the active servo channel.

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After the LPOS combining algorithm 338 has been executed, the status of both servo channels is checked and the appropriate intermediate state is entered. If both servo channels are still active, FSM 400 transitions from the combining state 14 to intermediate state 10. If only one servo channel is active, the FSM 400 transitions from the combining state 14 to either state 6 or 7. Finally, if both channels are inactive, the FSM 400 transitions from the combining state 14 to initial state 0.

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In certain embodiments, individual transitions recited in connection with FIG. 4 may be combined, eliminated, or reordered. In certain embodiments, instructions 334 (FIG. 3) are encoded in computer readable medium 332 (FIG. 3) wherein those instructions are executed by a processor 336 (FIG. 3) to implement FSM 400 (FIG. 4).

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In other embodiments, the invention includes instructions residing in any other computer program product, where those instructions are executed by a computer external to, or internal to, a data storage system, to implement FSM 400. In either case, the instructions may be encoded in computer readable medium comprising, for example, a magnetic information storage medium, an optical information storage medium, an electronic information storage medium, and the like. "Electronic storage media," may mean, for example and without limitation, one or more devices, such as and without limitation, a PROM, EPROM, EEPROM, Flash PROM, compactflash, smartmedia, and the like.

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The state transitions previously described in connection with FSM 400 may be repeated while the servo channels are being read. Thus, while the servo channels are being read, the system will continuously transition between the states of FSM 400 as acquisition flags and bit flags are detected.

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By way of example, and not by way of limitation, a typical state sequence of the FSM if both servo channels are active and servo channel 0 is ahead of servo channel 1 is:

$$10 \rightarrow 11 \rightarrow 14 \rightarrow 10 \rightarrow 11 \rightarrow 14 \rightarrow 10...$$

Another typical state sequence if both servo channels are active and servo channel 1 is ahead of servo channel 0 is:

$$10 \rightarrow 12 \rightarrow 14 \rightarrow 10 \rightarrow 12 \rightarrow 14 \rightarrow 10...$$

If servo channel 0 is active and servo channel 1 is inactive, a typical state sequence is:

$$6 \rightarrow 14 \rightarrow 6 \rightarrow 14 \rightarrow 6...$$

Another example of a typical state sequence where both servo channels are active, and new LPOS bit information is indicated by servo channel 0 before servo channel 1 becomes inactive is:

$$10 \rightarrow 11 \rightarrow 14 \rightarrow 6 \rightarrow 14 \rightarrow 6 \rightarrow 14 \rightarrow 6...$$

FSM 400 is designed such that it can operate in the presence of large time-varying skew between the two servo channels, without requiring explicit knowledge of the skew. In particular, the control scheme allows for a skew between the two servo channels of up to $\pm$ 100 μm for standardized TBS patterns, or fifty (50) percent of the servo frame length.

Specifically, if the servo format and tape path layout guarantee that the skew is kept below fifty (50) percent of the servo frame length, servo channel alignment ambiguity is avoided without explicit knowledge of the skew. In FIG. 4, the critical phase for correct servo channel alignment is at the first transition to intermediate state 10 from intermediate state 6 or intermediate state 7. In this phase, one channel is already active, and the second channel becomes active. To align the information from the two channels correctly, the respective frame boundaries of the two servo channels are analyzed, where information regarding the frame boundaries is received from an SRPI for each channel.

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As shown in FIG. 5A, if a second servo channel to become active lags behind the first servo channel by less than fifty (50) percent of the servo frame, a transition from intermediate state 6 or intermediate state 7 (FIG. 4) to intermediate state 10 (FIG. 4) occurs. Both channels are then used for LPOS bit detection. Alternatively, if the second servo

5   channel lags behind the first servo channel by more than fifty (50) percent of the servo frame (i.e., the second servo channel is actually ahead of the first servo channel), no transition to intermediate state 10 (FIG. 4) is made for the current servo frame.

Rather, a transition from intermediate state 6 (FIG. 4) or intermediate state 7 (FIG. 4)

10   to combining state 14 is carried out as soon as a bit flag from the first active servo channel is detected, i.e. new LPOS bit information is available for the first active servo channel. This latter scenario is illustrated in FIG. 5B.

As discussed in reference to FIG. 4, when leaving combining state 14, the system

15   transitions to intermediate state 10 if both servo channels are still active. Alternatively, a transition to intermediate state 6 or intermediate state 7 is made if only one servo channel remains active. With this approach, the correct alignment of both servo channels can be guaranteed for skew values of less than fifty (50) percent of the servo frame length.

20   In one embodiment, a dibit counter is used to determine the skew between the two servo channels. A servo channel can change state from inactive to active only at the end of a servo frame, i.e., after detecting eighteen (18) sequential dibits in bursts of 4, 4, 5, 5 dibits. In certain embodiments, the state of an inactive servo channel is checked after detecting fifty (50) percent of the frame length of the active servo channel. This position coincides with the

25   detection of the 8th dibit in a servo frame, or a dibit counter value of 8. If, at this position, the status of the second servo channel is active then, as discussed in reference to FIG. 5A, the second servo channel is lagging behind the first servo channel by less than fifty (50) percent of the servo frame length, and a transition to state 10 (FIG. 4) is performed.

30   While the preferred embodiments of the present invention have been illustrated in detail, it should be apparent that modifications and adaptations to those embodiments may

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occur to one skilled in the art without departing from the scope of the present invention as set forth in the following claims.

CLAIMS

1.   A method of monitoring a plurality of servo channels disposed in a data storage
device, comprising:

moving a sequential information storage medium comprising a plurality of servo
channels across a read/write head comprising a corresponding plurality of servo sensors,
wherein said read/write head is disposed in said data storage device, and wherein said data
storage device comprises a first servo channel, a second servo channel, and a finite state
machine ("FSM") comprising a single servo channel mode and a combined servo channel
mode;

asserting an acquisition flag by a servo channel if that servo channel is tracking a
servo pattern;

asserting a bit flag by a servo channel if a new LPOS bit is decoded;

operative if at least one acquisition flag is asserted, determining if a bit flag is
asserted by a servo channel associated with said asserted acquisition flag; and

operative if an acquisition flag and a bit flag are asserted by a servo channel,
determining a relative positioning of each servo sensor with respect to an associated servo
pattern.

2.   The method of Claim 1, further comprising:

when not detecting an acquisition flag asserted by either servo channel, placing said
FSM in an initial state;

when detecting an acquisition flag asserted by said first or second servo channel
while not detecting an acquisition flag asserted by said second or first servo channel,
respectively, transitioning from said initial state to a first FSM intermediate state;

when detecting a bit flag asserted by said first or second servo channel, transitioning
from said first FSM intermediate state to a FSM combining state;

utilizing LPOS information provided by said first or second servo channel only.

3.   The method of Claim 2, further comprising:

when not detecting an acquisition flag asserted by either servo channel, placing said
FSM in an initial state;

when detecting acquisition flags asserted by both said first servo channel and by said second servo channel, transitioning from said initial state to a second FSM intermediate state;

when detecting bit flags asserted by both said first servo channel and by said second servo channel, transitioning from said second FSM intermediate state to said FSM combining state;

utilizing LPOS information provided by both said first servo channel and said second servo channel.

4. The method of Claim 1, further comprising determining a skew between the first servo channel and the second servo channel.

5. The method of Claim 4, wherein each of said servo channels comprises a plurality of sequential servo frames, each servo frame comprising a plurality of servo dibits, wherein the method further comprises:

establishing a first dibit count for said first servo channel;

establishing a second dibit count for said second servo channel; and

calculating the skew by subtracting the first dibit count from the second dibit count.

6. An article of manufacture comprising a computer readable medium, computer readable program code to monitor a plurality of servo channels encoded in said computer readable medium, a finite state machine ("FSM") comprising a single servo channel mode and a combined servo channel mode encoded in said computer readable medium, the computer readable program code comprising a series of computer readable program steps to effect:

moving a sequential information storage medium comprising a plurality of servo channels across a read/write head comprising a corresponding plurality of servo sensors;

asserting an acquisition flag by a servo channel if that servo channel is tracking a servo pattern;

asserting a bit flag by a servo channel if a new LPOS bit is decoded;

operative if at least one acquisition flag is asserted, determining if a bit flag is asserted by a servo channel associated with said asserted acquisition flag; and

operative if an acquisition flag and a bit flag are asserted by a servo channel, determining a relative positioning of each servo sensor with respect to an associated servo pattern.

5   7.   The article of manufacture of Claim 6, wherein said computer readable program code further comprises a series of computer readable program steps to effect:

when not detecting an acquisition flag asserted by either servo channel, placing said FSM in an initial state;

when detecting an acquisition flag asserted by said first or second servo channel

10   while not detecting an acquisition flag asserted by said second or first servo channel, respectively, transitioning from said initial state to a first FSM intermediate state;

when detecting a bit flag asserted by said first or second servo channel, transitioning from said first FSM intermediate state to a FSM combining state;

utilizing LPOS information provided by said first or second servo channel only.

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8.   The article of manufacture of Claim 7, wherein said computer readable program code further comprises a series of computer readable program steps to effect:

when not detecting an acquisition flag asserted by either servo channel, placing said FSM in an initial state;

20   when detecting acquisition flags asserted by both said first servo channel and by said second servo channel, transitioning from said initial state to a second FSM intermediate state;

when detecting bit flags asserted by both said first servo channel and by said second servo channel, transitioning from said second FSM intermediate state to said FSM

25   combining state;

utilizing LPOS information provided by both said first servo channel and said second servo channel.

9.   The article of manufacture of Claim 8, wherein said computer readable program

30   code further comprises a series of computer readable program steps to effect determining a skew between the first servo channel and the second servo channel.

10. The article of manufacture of Claim 9, wherein each of said servo channels comprises a plurality of sequential servo frames, each servo frame comprising a plurality of servo dibits, wherein said computer readable program code further comprises a series of computer readable program steps to effect:

5   establishing a first dibit count for said first servo channel;

establishing a second dibit count for said second servo channel; and

calculating the skew by subtracting the first dibit count from the second dibit count.

11. A computer program product encoded in a computer readable medium and

10   useable with a programmable computer processor to monitor a plurality of servo channels, wherein a finite state machine ("FSM") comprises a single servo channel mode and a combined servo channel mode, the computer program product comprising:

computer readable program code which causes said programmable processor to move a sequential information storage medium comprising a plurality of servo channels across a

15   read/write head comprising a corresponding plurality of servo sensors;

computer readable program code which causes said programmable processor to assert an acquisition flag by a servo channel if that servo channel is tracking a servo pattern;

computer readable program code which causes said programmable processor to assert a bit flag by a servo channel if a new LPOS bit is decoded;

20   computer readable program code which, if at least one acquisition flag is asserted, causes said programmable processor to determine if a bit flag is asserted by a servo channel associated with said asserted acquisition flag; and

computer readable program code which, if an acquisition flag and a bit flag are asserted by a servo channel, causes said programmable processor to determine a relative

25   positioning of each servo sensor with respect to an associated servo pattern.

12. The computer program product of Claim 11, further comprising:

computer readable program code which, when not detecting an acquisition flag asserted by either servo channel, causes said programmable processor to place said FSM in

30   an initial state;

computer readable program code which, when detecting an acquisition flag asserted by said first or second servo channel while not detecting an acquisition flag asserted by said

second or first servo channel, causes said programmable processor to transition from said initial state to a first FSM intermediate state;

computer readable program code which, when detecting a bit flag asserted by said first or second servo channel, respectively, causes said programmable processor to transition from said first FSM intermediate state to a FSM combining state;

computer readable program code which causes said programmable processor to utilize LPOS information provided by said first or second servo channel only.

13. The computer program product of Claim 12, further comprising:

computer readable program code which, when not detecting an acquisition flag asserted by either servo channel, causes said programmable processor to place said FSM in an initial state;

computer readable program code which, when detecting acquisition flags asserted by both said first servo channel and by said second servo channel, causes said programmable processor to transition from said initial state to a second FSM intermediate state;

computer readable program code which, when detecting bit flags asserted by both said first servo channel and by said second servo channel, causes said programmable processor to transition from said second FSM intermediate state to a FSM combining state;

computer readable program code which causes said programmable processor to utilize LPOS information provided by both said first servo channel and said second servo channel.

14. The computer program product of Claim 13, further comprising:

computer readable program code which causes said programmable processor to determine a skew between the first servo channel and the second servo channel.

15. The computer program product of Claim 14, wherein each of said servo channels comprises a plurality of sequential servo frames, each servo frame comprising a plurality of servo dibits, wherein the computer program product further comprises:

computer readable program code which causes said programmable processor to establish a first dibit count for said first servo channel;

19

computer readable program code which causes said programmable processor to establish a second dibit count for said second servo channel; and

computer readable program code which causes said programmable processor to calculate the skew by subtracting the first dibit count from the second dibit count.

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16.   A data storage device comprising a first servo sensor, a second servo sensor, a first servo controller in communication with said first servo sensor, and a second servo controller in communication with said second servo sensor, wherein:

said first servo controller comprises a first acquisition flag indicating a first servo

10   channel has acquired a servo pattern, a first bit flag indicating the availability of a new LPOS bit, and a first servo sensor position indicator ("SRPI") providing a position of said first servo sensor with respect to a servo frame encoded in said first servo channel;

said second servo controller comprises a second acquisition flag indicating a second servo channel has acquired a servo pattern, a second bit flag indicating the availability of a

15   new LPOS bit, and a second servo sensor position indicator ("SRPI") providing a position of said second servo sensor with respect to a servo frame encoded in said second servo channel.

17.   The data storage device of Claim 16, further comprising an LPOS controller comprising an LPOS combining algorithm, wherein said LPOS controller is in

20   communication with said first servo controller and said second servo controller.

18.   The data storage device of Claim 17, wherein said LPOS combining algorithm uses a presence or an absence of said first acquisition flag, a presence or an absence of said second acquisition flag, a presence or an absence of said first bit flag, a presence or an

25   absence of said second bit flag, a presence or an absence of said first SRPI, and a presence or an absence of said second SRPI to switch between a singe servo channel mode and a combined servo channel mode.

19.   The data storage device of Claim18, wherein the LPOS controller implements a

30   finite state machine comprising an initial state, a plurality of intermediate states, and a combining state.

20

20.   The data storage device of Claim 19, wherein:

said first servo channel comprises a first servo sensor;

said second servo channel comprises a second servo sensor;

said first servo sensor detects a plurality of first sequential servo frames, each first

servo frame comprising a plurality of first servo dibits;

said second servo sensor detects a plurality of second sequential servo frames, each

second servo frame comprising a plurality of second servo dibits;

said first SRPI is a dibit counter for said plurality of first servo dibits; and

said second SRPI is a dibit counter for said plurality of second servo dibits.

21.   A data storage library comprising a plurality of data storage devices, wherein

each data storage device comprises a first servo sensor, a second servo sensor, a first servo

controller in communication with said first servo sensor, and a second servo controller in

communication with said second servo sensor, wherein:

said first servo controller comprises a first acquisition flag indicating a first servo

channel has acquired a servo pattern, a first bit flag indicating the availability of a new LPOS

bit, and a first servo sensor position indicator ("SRPI") providing a position of said first

servo sensor with respect to a servo frame encoded in said first servo channel;

said second servo controller comprises a second acquisition flag indicating a second

servo channel has acquired a servo pattern, a second bit flag indicating the availability of a

new LPOS bit, and a second servo sensor position indicator ("SRPI") providing a position of

said second servo sensor with respect to a servo frame encoded in said second servo channel.

22.   The data storage library of Claim 21, further comprising an LPOS controller

comprising an LPOS combining algorithm, wherein said LPOS controller is in

communication with said first servo controller and said second servo controller.

23.   The data storage library of Claim 22, wherein said LPOS combining algorithm

uses a presence or an absence of said first acquisition flag, a presence or an absence of said

second acquisition flag, a presence or an absence of said first bit flag, a presence or an

absence of said second bit flag, a presence or an absence of said first SRPI, and a presence or

an absence of said second SRPI to switch between a singe servo channel mode and a combined servo channel mode.

24.   The data storage library of Claim 23, wherein the LPOS controller implements a finite state machine comprising an initial state, a plurality of intermediate states, and a combining state.

25.   The data storage library of Claim 24, wherein:

said first servo channel comprises a first servo sensor;

said second servo channel comprises a second servo sensor;

said first servo sensor detects a plurality of first sequential servo frames, each first servo frame comprising a plurality of first servo dibits;

said second servo sensor detects a plurality of second sequential servo frames, each second servo frame comprising a plurality of second servo dibits;

said first SRPI is a dibit counter for said plurality of first servo dibits; and

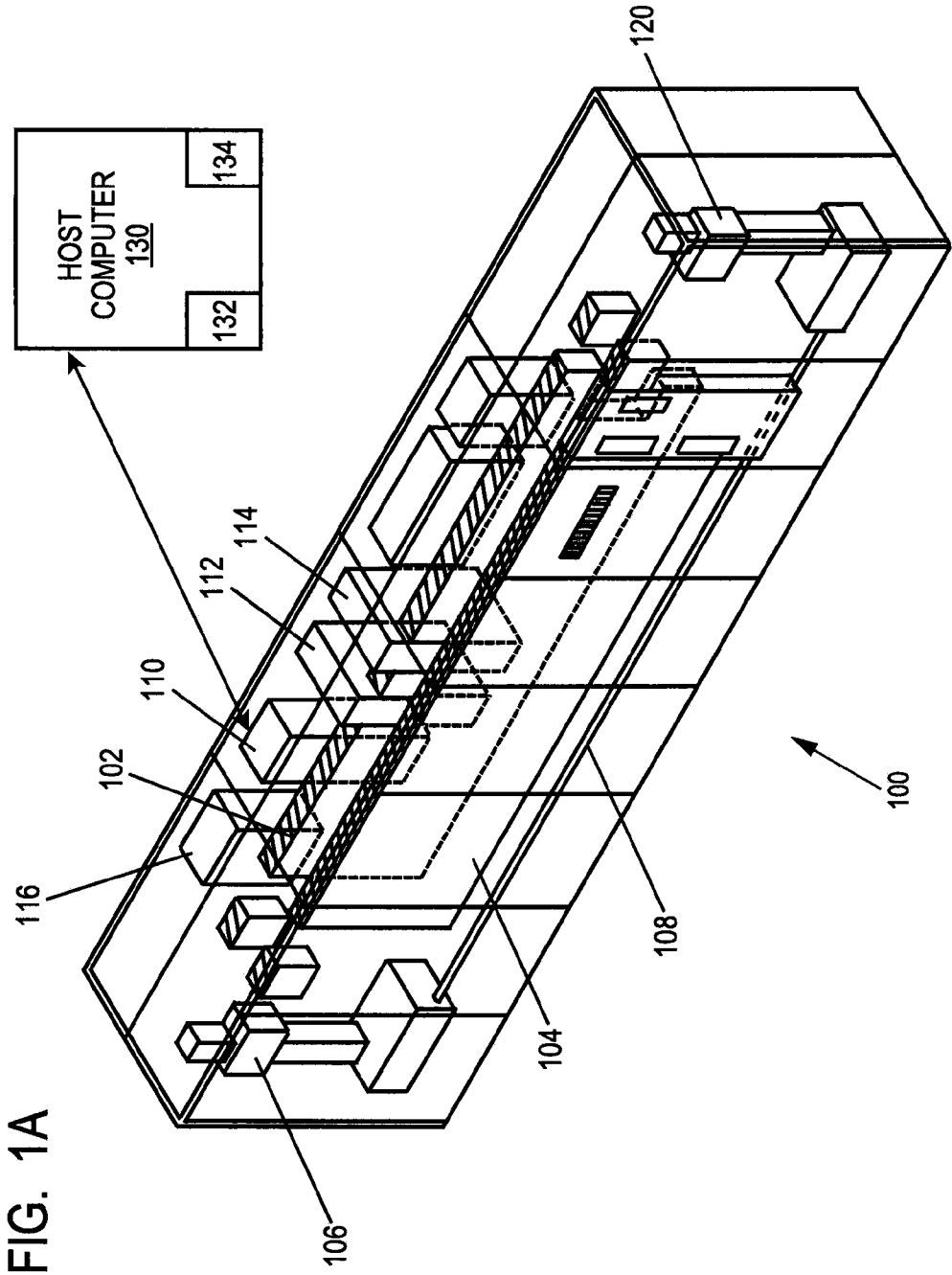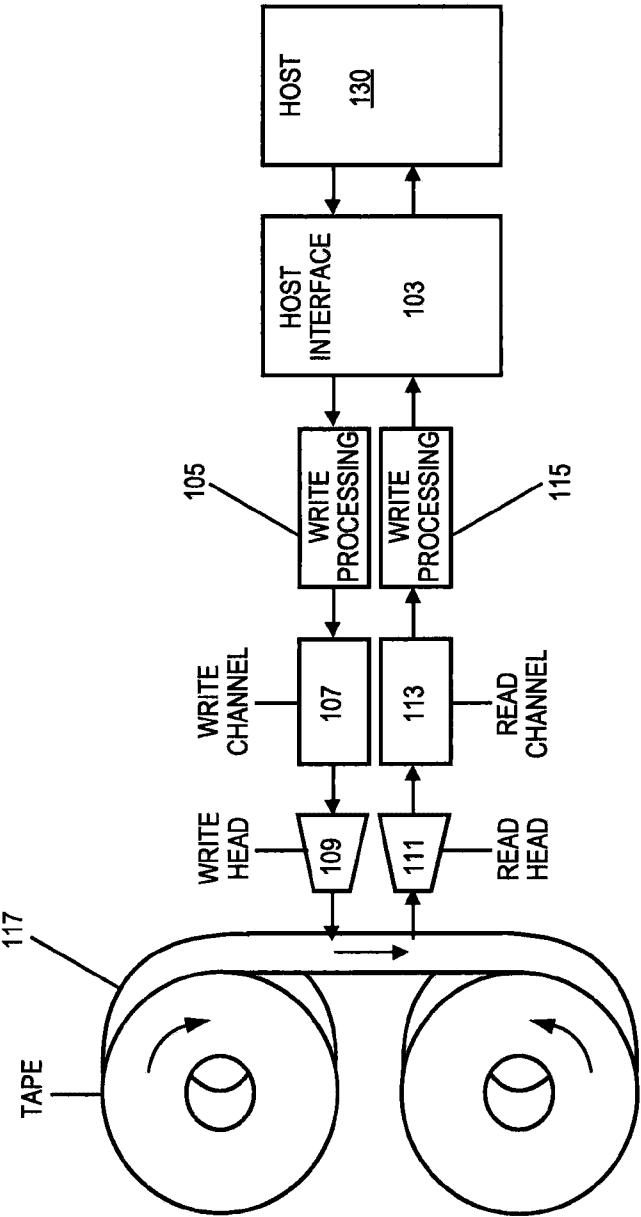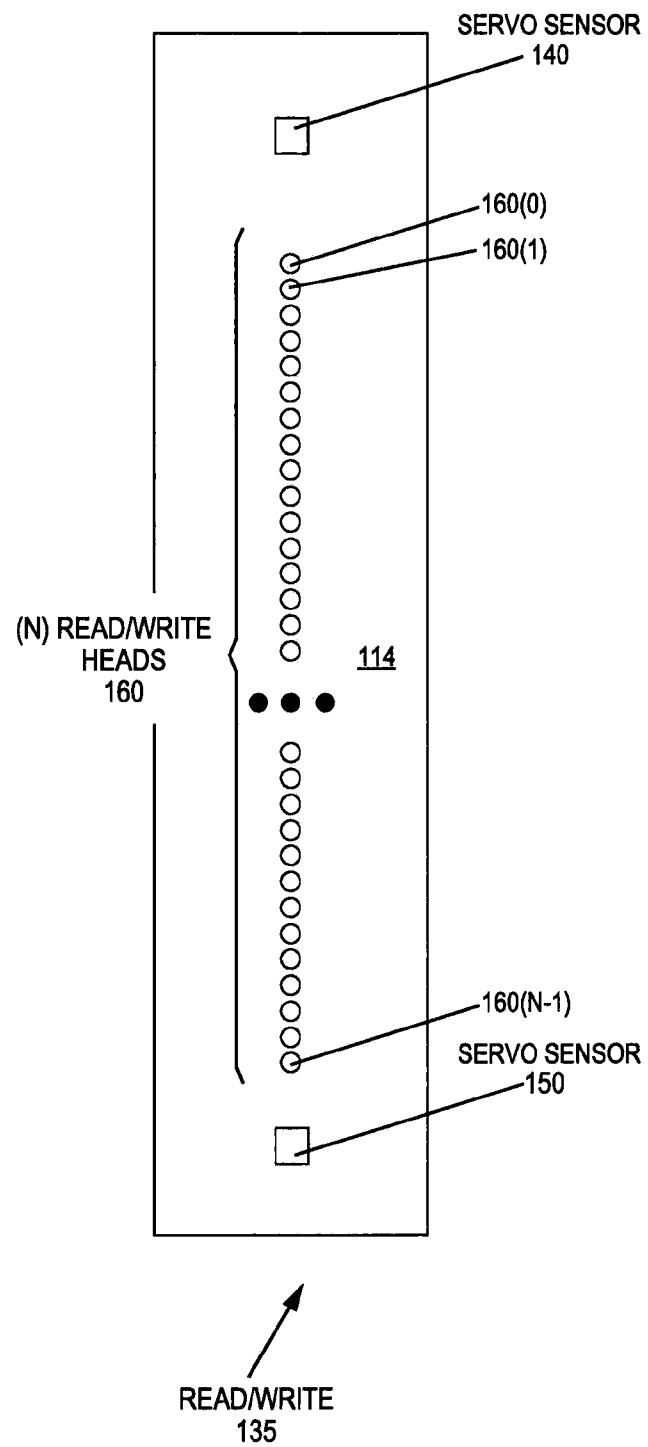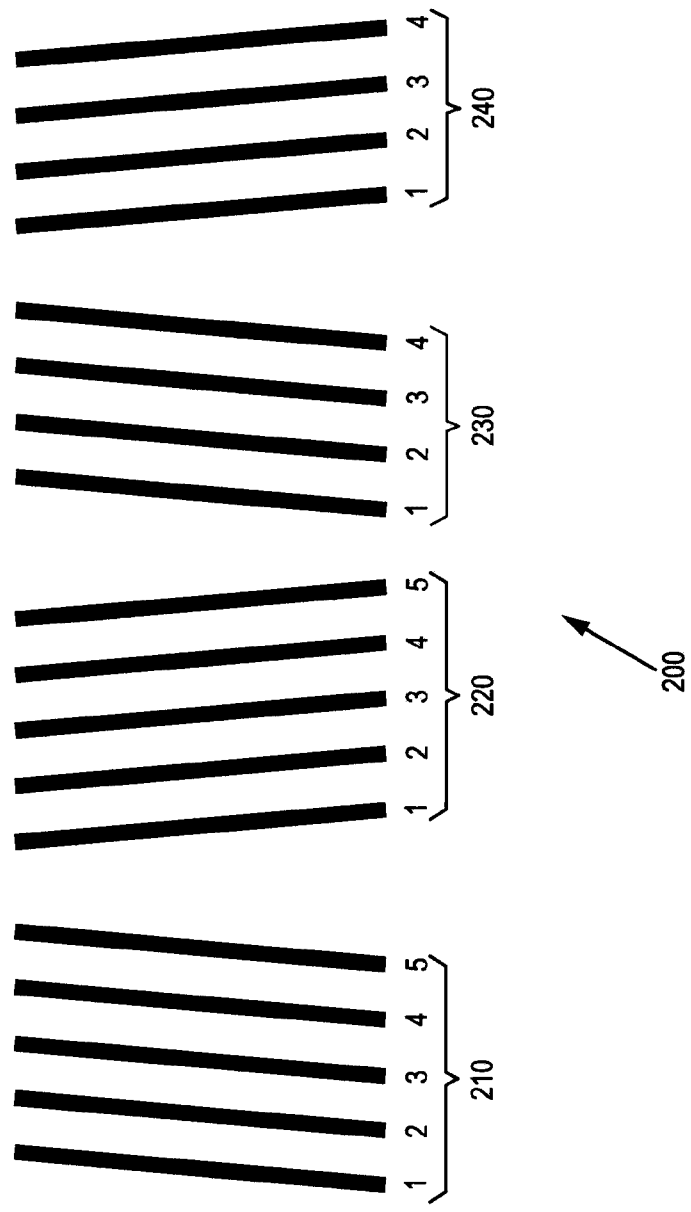said second SRPI is a dibit counter for said plurality of second servo dibit.

FIG. 1A
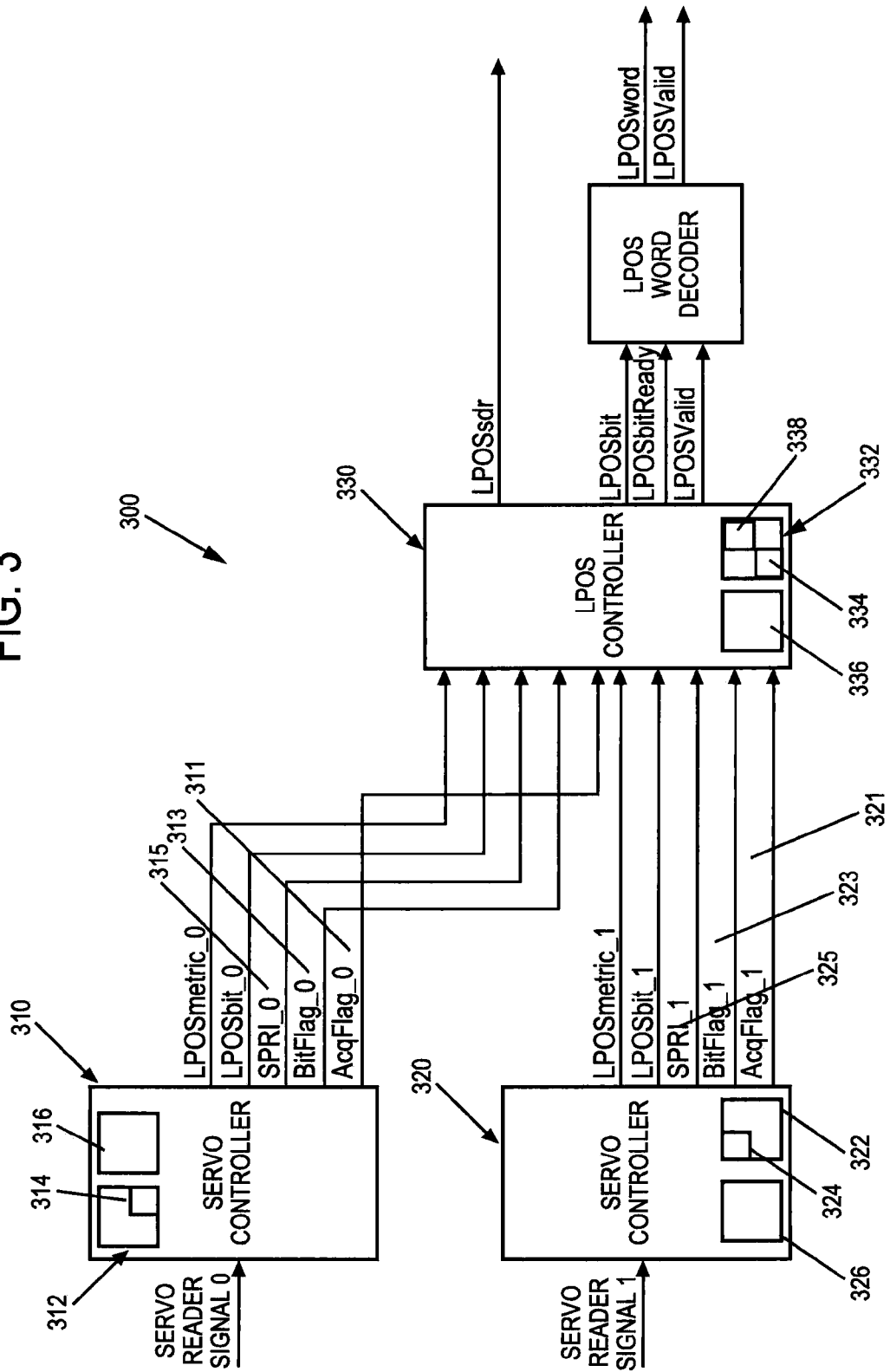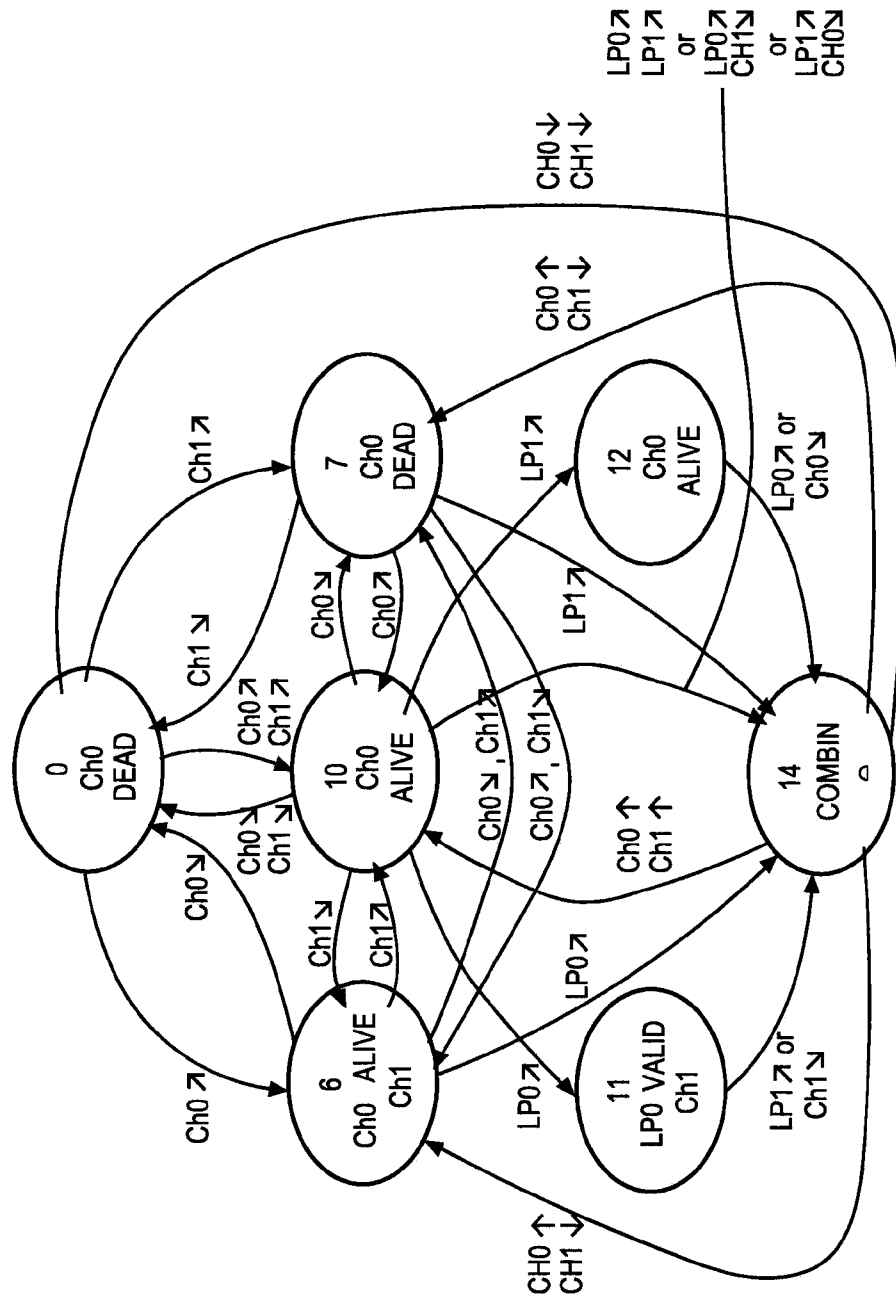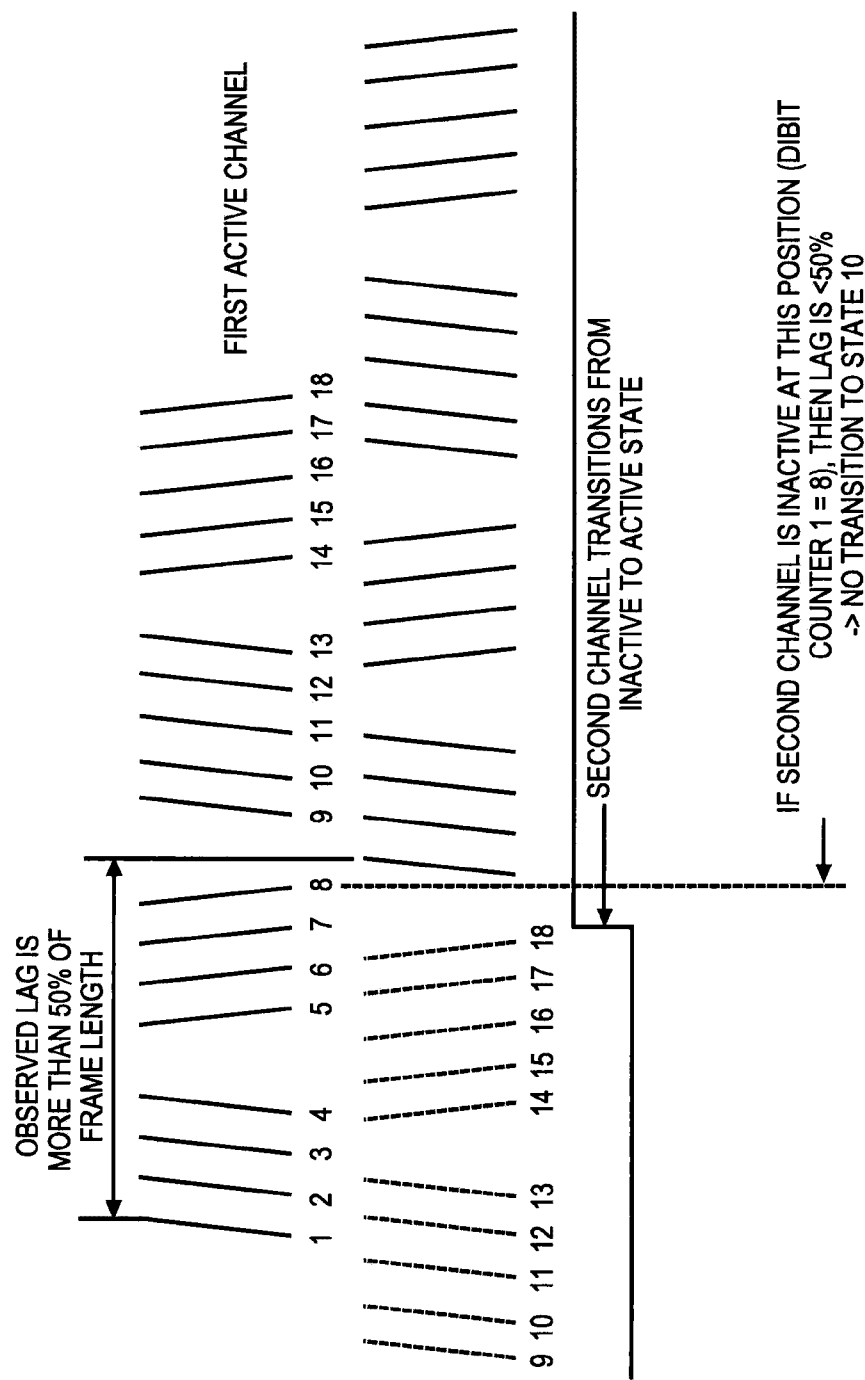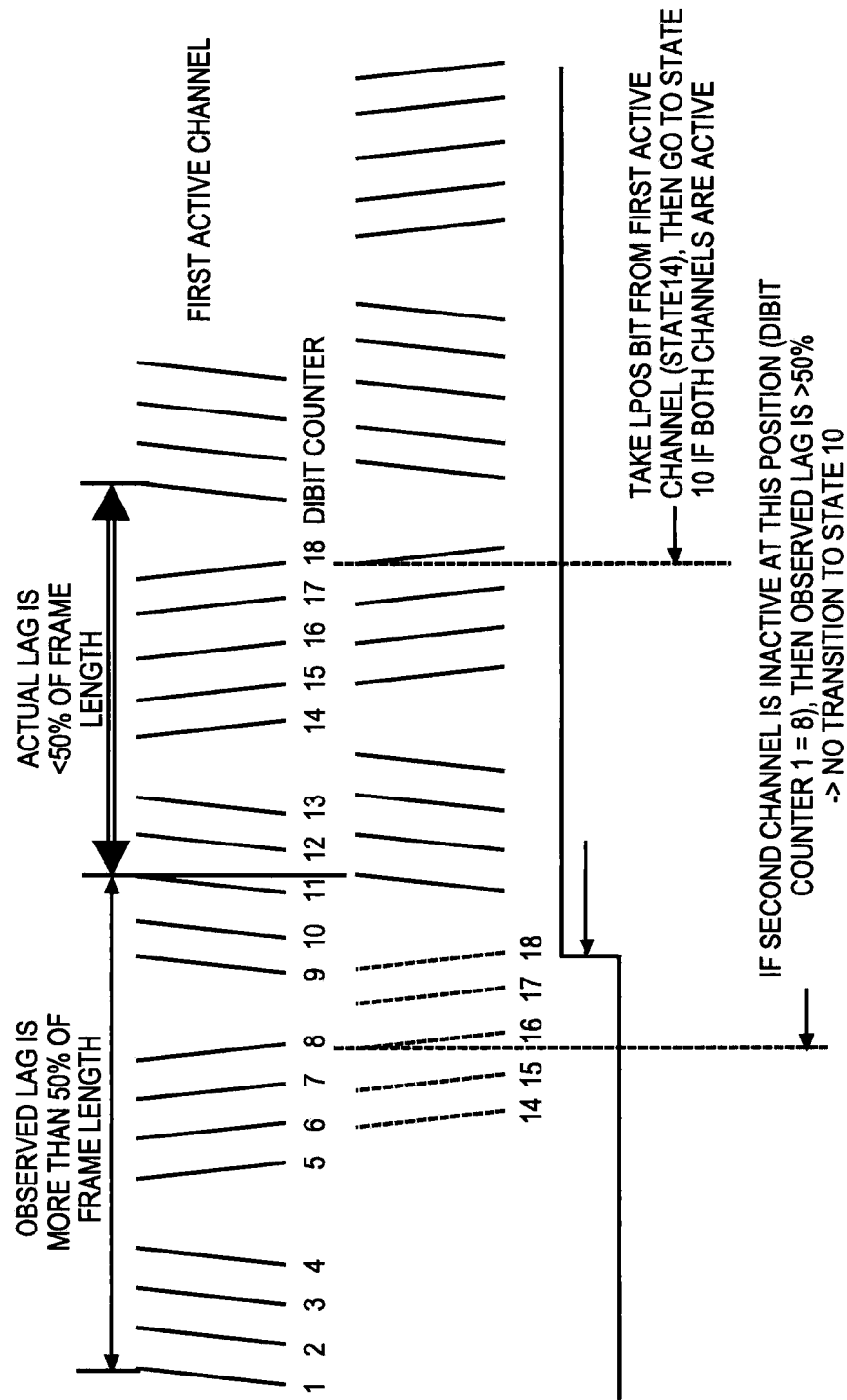
HOST
COMPUTER
130

132   134

FIG. 1B

FIG. 1C

SERVO SENSOR
140

160(0)

160(1)

(N) READ/WRITE
HEADS
160

114

160(N-1)

SERVO SENSOR
150

READ/WRITE
135

FIG. 2

FIG. 3

FIG. 4

FIG. 5A

OBSERVED LAG IS MORE THAN 50% OF FRAME LENGTH

FIRST ACTIVE CHANNEL

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18

9 10 11 12 13 14 15 16 17 18

SECOND CHANNEL TRANSITIONS FROM INACTIVE TO ACTIVE STATE

IF SECOND CHANNEL IS INACTIVE AT THIS POSITION (DIBIT COUNTER 1 = 8), THEN LAG IS <50% -> NO TRANSITION TO STATE 10

FIG. 5B

INTERNATIONAL SEARCH REPORT

A. CLASSIFICATION OF SUBJECT MATTER
INV. G11B5/584
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G11B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, INSPEC, WPI Data, IBM-TDB

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2008/024904 A1 (CHERUBINI GIOVANNI [CH] ET AL) 31 January 2008 (2008-01-31) paragraphs [0003], [0012], [0015], [0047], [0048], [0053], [0100], [0105], [0110], [0117], [0133]; claims 1,10; figures 4,17,28	1-25
A	US 2005/078398 A1 (HUTCHINS ROBERT A [US]) 14 April 2005 (2005-04-14) paragraphs [0024] - [0028], [0032], [0033]; figures 1,2	1-25
A	US 2006/114596 A1 (EATON JAMES H [US] ET AL EATON LEGAL REPRESENTATIVE GLY [US]) 1 June 2006 (2006-06-01) paragraphs [0022] - [0029]; figures 1-5	1-25

☐ Further documents are listed in the continuation of Box C.   ☒ See patent family annex.

* Special categories of cited documents :

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
29 July 2010	06/08/2010

Name and mailing address of the ISA/	Authorized officer
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Form PCT/ISA/210 (second sheet) (April 2005)

INTERNATIONAL SEARCH REPORT

Information on patent family members

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