

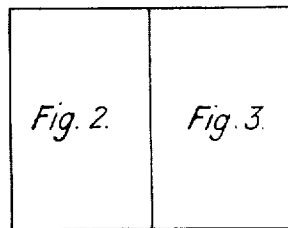
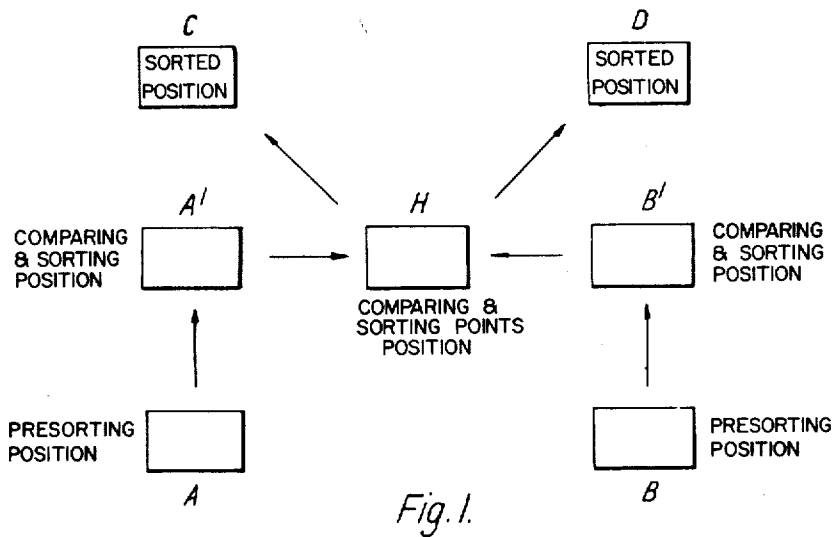
June 6, 1961

G. VAN MECHELEN
ELECTRICAL SORTING SYSTEM

2,987,705

Filed Jan. 23, 1957

5 Sheets-Sheet 1



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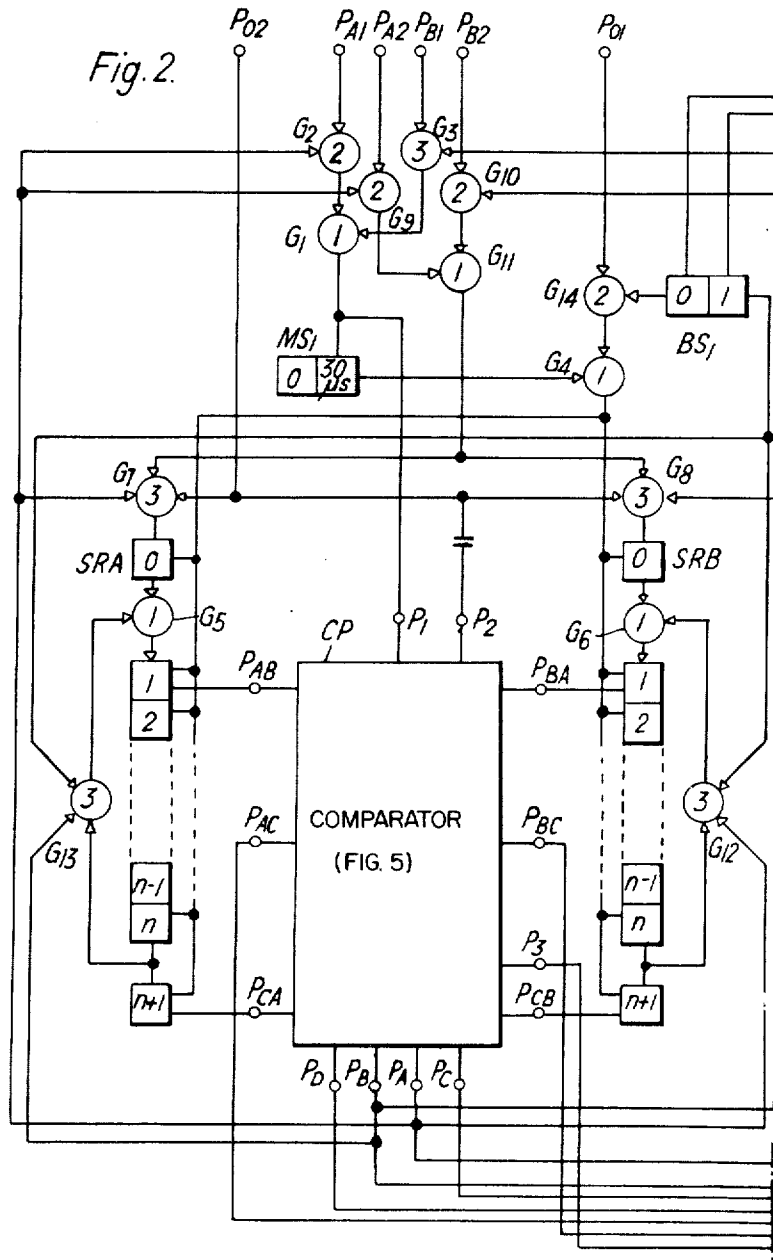
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5 Sheets-Sheet 4

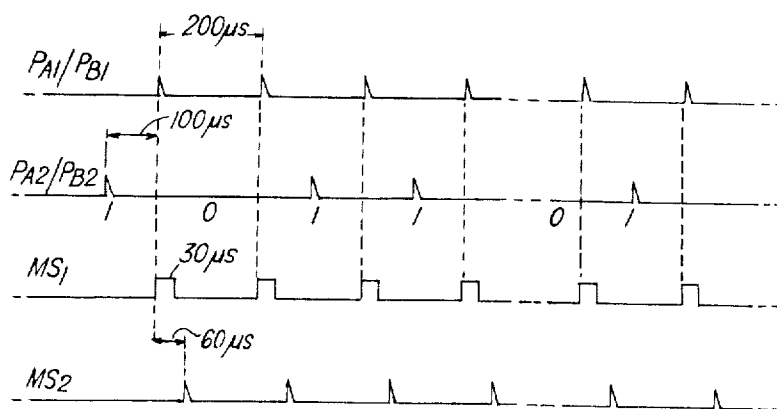
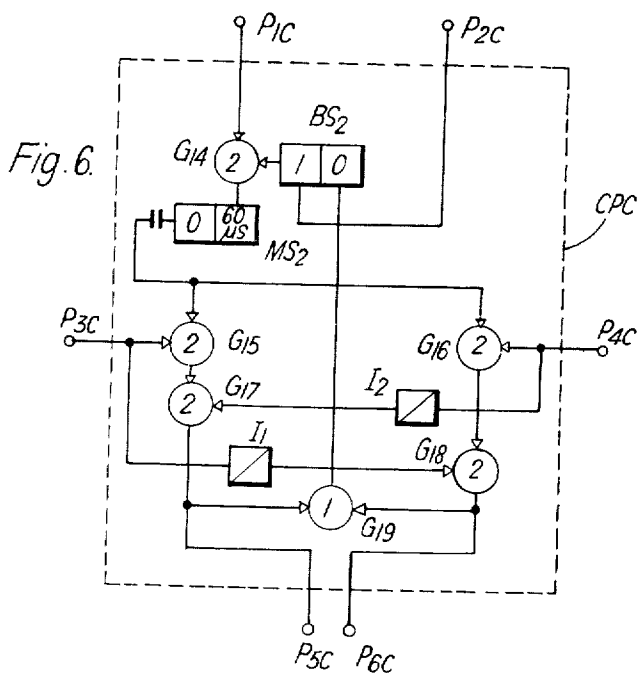


Fig. 4.

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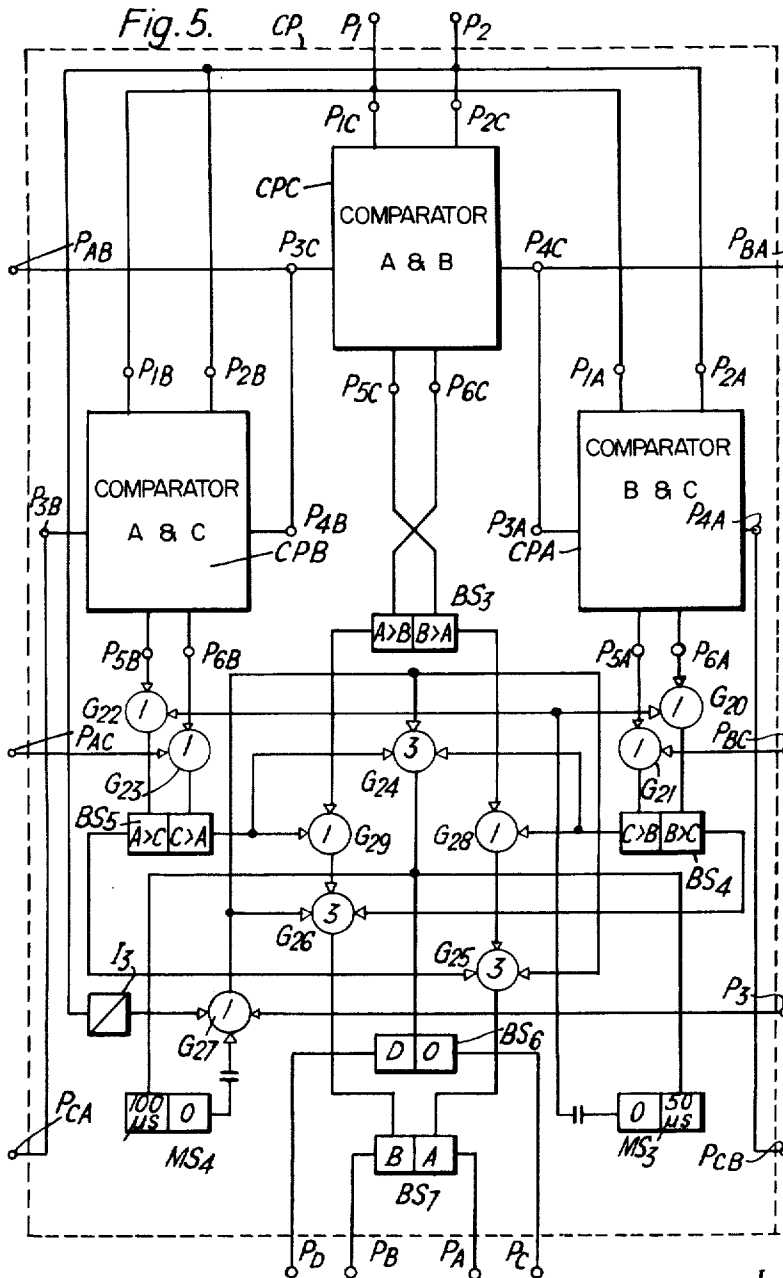
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5 Sheets-Sheet 5



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2,987,705

ELECTRICAL SORTING SYSTEM

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Filed Jan. 23, 1957, Ser. No. 635,884

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4 Claims. (Cl. 340—172.5)

The invention relates to an electrical sorting system. More particularly, it relates to an electrical sorting system using the principle of sorting by collating.

The principle of sorting numbers by collating implies comparisons between sets of numbers which are then made to form a sequence of ordered numbers. Such comparisons can be repeated until all numbers which were initially in a random order are finally obtained in a predetermined order, i.e. a single sequence with all numbers increasing or decreasing in values starting from the first. It leads essentially to all numbers being classified in their natural order at the end of the sorting process.

If a sequence is defined as a series of numbers which are in the prescribed order, the sorting process will involve a gradual reduction of the number of sequences. The initial number of sequences may be equal to the total number of numbers to be sorted, if they happen to be initially in the reverse order with respect to the predetermined order determining the way of sorting. In that case, each initial sequence comprises only a single number.

What appears to be the simplest way in which such comparisons can be conceived is to initially compare sets of two numbers and each time build a sequence of two numbers which are made to follow one another. When all numbers have been paired in this way, the new succession of all numbers can at most include a number of sequences equal to about half the total number of numbers to be sorted. Then, a new sort can be made to obtain sequences of four numbers and this time the new succession of all numbers can at most include a number of sequences equal to about one quarter of the total number of numbers to be sorted. By continuing in this manner, a single sequence, with all the numbers in the desired order, will finally be obtained.

The above principle of sorting is described in more detail by J. W. Mauchly in Lecture 22 entitled "Sorting and Collating" and part of volume III of "Theory and Techniques for Design of Electronic Digital Computers," Moore School of Electrical Engineering, University of Pennsylvania, June 30, 1948.

Such a principle of sorting by collating, which is binary in the sense that two sequences of numbers are compared to one another, or ultimately two numbers are compared to one another, has already led to practical industrial applications for automatically merging or intermeshing two ordered sequences of punched business cards into a single sequence. Such machines are well known and one may refer for example to the U.S. Patent No. 2,597,647.

When such a principle is used to build a single sequence from an initially arbitrary number of sequences, i.e. a group of numbers with an arbitrary or random distribution, and by successive predetermined steps as explained above, some inefficiency is noticed. Indeed, the system of binary collation explained above will require the complete file of N numbers to be processed $\log_2 N$ times, taking the next larger integral value of this expression, e.g. 7 times if $N=100$. But, considering the extreme cases precisely the same number of sorting passes will be required if the N numbers happen to be initially arranged in exactly the desired order, or in the order which is the exact reverse of the desired one.

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In the book by R. K. Richards entitled "Arithmetical Operations in Digital Computers" on pages 296 to 299, a modified principle of sorting by collating is referred to, which has the advantage of using whatever accidental classification is already present in the initial random distribution of the numbers or in any further intermediate distribution.

Just as the chances that the numbers are initially in the wanted order are most remote, the same is true with respect to the numbers being initially in the order exactly opposite to the desired one. Hence, in general the initial number of sequences will be appreciably smaller than N , the total number of numbers. If from the first pass, one compares a first sequence with a second sequence and the two which may both be of arbitrary length are merged to form a single sequence, an existing sequence shall never be broken and a minimum number of sorting passes will be used to obtain the final unique sequence in which all the N numbers are ordered as desired. Further, all sorting passes are alike and it is no longer necessary to count sequences of 2, 4, 8, 16, etc. according to the pass considered.

The last principle explained above necessitates the use of two input lists of numbers and two output lists of numbers. Initially, if it is assumed that the desired order is smaller in front and highest last, the first numbers from both input lists will be compared and the smaller of the two, C , will be placed as first number to start an output list. Next, the second number, A , from the input list which has supplied the first number, C , of the first output list will be compared with the first number, B , of the other input list as well as with the number C . If A and B are both larger or smaller than C , the smaller of A or B will be placed as second number of the output list already started by C or as first number to start the other list respectively. If only A or B is larger than C , which is larger will be placed as second number of the output list already started by C . As A or B is placed in an output list, a new number from the input list having supplied A or B enters into the comparison of three numbers which has just been explained. After all the numbers have been sorted in that manner, the sorting pass is ended and the two output lists can be considered as input lists for a further pass. Upon a single output list only being obtained, at the end of a pass, the sorting process is ended, all numbers being in the desired ascending order.

The main object of the invention is to realize an electrical sorting system embodying the above principle in such a way as to produce a simple and reliable arrangement.

In accordance with the main characteristic of the invention, an electrical sorting system wherein electrically represented numbers, e.g. cheque account numbers, eventually associated with electrically represented satellite information, e.g. cheque amounts, and eventually corresponding to physical objects, e.g. cheques or cheque carriers, to be sorted, are sorted by a binary collation process consisting in obtaining from a pair of initial successions of N_1 and N_2 numbers arranged in any arbitrary order, a new pair of successions of the N_1+N_2 numbers, in such a way that the first sequences of numbers ordered in the desired way and found in said two initial successions are merged together to constitute the first sequence of the first new succession, the second sequences found in said two initial successions being merged together to constitute the first sequence of the second new succession, and similar merging operations producing a new sequence alternately for the first and the second new successions, has the characteristic that two electrical shift registers are provided each with at least $n+1$ stages where n is the number of binary digits needed to char-

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acterize any number, that said two registers are respectively used to record a number from the first and from the second initial succession, that as a new number A from one of said initial succession is progressively inserted into one of said registers it is compared digit by digit with the number C previously recorded in this one register and which is progressively turned out of said one register, that said new number A while being inserted in said one register is simultaneously compared digit by digit with the number B previously recorded in said other register and which progressively re-circulates through said other register, that after said new number A has taken the place of said number C while said number B has taken its initial position in said other register, the means recording the results of the comparisons indicate the order of A, B and C, whereby in accordance with said results, said recording means cause the next number from said first or second initial succession to be inserted in a similar manner into the register corresponding to said first or second initial succession while the number which is then removed from said corresponding register is stored as the next number of one of said new successions, also in accordance with said results.

The above mentioned and other objects and characteristics of the invention will be better understood by referring to the following description of a detailed embodiment of the invention in relation to the accompanying drawings which represent:

FIG. 1, a diagram explaining the operations at a sorting stage;

FIG. 2, electronic circuits for comparing the numbers inscribed on the documents to be sorted;

FIG. 3, electrical control circuits cooperating with those of FIG. 2 and shows control circuits using telephone type relays which are designed to actuate the mechanisms (not shown) of the sorting stage in accordance with the result of the comparison performed by the circuits of FIG. 2;

FIG. 4, pulse waveforms appearing at various terminals;

FIG. 5, the comparator circuit represented as a block in FIG. 2;

FIG. 6, a comparator unit represented as a block in FIG. 5;

FIG. 7, the way to assemble FIGS. 2 and 3.

Referring to FIG. 1, it shows a diagram useful to explain the sorting process which the electrical circuits to be described later on are to control. Seven positions have been shown on the figure. The first two positions A and B are to indicate positions in which the first documents out of two input stores of documents will arrive. When the first document of the first input store is in the A position and when at the same time the first document of the second input store is in the B position, sorting can proceed by dispatching either the document in the A position to the intermediate position A', or by dispatching the document in the B position to the intermediate B' position. Between positions A and A' as well as between positions B and B', reading devices (not shown) will be assumed to be located in such positions that as the document moves along these respective positions, the characteristic number of the document which will determine how the document will be sorted, will be automatically analysed and a record of this analysis will be made.

When two documents have respectively reached the A' and B' intermediate positions after having had their numbers read, electrical comparison circuits will be in a position to determine which document bears the smallest number, or eventually if the two documents bear equal numbers.

If it is assumed that the sorting process is to be such that the final sorting pass should produce all the documents with numbers in ascending order, the smallest

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numbered document being in front and the highest numbered document being the last, the smaller numbered document in the A' or B' position will be further displaced to reach the points position H, while the other document will remain in its intermediate B' or A' position.

At the same time that the two documents in the intermediate positions were compared, a comparison should also have been made between the numbers characterising these documents and the number of the document which was the last to go through the points position H. In this manner three numbers are compared and considering the inequalities only, there are therefore six possibilities:

$$\begin{aligned} A > B > C \\ B > A > C \\ A > C > B \\ B > C > A \\ C > A > B \\ C > B > A \end{aligned}$$

For these conditions, A and B represent the numbers of the two documents which have been moved forward from the A and B positions respectively, while C represents the number of the document which was the last one having previously gone through the points position H.

The sorting by collating process which is to be controlled by the electrical circuits to be described later, is based upon the idea of building sequences of numbers from two inputs of numbers which are initially in any order whatever. It will be assumed that it is desired to obtain a final sequence comprising all the numbers and in an ascending order. The smallest sequence which can be present in the input piles of documents is the one comprising a single document only. This is the case when that document is preceded by a higher numbered document and followed by a lower numbered document. As the documents go through a first stage of sorting, by comparing a document from one input with a document from another input it will always be possible to build up a sequence comprising these two documents, by simply forwarding the lower numbered document in front of the other document. As long as it is possible to forward a document which has a higher number than the previously forwarded document, that higher numbered document may follow the previous one in the same direction. When neither of the two documents accompanying the input positions are higher than the previously forwarded document, the previously built sequence must now end and a new sequence should now be started by dispatching the lower numbered document. It is however desirable to dispatch the first document of this new sequence along another direction than the one previously used for the sequence which has just been terminated. In this manner, one obtains two outputs of documents which can contain various sequences, the number and the size of these sequences being arbitrary and depending on the original distribution of the documents.

The two outputs of documents which are thus obtained are convenient because they can then be used as respective inputs for a second sorting stage which, as well as the further stages, will sort in exactly the same way as the first sorting stage. The first output positions of the respective output stores have been indicated by C and D in FIG. 1.

Referring to the first of the six inequalities previously mentioned, B document should follow the C document since this will not break the current sequence and since this current sequence can in any case be further increased in size by one unit by forwarding at least the A document after the B one.

Referring to the second inequality, the conditions are the same as for the first one except that the order of A

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and B is now reversed which means that the A document is the one which should follow the C document.

Referring to the third inequality, only the A document is greater than the C one and accordingly only that A document can be sent forward in the same direction as C in order not to break the current sequence.

Referring to the fourth inequality, the conditions are the same as for the third except that the order of A and B is reversed which means that the B document should now follow the trace of C.

Referring to the fifth inequality, neither A nor B is greater than C and accordingly the current sequence must now be broken. The B document will be the one to go forward but in the opposite direction to that followed by C in order to start a new sequence. It is the B document which is sent forward because this leaves the possibility of building a new sequence containing at least two documents since A will be able to follow B.

Referring to the sixth and last inequality, the conditions are the same as for the fifth, except that the order between A and B has been reversed which means that the A document will now be sent forward in the opposite direction to that followed by C.

When a document reaches the points position H, it can be assumed that the points will be automatically switched over in the one or the other off normal position so as to direct the document carried by the points either in the direction of the first output position C or of the first output position D. As soon as the document leaves the points position H towards either the C or D position, one can further assume that the points will be automatically restored to their normal condition ready to accept the next document either from the intermediate position A' or from the intermediate position B'. As will be explained later, at this moment one should permit a new document to leave position A in order to reach position A', or another document to leave position B to reach position B'. Which document will be moved will of course depend on the origin of the document which was directed by the points. If that previous document came from the intermediate position A', the intermediate position B' is still occupied by a document and accordingly it is the next document occupying position A which should be moved to position A'. In the reverse case, it will be the document from position B which will be moved to position B'.

The electrical control circuits necessary to control a sorting stage following the rules explained above, will now be described.

To fix ideas, it may be assured that the documents are cheques inserted or otherwise supported in an individual carrier per cheque. This has the advantage of permitting the sorting of cheques of varying sizes and to obtain standard dimensions and physical properties for the documents to be sorted which facilitates the design of the sorting machine. Apart from bearing a cheque, the carrier will also bear a piece of magnetic tape on which information pertaining to the cheque will have been previously recorded. This information may be thought to consist of the account number of the cheque together with its amount. Thus, the amount is the satellite information previously mentioned. These two numbers may be serially recorded on the piece of magnetic tape and the sorting will be assumed to be made in accordance with the account numbers and subsidiarily, for equal account numbers, in accordance with the amounts.

Initially, the two inputs of the sorting machine which is not shown here will be filled by documents pressed against one another and for each input store, the first document of the stack will be in the positions A and B (FIG. 1) respectively. These two first documents are then ready to pass through the first sorting stage of the machine which will provide two new series of documents as these are progressively delivered to the output stores of which the first positions C and D have been shown. It is

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not essential that there should be an equal number of documents in each of the two input stores but for the first sorting stage of the machine, it appears nevertheless desirable that the documents should be more or less evenly distributed between the two inputs. This will in general give the best chances that ordered sequences of documents will be merged together using as few sorting stages as possible.

It will be evident also that the control equipment to be described is suitable for one sorting stage of a sorting machine and that each sorting stage of the machine will be provided with an entirely similar electrical control equipment. The number of stages of the sorting machine will best be determined by practical consideration such as the time which can be allotted to the sorting of a certain number of documents. In fact, the machine might well consist of one sorting stage only which would be repeatedly used for several sorting passes, until the final sorting pass is made which will be characterised by the fact that all the documents after passing the points position H (FIG. 1) will always be directed to the same output position such as C. At this moment, the sorting process will be terminated and all the documents will be classified in the desired order, i.e. the ascending order as previously assumed.

As each document passes from position A to position A' or alternatively, from position B to position B', the piece of magnetic tape on which the account number of the cheque is recorded together with the amount, will be read by a magnetic reading arrangement which will consist of two heads. The first magnetic reading head will read a first magnetic track on which synchronising information is inscribed by way of regularly occurring changes in the sense of magnetisation of the tape. The second magnetic reading head adjacent to the first will read a second track on the magnetic tape which is parallel to the first and on which information characterising the account number and the amount of the cheque is recorded, also by way of changes in the sense of magnetisation of the tape along this information track. As described in the U.S. application Ser. No. 411,523, filed February 17, 1954, a change in the sense of magnetisation on the information track can be taken to represent one of the two binary digits, while the absence of such a change can be taken to represent the other of the two binary digits. This shows why the other track carrying the synchronisation information is essential to be able to ascertain that for a particular unit bit of magnetic tape, there is a change in the sense of magnetisation for the information track or not. In this way, one determines the value of the binary digit magnetically stored on that particular bit of tape.

The outputs of the two magnetic reading heads will be connected to suitable amplifying and shaping devices, for example of the type disclosed in the U.S. Patent No. 2,704,361.

FIG. 2 shows four terminals PA₁, PB₁, PA₂ and PB₂ to which the pulses coming from the four reading heads located between positions A and A' on the one hand, and positions B and B' on the other hand are applied. At terminal PA₁ regularly occurring clock pulses are obtained by reading the clock track of a document passing from position A to position A'. At terminal PB₁, corresponding clock pulses appear when a document passing from position B to position B' is being read. At terminal PA₂, eventual information pulses are read from the information track of a document passing from position A to position A'. At terminal PB₂, corresponding eventual information pulses appear as a document passing from position B to position B' is read.

For the information pulses, i.e. pulses PA₂ and PB₂, it will be assumed that a pulse appears to indicate the binary digit 1 while the absence of a pulse indicates the binary digit 0.

FIG. 4 shows the type of pulse wave forms which may

appear either at the pair of terminals PA_1 and PA_2 or at the pair of terminals PB_1 and PB_2 . As shown, the information pulses regularly recur with a period of 200 microseconds, while the eventual information pulses characterizing the binary digit 1 are in anti-phase with respect to the information pulses. The partial information pattern shown in FIG. 4 therefore corresponds to 1 0 11 0 1

Since when a document passes from position A to position A' in order to replace the document previously located in position A', there is at that time no document passing from position B to position B', this means that the two pairs of reading heads shall never be effective at the same time and accordingly it is of interest to provide amplifying and shaping networks which can be used in common for the two reading positions. FIG. 2 shows that terminal PA_1 and terminal PB_1 for reading the clock pulses on both positions are both connected as inputs to the same mixer gate G_1 after passing through the individual coincidence gates G_2 and G_3 . These gates are indicated by circles and their input conductors terminate by arrows pointing towards the centre of the circle, while the numeral inside the latter indicates the number of input conductors which must be simultaneously activated in order to produce an output signal. Thus, the "or," or mixer, or buffer gates such as G_1 show a 1 inside the circle while the "and" or coincidence gates with two input conductors show a 2 or higher number inside the circle.

Hence, if gates G_2 and G_3 are never simultaneously unblocked, but only one at a time, the mixer gate G_1 may be assumed to contain the necessary common amplifying and shaping means which will serve either for the clock pulses appearing at terminal PA_1 or those appearing at terminal PB_1 . Of course, the pulses appearing at these terminals may in fact have already been preamplified if necessary so that the gating action of G_2 and G_3 takes place at a suitable level.

In general, it should be remarked that the description will only be concerned with the logical functions to be performed and that the devices which are needed to amplify or shape signals will not be particularly detailed. The designer should have no difficulty in selecting the appropriate devices which may be necessary to obtain suitable voltage current or power levels as well as suitable shapes for the signals, and this in accordance with the elements and combinations thereof which he wishes to use.

Gates G_2 and G_3 are respectively controlled by two of the comparator outputs. This comparator CP is merely represented as a block diagram in FIG. 2 but its details are shown in FIGS. 5 and 6 which will be described later. The four outputs of the comparator CP are represented by terminals PA , PB , PC and PD . Terminals PA and PB are used to produce signals which will determine which document is to be advanced towards one of the output positions C or D (FIG. 1). Either an activating signal will appear at terminal PA to indicate that a new document should be advanced from the input position A, or it will appear at terminal PB to indicate that a new document should be advanced from the input position B (FIG. 1). Since terminal PA is connected to G_2 while terminal PB is connected to G_3 , either G_2 or G_3 will be able to pass the clock signals from terminals PA_1 or PB_1 . These clock signals appearing at the output of G_1 when a document is being read either between the positions A and A' or between the positions B and B', will be applied to the input of a monostable device MS_1 represented by a rectangle divided into two squares each indicating the two possible conditions of the device. Condition 0 is the normal stable condition, while the indication of 30 microseconds inscribed in the second square indicates the time constant of MS_1 , i.e. the time it takes to return to its stable condition after having been triggered to its unstable condition. Hence, at the output of MS_1 pulses corresponding to the

received clock pulses will be applied to the mixer gate G_4 , but these pulses have a relatively well defined duration of 30 microseconds and the same period as the clock pulses, i.e. 200 microseconds. The waveform of these pulses is shown in FIG. 4.

From the output of G_4 , the received pulses are used as advancing pulses for the two shift registers SRA and SRB. Each of these shift registers is represented by a rectangle divided into $n+2$ squares, the first and the last squares respectively marked by 0 and $n+1$ being separately shown from the others. Each of these squares represents a stage of the shift register which may for example be designed in accordance with the U.S. Patent No. 2,649,502. Each square representing a stage of the shift register can occupy two possible electrical conditions and accordingly the shift register can be used to record a number electrically represented by n binary digits plus an additional binary digit. The additional stage labelled 0 and which is separated from the next stages by the gates such as G_5 and G_6 has been found convenient as an input stage in order to permit the advancing pulses to lag with respect to the eventual information pulses. This may be useful when possible undesirable phase shifts between the clock pulses and the eventual information pulses can occur due to inaccuracies produced by the reading devices. As shown, the advancing pulses issued from the output of G_4 are applied to all the stages of SRA and SRB. Each advancing pulse will cause the digital pattern registered on SRA and SRB to be advanced by one stage. As disclosed in the U.S. Patent No. 2,649,502, each stage may essentially include a cold cathode tube which may be ionized or not, and the advancing pulses will be applied to the cathodes of all the tubes in such a way as to de-ionize all the previously ionized tubes and leave the non-active tubes de-ionized. Upon the disappearance of the advancing pulse, thus after some 30 microseconds, those tubes which had previously been ionized will still provide a transient pulse in their anode circuit which will be sufficient to cause the ionization of the next tube forming the next stage, a suitable coupling between the anode circuit of any tube and the control circuit of the next tube being provided.

Just as the clock pulses appear either at terminal PA_1 or at terminal PB_1 , the eventual information pulses corresponding to these clock pulses will appear either at terminal PA_2 or at terminal PB_2 depending on whether a document is passing from position A to position A', or from position B to position B'. These information pulses are applied to inputs of the gates G_7 and G_8 through a gating arrangement comprising the coincidence gates G_9 and G_{10} as well as the mixer gate G_{11} . The gating arrangement comprising G_9 , G_{10} and G_{11} will be recognized as exactly similar to the gating arrangement comprising G_2 , G_3 and G_1 . Again, the activating condition present either at terminal PA or at terminal PB will unblock the A or the B path by way of unblocking G_9 or G_{10} respectively.

The gates G_7 and G_8 are essentially information entrance gates to SRA and SRB respectively. These coincidence gates are controlled from terminals PA and PB respectively. They are further controlled from the terminal PO_2 at which a pulse condition will appear during part of the time taken by the document to pass from the position such as A to the corresponding intermediate position A'. With a view to provide a pulse of suitable duration and position at terminal PO_2 one may consider that this is produced by a photocell arrangement comprising at least two cells. These two photocells which are not shown, may be assumed to lie in series in the path between A and A'. When the passage of the document blocks the first photocell which it meets during its travel towards its position A', this will correspond to the leading edge of the pulse to be produced at terminal PO_2 . One will arrange that at that moment, the piece of magnetic tape bear-

ing the information is already engaged under the corresponding reading heads but that the surface of the tape printed with the account number of the cheque and followed by the amount of the latter has not yet been reached. When the front edge of the document moving towards position A' now blocks the second photocell, this will cause the termination of the activating pulse condition at terminal P_{O2} . This second photocell will be located in such a position that this termination of the activating pulse at this terminal will happen when the piece of magnetic tape is still travelling under the corresponding reading heads, but when the area printed with the information has already filed past these heads. Hence, the purpose of this authorizing pulse at terminal P_{O2} is essentially to permit inserting the information printed on the magnetic tape only when it is really there, in order to avoid noise or other spurious signals picked up by the reading heads before or after the actual information is read, to be sent towards SRA or SRB. At terminal P_{O2} will also appear a corresponding authorizing pulse when a document is passed from position B to position B', this authorizing pulse being generated by an exactly similar photocell arrangement located this time on the path of a document moving between positions B and B'.

From what has been described so far, when a document is being read, the clock pulses at the output of G_1 will always produce advancing pulses at the output of G_4 which will be used to advance the information pattern both on SRA and on SRB, irrespective of whether the document which is being read is an A or a B document. At the same time however, the information pulses will either be able to flow through G_7 or through G_8 depending on whether an A or a B document is being read.

If it is assumed that a clock pulse or an advancing pulse always follows the eventual information pulse, and if it is assumed that patterns of n binary digits are already registered on stage 1 to n of SRA and of SRB, the first advancing pulse will advance these two patterns by one stage so that they will occupy the stages from 2 to $n+1$ in SRA and 1 in SRB. Immediately before this first advancing pulse however, the presence or the absence of an information pulse on the A document, will have caused stage 0 of SRA only to be placed in a condition corresponding to the first binary digit. If a pulse appears at the output of G_7 , one will assume that the 0 stage of SRA will record a 1, while it will be assumed to record a 0 if there is no such pulse.

Further advancing pulses will continue to advance the patterns on SRA and on SRB, but as the pattern on SRA is advanced, a new information pattern is gradually inscribed and represents the new information which is being read from the document travelling between positions A and A'. Whereas the previous information pattern registered on SRA is being gradually pushed out from this shift register and lost, as the binary digits gradually go out from the last stage $n+1$, this is not the case for the previous information pattern registered on SRB. For the latter, since it has been assumed that terminal P_A is activated, the signal at this terminal will permit to unblock the coincidence gate G_{12} which is inserted in the ring coupling between stage n and stage 1 of SRB. This gate G_{12} is also controlled by the bistable device BS1 which, as will be described later, should be assumed to have been placed in its condition 1 at the start of the operations. Hence, when terminal P_A provides an activating signal, gate G_{12} is unblocked and as the previous pattern of information is advanced through SRB it is gradually reinscribed through gates G_{12} and G_6 in series.

An identical ring coupling including the coincidence gate G_{13} and the mixer gate G_5 is provided between stages n and 1 of SRA but this coincidence gate G_{13} is controlled by the activating condition which may be present at terminal P_B which has been assumed to be inactive for the example considered.

When the first digit of the pattern previously registered

on SRA comes into stage $n+1$, the first digit of the information being read from the A document travelling between positions A and A' will occupy stage 1 of SRA. At the same time, the first digit of the pattern previously registered on SRB will occupy stage $n+1$ of SRB, as well as stage 1 of SRB since this previous information pattern is able to recirculate through G_{12} . Stages 1 of SRA and SRB are respectively coupled to the terminals P_{AB} and P_{BA} of the comparator CP. Also, stages $n+1$ of SRA and SRB are respectively coupled to the terminals P_{CA} and P_{CB} of this comparator CP.

This comparator CP which is detailed in FIGS. 5 and 6 is arranged so that it can always compare the pairs of conditions which successively appear at terminals P_{AB} and P_{BA} . It can also compare the pairs of conditions at terminals P_{AB} and P_{CA} . Further, it can compare the pairs of conditions existing at terminals P_{BA} and P_{CB} .

In this manner, while a new number A is inserted into SRA to replace an outgoing number C previously stored in SRA and while a previously stored number B recirculates in SRB, comparisons between A and B, A and C, and B and B will always be made. On the other hand, while a new number B is inserted in SRB to replace an outgoing number C previously stored in SRB, and while a previously stored number A recirculates in SRA, comparisons between B and A, B and C, and A and A will always be made.

It is readily remarked that out of these three comparisons, one is always pointless since it merely compares the previously stored number with itself. This particular comparison could therefore only be used as a check that things are proceeding in the right manner. But, the other two comparisons do not apparently permit the comparator CP to determine the order of the three numbers, since in one case the order of B and C is not determined and in the other case, the order of A and C is not determined. However, as will be explained later in relation to FIG. 5, the comparator CP is arranged in such a way that the two useful comparisons will nevertheless be sufficient to determine the order of the three numbers A, B and C and accordingly to activate either terminal P_A or terminal P_B to cause one of the two documents A and B to move forward to the points position H (FIG. 1) in accordance with the result of the comparisons. Also, the comparator CP will produce an activating signal either at terminal P_C or at terminal P_D to give an indication to the control circuit of FIG. 3 as to the output C or D (FIG. 1) to which the outgoing document should be sent. Hence there are four possible results of the comparisons performed by CP.

FIG. 2 also shows that the clock pulses applied to MS_1 are directed to terminal P_1 of the comparator CP. These pulses will be used in a manner later to be described, to activate the comparisons performed by the comparator. Further, terminal P_{O2} at which the authorising pulses generated by the photocell arrangements appear, is also connected to terminal P_2 of the comparator CP. A condenser coupling issued to indicate differentiation of the authorising pulse and its leading edge will be used for resetting operations while its trailing edge will be used to finally produce the activating signals at one of the two terminals P_A and P_B , and at one of the two terminals P_C or P_D .

At terminal P_{O1} , pulses having a duration of 30 microseconds and with a period equal to 200 microseconds appear. These pulses will thus be identical to the pulses produced by MS_1 in response to the reading of clock pulses, but the pulses at terminal P_{O1} are locally generated and constantly present at the input of the coincidence gate G_{14} . At the start of a sorting pass, BS1 will be triggered to its 0 condition for a short time during which a sufficient number of the locally generated advancing pulses at terminal P_{O1} will be able to flow through the gates G_{14} and G_4 in series in order to advance any residual pattern stored on SRA and SRB, or any patterns

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haphazardly set on these upon power being applied. The purpose of this operation is therefore to empty SRA and SRB so that when new sorting operations are started all the stages of SRA and SRB are in their 0 conditions corresponding therefore to the recording of 0 numbers.

It is desirable that at the beginning of the sorting operations 0 numbers should be recorded in SRA and SRB since otherwise, the first number A for example to be stored in SRA might be found to have such a relation to the initial arbitrary numbers stored in SRA and SRB, that it would result in the corresponding A document being sent forward. This would mean that the next A document would be recorded in SRA and this would not give an opportunity to the first B document, which has not yet been read, to be sent through the points position H (Fig. 1) immediately after the first A document was sent forward.

Finally, the comparator CP also shows three additional input terminals P_3 , P_{AC} and P_{BC} to which signals may eventually be applied from the sequence control circuit of FIG. 3 for a purpose which will be described later.

A description will now be given of the various sequences of operations which take place when a sorting pass is to begin. Before detailing the operations which take place in the circuit of FIG. 3, a summary of the functions of the various key contacts represented and of the various relays will be given.

Contacts functions:

- ks —start key contact.
- kt —stop key contact (used to stop a sorting pass at any moment for the purpose of restarting a fresh sorting pass).
- ku_1/ku_2 —intermediate stop key contacts (to be used for the purpose of temporarily stopping a sorting pass to be restarted later).
- kv —batch sorting key contact (to be used when it is desired that upon one of the two input stores having sent all its documents forward, the documents remaining in the other input store are sent forward to one or the other output positions in accordance with their initial sequences. Otherwise, flow sorting takes place which means that upon all the documents having left one input store, the sorting pass is stopped until this input store is refilled).
- ka_1/kb_1 —A and B input stores respectively occupied by at least one document in the corresponding input position.
- ka_2/kb_2 —A' and B' intermediate positions respectively occupied by a document.
- ka_3/kb_3 —points position H contacts indicating when they are both operated, that a document occupies the points position.
- of —points position H contact to indicate that the latter are in an off normal condition.

Relays functions:

- Ar/Br —Initial indication that the next A or B document is to be advanced from the input position to the intermediate position and through the reading position, and to replace the corresponding document going in one of the output stores.
- Aar/Bar —Document in the intermediate position to be advanced to the points position.
- Abr/Bbr —Prepares, the advancement of a document from the input position to the intermediate position.
- Acr/Bcr —Advances, the next document from the input position to the intermediate position.
- Adr/Bdr —Corresponding input store emptied of all its documents and to cause sorting to continue with the other documents in the other store in the case of batch sorting.
- Cr/Dr —Document in the points position to be directed to the C or to the D output position.
- Er —Responds to an intermediate or a final stop.

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- Fr —Releases Adr and Bdr upon both input positions having been emptied after batch sorting.
- Har —Points occupation relay.
- Hbr —Points liberation relay.
- Hcr/Hdr —Occupied points to direct the document to the C or the D output positions.
- Sr —Start relay immediately effective to cause the advancement of either the first A or B document towards its intermediate position.
- Sar —First start helping relay.
- Sbr —Second start helping relay.
- Scr —Start relay for advancing the first document from the other input position to the corresponding intermediate position.
- Tr —Stop relay.
- Ur —Intermediate stop relay.

Assuming that both input stores positions have been filled by a number of documents to be subjected to a sorting pass, and that the input positions A and B are occupied by the first documents, the starting key, which may be a push button, will be temporarily depressed causing the temporary closure of contact ks . Via break contact t_1 of the stop relay Tr which should not be operated at that moment, a circuit will be established between ground and a suitable battery potential at terminal P_F , and this will energise the start relay Sr . Contact s_1 therefore closes to provide a locking circuit for Sr independently of contact ks , and through the closed contacts aa_1 and ba_1 in series. The operation of Sr also displaces the change over contact s_2 which interrupts the connection between a suitable fixed D.C. potential at terminal P_E and the 0 input of BS_1 (FIG. 2). This will have the result of placing BS_1 in its 0 condition if it was not already in that condition. This may, for example, take place in practice by causing the grid of one of the tubes forming the flip-flop BS_1 to have its potential increased due to the opening produced by the operation of s_2 upon Sr being operated. This might cause an increase of the resistance between this grid and ground, this grid being on the other hand connected to the H.T. supply for the tube through the anode of the other tube forming the flip-flop and thus in conventional manner. If the tube, whose grid potential was so modified was not already conductive, its plate-cathode space will now be ionized while the other tube will become non-conductive. Hence, from the operation of contact s_2 , the local advance impulses at terminal P_{O1} will start to wipe out whatever information was contained in SRA and SRB (FIG. 2).

The operation of Sr will also produce the energisation of either relay Aar through make contact s_3 or relay Bar through make contact s_4 . Which of these two relays will be operated depends upon the initial condition of the comparator CP (FIG. 2). It is immaterial, at the start of the operations, which of the terminals P_A or P_B , and P_C or P_D are activated. One may assume for example that terminal P_A is activated while terminal P_B is not. This will mean that, a suitable fixed D.C. potential being present at terminal P_G , sufficient current will flow between this terminal and terminal P_A (FIG. 2) so that relay Ar is initially energised while relay Br is not. Hence, relay Aar operates in a circuit including resistance R_a , contact s_3 , winding of Aar , contacts ac_1 , a_1 and e_1 .

The operation of relay Aar will control a mechanism (not shown) which is able to displace a document in the A' intermediate position (FIG. 1) towards the points position H. As no such document has yet reached any of the intermediate positions, this first operation will be without any effect.

When relay Aar operates, through make contact aa_2 and the winding of relay Abr , a locking circuit is closed for Aar independently of contact s_3 . The resistance R_a will be assumed to have a sufficiently low value with respect to the resistance of relay Abr so that this last relay cannot yet operate at this moment due to the short-cir-

cutting effect produced by resistance R_a . The operation of Aar also closes contacts aa_3 and aa_4 . Depending on which of the two terminals P_C or P_D happens to be activated by the comparator CP (FIG. 2), either relay Cr or relay Dr will operate. One may assume, for example, that sufficient current flows between terminals P_C and P_G so that through make contact aa_3 relay Cr operates. Then, relay Cr locks through its contact c_1 in series with contacts hb_1 and SC_4 to ground.

When contact s_5 closed, it establishes an operating circuit for relay Sr which energises and locks through its make contact sa_1 in series with the break contact sc_1 . Upon relay Aar having been operated, contact aa_1 opens to cause the release of relay Sr .

The release of relay Sr opens contact s_3 whereby resistance R_a no longer short-circuits the winding or relay Abr which is now able to operate in series with relay Aar through the series contacts aa_2 , ac_1 , a_1 and e_1 . Contact ab_1 closes whereby relay Aar is now short-circuited and releases, opening its contact aa_2 , but relay Abr remains held through its make contact ab_1 . The release of relay Sr will also return contact s_2 to the position shown whereby the connection between the potential at terminal P_E and the 1 input of BS_1 (FIG. 2) will be interrupted. As previously explained in connection with the interruption, also by contact s_2 , of the connection between this terminal and the 0 input of BS_1 , this action will now have the effect of placing BS_1 into its 1 condition. From then on, recirculation of information will be permitted either for SRA or SRB, and for the latter in the case assumed here, since terminal P_A is activated. Relay Sr has been indicated to be a slow release relay since it should stay operated for a time sufficiently long to permit a complete wiping out of the patterns which may be initially recorded on SRA and SRB. This time evidently depends on n and on the period of advancement of the patterns, and the slow release relay may eventually be associated with such known means which will permit to secure the required time. Upon relay Aar having been released while relay Abr remained held, an operating circuit is closed for relay Acr through break contact aa_5 , make contact ab_2 , the winding of Acr and break contact e_1 .

Relay Acr energises and will cause the first document in the A input position to be moved towards the intermediate position A' . On its way to position A' , the first A document will be read as previously explained and the number of the document which is read will be compared to the numbers stored in SRA (FIG. 2) and in SRB. Since SRA and SRB are now wiped out to record 0 numbers, the first A document will be found greater than the numbers of the non-existing documents. This means that the first A document should not be the one to be sent to the points position H in accordance with the rules explained above, but that it is the missing document corresponding to the 0 inscription in SRB which should be sent forward.

In the meantime, as soon as relay Acr operated to dispatch the first A document through the reading position and to the intermediate position A' , a circuit will have been established for the operation of relay Sbr through make contact sa_2 and make contact ac_2 . In operating, relay Sbr locks through make contact sb_1 and the winding of relay Scr independently of the contact ac_2 . As long as this contact remains closed however, relay Sr remains short-circuited and cannot operate. The operation of the relay Acr will also open contact ac_1 thereby interrupting the holding circuit for relay Abr which releases. In turn, the release of relay Abr opens the contact ab_2 and relay Acr releases whereby relay Scr is permitted to operate in series with relay Sbr .

In order to positively prevent that upon Scr being operated on the release of relay Acr , Aar could be operated if relay Ar had not already de-energised, a holding circuit is provided for relay Acr . This includes make contacts ac_3 , a_2 and sb_2 in series. Hence, as long as Ar is still

operated, relay Acr cannot be released. When the latter relay releases, the comparison circuit has reacted in a manner which is in fact predetermined and relay Aar cannot operate upon the operation of Scr .

By the time that the first document has reached the intermediate position A' , a renewed operation of relay Aar is prevented because the eventual operating circuit for this relay is opened at contact ac_1 and also at contact a_1 since due to the comparison mentioned above, the activating potential at terminal P_A (FIG. 2) will have disappeared to be replaced by an activating potential at terminal P_B causing the operation of relay Br .

Hence, when relay Scr operates, contacts sc_2 and sc_3 will be closed, but whereas the closure of contact sc_2 cannot cause the operation of relay Aar , the closure of contact sc_3 will now establish an operating circuit for relay Bar . This includes the resistance R_b , make contact sc_3 , winding of Bar , contact bc_1 , make contact b_1 and break contact e_1 . As previously described for relay Aar , relay Bar locks through contact ba_2 in series with the winding of relay Bbr which cannot operate as long as it is short-circuited by the resistance R_b .

When operating, relay Scr opens contact sc_1 to interrupt the holding circuit for relay Sar which releases causing in turn the release of relays Sbr and Scr . Hence, the four starting relays Sr , Sar , Sbr and Scr are now released having performed their required functions.

The operation of relay Br will cause the corresponding mechanism to advance a document in the B' intermediate position to the points position H. However, this will still be without effect since the B document is missing. Upon the release of relay Scr , relay Bbr will be able to operate as it is no longer short-circuited by the resistance R_b . A holding circuit is closed for this relay through make contact bb_1 and this short-circuits relay Bar which releases. At this moment, a circuit for the operation of relay Bcr is established through ba_5 in series with bb_2 . The operation of relay Bcr will then cause the first document in the B input position to be advanced to the B' intermediate position passing through the corresponding reading position.

When relay Scr was operated, the opening of contact sc_4 interrupted the holding circuit for relay Cr which released. This means that the contacts c_2 and c_3 of relay Cr are now open. Accordingly, although the first A document and the first B document are now in their respective positions and that consequently the respective busy intermediate position contacts ka_2 and kb_2 are closed, neither the relay Aar nor the relay Bar can be short-circuited through their own break contacts aa_6 or ba_6 since both relays Cr and Dr are released. Depending upon which of the first two documents A and B is the smaller, the comparison circuit CP will cause that document to be sent forward to the points position. It will therefore be the first to pass through this points position.

If it is assumed that the A document is smaller, terminal P_A will have been activated when the first B document went through the corresponding reading position and accordingly relay Ar is operated permitting the energisation of relay Aar . This time the operating circuit will include contact ka_2 instead of the contacts of the starting relays such as Sr or Scr . In a manner entirely similar to that previously described, the operation of relay Aar will cause the first document to be sent to the points position, but this time the operation of relay Abr will be due to the fact that the first A document has left the intermediate position A' , thereby opening contact ka_2 . Upon the operation of relay Aar , relay Cr will reoperate through make contact aa_3 since terminal P_C will still be activated as there has not yet been any possibility for the output position to which a document should be directed to be changed. After the release of relay Aar caused by the operation of relay Abr , relay Cr will remain locked through contact c_1 , hb_1 and sc_4 . Relay Acr

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will again operate, to cause the second A document to be moved from the input position and to take the place of the first A document which has left the intermediate position A' to be dispatched to the points position H. In turn, relay *Abr* releases and this causes the release of relay *Acr* since the latter is no longer provided with a holding circuit, relay *Sbr* being released. The time of operation of relay *Acr*, just as that of relay *Aar* should, of course, be assumed to be sufficient to cause the document to be started either towards the intermediate position or towards the points position. Once the document has been started on its way, it is assumed that the mechanism will continue to propel it until it reaches the desired position.

When the second A document moves through the corresponding reading position, this might result in the comparator CP indicating that the first B document should now be moved towards the points position. This would be the case for example if that first B document is greater than the first A document but smaller than the second A document. Hence, terminal P_B could be activated thereby causing the operation of relay *Br* instead of relay *Ar*. When contact b_1 closes however, since relay *Cr* is operated, relay *Bar* is short-circuited by the series contacts kb_2 , sc_3 , be_6 and c_3 . Therefore, relay *Bar* cannot yet operate at that moment. The reason for this is to prevent a document to be sent from one of the intermediate positions to the points position, when the latter might still be occupied by the previous document. A similar short-circuiting circuit is provided for relay *Aar* (ka_2 , sc_2 , aa_6 and c_2 , d_2).

When the first A document reaches the points position H (FIG. 1), this will be assumed to produce the closure of the two points contacts ka_3 and kb_3 , upon the document having been fully inserted on the points position. If, as shown diagrammatically on FIG. 1, the sorting machine has two intermediate positions A' and B' symmetrically located with respect to the points position H, contact ka_3 might be closed upon an A document entering the points position, while contact kb_3 will be closed upon a document entering from the intermediate B' position. However, it can be arranged that upon the document having been fully inserted in the points position H while coming from the intermediate position A', contact kb_3 will also close following the closure of contact ka_3 (reversed sequence for a B document entering the B points position).

Upon the closure of these two contacts by the first A document, relay *Har* operates and locks through its make contact ha_1 in series with the winding of relay *Hbr* and contact c_4 . Relay *Hbr* cannot operate in this circuit as it is short-circuited by the series contacts ka_3 and kb_3 . The operation of relay *Har* also results in *Hcr* being energised through make contacts ha_2 , hbr and c_5 in series. Relay *Hcr* will be assumed to be the relay responsible for displacing the points position containing the first A document in such a way that it is directed towards the output position C. Relay *Hdr* would, of course, have operated to direct the busy points towards the output position D if relay *Dr* had been operated. Upon the busy points position being displaced, the off normal contact "of" will provide an additional locking circuit for relay *Har*.

The points will be assumed to be self controlled in the sense that upon the busy points having been displaced to one of their two off-normal conditions, the document present on the points will be automatically dispatched to the corresponding output position. When the document leaves the points position, it will be further assumed that means not shown will cause the automatic return of the points to their normal position ready to accept another document from either of the intermediate positions. Contacts kb_3 and ka_3 will be successively opened as the first A document leaves the point, but at that moment relay *Hbr* is still short-circuited by off nor-

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mal contact "of." When the points swing back to their normal position, contact "of" will be also opened and accordingly relay *Hbr* will operate in series with relay *Har*. The operation of relay *Hbr* opens at contact hb_1 the holding circuit for relay *Cr* which releases thereby releasing relays *Har* and *Hbr* due to the opening of contact c_4 .

At contact hb_2 , the temporary operation of relay *Hbr* immediately causes the release of relay *Hcr*.

Upon relay *Cr* having been released, contacts c_2 and c_3 are opened and either relay *Aar* or relay *Bar* can be operated through their respective intermediate position busy contacts ka_2 or kb_2 depending upon the results of the comparison. Whether *Aar* operates due to *Ar* being energised or whether relay *Bar* operates due to relay *Br* being energised, will result in operations similar to those already described. Likewise, upon the operation of *Aar*, or *Bar*, either relay *Cr* or relay *Dr* will operate. Since the first A document was sent to the C output position, it is clear that relay *Dr* can only operate due to the activation of terminal P_D upon both the first B document and the second A document having been found smaller than the first A document, which is the condition indicating a change of output.

Sorting will continue in the manner explained, until the last document from one of the two input stores has moved to the corresponding intermediate position. This document will remain in that intermediate position in accordance with the control given by the comparison circuit CP, and during the time that A documents can still be sent through the points without necessitating the insertion of that last B document in an output sequence. Upon this last B document being sent to the points position, it will not be replaced by a further B document in that position. Hence, no further information will be sent to the comparison circuit CP which will remain in the condition which caused the last B document to be dispatched to the points position. Therefore, the sorting operation will be stopped at that moment leaving an A document in the corresponding intermediate position and eventually leaving further documents in the A input store.

This type of sorting operation may be termed flow sorting. The machine stops of its own upon one of the input positions having been emptied. It will be necessary to refill that input position in order to continue the sorting process. If the sorting stage considered is not the first input sorting stage, one can wait until the previous sorting stage delivers further documents to the input store which has become empty at the sorting stage considered. By a further temporary closure of contact ks , a new start can be given and the sorting can continue. Of course, this might be made automatic by providing a contact arrangement detecting that documents are present in both input stores, which detection would have a result analogous to the closure of contact ks .

In opposition to flow sorting, one can also consider what may be termed as batch sorting and which consists in completing the sorting operations at any stage as long as there remain documents in one of the two input stores, and despite the fact that the other input store has been emptied. In that case, of course, the documents remaining in one input store will be merely sent forward in their present sequences. However, depending on these input sequences, these documents will be alternatively sent to the one and the other of the two output stores and the next sorting stage will generally be fed at its two input stores. Therefore, with the batch sorting method, a sorting stage might have one of its two input stores temporarily emptied but later refilled by documents coming through the previous sorting stage.

If batch sorting is desired, contact kv will be permanently closed by means of an appropriate key. Assuming that after a certain time, the B input store is emptied and not immediately refilled by the next B document, contact kb_1 normally operated by the first document to

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go out of the B input store will be released when the last B document moves to the intermediate position and is not replaced by a further B document in the B input store. Upon relay Bar being operated when the last B document in the B' intermediate position is required to be moved to the points position H, an operating circuit for relay Bdr will be closed through break contacts t_2 , kb_1 , make contact ba_7 , the winding of Bdr, and make contact kv and break contact e_1 . Relay Bdr operates and locks through make contact bd_1 in series with break contact f_1 . After relay Bbr operates in the normal manner causing the release of relay Bar and hence the operation of relay Bcr, the latter will be without effect since there are no further documents in the B input position. The energisation of relay Bcr will cause the release of relay Bbr, in turn producing the release of relay Bcr.

Upon relay Bdr being energised, change over contact bd_2 is displaced and the connection between terminals P_E (FIG. 3) and P_{BC} (FIG. 2) is interrupted. As will be shown later, this interruption, as long as it lasts, will have the result of forcing the comparator circuit CP which has hitherto remained in the condition previously attained and which caused the departure of the last B document to the points position, in such a position that it indicates $B < C$. Further, upon change over contact bd_2 establishing a connection between terminals P_E (FIG. 3) and P_C (FIG. 2) a pulse will be applied to the comparator circuit CP for the purpose of causing an eventual reversal of output for the next A document to be sent to the points position, and in a manner which will be detailed later.

A further result of the operation of relay Bdr is the closure of make contact bd_3 which bypasses contact a_1 , so that irrespective of the operation of relay Ar or Br, an operating circuit will always be established for relay Aar upon the closure of contact ka_2 which will be remembered to be the busy contact for the intermediate A' position. On the other hand, relay Bar can never be reoperated from the moment that the last B document has left the intermediate B' position, since the busy contact kb_2 will never be reoperated.

The reasons for the actions mentioned above and caused by the operation of relay Bdr can be explained as follows:

When the last B document was sent to the sorting position H, this must mean that the comparator indicated

$$A > B > C$$

or its two cyclic derivations, i.e.

$$B > C > A$$

$$C > A > B$$

B representing the number of the last B document, A that of the first remaining A document, and C the number of the document which immediately preceded B through the points position H. Since no further B document was moved through the corresponding reading position, the comparator circuit shall normally not be affected and would remain in a condition corresponding to one of the three relations mentioned immediately above. Therefore, it is clear that the comparator still indicates that a B document should be sent to the points position. Since this is pointless, the closure of make contact bd_3 appears to give a correct remedy since this will permit the first remaining A document to be sent to the points position upon the latter having been freed from the last B document, and this independently of the fact that relay Br is still operated. However, depending upon the relation between A and B, i.e. the first remaining A document and the last B document, the former should follow the same direction as the latter or not. It is clear that when $A > B$, A should follow the same direction as B, and when $B > A$, A must follow the direction opposite to that taken by B in order to start a new output sequence with the first remaining A document. Yet, it is only when one had $C > A > B$, that the comparator would still indicate a re-

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versal of output which in the particular case of the first remaining document for batch sorting, is wrong. Likewise, if the condition which caused the comparator to dispatch the last B document was $B > C > A$, this did not indicate a change of output for the last B document and correspondingly it does not indicate a change of output for the first remaining A document, which latter indication is wrong since it is in this particular case that the first remaining A document should follow the direction opposite to that taken by the last B document.

A very simple solution to the dispatch of the first remaining A document to the correct output position can be found if the comparator circuit CP is arranged in such a way that when it detects the particular condition

$$C > A > B$$

or

$$C > B > A$$

which means a change of output direction to start a new sequence with the lowest of A or B, after this indication has been received and utilised, the comparator circuit CP will automatically be reset to the respective conditions.

$$A > B > C$$

or

$$B > A > C$$

This means that the relation between A and B is maintained as received but the relations between A and C on the one hand and B and C on the other hand, are both artificially reversed.

Accordingly, out of the three possible conditions which were mentioned above as those which are the only ones which might have caused the departure of the last B document, there remain only two, i.e.

$$A > B > C$$

and

$$B > C > A$$

since the third was automatically and artificially changed into the first of the two above.

If, as already mentioned, the opening of change over contact bd_2 upon the operation of Bdr, changes the condition $B > C$ of the comparator, into $C > B$, the two possible conditions will then become

$$A > C > B$$

and

$$C > B > A$$

respectively. It is clear that these last two conditions respectively indicate that A should be sent forward in the same direction as B, or that A should be sent forward in the direction opposite to that taken by B. (One should recall that C is always used to indicate the previous document which was dispatched to the points and which in these cases was the last B document.)

The above explained modifications in the state of the comparator consequent upon the operation of relay Bdr would however remain without effect as far as the activation of the output terminals P_A , P_B , P_C and P_D of the comparator circuit CP (FIG. 2) are concerned, since it will be recalled that the comparisons are made active upon the authorizing pulses at terminal P_{O2} being terminated. Hence, despite the forced change on the comparator state due to the opening of contact bd_2 , terminal P_B will remain activated and consequently relay Br would stay energised. This would be of no consequence in view of the closure of contact bd_3 which will anyhow produce the departure of the first remaining A document, but if terminal P_C was activated when the last B document was sent through the points, and if $B > A$, the activation of this last terminal should now be replaced by the activation of terminal P_D to permit the first remaining A document to be moved to the output position opposite to that to which the last B document was directed. The missing trailing edge of the authorizing pulse normally

appearing at terminal P_{O2} will be replaced by a pulse generated by the closure of the connection between terminals P_E and P_3 , which pulse will exploit the modified state of the comparator circuit CP. Hence, depending on whether $A \geq B$, terminals P_C will remain activated or not, the deactivation of this terminal resulting of course in the activation of terminal P_D .

In fact, the only two possible conditions which are attained upon the operation of relay Bdr will always cause the deactivation of terminal P_B causing the release of relay Br , while relay Ar will now be energised as a result of the activation of terminal P_A .

Therefore, the first remaining A document will be directed to one of the two output positions depending on its value, and the further remaining A documents will be successively sent to the points position H to be directed to one of the two output positions, a change in the output position being obtained every time that a sequence of remaining A documents ends. Hence, the remaining A documents will be distributed to the two output positions in accordance with their input sequences, and the principle of distributing the documents to the two output positions depending on the available sequences will be maintained.

Although it has been shown that relay Ar will in any case be operated for the first remaining A document, the closure of make contact bd_3 will nevertheless play its part during the dispatch of further A documents. Since, as mentioned above, the comparator is forced by the opening of the connection between terminals P_E and P_{BC} into a condition corresponding to $C > B$, from then on the only three possible conditions which can be impressed on the comparator are

$$\begin{aligned} A &> C > B \\ C &> A > B \\ C &> B > A \end{aligned}$$

or

For the first and the last conditions above, these will cause the A document to be dispatched, with a reverse of the output position for the last condition. For the second condition however, this corresponds to a B document being sent in the opposite output position than the one previously followed by the previous document and hence, it is in such a case that make contact bd_3 will still permit the A document in the intermediate position A' to be dispatched, in a direction opposite to that followed by the previous A document.

When the last of the remaining A documents is advanced to the intermediate position A', contact ka_1 will be closed as a result of the A input position and store having also been emptied and upon the operation of the relay Aar , relay Adr will energise in the same manner as relay Bdr was previously operated. Upon relays Bdr and Adr being both energised, relay Fr operates through a circuit including contacts ad_4 and bd_4 in series. It interrupts the holding circuits for these two relays at make contact f_1 . Relays Adr and Bdr consequently release and in turn cause the release of relay Fr . The latter should be made slow to release in order to ensure that both relays Adr and Bdr are released before relay Fr can again close its contact f_1 .

Upon the points position H having been liberated by the last A document, the circuit will be completely released.

During a sorting pass it might be desirable for some reason to stop the sorting operation. Either one may wish to stop the operations and make a completely new sorting pass or else, a temporary hold in the operation is desired, it being intended to restart the latter at a later moment.

When a final stop is desired, contact kt will be temporarily closed by a suitable push-button arrangement resulting in the operation of relay Tr through break contact sa of the starting relay which should of course be released at that moment, and break contact ku_2 . Relay Tr in oper-

ating, prepares, via make contact t_2 , an operating circuit for relay Er . The latter will be completed upon either relay Aar or relay Bar being operated to indicate that a document has reached an intermediate position and should now be dispatched to the points position. For instance upon relay Aar being energised, the closure of make contact aa_8 will energise relay Er . This relay locks through its make contact e_2 in series with the break contacts hb_1 and sc_4 . At make contact e_1 , the operating circuits for various relays will be interrupted, and in particular, relay Acr will be prevented from operating upon the A document having caused the operation of relay Aar having been dispatched to the points position. Hence, no further A document will be transferred to the intermediate position A'. The sorting pass will be ended because the comparator is now in such a condition that relay Ar is energised and accordingly since relay Br is de-energised, the B document in the corresponding intermediate position stays put and blocks also further advance of documents, this time for the B input position. Relay Er will be released upon the temporary operation of relay Hbr subsequent to the points having been returned to their normal position upon the last A document having been dispatched to one of the two output positions. The sorting pass is definitely ended, all relays being released with the exception of relay Ar .

Another result of the operation of relay Er will have been the interruption of the connection between terminal P_E and the 0 input of BS_1 (FIG. 2) due to the opening of contact e_3 . This will cause BS_1 to be placed in its 0 condition in a manner previously explained, with the result that the local advance pulses at terminal P_{O1} will wipe out the numbers inscribed in SRA and SRB.

If an intermediate stop is desired, the operations will be similar to those which have just been described, except that the operation of relay Er will be initiated due to the closure of contact ku_1 controlled by a suitable key or push-button. In such a case, however, relay Tr will not be operated. Instead, relay Ur will be operated through break contacts sa and kt , and make contact ku_2 . It locks through contacts u , and sb_3 in series with either a_3 or b_3 . Hence, despite the opening of contact e_3 , the connection between terminal P_E and the 0 input of BS_1 will be maintained through make contact u_2 to prevent wiping out the registers SRA and SRB. Since relay Ar and consequently relay Ur remain operated during the intermediate stop, when the sorting pass is restarted by the closure of contact ks , the displacement of contact s_2 cannot interrupt the connection between terminal P_E and the 0 input of BS_1 . Hence, in this particular case, the registers SRA and SRB will not be wiped out at the beginning of the operations so that the previous numbers stored in these registers will be used in order to decide whether the document which remained in the intermediate B position, or the new A document sent to the corresponding intermediate position, should be sent forward to the points position and thence to one of the two output positions. Upon relay Sbr having been operated, which means that at that time relay Sr has already released, the holding circuit for relay Ur will be interrupted at contact sb_3 and this relay will release without any possibility of the connection between terminal P_E and the 0 input of BS_1 being interrupted. Relay Ur should be assumed to be slow releasing so that it remains operated if relay Ar releases to be replaced by the energisation of relay Br , or vice-versa.

The control of the sequences of operations having been fully described, the comparator circuit CP represented as a block in FIG. 2 will now be detailed by referring to FIG. 5.

The comparator circuit CP of FIG. 5 is shown to include three comparator units CPA, CPB and CPC each provided with four input terminals such as P_{1C} , P_{2C} , P_{3C} and P_{4C} for CPC and with two output terminals such as P_{5C} and P_{6C} for this same comparator unit. All three comparator units are absolutely identical and CPC is detailed in FIG. 6.

As shown in FIG. 6, each comparator unit comprises a bistable device, a monostable device, 6 gates and 2 inverters. Terminal P_{1C} , which as shown by FIG. 5 is connected to terminal P_1 , which as shown by FIG. 2 receives the clock pulses from the document which is being read, constitutes one input of the coincidence gate G_{14} , whose other input is activated when the bistable device BS_2 is in its 1 condition. This will be obtained upon a pulse appearing at the 1 input of BS_2 which is connected to terminal P_{2C} . In turn, this terminal is connected to terminal P_2 (FIGS. 2 and 5), and at this terminal will appear a pulse either corresponding to the leading or to the trailing edge of the authorizing pulse which appears at terminal P_{02} when a document is being read. It will be assumed that only the leading edge of this authorizing pulse can be effective to trigger BS_2 into its 1 condition. From that moment, every clock pulse will be able to pass through the gate G_{14} and will trigger the monostable device MS_2 into its off normal condition where it will remain for a period of 60 microseconds. When MS_2 returns to its 0 condition, a trigger pulse which will be termed a comparison pulse, will be generated at its output. This is indicated in FIG. 6 by condenser coupling from the 0 output of MS_2 to indicate that the condition is only a transient one when MS_2 flops back to its normal condition. Hence, MS_2 functions as a delay device and the comparison pulses derived from its output as clock pulses are applied to its input are shown in FIG. 4. These pulses are applied to inputs of the coincidence gates G_{15} and G_{16} , the outputs of which respectively constitute one input of the coincidence gates G_{17} and G_{18} whose outputs are respectively connected to terminals P_{5C} and P_{6C} . The other input of G_{15} is connected to terminal P_{3C} , while the other input of G_{16} is connected to terminal P_{4C} . Further, terminal P_{3C} is connected to the input of the inverter I_1 whose output constitutes the second input of G_{18} . On the other hand, terminal P_{4C} is connected to the input of the inverter I_2 whose output constitutes the second input of G_{17} . Finally, terminals P_{5C} and P_{6C} act as inputs for the mixer gate G_{19} whose output is connected to the 0 input of BS_2 .

As shown by FIGS. 5 and 2, terminal P_{3C} is connected to stage 1 of SRA through terminal P_{AB} . On the other hand, terminal P_{4C} is connected to stage 1 of SRB through terminal P_{BA} . This means that the electrical conditions appearing at terminal P_{3C} and P_{4C} correspond to the digits which are at that time inscribed in stages 1 of SRA and SRB respectively.

With shift registers of $n+2$ stages, where n is the number of binary digits necessary to characterise a number, as shown by FIG. 2, an eventual information pulse always precedes the corresponding clock pulse by 100 microseconds as shown in FIG. 4. Hence, with a previous number C stored in SRA on the stages 1 to n included, when a new number A begins to be read, the eventual first information pulse will be registered in stage 0 of SRA. In other words, if each stage of the registers is mainly constituted by a cold cathode tube, the presence of this first information pulse characterising the binary digit 1 will ionize this cold cathode tube. On the other hand, if there is no information pulse, corresponding to the binary digit 0, stage 0 of SRA will not be ionized. A hundred microseconds afterwards, the first clock pulse will advance the pattern recorded on SRA and SRB by one stage. This means that the previously recorded numbers C and B will now be registered on stages 2 to $n+1$ included of SRA and SRB respectively while the first digit of the new number A will be recorded on stage 1. Since the first clock pulse appearing at terminal P_{1C} (FIG. 6) is allowed to produce a comparison pulse 60 microseconds afterwards and which is applied to the gates G_{15} and G_{16} , this comparison pulse will be able to compare the conditions existing at terminals P_{3C} and P_{4C} . Whereas the con-

dition at terminal P_{3C} corresponds now to the first binary digit of number A, the electrical condition at terminal P_{4C} corresponds to the first binary digit of the number B previously recorded in SRB, and which is allowed to recirculate in that register.

If it is assumed that a 0 digit in stage 1 of SRA or SRB corresponds to an activating potential at terminals such as P_{3C} or P_{4C} , the corresponding gate G_{15} or G_{16} will be made conductive to pass the comparison pulses derived from the clock pulse. Since the gates G_{17} and G_{18} are respectively controlled from terminals P_{4C} and P_{3C} through the inverters I_2 and I_1 , a 0 digit will block the corresponding gate G_{17} or G_{18} , while a 1 digit will make the corresponding gate G_{17} or G_{18} conductive to accept the comparison pulse. This means that if the first binary digits of A and B are both 0 or both 1, the comparison pulse will be blocked either by the gates G_{17} and G_{18} or by the gates G_{15} and G_{16} . If the first binary digit of A is 0 while the first binary digit of B is 1, gates G_{15} and G_{17} are conductive while gates G_{16} and G_{18} are blocked. Hence the comparison pulse will be able to flow through the gates G_{15} and G_{17} in series to appear at terminal P_{5C} . On the other hand, if the first binary digit of A is 1 while the first binary digit of B is 0, the comparison pulse will appear at terminal P_{6C} .

As soon as a pulse appears either at terminal P_{5C} or P_{6C} while the number A is progressively inserted into SRA while at the same time the previously recorded B number in SRB is circulated through the stages 1 to n of this shift register, this comparison pulse will pass through G_{19} to trigger BS_2 into its 0 condition. This blocks gate G_{14} which means that the next clock pulse appearing at terminal P_{1C} will not be able to generate a corresponding comparison pulse.

The reason for this blocking action as soon as a comparison pulse appears either at terminal P_{5C} or P_{6C} , is that it has been assumed that the binary digits used to characterize the numbers have been ordered so that the first binary digit of any number has the greatest weight, while the last has the smallest weight, and in general the weight of any binary digit is smaller than that of the previous digit and larger than that of a next digit. Hence, as soon as it has been detected that a binary digit of number A is greater or smaller than the binary digit of same weight, of the B number, one knows that A is greater or smaller than B. Further, the comparison between the two numbers must cease to be effective since otherwise it is obvious that a wrong result might be obtained.

The above does not essentially mean that the numbers should be registered as binary numbers. They are merely recorded by way of n binary digits in any suitable manner but such that when all the numbers are ordered, all the respective binary numbers corresponding to the coded representation of the numbers are in the same order. For example, numbers of $n/4$ decimal digits could be recorded by n binary digits using 4 binary digits to characterise a decimal digit. The first 4 binary digits would correspond to the decimal digit of highest weight of the decimal number and so on. Further, for every combination of 4 binary digits characterising a decimal digit, the first binary digit would have the highest weight and so on. For example, the following code could be used to characterise the decimal digits:

0	0000	5	1000
1	0001	6	1001
2	0010	7	1010
3	0100	8	1100
4	0101	9	1101

From this coding scheme it is seen that the first binary digit has a constant weight of 5, the second a weight of 3, the third a weight of 2 and the fourth a weight of 1. According to the rank of the decimal digit concerned,

these weights will then be multiplied by corresponding powers of 10. Although this binary coding of the decimal digits uses a so-called constant weight code, this is not essential.

It may be remarked also that although the circuit FIG. 6 is concerned with the case where the highest weights appear first, exactly the reverse order could be used with the lowest weight in front. In such a case however, the gate G_{19} should be suppressed and it would be the last comparison pulse appearing either at terminal P_{5C} or P_{6C} which would determine which of the two numbers is greater than the other. Since as shown by FIG. 5, terminals P_{5C} and P_{6C} lead to the respective inputs of a two input bistable device BS_3 , the latter might be switched over from one to the other stable condition several times during the dynamic comparison of the two numbers. However, only the last pulse appearing at one of the two terminals would determine the correct result of the comparison. Hence, provided the state of BS_3 is not exploited before all the digits of the two numbers have been compared to one another, the scheme shown in FIG. 6 could also be used when the binary digit with the lowest weight is in front.

One will remark also that the arrangement of FIG. 6 does not necessitate the comparisons between pulses of substantially the same length. The conditions at terminals P_{3C} and P_{4C} will remain for about 170 microseconds and the comparison pulse at the inputs of G_{15} and G_{16} is a trigger pulse of very short duration.

The shift registers SRA and SRB shown in FIG. 2 are shown to be provided with an $(n+2)$ th stage called the 0 stage, at the input. These extra stages are not absolutely essential and might be dispensed with if the clock pulses instead of lagging by a half period of 100 microseconds behind the eventual corresponding information pulses, would lead these pulses by the same interval of time. What is essential is to have at least $n+1$ stages for the registers so that a digit of the incoming number such as A can always be compared with the digit of corresponding rank of the number recirculating in B, or of the number C leaving SRA.

Returning to FIG. 5, the comparator units CPB and CPA function in exactly the same way as the comparator unit CPC detailed above in relation to FIG. 6. From FIGS. 5 and 2 it will be seen that whereas CPC successively compares the digits A and B, CPB compares the digits of A and C and still assuming that A is the number which is being progressively registered in SRA, CPA will be ineffective at that moment in the sense that it will merely compare the number B with itself since the number B is recirculating through SRB as shown in FIG. 2. If the number B was coming into SRB while the number A previously recorded in SRA was recirculating through that register, it would be the comparator unit CPB which would not make a comparison beyond comparing A with itself.

Hence, taking as example the case of A being inserted in SRA, A is compared with B and A is compared with C the outgoing number. Despite the fact that B is not compared with C, the two comparisons which are performed will nevertheless provide an indication of the order between A, B and C which can be ordered in six different ways, without regard to the special cases of equalities.

The reason justifying the fact that the recirculating number B is not actually compared with the outgoing number C is the following:

If when A comes in to replace C in SRA, the bistable device BS_4 indicates B greater or smaller than C, these relations are respectively applicable with respect to the C number presently leaving SRA despite the fact that they were obtained with regard to the number which left SRB when the B number now inscribed in SRB was inserted therein.

The bistable device BS_4 is of course analogous to the bistable device BS_3 and records the results of the comparison given by CPA by having its two inputs connected to the terminal P_{5A} and P_{6A} through the mixer gates G_{21} and G_{20} respectively. Likewise, BS_5 indicating the relation between A and C has its two inputs connected to the terminal P_{5B} and P_{6B} through the respective mixer gates G_{22} and G_{23} .

If it is assumed, BS_4 registers $B > C$, it means that when B came into SRB it was found larger than the number which left SRB at that time. If the B number has stayed into SRB since then, it must mean that the number which was at that moment stored in SRA left and that it was therefore smaller than B, and greater than the number which left. Since then, all the numbers which have passed through SRA cannot have decreased in value but they must have remained smaller than B. Hence, the number C which is now leaving SRA must in fact be smaller than B.

On the other hand, if BS_4 indicates $C > B$, it means that when B came into SRB it was smaller than the number leaving SRB at that time. If B stayed in SRB, this must mean that the number which was at that time stored in SRA left and that it was therefore greater than the number which left and than B, provided that the number which left and was replaced by B was not at the same time also greater than the number stored in SRA. With this important provision on which a further explanation will be given, the number which left SRA after B had been registered in SRB must have been greater than B. Further, the numbers which have since then passed through SRA cannot have decreased in value and the number C which is now leaving SRA to be replaced by A must therefore be greater than B as indicated by the condition of BS_4 .

Hence, the above reasoning proves that the condition of BS_4 , i.e. B greater or smaller than C does give a correct indication of the relation between the number C presently leaving SRA and the number B stored in SRB and recirculating in the latter register, despite the fact that BS_4 was set in its condition while the B number was compared with a number other than that presently leaving SRA. But, this reasoning is only valid provided an outgoing number was not at any time greater than the incoming number and greater than the recirculating number. Such a condition can of course, arise, but the comparator is provided with means which will cause an automatic restoration of the bistable devices BS_4 and BS_5 upon these being found to respectively indicate $C > B$ and $C > A$. If such an condition arises, BS_4 and BS_5 are automatically placed in the conditions $B > C$ and $A > C$ respectively. This automatic reset was already mentioned previously and as particularly useful in connection with batch sorting upon the operation of relay *Adr* or *Bdr*. The main usefulness of this automatic reset is however to permit making only a comparison between the incoming and the outgoing number, and between the incoming and the recirculating number, while avoiding making a comparison between the recirculating and the outgoing number. This could, of course, be made but it would mean that the comparator units CPA and CPB would not have permanent input connections. Upon a number coming into SRA, the connection between terminals P_{4A} and P_{CB} would have to be replaced by a connection between terminals P_{4A} and P_{CA} . On the other hand, upon a number coming into SRB, the connection between terminals P_{3B} and P_{CA} would have to be replaced by a connection between terminals P_{3B} and P_{CB} . This would then permit to make effective comparisons between the three pairs of numbers. This is not difficult to achieve since the switching over could be controlled by the activating potential present either at terminal P_A or at terminal P_B and which indicates the shift register into which a number is coming, but additional gating means would be necessary.

One may remark that the reasoning justifying the comparison of two pairs of numbers only out of the three is incomplete in so far as the condition $B > C$ is concerned since this might have resulted from the explained automatic reset, upon the B number in SRB and a number entering SRA having both been found smaller than the number which was leaving SRA at that time. But, if the B number stayed since then in SRB, this must mean that the number having entered SRA at that moment was smaller than B. One is therefore brought back to the general reasoning for the condition $B > C$ since although all the numbers having passed through SRA may have increased in value, they must nevertheless have remained smaller than B. Hence the C number which is now leaving SRA is truly smaller than B as indicated by the condition of BS₄.

After a number A has been fully entered in SRA, the bistable devices BS₃, BS₄, BS₅ are now set in respective conditions which indicate the correct relationship between A, B and C. The circuit of FIG. 5 is therefore ready to exploit these conditions in order to activate one of the terminals P_A and P_B, and one of the terminals P_C and P_D. This activation will be performed by the differentiated trailing edge of the authorizing pulse at terminal P_{O2} and which appears at terminal P₂. Whereas the leading edge of this authorizing pulse was used to make the circuit of FIG. 6 ready to make a comparison, the inverter I₃ indicates that the differentiated trailing edge of this authorizing pulse will appear as an active signal at the output of I₃ which is connected to an input of the mixer gate G₂₇. As the output of G₂₇ is connected to an input of the three gates G₂₄, G₂₅ and G₂₆, this output signal will attempt to pass through one of these three coincidence gates. The first G₂₄, has two further inputs respectively controlled by BS₄ indicating $C > B$ and by BS₅ indicating $C > A$. The second, G₂₅, has two further inputs respectively controlled by BS₄ indicating $C > B$ and through the mixer gate G₂₈, and by BS₅ indicating $A > C$. Finally, the third, G₂₆, has two further inputs respectively controlled by BS₄ indicating $B > C$ and by BS₅ indicating $C > A$, through the mixer gate G₂₈. Further, alternatively to G₂₅ being controlled by BS₄ indicating $C > B$ it can also be controlled by BS₃ indicating $B > A$ through G₂₈. Similarly, G₂₆ apart from being controlled by BS₅ indicating $C > A$, it can also be controlled by BS₃ indicating $A > B$ through G₂₈.

It can be remarked that when a pulse appears at the output of G₂₇, one and only one of the three coincidence gates G₂₄, G₂₅ and G₂₆ will always be ready to let that pulse flow through.

If the pulse is able to flow through gate G₂₅, this means that the conditions are such that the A number corresponds with a document which should be made to advance to the points position and to be directed to an output position which is the same as the one to which the C document was sent. Also this will mean that the next A document should come from the A input position to have its number inscribed in SRA. Hence, the output of G₂₅ constitutes the first input of the bistable device BS₇ and the output terminal P_A, corresponding to the A condition of BS₇, will be activated. Likewise, if it is G₂₆ which delivers an output signal, this will trigger BS₇ into its B position if it was not already in that condition and terminal P_B will be activated.

If the pulse at the output of G₂₇ is on the other hand able to penetrate through G₂₄, this is because A and B are both smaller than C. Hence, a change of output is required either for the A or the B document. The appearance of this pulse at the output of G₂₄ does not therefore indicate which of the A or B document should be sent forward, but that whatever document is sent forward, it will have to follow a direction opposite to that taken by the C document. This output pulse is applied to the single input of the bistable device BS₆ which therefore acts as a scale-of-two counter. If it was in

condition C activating terminal P_C it will now pass into condition D activating terminal P_D and vice versa.

Apart from being connected to the single input of BS₆, the output of G₂₄ is also connected to the inputs of the monostable devices MS₃ and MS₄. The first is shown to have a time constant of 50 microseconds and the second a time constant of 100 microseconds. They serve as pulse delay devices for the pulse which may appear at the output of G₂₄. Some 50 microseconds after having been triggered by the pulse at the output of G₂₄, MS₃ by being restored to its stable condition, will produce a pulse which, through the respective mixer gates G₂₀ and G₂₂ will trigger BS₄ and BS₅ into conditions respectively indicating $B > C$ and $A > C$. This is the reset operation previously explained.

A further 50 microseconds afterwards, MS₄ which was triggered simultaneously with MS₃, by automatically returning to its stable 0 condition, will generate a pulse which through G₂₇ will be applied to the three gates G₂₄, G₂₅ and G₂₆, just as the pulse at the output of I₃ was applied to these three coincidence gates. However, G₂₄ is now blocked and either G₂₅ or G₂₆ is unblocked. Hence, the pulse produced by MS₄ will appear either at the output of G₂₅ or at the output of G₂₆ to place or leave BS₇ in the condition indicating whether the A or the B document should be sent to the points position.

The time constants of MS₃ and MS₄ are not in any way critical since it is merely desired that an output pulse generated by MS₃ should follow its input pulse and that the output pulse generated by MS₄ should follow that generated by MS₃. One could, of course, trigger MS₄ with the output signal of MS₃ and in such a case MS₃ and MS₄ might for example have the same time constant of 50 microseconds.

A further input of the mixer gate G₂₇ is connected to terminal P₃ which as shown by FIGS. 3 and 2 can receive a pulse when either of the batch sorting relays A_{dr} or B_{dr} operates to connect terminal P_E through make contact *ad*₂ or *bd*₂ to terminal P₃ via a differentiating circuit indicated by a condenser coupling. Hence, this pulse which is needed due to the last document in an input position not having been replaced by a further document, will simply investigate the conditions of the comparator circuit CP in exactly the same way as the pulse generated by the trailing edge of the authorizing pulse at terminal P₂ investigates the conditions of the comparator after every comparison. Such a pulse for batch sorting will of course have been preceded by the opening of the connection between terminals P_{BC} and P_E or P_{AC} and P_E having, through the mixer gates G₂₁ or G₂₃, caused BS₄ or BS₅ to be placed in the conditions $C > B$ or $C > A$ respectively.

With respect to the pulse generated by the closure of relay A_{dr} or B_{dr} at terminal P₃, the design of the comparator circuit CP including the reset feature has the further advantage that eventual contact vibrations can easily be dealt with. Indeed, if more than one effective pulse should appear at terminal P₃ and if BS₄ and BS₅ indicate $C > B$ and $C > A$, more than one pulse could reach the scale-of-two circuit BS₆ which might therefore respond incorrectly. However, some 50 microseconds after the first pulse, MS₃ will trigger BS₄ and BS₅ so that G₂₄ becomes blocked and this gate cannot accept eventual further pulses at the terminal P₃. Gate G₂₅ or G₂₆ can accept them together with the pulse generated by MS₄ but this is of no consequence since gates G₂₅ and G₂₆ feed into a particular input of the two input bistable devices BS₇. The time constant of MS₃ can evidently be selected so that G₂₄ cannot pass more than one pulse appearing at terminal P₃.

It will be observed that the circuit of FIG. 5 does not need to exploit an eventual condition of the comparator units CPA, CPB and CPC such that one of these would

indicate that the two numbers which it has compared are equal. Considering the circuit of FIG. 6, the comparator unit can readily provide such an indication by the fact that BS₂ after a comparison, would have remained in its 1 condition. However, as will be now explained, the detection of such an equality condition is not needed. This means that, if the numbers are compared with the weights of their digits in ascending order, lowest weight in front, not only the gate G₁₀ but also the bistable device BS₂ could be dispensed with. In such a case, one might also avoid the gate G₁₄. Further, the monostable device MS₂ which is provided in each comparator unit such as CPC could then be common for the three comparator units since an individual blocking of the comparison pulses arriving at a particular comparator unit such as CPC would no longer be needed. One would merely require that the comparison pulses follow the clock pulses by some suitable interval of time necessitating only a single common monostable device.

The adequate functioning of the circuit of FIG. 5 in the case of equalities between numbers, is again due to the reset feature for the bistable devices BS₄ and BS₅ in the event that both A and B are smaller than C.

Two cases of equalities can be considered. Either the incoming number in one register is equal to the number which is already stored in the other register, or it is equal to the number which it replaces in said one register.

Considering the case of the numbers A and B having been compared with the outgoing number C with the result that A went out, one will first assume that the number A' which comes in to replace A is equal to B. If A went out, this means that one had the conditions

$$B > A > C$$

or

$$A > C > B$$

or

$$C > B > A$$

Considering now that A' is equal to B, the three previous conditions will respectively lead to

$$B > A' > A$$

or

$$A > A' > B$$

or

$$B > A' > A$$

These last three conditions can be readily verified by considering for example the first. Since one had $B > A$, this will on the one hand lead to $B > A'$ since the comparator unit CPC and more particularly BS₃ will stay in its previous condition. On the other hand, the previous $B > A$ condition leads to $A' > A$ since $B = A'$.

As can be readily inspected, the three possible conditions obtained after the insertion of $A' = B$ into SRA are such that either the A' or the B document is sent forward which is immaterial, but that the B document will be sent in the reverse direction to that taken by the A document in the case that A was greater than C which was in turn greater than B.

In fact, the three conditions which have been considered above include the one where C is greater than B which in turn is greater than A, which condition cannot stay when the reset is used. The automatic reset will produce instead B greater than A which in turn is greater than C. Hence, with or without automatic reset, the case of an incoming number being equal to the number already stored in the other register is adequately dealt with despite the absence of the inspection of an equality in the actual comparison.

Considering now the case where $A' = A$, the three possible conditions which may have led to the entrance of A' to replace A are the same as before but in view of

the equality $A' = A$ one can now derive the corresponding conditions

$$B > A' > A$$

or

$$A' > A > B$$

or

$$B > A > A'$$

This can be explained for example by considering the previous $B > A > C$ condition, i.e. the first possibility. On the one hand, $A > C$ leads to $A' > A$ since the comparator unit CPB and particularly BS₅ will stay in its previous condition. On the other hand, $B > A$ leads to $B > A'$ in view of the equality between $A > A'$.

For the first two possibilities, one observes that the A' document shall necessarily follow the A document in the same direction, which is the correct course. For the third possibility, this indicates that the B document shall follow the A document. This is not correct because it would mean that despite $A' = A$, the A' document is not allowed to follow the A document although it is smaller than B but not smaller than A.

However, this third possibility arises when both A and B are smaller than C which condition is not allowed to persist until the next comparison due to the automatic reset. Hence, the third possibility will in fact not exist and it is automatically replaced by the first which leads to correct operations.

Although the invention has been described in relation to the sorting of documents such as cheques bearing magnetic marks indicating their characteristic numbers, or being supported on document carriers which in turn also carry pieces of magnetic tape on which said numbers are inscribed, it will be clear that the invention is not particularly limited to such an application. First of all, if one considers document carriers, the documents might well be ordinary letters for example, which would be automatically sorted in the manner explained after the mail had first been processed by operators to associate each letter with its carrier bearing indicia characterising the address of the corresponding letter. Further, there might not be any documents at all associated with the numbers. This might for example correspond to telephone numbers associated with satellite information characterizing the cost of a telephone call made by the corresponding telephone subscribers. Such information may be randomly recorded as the calls are made, but later on a sorting in accordance with the calling substation numbers is useful for accounting purposes so that any calling subscriber can be properly debited for all his calls. In such a case, there would be two input magnetic tapes and two output magnetic tapes and each sorting pass would be made substantially in the manner described, the sequence controller of FIG. 3 being of course suitably modified, but the comparator arrangement of FIGS. 2, 5 and 6 remaining substantially the same.

Each number which is used for sorting into the required final natural order will in general be accompanied by a satellite number or numbers. In the case of cheque sorting which has been particularly envisaged, the sorting is made in accordance with the account number but the latter is also accompanied by a number characterizing the amount. The two numbers may be serially inscribed on the same piece of magnetic tape or not. In the description of the embodiment of the invention, no particular attention was paid to the account number being followed or not by the amount. If it is, the shift registers can well store the two numbers in series and in such a case the sorting will be made in accordance with the account numbers as recorded, but for cheques bearing the same account numbers, a subsidiary sort will automatically be made in accordance with the various amounts of these cheques. This may in fact prove to be a useful feature. Alternatively, a separate piece of magnetic tape could be used for recording the amounts, or in general arrangements could be made so that the

amounts or more generally any satellite information would not be read at all, in which case the shift registers would only need to record the account numbers. Then, for a series of cheques bearing the same account number, after the final sorting pass, these would be found together but they would not necessarily be ordered in accordance with the amounts.

The use of the shift registers in accordance with the invention does not necessarily imply the use of the particular comparator circuit shown in FIG. 5, but the latter has been shown to possess advantages particularly from the point of view of simplicity. Also, the shift registers are initially made to indicate 0 numbers in order to properly start a sorting pass. Again, this is not absolutely essential since one could also make a correct start by a special use of the comparator circuit at the start of the operations, while at least one of the arbitrary fictitious numbers would still be stored in the shift registers. Such a solution is however believed to be rather more complicated than the simple wiping out of the shift registers at the start of the operations.

Further, the gates such as G_2 , G_3 and G_9 , G_{10} might not be found absolutely essential bearing in mind that pulses either appear at P_{A1} and P_{A2} or at P_{B1} , and P_{B2} and that it is only required that the eventual information pulses at P_{A2} or P_{B2} should be directed to the 0 stage of either SRA or SRB respectively, which is in any case obtained by G_7 and G_8 .

Therefore, while the principles of the invention have been described above in connection with specific apparatus, it is to be clearly understood that this description is made only by way of example and not as a limitation on the scope of the invention.

What is claimed is:

1. In an electrical sorting system for sorting electrically represented numbers associated with electrically represented satellite information in which the numbers to be sorted are arranged in first and second initial successions of N_1 and N_2 numbers, each succession being in any arbitrary order, and the sorting is done by a binary collation process which obtains a new pair of successions of the N_1 and N_2 numbers in such a manner that the first sequences of numbers ordered in the desired manner and found in said two initial successions are merged together to constitute the first sequence of the first new succession, and the second sequences found in said two initial successions are also merged together to constitute the first sequence of the second new succession, and similar merging operations produce a new sequence alternately for the first and the second new successions, the combination of a first and a second electrical shift register, each having at least $n+1$ stages, where n is the number of binary digits needed to characterize any number, means for progressively inserting numbers alternately in said first and second registers respectively from said first and said second initial successions, means for simultaneously and progressively recirculating a number in one of said registers while a new number is being inserted in the other of said registers, means responsive to the progressive insertion into one of said registers of a number from one of said initial successions for progressively expelling the number previously recorded therein, first comparing means for comparing the expelled number from said first shift register digit-by-digit with the number progressively inserted therein, second comparing means also responsive to the progressive insertion of a number into one of said registers from one of said initial successions for comparing said inserted number digit-by-digit with the number being recirculated in said other register, third comparing means responsive to the progressive insertion into said second register of a number from said second initial succession for comparing the number being expelled from said second register digit-by-digit with the

number being inserted therein, means responsive to the complete insertion of a number from one of said initial successions into one of said registers and controlled by all of said comparing means for indicating the order of the three numbers compared, and means controlled by said indicating means for operating said number inserting means to insert a number from that succession corresponding to the register from which a number is to be expelled.

2. In an electrical sorting system, the combination, as defined in claim 1, in which the indicating means comprises first, second, and third bistable devices controlled respectively by the first, second and third comparing means, means for triggering each of said bistable devices into one state when a particular one of the two numbers compared by the corresponding comparing means is larger and into the other state when the other number is larger, first, second, and third gates, means for causing said first gate to deliver an output signal when said first and third bistable devices together indicate that the number expelled from either register is larger than the number in both registers, thus indicating that the expelled number is the last number of a sequence in a first or second new succession, means for causing said second gate to deliver an output signal when said first and third bistable devices together indicate that said expelled number is smaller than the number in said first register and larger than the number in said second register, thus indicating that a sequence in a new succession is not complete and that the sequence should be continued from said first register, means for causing said third gate to deliver an output signal when said first and third bistable devices together indicate that said expelled number is smaller than the number in said second register and larger than the number in said first register, thus indicating that a sequence in a new succession is not complete and that the sequence should be continued from said second register, a fourth bistable device operating as a scale-of-two counter, the two stable states of which correspond respectively to said first and second new successions, means for causing signals delivered by said first gate to trigger said fourth bistable device alternately from one bistable state to the other, a fifth bistable device in which the first and second bistable states correspond respectively to said first or said second register having to continue the sequence including said expelled number, means for causing the signal delivered by said second gate to trigger said fifth bistable device into its first state and means for causing the signal delivered by said third gate to trigger said fifth bistable device into its second state.

3. In an electrical sorting system, the combination as defined in claim 2, further comprising means responsive to the signal delivered by the first gate for causing a reversal of the states of both the first and third bistable devices, and means for preventing the second and third gates from delivering a signal until after said reversal has been accomplished.

4. In an electrical sorting system, the combination, as defined in claim 2, further comprising means responsive to one of the initial successions of numbers having all been inserted in the corresponding register for rearranging the states of the first and third bistable devices to cause the first gate to deliver an output signal, whereby any remaining numbers are alternatively stored in one or the other of the two new successions in accordance with their initial sequences.

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