(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
13 February 2025 (13.02.2025)

WIPO | PCT

(10) International Publication Number
WO 2025/035150 A1

(51) International Patent Classification:
H01L 21/768 (2006.01) *H01L 29/66* (2006.01)
H01L 23/528 (2006.01)

(21) International Application Number:
PCT/US2024/041939

(22) International Filing Date:
12 August 2024 (12.08.2024)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
63/518,691 10 August 2023 (10.08.2023) US

(71) Applicant: **GEORGIA TECH RESEARCH CORPORATION** [US/US]; 926 Dalney Street NW, Atlanta, Georgia 30318 (US).

(72) Inventor: **NIMBALKAR, Pratik**; 791 Atlantic Drive NW, Atlanta, Georgia 30318 (US).

(74) Agent: **TANPITUKPONGSE, Paul T.** et al.; Meunier Carlin & Curfman LLC, 999 Peachtree Street NE, Suite 1300, Atlanta, Georgia 30309 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CV, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IQ, IR, IS, IT, JM, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, MG, MK, MN, MU, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, WS, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, CV, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SC, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, ME, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:
— *of inventorship (Rule 4.17(iv))*

Published:
— *with international search report (Art. 21(3))*

(54) Title: POLYMERIC PACKAGE SUBSTRATES AND METHODS OF FABRICATION

(57) **Abstract:** An example method for fabricating an interconnect includes using the spontaneous deposition of a vapor-phase monomer of parylene onto a workpiece to form a parylene polymer layer or a build-up structure of layers in the workpiece for use in device or component fabrication, electronic manufacturing, encapsulation, and packaging, or integration packaged substrate, e.g., semiconductor devices, e.g., chiplets, via advanced multi-surface, interconnects. The example method further includes planarizing or over-planarizing the polymer to expose surfaces of a metal layer, forming additional metal layers, and introducing additional vapor monomer. An example device includes a high-density interconnect wiring structure, including a high-density metal wiring with a first wire and a second wire, and a dielectric layer formed between the first metal wire and the second metal wire, wherein the dielectric layer is conformally applied and spontaneously deposited.

WO 2025/035150 A1

POLYMERIC PACKAGE SUBSTRATES AND METHODS OF FABRICATION

Related Application

[0001] This application claims priority to, and the benefit of, U.S. Provisional Patent Application No. 63/518,691, filed August 10, 2023, entitled "EMBEDDED INTERCONNECT BRIDGE AND METHODS OF MAKING THE SAME," which is incorporated by reference herein in its entirety.

Background

[0002] Semiconductor packages provide an enclosure for semiconductor devices (e.g., integrated circuits). Semiconductor packages both protect the semiconductor device and provide connections to the semiconductor device. Packages can include leads that couple the semiconductor device to various types of connectors and connections.

[0003] In some devices, a semiconductor package can include multiple semiconductor devices formed on a substrate. The semiconductor package can include connections formed on the substrate to couple the multiple semiconductor devices and/or connections formed on the substrate to connect the semiconductor devices to external devices.

[0004] There are benefits to the improvements of semiconductor package interfaces and methods of fabricating semiconductor packages among other electrical devices and components.

Summary

[0005] Exemplary methods, systems, and devices are disclosed for the spontaneous deposition of a vapor-phase monomer of parylene, which could occur at or near ambient temperature, onto a workpiece to form a parylene polymer layer or a build-up structure of layers in the workpiece for use in device or component fabrication, electronic manufacturing, encapsulation, and packaging, or integration semiconductor devices, e.g., chiplets, via advanced multi-surface, and interconnects.

[0006] The exemplary spontaneous deposition of parylene can be employed to form a number of geometries to produce a finished electronic device with desirable electrical and mechanical properties, particularly with a low dielectric constant that is desirable for next-generation 5G, 6G, and millimeter-wave communication devices and components, photovoltaic cells, processors, GPU, AI chips, while being mechanically durable and chemically resistant to moisture. The spontaneous deposition via polymeric vapor can be performed, similar to chemical vapor deposition, but at a pressure at least 4 orders of magnitude higherthan that of near vacuum operation typically employed for CVD and at or

near ambient temperature, and/or without any curing. With more relaxed manufacturing and/or fabrication environments (lower temperatures, no curing, less vacuum), the exemplary methods and system can be performed in a more straightforward operation and/or at a higher speed of fabrication.

[0007] Spontaneous polymerization is that which occurs in the absence of an added radical source. During spontaneous polymerization, the monomer that is present in high concentrations tends to form a fabric-like structure on the substrate or within the pre-existing networks of the polymer. Additionally, spontaneous polymerization of vapor-phase monomers directly onto the workpiece can eliminate the stresses due to curing and thermal expansion. This characteristic can be beneficially employed, particularly for larger panel-scale substrates and larger body-size interposers for advanced semiconductor packaging. The typical fabrication process for polymer layers often employs heating can cause the workpiece (e.g., semiconductor) to warp, thus limiting the size of the workpiece that can be employed with conventional processes. Larger semiconductor devices can be used in high-performance computing applications which can benefit from larger substrate sizes. The accumulated stresses due to multiple layers of polymer also cause cracking of brittle substrates such as glass and organic laminates. The use of low-stress polymer deposition processes such as spontaneous polymerization of parylenes can reduce these stresses significantly thereby preventing cracks and improving the reliability of substrates.

[0008] An example embodiment of the present disclosure includes polymeric package substrates and methods of fabrication for the polymeric package substrates. The example embodiments described herein can overcome the limitations of conventional polymer dielectrics. Those polymer dielectrics used in package substrates are often applied using vacuum lamination or liquid spin coating. These polymer dielectrics need to be cured as a part of the application process. This induces stresses in the substrate due to curing shrinkage associated with these dielectrics. These shrinkages occur due to the presence of solvent in these dielectrics. The curing stresses cause warping of the substrates, especially when the panel sizes or package/substrate sizes are considerably large. These conventional polymer dielectrics need to be cured before undergoing any further processing due to the inadequate mechanical stability of uncured dielectrics. The trend in semiconductor packaging is towards larger body/package/substrate sizes. Therefore, low-stress polymer dielectrics, as described in embodiments of the present disclosure, can overcome these issues by providing large body/package/substrate sizes with minimum warpage. Larger substrates also have a problem of cracking during singulation or dicing. With the help of low-stress polymers like parylene,

the stresses are significantly reduced since there is no curing shrinkage due to absence of solvents. These reduced stresses give improved reliability and prevent cracking of substrates during singulation and during operational use.

[0009] In some embodiments, the exemplary system and method can be employed for a molded substrate or other substrate described herein, e.g., with embedded chips for fan-out or embedded wafer bonding. Polymer dielectrics can be deposited on the molded substrate to form interconnections between multiple embedded/molded chips, chiplets (small, modular chips that can be combined to form a complete system-on-chip (SoC)), devices, components, passives, and/or actives.

[0010] An example embodiment of the present disclosure includes polymeric package substrates and methods of fabrication for the polymeric package substrates. The example embodiments described herein can overcome the limitations of conventional polymer dielectrics. Those polymer dielectrics used in package substrates are often applied using vacuum lamination or liquid spin coating. These polymer dielectrics need to be cured as a part of the application process. This induces stresses in the substrate due to curing shrinkage associated with these dielectrics. These shrinkages occur due to the presence of solvent in these dielectrics. The curing stresses cause warping of the substrates, especially when the panel sizes or package/substrate sizes are considerably large. These conventional polymer dielectrics need to be cured before undergoing any further processing due to the inadequate mechanical stability of uncured dielectrics. The trend in semiconductor packaging is towards larger body/package/substrate sizes. Therefore, low-stress polymer dielectrics (as described in embodiments of the present disclosure) can overcome these issues by providing large body/package/substrate sizes with minimum warpage.

[0011] The example embodiment of the present disclosure includes polymer dielectrics such as parylenes that can be vapor deposited. The mechanism of deposition in such dielectrics can be different than the conventional dielectrics. For example, Parylene can be vapor deposited onto substrates with a process that resembles chemical vapor deposition (CVD). However, the process pressures are higher at 10-100 mTorr (e.g., 100 mTorr) compared to the conventional vapor deposition pressures of $<10^{-5}$ Torr. Parylene deposition is not a line-of-sight deposition, meaning the gaseous monomer uniformly deposits on all surfaces it comes into contact with. This results in truly conformal and uniform coatings without porosity over large panel areas. Parylene deposition can include three main steps- (1) Vaporization, (2) Pyrolysis, and (3) Deposition. The first step is the vaporization of the solid dimer can be carried out at 80-200°C (e.g., 150 °C). Pyrolysis of the vaporized dimer can be

carried out in the pyrolysis chamber at 400°C -800°C (e.g., 680 °C). The cleavage of the methylene-methylene bonds occurs during pyrolysis, which can yield the stable monomer diradical- para-xylylene. The monomer vapor then enters the deposition chamber, which can be at room temperature. The deposition and polymerization of parylene occur spontaneously on the substrate.

[0012] Spontaneous polymerization on the substrate can reduce or eliminate the curing stresses associated with conventional polymer dielectrics. This can minimize the warpage of the substrates, thus allowing better process control during the subsequent processing steps. Low warpage is especially crucial for lithography. Significantly warped substrates cause sub-optimal focusing during lithography, leading to poor resolution of photoresists. The accumulated stresses due to multiple layers of cured polymer can lead to cracking of the brittle substrate cores. Spontaneous polymerization eliminates the curing stresses, thereby minimizing the accumulated stresses in a multilayer substrate.

[0013] Polymerization of these polymers can take place at ambient/room temperatures, thereby eliminating the thermal stresses. Furthermore, spontaneous polymerization also eliminates the curing step, which is often necessary with conventional polymer dielectrics for further processing.

[0014] Thermal processes are usually expensive due to the consumption of high power and long process durations. Curing processes can add high or significant costs to conventional package substrates due to the multiple curing steps required for each layer of dielectric. Spontaneous polymerization on substrates also eliminates multiple curing steps, thereby lowering the cost significantly. The core substrate can be organic laminate, glass, silicon, metal, polymer mold compound, fan-out, or a combination of one or more of those.

[0015] Vapor deposition of polymer dielectrics also allows deposition on both sides simultaneously, thus lowering the costs further. Furthermore, core substrates having through-holes can be coated with vapor-deposited polymer dielectrics due to their conformal coating characteristic.

[0016] Curing stresses can also cause the cracking of fragile substrate materials such as glass. Spontaneous polymerization also reduces the chances of such cracking due to zero curing stresses.

[0017] Such spontaneously deposited polymer dielectrics can be used in a package substrate for multiple layers having different functions, such as a build-up dielectric layer, solder-mask layer, thermal-interface material, underfill, and/or an overmold.

[0018] When used as a thermal-interface material, a thin conformal layer of the polymer dielectric can be deposited onto the package, followed by the deposition of a high thermal conductivity material such as a metal or a composite.

[0019] Parylenes also have other unique properties, such as excellent barrier resistance to moisture, vapor, and corrosive gases. Parylenes have a low coefficient of friction and some of them are also biocompatible, making them useful in a variety of bio-compatible packaging applications. Low dielectric constant and low dielectric loss of Parylene-HT and Parylene-N are useful for high-frequency applications in semiconductors and electronic components.

[0020] Non-limiting examples of spontaneously deposited polymers that can be used in embodiments of the present disclosure include poly-para-xylylenes, which are widely known by their commercial names- Parylene-N, Parylene-C, Parylene-D, Parylene AF-4 atoms), Parylene SF, Parylene HT (AF-4, SCS product), Parylene A, Parylene AM (one methylene amine group per repeat unit), Parylene VT-4 (generic name, fluorine atoms on the aromatic ring), Parylene CF, and Parylene X (a cross-linkable version, not commercially available). Package substrates can utilize one or a combination of the above-mentioned polymers.

[0021] In some aspects, implementations of the present disclosure include a method of fabricating an interconnect, the method including: formation of a metal layer on a base substrate (e.g., glass, fused silica, glass ceramic or ceramic, or dielectric); formation of copper pillars on at least a portion of the first metal layer; vaporizing a source material at a first temperature and a first pressure to form a vapor dimer of the source material; heating the vapor dimer in an inert environment to a second temperature to form a vapor monomer at a second pressure, wherein the second temperature is higher than the first temperature, and wherein the second pressure is lower than the first pressure; and introducing the vapor monomer to a chamber having a workpiece for an interconnect (e.g., bridge die, high-density interconnect) having an exposed surface and plurality of metal pillars to spontaneously deposit and polymerize the vapor monomer to form a first layer of a conformal layer of a polymer on at least the exposed surface of the workpiece and surrounding the plurality of metal pillars; planarizing or over-planarizing the polymer to expose a plurality of top surfaces of the plurality of metal pillars; forming additional metal layers, including a second metal layer having metal pillars, on the polymer and the exposed top surfaces of the plurality of metal pillars; introducing additional vapor monomer to the chamber to spontaneously deposit and polymerize the additional vapor monomer to form an additional layer, including a second

layer, of a conformal layer of the polymer on at least the exposed top surfaces of the plurality of metal pillars; planarizing or over-planarizing the polymer of each of the additional layers, including the second layer, to expose respective top surfaces of the plurality of metal pillars of the additional metal layers; and forming a top metal layer on a top polymer layer having the exposed plurality of top surfaces to form the interconnect.

[0022] In some aspects, implementations of the present disclosure include a method, including: a) depositing a metal seed layer on a base substrate (e.g., glass, fused silica, glass ceramic or ceramic, or dielectric); b) forming a first metal layer on the metal seed layer; c) applying a layer of a photoresist on a top surface of the first metal layer and patterning the photoresist, followed by forming the plurality of metal pillars at predetermined locations on the first metal layer; d) removing the photoresist layer and exposed portions of the metal seed layer; e) conformally depositing an inorganic barrier layer on metal structures and exposed top surface portions of a base substrate to form the first layer; f) conformally depositing an overburden layer of a polymer dielectric on the inorganic barrier layer and underlying metal structures; g) planarizing or over-planarizing the polymer dielectric to expose the top surfaces of the plurality of metal pillars; and h) forming a metal layer connected to the exposed top surfaces of the plurality of metal pillars.

[0023] In some aspects, implementations of the present disclosure include a method, wherein the metal seed layer is deposited on the base substrate using electroless, physical vapor deposition (PVD, chemical vapor deposition (CVD) or a sputtering process.

[0024] In some aspects, implementations of the present disclosure include a method, wherein the inorganic barrier layer is made from a material including SiO2, SiC, Si3N4, MgO, ZrO2, SiOx, AlOx, SiNx, TiOx, TaNx, WNx, Ta, Ti or a combination of these. Where ‘x’ is a stoichiometric coefficient ranging from 0.01 to 10.

[0025] In some aspects, implementations of the present disclosure include a method, wherein the overburden layer of the polymer dielectric is formed by a spontaneous polymerization or chemical vapor deposition (CVD) process, wherein the spontaneous polymerization or CVD process do not have filler particles.

[0026] In some aspects, implementations of the present disclosure include a method, wherein the polymer dielectric is a poly-para-xylylene, an acrylic, an epoxy, a polyurethane, a silicone, a poly(tetrafluoroethylene), a polyimide, a fluoropolymer or any combination thereof.

[0027] In some aspects, implementations of the present disclosure include a method, further including: i) completing steps b) through h) again.

[0028] In some aspects, implementations of the present disclosure include a method, wherein steps f), g), h), and i) are completed more than one time.

[0029] In some aspects, implementations of the present disclosure include a bridge die prepared by a process of the methods described herein.

[0030] In some aspects, implementations of the present disclosure include an electronic device including a bridge die.

[0031] In some aspects, implementations of the present disclosure include a device (e.g., a bridge die, an interposer, or a die substrate) including: a high density interconnect wiring structure including: high-density metal wiring, including a first wire and a second wire; a dielectric layer formed between the first metal wire and the second metal wire, wherein the dielectric layer is conformally applied and spontaneously deposited.

[0032] In some aspects, implementations of the present disclosure include a device, wherein the high density interconnect wiring structure has a high aspect ratio metal traces having its cross-sectional dimensions in a range from 0.1 micrometer to 100 micrometers, and wherein the plurality of pillars are surrounded by low-k dielectric material having dielectric constant less than 3.

[0033] In some aspects, implementations of the present disclosure include a device, wherein the ratio of (i) a height to width or (ii) a width to height has a range from 0.1 to 10.

[0034] In some aspects, implementations of the present disclosure include a device, including: one or more chips, chiplets, dies, devices, components, passive components, and/or active components, wherein the one or more chips, chiplets, dies, devices, components, passive components, and/or active components are connected to another component by the first wire and the second wire.

[0035] In some aspects, implementations of the present disclosure include a device, wherein the high density interconnect wiring structure forms an asymmetric interconnect structure having multiple layers of polymer and metal disposed on to a base substrate (e.g., glass, fused silica, glass ceramic or ceramic, or dielectric) on either side of the base substrate.

[0036] In some aspects, implementations of the present disclosure include a device, wherein the metal wiring has an interface layer including roughened copper, roughened inorganic material, roughened organic material, or a combination thereof.

[0037] In some aspects, implementations of the present disclosure include a device, wherein the metal wiring has an interface layer including nano-roughened copper and a silane coupling agent.

[0038]

[0039] In some aspects, implementations of the present disclosure include a device, wherein the silane coupling agent includes 3-Methacryloxypropyltrimethoxysilane (e.g.,C10H20O5Si).

[0040] In some aspects, implementations of the present disclosure include a device, wherein the base substrate has an area having a percentage covered by metal of at least 10%.

[0041] In some aspects, implementations of the present disclosure include a device, further including: embedded substrate having cavities, including (i) a first cavity with a first depth value and (ii) a second cavity with a second depth value.

[0042] In some aspects, the device includes a silane or siloxane coupling agent deposited on copper, polymer, dielectric, glass, substrate material or a combination of these.

[0043] In some aspects, the device includes metal pillars or underlying metal structures having an average variation in thickness or height in the range from 1% to 50%.

[0044] In some aspects, the metal pillars are substantially perpendicular to the underlying (first) metal layer.

[0045] In some aspects, the dielectric layer either (i) has a melting point higher than 250 °C or (ii) has a step coverage of at least 50%.

Brief Description of the Drawings

[0046] The skilled person in the art will understand that the drawings described below are for illustration purposes only.

[0047] Figs. 1A, 1B, 1C, and 1D each shows an example semi-additive process for device fabrication, according to an example embodiment of the present disclosure.

[0048] FIG. 2A illustrates an example deposition process of a polymer layer onto a workpiece during the fabrication of a device, e.g., as described in relation to Figs. 1A – 1D.

[0049] Fig. 2B shows the spontaneous polymerization process of parylene, or other polymers or material described herein, along with a representative image of the deposition equipment.

[0050] Fig. 2C shows the molecular structures of Parylene-N, Parylene-C, and Parylene-HT.

[0051] Figs. 3A-3I each show example fabrication operations employing the spontaneous polymerization of a vapored monomer, e.g., as described in relation to Figs. 1A – 1D, in accordance with an illustrative embodiment.

[0052] Figs. 4A-4F each shows an example device fabricated as a package substrate, a semiconductor substrate, and a glass substrate, respectively.

[0053] Figs. 5A-5F illustrate example interconnects and methods of manufacturing interconnects where Fig. 5A illustrates an example method of fabricating a bridge die, Fig. 5B illustrates an example bridge die including multiple alternating ground and signal layers, Fig. 5C illustrates an example interposer with more metal and polymer layers on one side than on the other side (referred to herein as asymmetric build-up), Fig. 5D illustrates conformal deposition of polymer between wiring and/or features having high aspect ratio, Fig. 5E illustrates different elements of an example interconnect, and Fig. 5F illustrates dimensions of different elements of an interconnect.

[0054] Fig. 6A shows a top view of an example substrate and a calculation of metal area percentage, in accordance with an illustrative embodiment. Optionally , embodiments of the present disclosure include metal coverage of greater than 10%, which can better adhere to polymer.

[0055] Fig. 6B shows a process for adhesion enhancement between substrate and parylene, in accordance with an illustrative embodiment.

[0056] Fig. 6C shows a process for adhesion enhancement between parylene, copper and substrate, in accordance with an illustrative embodiment.

[0057] Fig. 6D shows a process for adhesion enhancement between copper and polymer, in accordance with an illustrative embodiment.

[0058] Fig. 6E shows an example formula for a silane coupling agent that can be used in embodiments of the present disclosure, and Fig. 6F shows an example bonding mechanism of silane.

[0059] Fig. 7 shows a process for formation of vias using copper pillars when there is a variation in the heights of copper pillars and copper pads, in accordance with an illustrative embodiment.

[0060] Fig. 8 shows example geometries of copper pillars, in accordance with illustrative embodiments.

[0061] Fig. 9 shows an example electroplated 1μmCu RDL traces formed using Heidelberg MLA-150

[0062] Fig. 10 shows a process flow of the Cu etch process using a sputtered Ti(50 nm) barrier coating, in accordance with an illustrative embodiment.

[0063] Fig. 11 shows a microvia with 3μm diameter drilled in Parylene-HT, in accordance with an illustrative embodiment.

[0064] Fig. 12 shows an overall process flow for a microvia formation technique, in accordance with an illustrative embodiment.

[0065] Figs. 13A-13D illustrate steps of an illustrative embodiment, where Fig. 13A: shows formation of bottom Cu pads where 3.5μm pads at 20μm pitch are shown; Fig. 13B shows parylene-HT deposition where 2μm vias at 10μm conformally deposited with Parylene-HT are shown; Fig. 13C shows3μm vias after planarization; Fig. 13D shows top metal layer formation, where daisy chains structure having 3μm vias at 20μm pitch are shown

[0066] Fig. 14 shows an FIB cross-section of daisy chains structure having 3μm vias at 10μm pitch.

[0067] Fig. 15 shows an SEM image of 1.5μm vias at 2.5μm pitch.

[0068] Fig. 16A shows an effect of via height and via angle on TSR in microvias in ULK dielectric candidates.

[0069] Fig. 16B shows an effect of scaling microvia dimensions on both total strain range and number of cycles to failure.

[0070] Figs. 17A and 17B show stresses in dielectrics, where Fig. 17A shows an effect of RDL L/S and aspect ratio on stress in dielectric and Fig. 17B: shows stress developed in ULK dielectric candidates due to thermal cycling.

[0071] Figs. 18A and 18B show adhesion strengths, where Fig. 18A shows the effect of Cu deposition rate on adhesion strength and Fig. 18B shows Effect of Ti deposition rate on adhesion strength

[0072] Figs. 19A and 19B show effects of bake processes, where Fig. 19A shows Adhesion strength for Ar and Ar-O_2-bake processes for different dielectrics and Fig. 19B shows roughness (Ra) values for Ar and Ar-O_2-bake processes for different dielectrics. Figs. 20A-20C show spectra plots, where Fig. 20A shows XPS C-1s spectra of Ti-deposited ABF; Fig. 20B shows Infrared spectra of pristine, Ar treated and Ar-O_2-bake treated ABF dielectric in $1300 - 1800\ \mathrm{cm}^{-1}$; and Fig. 20C shows infrared spectra of pristine, Ar treated and Ar-O_2-bake treated ABF dielectric in $2700 - 3100\ \mathrm{cm}^{-1}$.

[0073] Figs. 21A and 21B show XPS C-1s spectra, where Fig. 21 shows XPS C-1s spectra of Ti-deposited, Ar treated ABF dielectric and Fig. 21B: XPS C-1s spectra of Ti-deposited, Ar-O_2-bake treated ABF dielectric.

[0074] Fig. 22: XPS depth profile of Ti-deposited ABF (a) Ti 2p (b) C-1s (c) O-1s

[0075] Fig. 23: Contact angles of water drop on plasma treated dielectrics

[0076] 999

[0077] Fig. 24A shows the effect of the aspect ratio and L/S on RDL resistance. Fig. 24B shows the effect of aspect ratio on total capacitance (self-capacitance + mutual capacitance) of an RDL line with 1 μm width.

[0078] Fig. 25 shows the simulated eye diagrams obtained for SiO2 and Parylene-HT.

[0079] Fig. 26 show insertion losses, return losses, Far-end crosstalk, and Near-end crosstalk, in a stripline with Parylene-HT and SiO_2 as dielectrics.

[0080] Fig 27 shows a schematic used to analyze the reflection loss in a stripline with Parylene-HT and SiO_2 as dielectric.

[0081] Figs. 28A and 28B show an example conventional semi-additive process flow, e.g., used in package substrates, using vacuum lamination or liquid spin coating and associated warpage issues.

[0082] Fig. 29 illustrates a comparison of an example embodiment of the present disclosure including parylene-HT RDL against alternative technologies.

Detailed Specification

[0083] The details of one or more embodiments of the invention are set forth in the accompanying drawings and the description below. Other features, objects, and advantages of the invention will be apparent from the description and drawings and from the claims.

[0084] Throughout the description and claims of this specification, the word "comprise" and other forms of the word, such as "comprising" and "comprises," means including but not limited to, and is not intended to exclude, for example, other additives, components, integers, or steps.

[0085] To facilitate an understanding of the principles and features of various embodiments of the present disclosure, they are explained hereinafter with reference to their implementation in illustrative embodiments.

[0086] Some references, which may include various patents, patent applications, and publications, are cited in a reference list and discussed in the disclosure provided herein. The citation and/or discussion of such references is provided merely to clarify the description of the disclosed technology and is not an admission that any such reference is "prior art" to any aspects of the disclosed technology described herein. In terms of notation, "[n]" corresponds to the nth reference in the list. For example, [1] refers to the first reference in the list. All references cited and discussed in this specification are incorporated herein by reference in

their entireties and to the same extent as if each reference was individually incorporated by reference.

[0087] Example semi-additive process flow for a multilayer package substrate

[0088] Figs. 1A, 1B, 1C, and 1D each show an example semi-additive process 100 (shown as 100a, 100b, 100c, and 100d, respectively) for device fabrication, according to an example embodiment of the present disclosure. For Parylene, the process can include vapor deposited onto substrates with a process that resembles chemical vapor deposition (CVD). However, the process pressures can be beneficially higher, e.g., 10-100 mTorr (e.g., 100 mTorr), compared to the conventional vapor deposition pressures of $<10^{-5}$ Torr. The deposition can additionally not be line-of-sight deposition to allow the gaseous monomer to uniformly deposit on all surfaces it comes into contact with. This results in truly conformal and uniform coatings without porosity over large panel areas.

[0089] In the example shown in Figs. 1A, 1B, 1C, and 1D, the process 100a, 100b, 100c, 100d each includes vaporizing (102) a source material at (i) a first temperature greater than vaporization temperature and (ii) a first pressure, e.g., vaporization pressure, to form a vapor dimer of the dielectric. The vaporization of the solid dimer, e.g., for parylene, can be carried out at 80-200°C (e.g., 150 °C). In some embodiments, the vaporization temperature is around 80°C, 90°C, 100°C, 110°C, 120°C, 130°C, 140°C, 150°C, 160°C, 170°C, 180°C, 190°C, or 200°C.

[0090] The dielectric may be a poly-para-xylylene, e.g., Parylene-HT, Parylene-N, Parylene-C, Parylene-D, Parylene AF-4, Parylene-SF, Parylene-A, Parylene-AM (one methylene amine group per repeat unit), Parylene VT-4 (generic name, fluorine atoms on the aromatic ring), Parylene-CF, and Parylene-X (a cross-linkable version, not commercially available).

[0091] In some embodiments, the dielectric is an acrylic, an epoxy, a polyurethan, a silicone, a poly(tetrafluoroethylene), a polyimide, a fluoropolymer, or a combination thereof. The dielectric may be vaporized from a liquid or solid. The dielectric may have a dielectric constant less than 3, e.g., ultra-low k dielectric, or it may have a high k dielectric, e.g., for use in a capacitor, e.g., from 3 to 50, e.g., about 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, or 50.

[0092] The vaporization temperature and pressure may vary based on the selected dielectric material, which may be chosen for attributes including a low dielectric constant,

stability under semiconductor processing conditions, and compatibility with subsequent manufacturing steps of semiconductor devices.

[0093] Following vaporization, the process 100a (as well as 100b, 100c, 100d) then includes heating (104) the vapor dimer in an inert environment to a second temperature, e.g., at least or greater than the pyrolysis temperature, to form a vapor monomer at a second pressure, e.g., pyrolysis pressure. The second temperature is higher than the first temperature, and the second pressure is lower than the first pressure. This heating step occurs within a temperature range that ensures the complete transformation of the vapor dimer to a monomer, subject to the physical properties of the dimer and the ambient environment conditions. The inert environment prevents undesired chemical reactions during pyrolysis. Pyrolysis of the vaporized dimer of parylene can be carried out in a pyrolysis chamber at 400-800°C (e.g., 680 °C). The cleavage of the methylene-methylene bonds occurs during pyrolysis, which can yield the stable monomer diradical- para-xylylene.

[0094] Following pyrolysis, the process 100a (as well as 100b, 100c, 100d) then includes introducing (106) the vapor monomer to a chamber having workpiece having an exposed surface to spontaneously deposit and polymerize the vapor monomer to form a layer of a polymer of that monomer on at least the exposed surface of the workpiece, the chamber having a spontaneous polymerization environment at a third temperature lower than the second temperature and a third pressure lower than the third pressure. The heated monomer vapor can enter the deposition chamber, which can be at room or ambient temperature (e.g., at or near 25°C). The deposition and polymerization of parylene occur spontaneously on the substrate to form a uniform and conformal layer.

[0095] Vapor deposition of polymer dielectrics may be performed to deposit on both sides simultaneously. Thus, the fabrication of devices can be further reduced with respect to cost and time. Furthermore, core substrates having through-holes can be coated with vapor-deposited polymer dielectrics due to their conformal coating characteristic.

[0096] Such spontaneously deposited polymer dielectrics can be used in a package substrate for multiple layers having different functions, such as a build-up dielectric layer, solder-mask layer, thermal-interface material, underfill, and/or an overmold. In some embodiments, the spontaneous polymerization can occur in a chamber having a temperature of -80 – 200 C, e.g., around -50°C, -40°C, -30°C, -20°C, -10°C, 0°C, 10°C, 20°C, 30°C, 40°C, 50°C, 60°C, 70°C, 80°C, 90°C, 100°C, 110°C, 120°C, 130°C, 140°C, 150°C, 160°C, 170°C, 180°C, 190°C, or 200°C. The spontaneous polymerization can occur in a chamber having a pressure between 10-100 mTorr (e.g., 100 mTorr), e.g., 10 mTorr, 20 mTorr, 30

mTorr, 40 mTorr, 50 mTorr, 60 mTorr, 70 mTorr, 80 mTorr, 90 mTorr, 100 mTorr. The pressure can be higher than 10^{-1} Torr (e.g., between 10^{-1} and 10^{-5} Torr, e.g., around 10^{-2}, 10^{-3}, 10^{-4} Torr.

[0097] In some embodiments, additives may be present in the chamber to embed such additives in the polymer.

[0098] Spontaneous polymerization of vapor-phase monomers directly onto the workpiece can eliminate the stresses due to curing and thermal expansion associated with other polymer deposition techniques. For larger panel-scale substrates and larger body-size interposers for advanced semiconductor packaging, this can be beneficial in avoiding the warpage of the workpiece to allow for larger size substrates to be used. Low warpage is especially crucial for lithography. Significantly warped substrates cause sub-optimal focusing during lithography, leading to poor resolution of photoresists.

[0099] Spontaneous polymerization also reduces the chances of such cracking due to zero curing stresses. Curing stresses can also cause the cracking of fragile substrate materials such as glass. Thermal processes are also expensive due to high power consumption and long process durations. Curing processes can also add high or significant costs to package substrate fabrication due to the multiple curing steps required for each layer of dielectric. In eliminating multiple curing steps via spontaneous polymerization operation, the cost of fabrication can be reduced significantly.

[0100] The workpiece may be composed of any material pertinent to semiconductor device fabrication, including glass, metal, silicon, or previously deposited layers of the device. The chamber is maintained under conditions that support spontaneous polymerization, characterized by specific temperature and pressure settings suitable for the deposition process. The workpiece may include a semiconductor wafer, a glass panel, or a portion of a semiconductor device that necessitates a polymeric layer for purposes such as mechanical stability, electrical function, or as part of a thermal management system. In various embodiments, the polymer layer deposited may act as a dielectric layer, a barrier layer, or a structural layer in the fabricated semiconductor device. The workpiece may be a single solid substrate or a multi-part substrate. Workpieces may include a core substrate, e.g., made of organic laminate, glass, silicon, metal, polymer mold compound, fan-out, or a combination of one or more of those.

[0101] *Multi-part Substrate*

[0102] Fig. 1B additionally shows processing 100b of the multilayer fabrication described in Fig. 1A for a multi-part substrate. The process 100b can initiate with the multi-

part substrate being provided (108) for the fabrication. The fabrication operation of Fig. 1A can be employed for the fabrication of integration devices having embedded chips/chiplets, devices, components, passives, and/or actives. The polymer can be deposited conformally to encapsulate the embedded chips/chiplets, devices, components, passive components, and/or active components.

[0103] The process 100b may be employed to fabricate a package substrate comprising a combination of filters, antennas, circulators, baluns, diplexers, power splitter & combiner, mixer, phase shifters, voltage-controlled oscillators, frequency multipliers and dividers, low noise amplifiers, power amplifiers, inductors, capacitors, co-planar waveguides, microstrip, waveguides for 5G and mm-wave wireless communication.

[0104] *Multi-layer device*

[0105] Fig. 1C additionally shows processing 100c of the multilayer fabrication by successively performing the operation described in Fig. 1A. Process100c includes forming (112) a metal layer over the polymer. Process 100c then includes introducing (114) additional vapor monomer to the chamber to spontaneously deposit and polymerize the additional vapor monomer to form another layer of the polymer over the metal layer or a portion thereof.

[0106] *Copper Tracing.* To form the metal layer over the polymer, photoresists (PRs), e.g., dry-film photoresists, can be laminated onto the substrate. In some embodiments, a spin-coating process can be used for liquid photoresist. Electroplating can then be carried out to form the metal layers to which the additional layer of layer of the polymer can be deposited.

[0107] Fig. 1D additionally shows processing 100d, including multilayer fabrication. Vaporizing 102, heating 104, and introducing 106 are performed as described with reference to Figs. 1A and 1C. At step 116, a portion of the polymer is selectively removed. Optionally, the selective removal of polymer can be performed by plasma and/or wet chemical etching. The processing 100d shown in Fig. 1D can optionally be used to form a waveguide, as a non-limiting example. Introducing 114, also described with reference to Fig. 1C, can then be performed to form another layer of polymer. It should be understood that the steps of processing 100d can be repeated any number of times to form different structures (e.g., multiple waveguides) in multiple layers of polymer material.

[0108] *Example Devices.* The multi-layer fabrication can be used to fabricate a package substrate with multiple polymer and metal layers where the polymer build-up layers

are deposited on a substrate in such a way that the polymer polymerizes on the substrate during deposition.

[0109] In an example, a package substrate having a core substrate with multiple layers of copper and polymer dielectric may be deposited per the exemplary method. Microvias/blind vias may be formed in the polymer using laser drilling for the vertical connection of two metal layers.

[0110] In another example, a package substrate involving polymer dielectric deposited per the exemplary method may be deposited onto various RF components, followed by the deposition of a thin layer of a conductive material, metal, high-k dielectric, and/or a composite for electromagnetic interference shielding.

[0111] In yet another example, a package substrate may have a cavity for embedded chips/chiplets, devices, components, passives, and/or actives to which the polymer deposited per the exemplary method may be deposited conformally to fill the open areas of the cavity and create an overburden. The process may be followed by a planarization process to remove the overburden.

[0112] In yet another example, a package substrate may have a layer of high-density capacitors for power delivery. The capacitor can be made of two metal electrodes with a thin layer of polymer dielectric in between the electrodes. The thickness of the polymer dielectric may be in the range of 1 nanometers to 10 micrometers, e.g., about 1 nm, 5 nm, 10 nm, 20 nm, 30 nm, 40 nm, 50 nm, 60 nm, 70 nm, 80 nm, 90 nm, 100 nm, 200 nm, 300 nm, 400 nm, 500 nm, 600 nm, 700 nm, 800 nm, 900 nm, 1 μm. The polymer dielectric for capacitors maybe having a high dielectric constant from 2 to 100.

[0113] **Example Spontaneous Polymerization**

[0114] FIG. 2A illustrates an example deposition process 200 (e.g., of process 100a, 100b, 100c, or 100d) of a polymer layer onto a workpiece 208 during the fabrication of a device. In the example shown in Fig. 2A, the process 200 begins in the vaporization chamber 202 and converts a source material into a vapor dimer under specific vaporization temperature and pressure 203. The vaporization chamber 202 may be filled with an insert gas 210 (e.g., nitrogen). The vaporization parameters of chamber 202 may vary, as different polymers may require different temperatures and pressures for vaporization.

[0115] An example feedstock for parylene-C, as a source material, is "DPX-C" comprising principally 92% di-chlorinated molecules and 8% trichloro- and poly-chlorinated molecules.

[0116] Once the vapor dimer forms, it is transferred to a pyrolysis chamber 204 filled with an insert gas 212 (e.g., nitrogen), where it undergoes a transformation induced by temperature. The pyrolysis temperature and pressure 205 are controlled to ensure the breakdown of the vapor dimer into a vapor monomer, a process shown by the pyrolysis, which requires the vapor dimer to exceed melting temperature, $T_{melt\ polymer}$, of the polymer (shown as $T > T_{melt\_polymer}$).

[0117] The vapored monomer is then introduced into the deposition chamber 206 having a spontaneous deposition temperature and pressure 207. The spontaneous deposition temperature is at or near ambient temperature (shown as $T \geq T_{ambient}$). The vapored monomer can be introduced into the deposition chamber 206 while at or near the melting temperature. In the deposition chamber 206, the vapored monomer is cooled (226) to spontaneously polymerize as a polymer layer on the workpiece 208.

[0118] The evolution of temperature and pressure throughout the process is depicted through the temperature plot 214 and the pressure plot 216. The temperature must first surpass vaporization temperature 220 to vaporize a source dielectric (shown as $T > T_{vapor\_polymer}$) and then elevate to or beyond the melting temperature (222) of the polymer (shown as $T > T_{melt\_polymer}$) before decreasing to be at or near the spontaneous deposition temperature 228 during a deposition time period 224, ensuring that the deposition occurs under a condition conducive to spontaneous layer formation on the workpiece 208 in the spontaneous deposition chamber 206.

[0119] Pressure is modulated within the system. It begins within the vaporization chamber 202 at a pressure level (232) during a vaporization time period 230 conducive to the vaporization of the polymer. As the process transitions into the pyrolysis chamber 204, pressure is decreased to an intermediate pressure 236 (optional) during an intermediate pressure period 234, and eventually reaches a pressure 240 within the spontaneous deposition chamber 206, conducive for spontaneous deposition during a spontaneous deposition period 238. The reduction to a pressure range of around 10^{-1} Torr is crucial to ensure proper deposition and polymerization of the vapor monomer onto the workpiece 208. The pressure can be higher than 10^{-1} Torr (e.g., between 10^{-1} and 10^{-5} Torr, e.g., around 10^{-2}, 10^{-3}, 10^{-4}, which is an order or orders or magnitude less than conventional CVD).

[0120] *Parylene Spontaneous Polymerization.* The term "parylene," as used herein, generally refers to a class of polymer having para-benzenediyl rings ($-C_6H_4-$) connected by 1,2-ethanediyl bridges ($-CH_2-CH_2-$). Parylene HT replaces the alpha hydrogen atom

of the N dimer with fluorine. Parylene can be vapor deposited onto substrates with a process that resembles chemical vapor deposition (CVD). However, the process pressures are higher, being about 0.1 Torr, as compared to the conventional vapor deposition pressures of about than 10^{-5} Torr. Parylene deposition is not a line-of-sight deposition, meaning the gaseous monomer uniformly deposits on all surfaces it comes into contact with. This can result in truly conformal and uniform coatings without porosity over large panel areas. Parylene deposition consists of three main steps- (1) Vaporization, (2) Pyrolysis, and (3) Deposition.

[0121] Vaporization (e.g., 218) of the solid dimer of parylene can be carried out at ≈ 150°C (e.g., 220). Pyrolysis of the vaporized dimer can be carried out in the pyrolysis chamber at 680°C (e.g., 222). The cleavage of the methylene-methylene bonds occurs during pyrolysis to yield a stable monomer diradical-para-xylylene. The monomer vapor then enters the deposition chamber, e.g., maintained at or near ambient temperature (e.g., 25°C). The deposition and polymerization of vapor parylene monomer occur spontaneously on the substrate (e.g., 208).

[0122] Fig. 2B shows the spontaneous polymerization process of parylene (or other polymers or material described herein), along with a representative image of the deposition equipment. Indeed, the process may be performed using commercially available semiconductor processing equipment, e.g., for chemical vapor deposition or electroless, physical vapor deposition (PVD).

[0123] Fig. 2C shows the molecular structures of Parylene-N, Parylene-C, and Parylene-HT.

[0124] **Example Fabrication Steps**

[0125] Figs. 3A-I each show example fabrication operations 300 (shown as 300a, 300b, 300c, 300d, 300e, 300f) involving the spontaneous polymerization of a vapored monomer as described in relation to Figs. 1A – 1D, in accordance with an illustrative embodiment.

[0126] In Fig. 3A and 3B, operations 300a, 300b show an operation to form a single or multiple layers of polymer via spontaneous polymerization of a vapored monomer. In Fig. 3A, a workpiece 208 (shown as 208a) is provided (302) and is then deposited (304) with a layer of a polymer (e.g., parylene) (shown as "dielectric layer #1" 306a) per the method described in relation to Fig. 1A.

[0127] The process 300a may be successively repeated (308) to generate a build-up structure of multiple layers of the polymer (shown as "dielectric layer #1" 306a, "dielectric

layer #2" 306b, to "dielectric layer #n" 306n), e.g., per the method described in relation to Fig. 1C.

[0128] In Fig. 3B, operation 300b shows multiple workpieces 208 (shown as 208b) being processed, e.g., per the method described in relation to Fig. 1B.

[0129] *Double-sided fabrication.* Fig. 3C and 3D shows operations 300c, 300d to form on two sides of a workpiece a single or multiple layers of polymer via spontaneous polymerization of a vapored monomer. Fig. 3C shows the operation over a single workpiece. Fig. 3D shows the operation for a multi-part workpiece, e.g., as described in relation to Fig. 3B.

[0130] In Fig. 3C, a workpiece 208 (shown as 208a) is provided (310) that is maintained in a deposition chamber with exposed top and bottom surfaces. The workpiece 208a is then deposited (312) with a layer of a polymer (e.g., parylene) (shown as "dielectric layer #1" 306a and "dielectric layer #1'" 306a') per the method described in relation to Fig. 1A. Because of the non-line-of-sight nature of the operation, a layer of the polymer is uniformly and conformally formed on both sides of the exposed surfaces.

[0131] Process 300c may be successively repeated (314) to generate a build-up structure of multiple layers of the polymer on both sides of the device (shown as "dielectric layer #1" 306a, "dielectric layer #2" 306b, to "dielectric layer #n" 306n and "dielectric layer #1'" 306a', "dielectric layer #2'" 306b', to "dielectric layer #n'" 306n'), e.g., per the method described in relation to Fig. 1C.

[0132] *Metal Layer and Polymer Layer Fabrication.* Fig. 3E shows operation 300e (via steps 316 – 332) to form a workpiece having a metal layer and a layer of polymer via spontaneous polymerization of a vapored monomer. In the example shown in Fig. 3E, a workpiece 208 (shown as 208a) is provided (316). The workpiece 208a is then deposited (318) with a layer of a polymer (e.g., parylene) (shown as "dielectric layer #1" 306a). A photoresist layer 334 is then applied (320). The photoresist layer 334 can be patterned and removed (322) resulting in the workpiece with cavities 338 shown at step 324. Electroplating can be performed (326) to deposit a metal pattern in a metal layer 336. The photoresist layer 334 is then removed (328) to provide an exposed metal layer 336 (shown as 336a at step 330). Subsequently, a second polymer layer 306b can be deposited over the metal layer 336a, to form the multi-layer structure. In some embodiments, a planarization operation is performed to treat the polymer layer 306b prior to further processing.

[0133] The process 300e may be successively repeated (332) to generate a build-up structure of multiple layers of the polymer (shown as 306a, 306b, 306c) and the metal layer (336a, 336b).

[0134] Further processing (not shown) may be performed, e.g., to form micro vias/blind vias, e.g., via laser drilling and subsequent metallization.

[0135] In some embodiments, the cavity (338) can be employed to embed chips/chiplets, devices, components, passives, and/or actives to which a polymer layer can be deposited per the exemplary method to fill the open areas of the cavity and create an overburden. The process may be followed by a planarization process to remove the overburden.

[0136] In some embodiments, the cavity (338) can be employed to form a layer of high-density capacitors. Two metal electrodes can then be formed with a layer of the polymer dielectric formed therebetween.

[0137] *Metal Layer and Polymer Layer Fabrication with Inter-layer Vias and Through-Package Vias.* Fig. 3F shows operation 300f (via steps 340 – 358) to form a workpiece 208 (shown as 208b) having a metal layer and a layer of polymer via spontaneous polymerization of a vapored monomer. In the example shown in Fig. 3F, a workpiece 208b is provided (340) having two sides exposed, e.g., as described in relation to Fig. 3D, the workpiece 208b having through-package-vias drilled 360 therein. The same operation can be performed for a single exposed surface, e.g., as described in relation to Fig. 3C.

[0138] In Fig. 3F, the workpiece 208b is then deposited (shown as "dielectric application" 342) with a layer of a polymer (e.g., parylene) (shown as 306a). A copper seed layer is deposited (344) to form a metal layer 362 over the polymer layer 306a and within the through-package-vias drilled 360. A photoresist layer 364 is then applied (346). The photoresist layer 364 (shown as 364a) is then patterned 348. The photoresist layer 364 is then removed, and electroplating is then performed (350) to deposit a metal pattern to form a metal layer 366 that connects to the through-package-vias drilled 360. The seed layer 344 (not shown) is then removed (352), e.g., via etching. Subsequently, a second polymer layer 306b is then deposited 354 over the metal layer 366 to form the multi-layer structure. The second polymer layer 306b is then drilled to form (356) microvias (368). The microvias (368) are filled, and an additional metal layer (370) is formed (358), e.g., via a metallization operation.

[0139] Indeed, the process (e.g., 340 – 356) may be successively repeated to fabricate multiple layers of the metal layers and dielectric layers.

[0140] In some embodiments, the cavity (338) can be employed to embed chips/chiplets, devices, components, passives, and/or actives to which a polymer layer can be deposited per the exemplary method to fill the open areas of the cavity and create an overburden. The process may be followed by a planarization process to remove the overburden. As used herein, planarization refers to cutting, polishing, fly-cutting, or any other process that is used to make a surface flat (e.g., by removing the overburden).

[0141] Fig. 3G illustrates an example embodiment of a process 300g for the formation of vias in embedded components, according to implementations of the present disclosure. At step 372, copper pillars are formed on a component that can be embedded in a substrate cavity. At step 374, a substate is formed with different depths of cavities. At step 376, one or more components with copper pillars are embedded into the substrate(s) formed at step 374. The height of the copper pillars can optionally be proportional to the depth of the cavity. At step 378, a dielectric is applied to form an overburden on top of the pillars. At step 380, planarization is performed to remove excess dielectric from the top of the pillars for electrical contact.

[0142] Fig. 3H illustrates an example embodiment of a process 300g for the formation of vias in embedded components, according to implementations of the present disclosure. At step 382, copper pillars are formed on a component that can be embedded in a substrate cavity. At step 384, a substate is formed with different depths of cavities. At step 376, one or more components with copper pillars are embedded into the substrate(s) formed at step 374. Optionally, the height of the copper pillar compensates for the variation of the depth of the cavities. At step 388, a dielectric is applied to form an overburden on top of the pillars. At step 390, planarization is performed to remove excess dielectric from the top of the pillars for electrical contact. In another example, the thickness or height of the components may be different, and the copper pillar height may be adjusted to compensate for the height differences. In another example, height or thickness of components, height of copper pillars, depth of cavities may all be non-uniform or different or may have variations. A combination of height of components, height of copper pillars and depth of cavities may be adjusted to compensate for the differences such that after planarization, top of all copper pillars are exposed and available for making electrical contacts with the subsequent metal layers.

[0143] Fig. 3I shows components embedded in a substrate. Components may have different thickness or height values. Copper pillars may be of different heights. Cavities may have different depth values. All these parameters may be adjusted to compensate for the

differences such that after planarization all copper pillars are exposed and available for electrical contact formation.

[0144] Additional examples of processing, in addition to those described or referenced herein, that may be performed on the polymer layer 306 is provided in U.S. Patent Publication No. US20230215762A1, which is incorporated by reference herein in its entirety.

[0145] **Example Devices**

[0146] Figs. 4A – 4F each shows an example device fabricated as a package substrate, a semiconductor substrate, and a glass substrate, respectively.

[0147] Package substrates can be used for the core semiconductors of mobile devices and PCs. The package substrate can transmit electric signals between semiconductors and the main board and protects semiconductors from external stress. Compared with general substrates, as the package substrate is a high-density circuit substrate containing more microcircuits, the assembly defects and incurred costs in directly bonding expensive semiconductors to the substrate can be reduced.

[0148] A semiconductor substrate (e.g., Si), also known as a wafer, is a solid substance that serves as the foundation for microelectronic devices. The substrate is the base material upon which epitaxial layers are deposited to form structures, which then undergo microfabrication processes to produce the end product.

[0149] Glass substrate (e.g., SiO_2) can handle higher temperatures leading to superior thermal and mechanical stability for chips. Glass substrates can be employed for higher interconnect density.

[0150] The dielectric layer may be used to attach a metal layer for heat spreading, EMI shielding, or via interconnects (Fig. 4D). Optionally, the bridge die, an interposer, or a substrate can have a metal wiring layer attached to a dielectric layer in between the substrate material and the metal layer (not shown). Alternatively or additionally, the metal wiring layer may be directly attached to the base substrate material.

[0151] Fig. 4E shows the dielectric layer may be used to encapsulate a substrate while also filling in cracks. Fig. 4F shows the dielectric layer encapsulating a diced package substrate having ICs mounted thereon while filling up cracks during a dicing operation.

[0152] *RF devices.* The exemplary system and method can be employed to integrate and/or fabricate package substrate other others described herein, e.g., as described in relation to Fig. 4A – 4D, that can include any combination of filters, antennas, circulators, baluns, diplexers, power splitter & combiner, mixer, phase shifters, voltage-controlled oscillators, frequency multipliers and dividers, low noise amplifiers, power amplifiers, inductors,

capacitors, co-planar waveguides, microstrip, waveguides for 5G and mm-wave wireless communication.

[0153] *Waveguide and optical electronics.* In some embodiments of the present disclosure, the package substrate or others described herein, e.g., as described in relation to Fig. 4A – 4D, can include optical waveguides made of polymer dielectrics described herein. The process of fabricating waveguides can optionally include polymer deposition and selective removal of polymer from specific areas using plasma and/or wet chemical etching.

[0154] Embedded Interconnect Bridges

[0155] With reference to Figs. 5A-5D, embodiments of the present disclosure include embedded interconnect bridges and methods of making embedded interconnect bridges that can overcome the limitations of conventional polymer dielectrics and methods of making conventional polymer dielectrics.

[0156] Conventional polymer dielectrics used in package substrates are applied using vacuum lamination or liquid spin coating. These polymer dielectrics need to be cured as a part of the application process. This induces stresses in the substrate due to curing shrinkage associated with these dielectrics. These shrinkages occur due to the presence of solvent in these dielectrics. The curing stresses cause warping of the substrates, especially when the panel sizes or package/substrate sizes are considerably large. These conventional polymer dielectrics need to be cured before undergoing any further processing due to the inadequate mechanical stability of uncured dielectrics. The trend in semiconductor packaging is towards larger body/package/substrate sizes. Therefore, low-stress polymer dielectrics are critical to enable large body/package/substrate sizes with minimum warpage. Bridge dies have redistribution layers only on one side of a base substrate. Polymer dielectrics are available as either prepregs or liquids, requiring them to be cured before they can be processed further. Thermal processes are usually expensive due to the consumption of high power and long process durations. Curing processes add significant costs to the conventional package substrates due to the multiple curing steps required for each layer of dielectric. Curing stresses can also cause cracking of fragile substrate materials such as glass. Curing shrinkages associated with polymer dielectrics induce significant stresses in the substrate. With bridges having one-sided redistribution layers, the stresses are not balanced, therefore causing processing and reliability challenges. The substrate warpage increases with an increase in size. Fabricating bridge dies on a large panel substrate is challenging due to the large warpage.

[0157] In some instances, certain polymer dielectrics, such as parylenes (i.e., polymers with backbones consisting of para-benzenediyl rings ($-C_6H_4-$) connected by $1,2,-$ ethanediyl bridges $(-CH_2-)$) are vapor deposited onto substrates with a process that resembles chemical vapor deposition (CVD). However, the process pressures are higher ~0.1 Torr compared to the conventional vapor deposition pressures of $< 10^{-5}$ Torr. Parylene deposition is not a line-of-sight deposition. As such, the gaseous monomer uniformly deposits on all surfaces it comes into contact with. This results in truly conformal and uniform coatings without porosity over large panel areas. Parylene deposition consists of three main steps- (1) Vaporization, (2) Pyrolysis, and (3) Deposition. The first step is the vaporization of the solid dimer, which is carried out at $\sim 150°C$. Pyrolysis of the vaporized dimer is carried out in the pyrolysis chamber at $680°C$. The cleavage of the methylenemethylene bonds occurs during pyrolysis that yields the stable monomer diradical- paraxylylene. The monomer vapor then enters the deposition chamber which is at room temperature. The deposition and polymerization of parylene occur spontaneously on the substrate.

[0158] A polymer dielectric that polymerizes on the substrate from the vapor phase monomers induces minimal to zero stresses due to the absence of curing shrinkage. Such dielectric eases processing and prevents cracking or excessive warpage of the base substrate. Spontaneous polymerization on substrate eliminates the curing stresses associated with the conventional polymer dielectrics. This minimizes the warpage of the substrates, thus allowing better process control during the subsequent processing steps. Low warpage can be important for lithography. Significantly warped substrates cause suboptimal focusing during lithography, leading to poor resolution of photoresists. Furthermore, spontaneous polymerization also eliminates the curing step which can be necessary with the conventional polymer dielectrics for further processing.

[0159] Spontaneous polymerization can also reduce the chances of such cracking due to zero curing stresses. Spontaneous polymerization on substrates also eliminates multiple curing steps, thereby lowering the cost significantly. The core substrate can be organic laminate, glass, silicon, metal, polymer mold compound, fan-out, or a combination of one or more of those.

[0160] Spontaneous polymerization on rough surfaces of metal/glass/silicon/ceramic can also lead to enhanced adhesion between the polymer and metal/glass/silicon/ceramic because of the improved mechanical interlocking. Spontaneously deposited polymer can also

deposit into cracks and defects present on material surfaces, thereby providing protection against crack propagation and/or brittle fracture of materials.

[0161] Examples of spontaneously deposited polymers are poly-para-xylylenes, which are widely known by their commercial names Parylene-N (completely linear un-substituted polymer obtained by polymerization of the para-xylylene intermediate; it is a primary dielectric exhibiting a very low dissipation factor, high dielectric strength and a low dielectric constant invariant with frequency), Parylene-C (completely linear parylene polymer with substitution of a chlorine atom for one of the para-benzenediyl ring hydrogens; exhibits very low permeability to moisture and corrosive gasses), Parylene-D (completely linear parylene polymer with substitution of a chlorine atom for two of the para-benzenediyl ring hydrogens; similar properties to Parylene C with added ability to withstand slightly higher use temperatures), Parylene HT (completely linear un-substituted polymer with backbone consisting of -C_6H_4 - rings connected by -CF_2 - bridges; useful in high temperature and long term UV stability applications; also marketed as Parylene AF-4 and Parylene SF; generated from α,α'-diphenoxy- $\alpha,\alpha,\alpha',\alpha'$-tetrafluoro-para-xylene or α,α' dibromo- $\alpha,\alpha,\alpha',\alpha'$-tetrafluoro-para-xylene), Parylene E (parylene polymer with substitution of and ethyl group for one of the para-benzenediyl ring hydrogens and para-benzenediyl rings are bridged with $-(CH_2)_2$ - groups), Parylene A, Parylene M (parylene polymer with substitution of a methyl group for one of the para-benzenediyl ring hydrogens and parabenzenediyl ring are bridged with $-(CH_2)_2$ - groups), Parylene AM-2 (parylene polymer where para-benzenediyl rings are bridged with $-CH(CH_3)-CH(CH_3)$ - groups generated from the precursor α,α'-dimethyl-α,α'-dimethoxy-p-xylene), Parylene AM (one methylene amine group per repeat unit), Parylene VT-4 and Parylene CF (generic names, fluorine atoms substituting the four aromatic ring hydrogens), and Parylene X (a cross-linkable version, not commercially available). Package substrate can utilize one or a combination of the above-mentioned polymers.

[0162] Free-standing parylene films are also available in the market. These free-standing films can be applied to the substrates by applying heat and pressure and they would not require curing. However, these films won't adhere well to the substrate. Additionally, they won't be able to flow and fill the fine spaces between high-density wiring and micro-scale interconnect structures.

[0163]

[0164] Embodiments of the present disclosure can include the following process steps: formation of a first metal layer on the base substrate or dielectric; formation of metal

pillars by semi-additive process; etching metal seed layer; deposition of interface materials; application of conformally deposited polymer dielectric to create an overburden; planarizing overburden and optionally repeating any or all of the steps.

[0165] Method of Fabricating Embedded Interconnect Bridges

[0166] An example process 500 for fabricating a bridge die according to the present disclosure can have the following steps as shown in Fig. 5A. The process of Fig. 5A can be modified to include additional process steps as may be necessary based upon the required properties or configurations of the fabricated bridge die. In the first step 502, shown in Fig. 5A, a suitable metal seed-layer is deposited onto a thin base substrate. The base substrate may be supported by a thicker carrier wafer. The metal seed layer can be deposited by any suitable method known to one of ordinary skill in the art, such as, for example chemical vapor deposition (CVD), sputtering, and so on. Optionally, the thicker carrier can be de-bonded before or after bridge die singulation.

[0167] In the second step 504, shown in Fig. 5A, a suitable first metal layer is formed on the seed layer by photoresist patterning, electroplating/electrodeposition, and photoresist removal. The seed-layer is not etched off after the first metal layer formation.

[0168] In the third step 506, shown in Fig. 5A, another layer of photoresist is applied on top of the first metal layer and patterned. Suitable metal pillars are then formed at desired locations on top of the first metal layer.

[0169] In the fourth step 508, shown in Fig. 5A, after forming the metal pillars, the photoresist is removed, and any exposed metal seed-layer is etched off.

[0170] In the fifth step 510, shown in Fig. 5A, a thin layer of an inorganic barrier (e.g. SiO_2, Si_3N_4, MgO, ZrO_2, tungsten nitride, etc.) is conformally deposited on top of the metal structures, including the entire metal pillars formed in the third step and exposed base substrate top surfaces.

[0171] In the sixth step 512, shown in Fig. 5A, a polymer dielectric is conformally deposited to cover all metal structures (which have been coated with the inorganic barrier layer). A thick layer of polymer is deposited such that an overburden of the polymer dielectric is formed over the metal structures. In some instances, the polymer dielectric is formed by a spontaneous polymerization process. In some instances, the polymer dielectric is formed by the spontaneous polymerization of a para-xylylene intermediate to form a Parylenetype polymer (for example, Parylene polymers described above). In some instances, the polymer dielectric is formed by electroless, physical vapor deposition (PVD) or chemical vapor deposition (CVD), where one or more precursors react to form the desired polymer. In

general, however, polymer precursors capable of spontaneous polymerization that would be suitable for the formation of polymers used in bridge dies can be used in this step.

[0172] In the seventh step 514, shown in Fig. 5A, a planarization process is conducted to remove the polymer dielectric. The top of the metal pillars is also planarized to remove any inorganic barrier layer material located on the top surface of metal pillars (as previously deposited in the fifth step) to expose the metal on the top surface of the pillars. In some instances, an over-planarization process can be performed to ensure that metal pillars are open all over the panel substrate area. In some instances, an over-planarization process can also be employed to logically adjust the height of the metal pillar structures. As shown in subsequent steps, the planarized metal pillars will, in part, form micro-vias/vertical interconnects of the bridge die.

[0173] In the eighth step 516, shown in Fig. 5A, another metal layer is formed connecting to the opened metal pillars, thus completing electrical contact. Similar metal lines/pads and pillars may be formed; an inorganic barrier layer may be deposited. Dielectric deposition and planarization may be done. In general, the eighth step is performed by repeating the second through seventh steps above.

[0174] In the ninth step 518, shown in Fig. 5A, the sixth through eighth steps are repeated to form a bridge die with as many alternating ground and signal layers as can be required for the end-use of the bridge die (See, e.g., Fig. 5B).

[0175] Table 1 compares the characteristics of a silicon bridge and a glass bridge fabricated using the exemplary method described herein.

Table 1: Si Bridge and Glass Bridge example characteristics

	Si Bridge	**Glass Bridge**
Dielectric	$SiO_2 (Dk = 3.9)$	ULK dielectrics ($Dk < 2.5$)
RDL dimensions	$2/2\mu m$ (Intel), 0.8/0.8 mm (TSMC)	$1/1\mu m$ High AR
Total Thickness	$> 75\mu m$ (Requires wafer thinning)	$\sim 50\mu m$ ($30\mu m$ glass + RDL layers)
Bandwidth	$>$ 1.5 Tbps/mm	$>$ 5 Tbps/mm
Process	- Wafer-scale dual-damascene	- Panel-scale Hybrid SAP
Cost	High	Lower
Reliability	High	High with Glass CTE 3ppm/K
Warpage	Low	Controllable with CTE

[0176] In addition, a benefit of the above process for fabricating a bridge die, according to embodiments of the present disclosure, is that the inorganic barrier layer is coated on the metal pattern in fewer steps than that of prior art processes, thus reducing the costs. Specifically, the inorganic barrier material is coated on the metal pillars and lines/pads (for signal and ground layers) in a single step as opposed to two steps if done individually.

[0177] Another benefit of the above process for fabricating a bridge die, according to embodiments of the present disclosure, is that micro-via opening and barrier layer removal are done by planarization. This avoids the use of barrier layer etching techniques that rely upon, for example, plasma or reactive ion etching.

[0178] Another benefit of the above process for fabricating a bridge die, according to embodiments of the present disclosure, is that metal pillars formed during the process form the micro-vias. The dimensions of the metal pillars are defined by photoresist opening. Thus, micro-vias can be scaled to smaller dimensions using this process. Micro-via height can be controlled by planarization or over-planarization.

[0179] Another benefit of the above process for fabricating a bridge die according to embodiments of the present disclosure is that the use of polymer dielectric precursors that spontaneously polymerize directly on shaped surface features (such as metal pillars, lines, and pads) can result in a complete conformal coating of the shaped surface features with minimal to zero curing stresses translated to the surface features or underlying bases substrate during formation of the polymer dielectric. In prior art processes, high aspect ratio patterns such as the metal pillars and metal lines cannot be completely covered with the conventional liquid or prepreg dielectrics.

[0180] According to various aspects of the disclosure, embedded bridge interconnect die on a thin base substrate can be formed and can have high-density wiring for connecting chips, chiplets, dies, devices, components, passives, and/or actives. Bridge dies, according to the disclosure, have multiple metal and dielectric layers on one side of the base substrate. According to various aspects of the disclosure, the base substrate may be a glass, a fused silica, a glass ceramic, or a ceramic. In some instances, the base substrate can have a thickness ranging from 1 micrometer to 200 micrometers. In some instances, the base substrate can have a coefficient of thermal expansion ranging from 0.1ppm/K to 20ppm/K, which may be optimized as needed for the reliability of particular interconnections.

[0181] According to various aspects of the disclosure, the polymer dielectric used for the build-up layers may be polymer monomers that polymerize with minimal to zero

shrinkage during deposition. The polymer used for dielectric layers is such that it is formed by monomer polymerization during a deposition process, thus eliminating the need for thermal or UV curing as with conventional polymer dielectrics. In some instances, the deposition/polymerization may take place at ambient temperatures. In some instances, the deposition/polymerization may take place at controlled elevated temperatures to minimize thermal stresses.

[0182] According to various aspects of the disclosure, the polymer dielectric to be vapor deposited can be one or a combination of a poly-para-xylylene (Parylene-HT, Parylene-N, Parylene-C, Parylene-D, Parylene AF-4, Parylene-SF, Parylene-A, Parylene-AM, Parylene VT-4, Parylene-CF, and Parylene-X), an acrylic, an epoxy, a polyurethane, a silicone, a poly(tetrafluoroethylene), a polyimide and a fluoropolymer. The polymer dielectric may be chosen to have a low dielectric constant or permittivity of less than 3, thus, improving the electrical characteristics of the bridge die for faster signal transfer between chips/chiplets/dies/components.

[0183] In some instances, processes for fabricating a bridge die (FIG. 5A) can be conducted on a single thin wafer base substrate. In some instances, processes for fabricating a bridge die (FIG. 2) can be conducted on large rectangular or square base substrate panels on, for example the scale of 10 s of centimeters or one or more meters. The base substrate wafer or panel substrate may be supported by a thicker temporary carrier during processing. After completion of the bridge die, the temporary carrier may be de-bonded before or after singulation.

[0184] In accordance with various aspects of the disclosure, bridge dies may include inorganic barrier layer coatings on metal wires/structures for protection against dielectric breakdown. The inorganic barrier layer may be a dielectric having a higher dielectric breakdown strength than the polymer dielectric to provide enhanced protection against electrical failure.

[0185] Bridge dies produced according to various aspects of the disclosure may have a ratio of the total thickness of build-up layers to the thickness of the base substrate ranging from 0.01 to 0.5.

[0186] Bridge dies produced according to various aspects of the disclosure may have multiple signal and ground layers. Wires, lines, traces, and connections in the signal layer can optionally have a height-to-width ratio ranging from 0.1 to 10. Spacing distances between adjacent signal wires, lines, traces, and connections can optionally be larger than their corresponding width for lower capacitance.

[0187] In some embodiments, the individual bridge dies after singulation or dicing and can be coated with the spontaneously deposited polymer to coat inside the edge defects to prevent cracking failure of the individual dies.

[0188] In some embodiments, the process described herein (e.g., FIG. 5A) can be used for building an interposer with asymmetric build-up, i.e., having more metal and polymer layers on one side than the other. The spontaneously deposited polymer layers would be beneficial in minimizing overall stresses due to the asymmetric build-up. As non-limiting examples, the base substrate can be glass, silicon, metal, or ceramic substrate with (or without) through package vias (TPVs). FIG. 5C shows an example schematic of such an interposer.

[0189] *High Aspect Ratio Conformal Deposition.* Fig. 5D shows an additional example of conformal deposition of polymer between wiring and/or features having a high aspect ratio. As shown, the metal traces (e.g., copper) and vias can be fabricated with high-aspect ratios, i.e., having high thickness relative to the length and width. The high aspect ratio features can be incorporated into various embodiments described herein, including, for example, the bridge die as described in relation to Fig. 5B, an interposer as described in relation to Fig. 5C. High aspect ratio can beneficially reduce the resistance of the wires by increasing the cross sectional area of wires The width and height of traces can reduce the resistance of the wires. The spacing between the traces may be adjusted to optimize or reduce the capacitance of the wires. Therefore, by controlling the dimensions and aspect ratio of wires, optimum or lower resistance and capacitance can be achieved.

[0190] A high aspect ratio can be defined as having a greater than 1.5:1 ratio, e.g., 2:1, 2.5:1, 3:1 ratio, etc., of thickness relative to the length and width. Bridge dies produced according to various aspects of the disclosure may have a ratio of the total thickness of build-up layers to the thickness of the base substrate ranging from 0.01 to 0.5. Wires, lines, traces, and connections in the signal layer can have a height-to-width ratio ranging from 0.1 to 10, e.g., about 2, 3, 4, 5, 6, 7, 8, 9, 10 ratio.

[0191] *Interconnect with Interface Material.* Fig. 5E shows an example of different types of interconnect, including two interface layers. In the non-limiting example of Fig. 5E, interface layer 1 can be Ti, Cu, Cr, Ni, Pd, Pt, W, or a combination thereof. Alternatively or additionally, interface layer 2 can be nano-roughened copper, coupling agent, silane, inorganic compound, organic material, or a combination thereof.

[0192] *Example Dimensions.* Fig. 5F shows example proportions and dimensions of the devices that can be formed using methods of the present disclosure. As shown in Fig. 5F,

L & S can optionally range from 0.1um to 100um. The ratio of L/S, H/L, H/S can optionally range from 0.1 to 10. D & d can optionally range from 0.1 μm to 500 μm. The ratio of d/D can optionally range from 0.1 to 1. H1 & H2 can optionally range from 0.1um to 100um. The ratio of H1/H2 can optionally range from 0.1 to 10. The ratio of d/H1 can optionally range from 0.1 to 10. The ratio of D/H2 can optionally range from 0.1 to 10. The thickness of layer 1 an layer 2 may be in the range of 0.1 nanometer to 1 micrometer.

[0193] Method of Fabrication and Bridge Die Device

[0194] Example aspects of the present disclosure are provided for illustrative purposes. In some aspects, the present disclosure includes a process for fabricating a bridge die, where the process includes: a) depositing a metal seed-layer on a base substrate; b) forming a first metal layer on the metal seed-layer; c) applying a layer of a photoresist on a top surface of the first metal layer and patterning the photoresist followed by forming a plurality of metal pillars at predetermined locations on the first metal layer; d) removing the photoresist layer and exposed portions of the metal-seed layer; e) conformally depositing an inorganic barrier layer on metal structures and exposed base substrate top surface; f) conformally depositing an overburden layer of a polymer dielectric on the inorganic barrier layer and underlying metal structures; g) planarizing or over-planarizing the polymer dielectric to expose top surfaces of the plurality of metal pillars; h) forming a metal layer connected to the exposed top surfaces of the plurality of metal pillars.

[0195] Optionally, the steps of the example aspect can be performed in different orders, and/or any or all of the steps can be repeated. For example, steps b-h can be repeated one or more additional times. Alternatively or additionally, steps f through i can be repeated more than one time, for example.

[0196] In some embodiments, the metal seed-layer is deposited on the base substrate using electroless, physical vapor deposition (PVD), chemical vapor deposition (CVD), or a sputtering process.

[0197] In some embodiments, the first metal layer is formed on the metal seed-layer by a process comprising photoresist patterning, electroplating/electrodeposition and photoresist removal.

[0198] In some embodiments, the inorganic barrier layer is made from a material comprising inorganic barrier layer is made from a material comprising SiO_2, Si_3N_4, SiC, MgO, ZrO_2, or tungsten nitride. SiOx, AlOx, SiNx, TiOx, TaNx, WNx, Ta, Ti where ‘x’ is the stoichiometric coefficient ranging from 0.01 to 10.

[0199] In some embodiments, the overburden layer of the polymer dielectric is formed by a spontaneous polymerization or chemical vapor deposition (CVD) process.

[0200] In some embodiments, the polymer dielectric is a poly-para-xylylene, an acrylic, an epoxy, a polyurethane, a silicone, a poly(tetrafluoroethylene), a polyimide, a fluoropolymer, or any combination thereof.

[0201] In some embodiments, the present disclosure includes a bridge die, where the bridge die is prepared according to the example processes described herein. Alternatively or additionally, the present disclosure includes electronic devices, including bridge dies prepared according to the processes described herein.

[0202] With reference to Figs. 6A-6F, Fig. 7, and Fig. 8, embodiments of the present disclosure include methods that can be used to form high-density connections.

[0203] *Example Metal Surface Area.* Fig. 6A shows a top view of an example substrate and a calculation of metal area percentage in accordance with an illustrative embodiment.

[0204] *Silane Adhesion Enhancements.* Fig. 6B shows an example process for adhesion enhancement between substrate and parylene in accordance with an illustrative embodiment. At step 602, a substrate 604 is provided with through-package vias (TPVs) 605a, 605b, and cavities 606a, 606b. At step 607, silane 608 is conformally coated in the TPVs 605a, 605b and cavities 606a, 606b. At step 610, parylene 612 is deposited onto the silane 608. Silane may form siloxane or polysiloxane when deposited on a surface.

[0205] Fig. 6C shows an example process 614 for adhesion enhancement between parylene, copper, and substrate, in accordance with an illustrative embodiment. At step 616 a substrate 604 is provided with copper coating 618. At step 620, silane 608 is conformally coated onto the copper coating 618 and substrate 604. Optionally, the substrate 604 can be a glass substrate. At step 622, parylene 612 is deposited onto the silane 608.

[0206] Fig. 6D shows an example process flow for adhesion enhancement between copper and polymer. The example process can include any or all of the following steps: (A) nano-roughening of copper to provide mechanical interlocking sites; (B) application of coupling agent such as silane that is applied in the roughened surface of copper; (C) polymer is then applied to the rough surface of copper and bonded with the coupling agent or silane; (D) polymer is continually applied to conformally fill the spaces between the copper structures. It should be understood that the steps shown in Fig. 6D can be performed in different orders, repeated, and/or performed with intervening steps (not shown), according to various embodiments of the present disclosure.

[0207] It should be understood that embodiments of the present disclosure can include many different types of coupling agents and/or coatings. As non-limiting examples, the high-density interconnect structure may have an organic or inorganic layer or coating on metal wiring for improved adhesion between metal and spontaneously deposited polymer. The organic or inorganic material of the layer may be a silane coupling agent. Silane coupling agents can form a durable bond between organic and inorganic materials. The general formula for a silane coupling agent typically shows the two classes of functionality: hydrolyzable group X and an organofunctional group R. X is a hydrolyzable group, typically alkoxy, acyloxy, halogen, or amine. Silane coupling agents may be deposited by vapor phase deposition, liquid coating, liquid dipping, spray coating, or solid powder-based process.

[0208] Fig. 6E shows an example formula for a silane coupling agent that can be used in embodiments of the present disclosure, and Fig. 6F shows an example bonding mechanism of silane. Silane coupling agents can form a durable bond between organic and inorganic materials. The general formula for a silane coupling agent typically shows the two classes of functionality, including a hydrolyzable group X and an organofunctional group R.

[0209] *Variation in Height from Deposition.* Fig. 7 shows an example process 700 for the formation of vias using copper pillars when there is a variation in the heights of copper pillars and copper pads, e.g., due to the deposition process, in accordance with an illustrative embodiment. At step 702, copper pads 704a, 704b, 704c are formed on a substrate 706 with a plurality of copper pillars 705 extending from the copper pads. As shown in Fig. 7, different numbers of copper pillars 705 can be used, and the present disclosure contemplates that any number of copper pillars 705 and pads, as well as different proportions of copper pillars 705 and copper pads 704a, 704b, 704c, can be used in various embodiments of the present disclosure. At step 708, polymer 710 is deposited on the substrate. At step 712, planarization is performed to remove excess polymer 710 from above the copper pads 704a, 704b, 704c and expose the copper pads 704a, 704b, 704c.

[0210] *Pillar Formation.* Fig. 8 shows example geometries of copper pillars in accordance with illustrative embodiments. Fig. 8 illustrates an example copper pad 801 formed on a substrate 706, with three different example configurations of copper pillars. In the first configuration, copper pillars 802a, 802b narrow as they extend from the copper pad 801. Therefore, the width of the top of the copper pillar 802a, 802b (shown as D1) is smaller than the width at the bottom of the copper pillars 802a, 802b (shown as D2). This can result in the angle formed by a side of the copper pillars 802a, 802b with the copper pad 801 being greater than 90 degrees.

[0211] In the second configuration, copper pillars 804a, 804b become wider as they extend from the copper pad 801. Therefore, the width of the top of the copper pillar 804a, 804b (shown as D3) is greater than the width of the bottom of the copper pillar 804a, 804b (shown as D4). This can result in the angle formed by a side of the copper pillars 804a, 804b with the copper pad 801 less than 90 degrees.

[0212] In the third configuration, copper pillars 806a, 806b have the same width as they extend from the copper pad 801 (shown as D5) as the width at the surface of the copper pad 801. Thus, the width of the copper pillars 806a, 806b (shown as D5) is constant, and the angle the copper pillars 806a, 806b form with the copper pad 801 is a right angle (90 degrees).

[0213] It should be understood that embodiments of the present disclosure can include copper pillars with any geometries/proportions and that the examples of shapes and proportions shown in Fig. 8 are only non-limiting examples.

[0214] Additionally, the present disclosure contemplates that a silane coupling agent can be deposited. The silane or siloxane coupling agent can optionally be deposited on copper, polymer, dielectric, glass, substrate material, and/or any combination of these materials.

[0215] Organosilanes are widely used in surface treatment applications, where the majority of these compounds feature one organic substituent and three hydrolyzable substituents. In typical applications, the alkoxy groups in trialkoxysilanes undergo hydrolysis to form silanol-containing species. The silane reaction mechanism involves four key steps, which may occur simultaneously following the initial hydrolysis. Upon interaction with a substrate surface, each silicon atom in the organosilane generally forms a single covalent bond with the substrate, while the two remaining silanol groups either remain free or condense. The organic substituent (R group) is preserved for subsequent covalent reactions or physical interactions with other phases. The silanes may be used under anhydrous conditions, aligning with requirements for monolayer and vapor phase deposition. Reaction times typically range from a few minutes to 12 hours at elevated temperatures between 50 °C and 120 °C. Among the alkoxysilanes, methoxysilanes are uniquely effective for vapor deposition without the need for catalysis, while cyclic azasilanes are identified as particularly efficacious for vapor phase deposition. The hydrolysis water necessary for these reactions may be introduced from various sources, including direct addition, existing on the substrate surface, or from atmospheric moisture. The degree of silane polymerization is controlled by the water availability and the nature of the organic substituent; low solubility of the silane in water

favors a higher degree of polymerization. Silanes with multiple organic substitutions, particularly those containing phenyl or tertiary butyl groups, promote the formation of stable monomeric silanols. The thickness of the resulting polysiloxane layer is influenced by the concentration of the siloxane solution used in the process. Although a monolayer is typically preferred, the solution concentrations commonly employed may lead to multilayer adsorption. For instance, a 0.25% silane solution deposited onto a glass substrate may result in the formation of three to eight molecular layers. These layers can form a loosely interconnected network, intermixed structures, or a combination thereof, as is observed with most deposition techniques. The functional groups within these layers generally orient horizontally on the substrate surface, though not necessarily in a planar configuration. Covalent bond formation to the substrate surface may exhibit a degree of reversibility, where bonds may form, break, and reform during the process of water removal—typically achieved by heating to 120 °C for 30-90 minutes or through evacuation for 2-6 hours—allowing for the relief of internal stresses and positional adjustment of interface components. The application of silane coatings may be performed using a variety of methods, including but not limited to spray deposition, vapor deposition, aqueous solution, aqueous alcohol solution, or spin-on techniques. Trialkoxysilanes are the preferred starting materials for substrate modification due to their tendency to deposit as polymeric films, thereby enhancing surface coverage and facilitating the introduction of organic functionalities. Siloxane is a kind of organosilicon compounds which is composed of –Si–O–Si–O– backbones with side chains R attached to the silicon atoms (R_2SiO), where R is a hydrogen atom or an organic radical possibly bearing functional groups. In some aspects, the coupling agent may be a chemical compound consisting Si, O, H, C or organic groups in a variety of combinations or proportions.

[0216] Nano-roughening of copper surfaces is a technique employed to enhance adhesion between copper and polymers in semiconductor packaging applications. By creating nanoscale roughness on the copper surface, the effective surface area is significantly increased, allowing for stronger mechanical interlocking and improved bonding with the polymer. This enhanced adhesion is crucial in semiconductor packaging, where reliable interfaces between different materials are essential for device integrity and performance. Nano or micro roughening of copper may be done by a variety of wet chemical processes involving acidic or basic chemicals. The average roughness values of processed copper may be in the range of 1 nanometers to 10 micrometers.

[0217] Optionally, the methods described herein can include forming metal pillars and/or underlying metal structures, where the average variation in thickness and/or height is

in the range from 1% to 50%. Alternatively or additionally, the metal pillars are substantially perpendicular to the underlying metal layers (e.g., the first metal layer).

[0218] Optionally, the polymers used in the present disclosure can have any combination of, or all of, the following characteristics: a melting point higher than 250°C, an ablation threshold above 1 J/cm^2, and/or a step coverage of at least 50%.

[0219] **Experimental Results and Additional Examples**

[0220] A study was conducted to develop package redistribution layers (RDL) using the exemplary methods and systems described herein. RDL can interconnect various system components such as logic, memory, and passive components as components of an electronic package.

[0221] *Materials, processes, and tools for ULK Dielectrics*

[0222] Parylene is a group of polymers that consists of para-benzenediyl rings ($-C_6H_4-$) connected by 1,2-ethanediyl bridges ($-CH_2-CH_2-$). Parylene is vapor deposited onto substrates with a process that resembles chemical vapor deposition (CVD). However, the process pressures are higher ≈ 0.1 Torr compared to the conventional vapor deposition pressures of $< 10^{-5}$ Torr. Parylene deposition is not line-of-sight deposition; in other words, the gaseous monomer uniformly deposits on all surfaces it comes into contact with. This results in truly conformal and uniform coatings without porosity over large panel areas. Parylene deposition consists of three main steps- (1) Vaporization, (2) Pyrolysis, and (3) Deposition.

[0223] In an example process, vaporization of the solid dimer is carried out at $\approx$ 150°C. Pyrolysis of the vaporized dimer is carried out in the pyrolysis chamber at 680°C. The cleavage of the methylene-methylene bonds occurs during pyrolysis, yielding the stable monomer diradical- para-xylylene. The monomer vapor then enters the deposition chamber which is at room temperature. The deposition and polymerization of parylene occur spontaneously on the substrate.

[0224] *Materials, processes and tools for 1× 3 Cu micrometer traces.* Chemically amplified, high-resolution, positive-tone photoresists for fine line RDL patterning Dry-film photoresists (PRs) are used in package substrate manufacturing as they can be laminated onto the substrate as compared to the more difficult spin-coating process used for liquids. Currently, photoresists used in packaging are negative-tone mainly due to their lower costs. There are several issues associated with negative-tone photoresists, such as adhesion- to seed-layer Cu , low resolution, larger thickness and difficulty in stripping. These issues become

more challenging for finer RDL patterning at 1 μmL/S. Because of fine line dimensions, the adhesion of PR to Cu becomes crucial. Poor adhesion leads to delamination and poor yields after development. Negative-tone PRs have poor resolution and are available in larger thicknesses > 5 μm. This is a major challenge to fine-line patterning as a larger Depth-of-focus (DoF) is necessary to resolve 1 μmL/S. Negativetone PRs get cross-linked when exposed to UV radiation. The unexposed regions are then dissolved during development to form the RDL pattern. Cross-linked PR is hard to strip and thus leads to residues that cause short defects in RDL. The advantages of positive tone photoresists are higher resolution, higher yield due to fewer defects and they can be easily stripped because they do not undergo crosslinking reactions during processing. Generally, the chemically amplified photoresist is composed of hydrophobic polymer with a protecting group and a photo-acid generator (PAG). The PAG molecule generates acid during the UV exposure process, and acid works as a catalyst for the deprotection reaction during the post-exposure bake. The polymer in the exposed area changes from hydrophobic to hydrophilic completely and is dissolved in the developer solution. As a result, a positive-tone photoresist enables better resolution than a negative-tone photoresist. The sensitivity of positive photoresist can be controlled by controlling photo-acid generation, providing high aspect ratio structures while maintaining low exposure doses. In the example embodiment described in this study, the aspect ratio of RDL is defined as the ratio of the Cu/PR height to the half-line-pitch.

[0225] The example process parameters are given in Table 3.3. Dose values were varied from 90 to 110 mJ/cm^2. 3D optical profiling of the pattern was not possible due to the transparent nature of the photoresist. The optimal dose value was found to be close to 100 mJ/cm^2. 1 μmL/S were resolved at 95 – 105 mJ/cm^2 dose values. Though 1 μmL/S seems resolved even at 90 mJ/cm^2, the traces did not get plated denoting incomplete PR opening. While at 110 mJ/cm^2, the lines are visibly over-exposed. Plasma descum was carried out using O_2 gas for making the PR surface hydrophilic and to remove PR residue. Electroplating was carried out at a plating current density of about 10 mA/cm^2. PR stripping was carried out using an EKC-162 stripping solution. Due to the positive tone of the PR, no residue is left after stripping.

[0226] *Maskless lithography for high aspect ratio patterning.* Mask-less lithography (MLL) systems, also known as 'Direct Laser Write (LDW)' systems, use a rasterized or vectorized laser beam to expose the pattern from a CAD design. MLL systems are used for panel substrate manufacturing mainly in fan-out packages [A. Pizzagalli, "Lithography technology and trends for advanced packaging," in 2016 China Semiconductor Technology

International Conference (CSTIC), IEEE, 2016, pp. 1-3; M. Lapedus, Lithography challenges for fan-out]. There are advantages offered by MLL. With the use of a laser source, the resolution achievable with MLL is dependent on the laser beam diameter, and it can be smaller than the resolutions of conventional aligners and steppers. MLL systems differ from traditional aligners and steppers in the directionality of radiation. A laser is a highly coherent and collimated beam of light having parallel rays resulting in minimal divergence as it propagates [M. Griot, "Introduction to laser technology," Technical Guide, pp. 10-6, 2009]. This results in a high DoF, which is not achievable with the traditional systems. MLL systems have been reported to have DoF as high as $\pm 12\mu$m [B. Matuskova, B. Považay, R. Holly, F. Bügelsack, T. Zenger, T. Uhrmann, and B. Thallner, "Maskless lithography optimized for heterogeneous and chiplet integration," in 2020 International Wafer Level Packaging Conference (IWLPC), IEEE, 2020, pp. 01-06].

Table 3.3: Example process parameters

Process step	Process parameters
Step 1: PR Lamination	Equipment: Meiki Vacuum Laminator Top plate temperature = 70°C Bottom plate temperature = 30°C Vacuum setpoint = 0.5 MPa Vacuum reach time = 30 seconds Vacuum hold time = 30 seconds
Step 2: Pre-exposure bake	Equipment: Hotplate Temperature = 130°C Duration = 3 minutes
Step 3: Exposure	Equipment: Heidelberg MLA 150 Wavelength = 375 nm Dose = 90 to 110 mJ/cm^2 Defocus = -2
Step 4: Post-exposure bake	Equipment: Hotplate Temperature = 90°C Duration = 4 minutes
Step 5: Development	Equipment: Puddle development Solvent = 2.38% TMAH (Tetra methyl ammonium hydroxide) Temperature = 32°C Duration = 90 seconds
Step 6: Plasma descum	Equipment: Oxford end-point RIE Plasma gas composition = 50 sccmO_2 Duration = 2 minutes

Step 7: Electroplating	Plating chemistry: Atotech Plating current density = 10 mA/cm^2
Step 8: PR stripping	Chemical: EKC-162 Temperature = 32 °C Duration = 2 minutes

[0227] In the study, Heidelberg MLA-150 was used for the fabrication of fine-line RDL. Fig. 9 shows the SEM image of electroplated 1 µm traces formed using MLA-150. RDL traces with zero taper were formed in a 5 µm thick photoresist denoting a Depth-ofFocus (DoF) of greater than ± 5 µm. Furthermore, dynamic autofocus of MLA-150 was found to be useful in correcting aberrations due to non-planarity, thickness variations, and substrate warpage.

[0228] Glass has numerous advantages over conventional organic laminates for fine-line patterning [R. Tummala, B. Deprospo, S. Dwarakanath, S. Ravichandran, P. Nimbalkar, N. Nedumthakady, and M. Swaminathan, "Glass panel packaging, as the most leading-edge packaging: Technologies and applications," in 2020 Pan Pacific Microelectronics Symposium (Pan Pacific), 2020, pp. 1-5]. Ultra-low roughness ($R_{RMS} < 1$ nm) of glass is advantageous in minimizing diffused reflections at the copper seed layer-photoresist interface, thus providing very fine lithographic dimensions. The smoothness of the copper seed layer on the glass was evident. Furthermore, the tunable coefficient of thermal expansion (CTE) of glass can be used to minimize the warpage of the substrate, providing ultra-high IO density multilayer RDL packages.

[0229] *Example Cu etching process.* Fig. 10 shows the process flow of an embodiment of the Cu etch technique described by the present disclosure. Most process steps are the same as the conventional SAP, with an intermediate step for barrier coating on RDL side walls. A detailed process description is followed.

[0230] For the study, glass substrates (sold under the trade name EN-A1) were obtained from AGC and were used for direct Cu metallization without an intermediate polymer dielectric layer. Copper-glass adhesion was found to be sufficient to prevent delamination of RDL traces. Glass substrates were treated with Ar (45 sccm, 150 W) and O_2(50sccm, 250 W) plasmas for 5 mins each using Oxford end-point RIE. Plasma-treated substrates were then deposited with 50 nm titanium seed followed by a 200 nm copper seed layer by DC sputtering (trade name: Unifilm sputterer). This was followed by photoresist lamination and patterning. A high-resolution, positive-tone photoresist with 5μm thickness

was used . This photoresist is optimized for 365 nm wavelength. A Heidelberg MLA-150 with a 375 nm UV source was used for patterning. Electroplating of copper was performed at a plating current density of $1 - 1.5$ A/dm^2 under galvanostatic conditions using electrolyte solution (trade name: Atotech Cupracid TP). Titanium barrier deposition was performed using a Unifilm sputterer. About 50 nm of titanium was initially deposited conformally over the whole substrate area. Selective anisotropic etching of titanium was carried out using Oxford end-point RIE. The plasma gas composition was: CHF_3, Ar, and O_2 (30, 20, 5 sccm, respectively). At 200 watts of RF power, the plasma duration was about 8 minutes to etch 50 nm of titanium. Plasma etching is a directional process resulting in the etching of titanium from the areas perpendicular to the direction of plasma. This resulted in the titanium barrier remaining only on the side walls of RDL features. Conventional copper etching was performed using etching chemistry provided by Atotech A spray etching system with a conveyor was used for copper etching. The etch rate was optimized by controlling the conveyor speed and temperature of the etchant. About 1.5X (300 nm) of etching (50% over etch) was performed for a 200 nm seed layer to ensure its complete removal. The titanium barrier remained unaffected by copper etchant and thereby protected the sidewalls. The next step involved simultaneous etching of the titanium seed layer and barrier. Hydrochloric acid-based titanium etchant was used. Etching temperature was 40°C with an etch duration of ≈ 10 seconds for 50 nm titanium. In order to improve Ti barrier-copper adhesion, a surface cleaning step using acid dip followed by argon plasma was performed before coating. Hitachi SU8230 was used for SEM images. Thermo Fisher Helios 5CX (FIB-SEM) was used for taking SEM images with FIB cross sectioning.

[0231] About $4 \times$ (800 nm) seed etch was carried out to demonstrate the effectiveness of the titanium barrier. No changes in L/S dimensions were observed for the barrier-coated sample, whereas the standard wet-etched sample showed 1.6μm smaller linewidth. The thin barrier layer on the side walls was still intact, demonstrating the effectiveness of the barrier. The barrier layer did not prevent a reduction in the height of Cu traces.

[0232] The Cu traces are conformally coated with a 50 nm thin titanium barrier layer. The L/S is $1.4/0.6\mu$m before and after Cu etching. The Cu seedlayer thickness is about 200 nm on the glass surface. A total 150%Cu etch equivalent to 300 nm Cu was carried out to ensure the complete removal of the seed layer. The absence of a Cu seed layer at the bottom of the traces is visible. It is evident that there is almost no difference in L/S dimensions.

Without the titanium barrier layer, 150% etch would result in a net 600 nm reduction in linewidth and an equal increase in the spacing between Cu traces. Minute differences in the L/S dimensions are due to slight dimensional variations over the whole substrate area. The FIB cross-section after Cu and Ti etch. Ti etching was carried out to remove the Ti seed layer as well as the barrier coating on the side walls. Complete etching of copper (200 nm) and titanium (50 nm) was confirmed by the Energy-dispersive Spectroscopy (EDS) maps of Cu and Ti. No Cu or Ti was detected from the spaces between Cu lines, denoting their complete removal. Titanium etching did not result in any dimensional changes. The height of the Cu traces is 3.3μm, corresponding to an aspect ratio of 3.3. The height of the traces looks larger in the SEM images due to cross-sectioning at 52° angle. Another noteworthy aspect is the smoothness of Cu traces after Cu&Ti etching. Wet etching usually results in a rough trace profile which is detrimental for high-frequency applications. The titanium barrier is seen to protect the side-walls, resulting in a smoother profile. The cracks at the bottom of the traces were formed at the Ti – Cu interface due to the ion beam damage during cross-sectioning. 0.8μm RDL traces were achieved using the Ti barrier process described herein. The L/S is 1.0/0.6 μm with a trace height of 2μm.

[0233] Embodiments of the present disclosure, including the example embodiment described in this study, address limitations of the current generation SAP RDL technology lithography, substrate, and Cu etching. Glass panel substrates with laser direct writing provide a path forward for low-cost high-density substrates for high-bandwidth applications. The example embodiments of a Cu etching process described herein can be utilized for further RDL scaling below 0.5μm using SAP, providing much higher bandwidth densities. Another example application of this technology is in high-frequency applications such as 5G and 6G, where low RDL roughness and fine dimensional control of system components (antennas, waveguides, filters, etc.) can be beneficial. Furthermore, the example embodiment's etching process can provide higher RDL yields than conventional etching. For achieving high RDL yield, over-etching of the seed layer can be necessary to ensure its complete removal. However, it leads to further side-wall etching, thus decreasing the electrical performance. Using the etch barrier coating described herein, it is possible to prevent dimensional changes, thus preventing performance losses and, at the same time, achieving good yield. The barrier layer can optionally be etched away or left on the side walls for protection against ionic migration or electro-migration as necessary.

[0234] The study of the example embodiment shows sub-micrometer RDL directly on glass substrates enabled by maskless lithography and advanced semi-additive processing. 0.8μm RDL was demonstrated with L/S of 1.0/0.6μm. The highest aspect ratio of Cu RDL traces achieved in this study was 3.3 for 1μm traces. The study also includes an etch barrier process for precise control of RDL dimensions. A 50 nm thick coating of titanium was preferentially coated on the side walls of copper RDL. The titanium coating acts as a physical barrier against copper etchants and prevents dimensional changes in RDL linewidth and spacing. The barrier can be etched away using titanium wet etchants and thus does not affect the electrical performance of the RDL. This process extends the capabilities of traditional SAP, providing the benefit of lower costs compared to the alternatives. This process can optionally be used for RDL scaling below 0.8μm.

[0235] *Materials and Processes for 2μm microvias and < 1μm alignment.* Via formation in package substrates has been carried out using laser drilling for both blind microvias as well as through vias. Laser drilling utilizes a concentrated laser beam that is used to ablate the polymer material. In this method, the microvia diameter achievable is limited by the laser beam diameter as well as the wavelength of the laser source. Conventionally, UV lasers are used due to the interaction of UV radiation with polymers. However, UV laser drilling has reached its limit with respect to microvia formation. Next-generation IO pitches require microvia diameters < 5 μm, which can be difficult to achieve using laser systems. Photovia is one of the options being adopted by the industry for < 5μm microvias. However, ULK dielectrics, such as parylenes, are not photosensitive. Furthermore, they are not designed for laser-via drilling. The higher melting point and thermal stability of Parylene-HT impose challenges with regard to laser drilling. Fig. 11 shows microvia with a diameter 3.1μm diameter drilled in 3.5μm thick Parylene-HT using ESI Cornerstone picosecond UV laser. The laser drilling parameters were- Power = 0.06W, Pulses = 10, Z-offset = 30 μm. Parylene-HT has a very high melting point of 550°C, which makes it very challenging to ablate the polymer. Furthermore, a lot of debris is created, as seen in the image before plasma cleaning. Plasma cleaning can remove the debris, although it results in reduced dielectric thickness. The shape of the microvia is very uneven with a very low yield. For the given laser settings, very few microvias were opened. The laser power used was very low and comparable to the laser power fluctuations. In addition, for thermo-mechanical reliability of finer microvias, it can be beneficial to accurately control the microvia shape and height,

which is not possible with laser drilling. For all these reasons, laser drilling of microvias in ULK dielectrics is not feasible.

[0236] Laser drilling of vias can be especially challenging for polymers such as Parylene-HT that have very high melting point and/or ablation threshold. Melting point may be defined as the temperature at which heat flow properties show signs of change in the differential scanning calorimetry analysis.

[0237] *Process for microvia formation in ULK dielectrics.* Embodiments of the present disclosure include processes for the formation of microvias in ULK dielectrics. Fig. 12 shows the overall process flow for the formation of a daisy chain structure.

[0238] An example embodiment of a method for forming microvias in UKL dielectrics includes seed layer deposition on the desired substrate. In the study, glass was used directly as a substrate without an intermediate dielectric. The substrate with a seed layer is used for the formation of copper pads. In the study, microvias with diameters 2-4 μm were targeted. The Cu pad width was designed to be 0.5μm larger than the via size, e.g., alignment tolerance of $\pm$0.25 µm. The via pitch of 10 µm and 20 µm was targeted. Fig. 13A shows the optical images of Cu pads with 3.5 µm width and 20 µm pitch. A positive-tone photoresist was used for patterning, and the process parameters were the same as described in the earlier sections. The Cu seed layer was not etched after the formation of Cu pads.

[0239] After the formation of via landing pads, Cu pillars were plated on top of the pads utilizing the Cu seed layer. The main challenge in this step is that the photoresist opening is limited by the photoresist topography and thickness. In the study, the minimum via diameter of 1.6μm was resolved with a relatively lower yield. Vias with diameters 2.5μm and above were resolved with 100% yield.

[0240] Using laser direct writing and chemically amplified photoresist, microvias or pillars with almost zero taper can be produced. Vias having close to zero taper or having a vertical profile have better mechanical reliability as well better yield. Fig. 8 depicts pillars or vias having different taper angles. A tapered profile as shown in the first and second figures from the left are obtained with non-chemically amplified photoresist and/or lithography technique with low depth of focus. Whereas the rightmost figure depicts a perfectly vertical pillar profile having the taper angle of 90-degrees. This can be achieved by a combination of chemically amplified photoresist and laser direct writing system. Fig. 15 demonstrates high-density fine pitch pillar structures formed using this technique.

[0241] The example method can include dielectric deposition. A total thickness of 6 μm was deposited conformally, covering the pillars and Cu pads. Conformal deposition resulted in an overburden of 1-2 μm over the flat regions 5 μm to 6 μm over the Cu pillars. Fig. 13B shows the 2 μm pillars with conformally deposited Parylene-HT, and Fig. 13C shows, at Step 4, 3 μm vias after planarization.

[0242] Before the formation of the top metal layer, the overburden dielectric can be removed in order to open the vias for electrical connection. Mechanical planarization was performed using a Logitech LP50 lapper. Alumina slurry having 1μm particle size was used for removing the excess material. The substrates were polished until the dielectric overburden was completely removed, and the vias were slightly polished. Opening of vias was confirmed using laser profilometry function in an optical profiler (trade name: Keyence VK-X3000). The laser profilometry was able to differentiate between copper and polymer better than optical wavelength, as seen from the contrast difference in Fig. 13B. A challenge in this step is dielectric residue preventing electrical contact between the top metal layer and the vias.

[0243] Finer alumina particle size is desired as large particle sizes result in excessive mechanical deformation. In the study, 1 μm alumina slurry caused excessive deformation in < 3 μm vias.

[0244] Low-k polymer dielectrics that do not contain filler material (e.g. SiO2) can provide benefits over conventional ABF-like dielectrics. The filler material can pose challenges with respect to planarization because of the difference in mechanical properties of polymer and the filler material. Especially with CMP or lapping techniques, the filler material makes it difficult to planarize evenly due to the filler material being harder than the polymer matrix. The choice of the slurry thus becomes very critical. However, with filler-less dielectrics such as parylenes provide better uniformity because of a more homogeneous topography. Mechanical planarization techniques such as fly-cut planarization can provide better uniformity as it is not selective with respect to the filler or polymer materials.

[0245] The final step involves top metal layer formation using conventional SAP steps described earlier. Fig. 13D shows the top metal layer completing the daisy chain structure of 3 μm vias at 20 μm pitch. The alignment marks also get polished during the planarization step and are deformed thus lowering the alignment accuracy. The top metal layer is designed with $\pm 1\mu$m tolerance as compared to ±0.25 μm tolerance for the via alignment.

[0246] Fig. 14 shows the FIB cross-section of 3 μm diameter via a daisy chain structure of 100 vias built using the example process. Via height was 1μm after planarization with a via pitch of 10μm. The top pad-via interface appears rough due to the mechanical planarization step. Dielectric residue between the pad and via is another challenge causing the discontinuity. Better planarization process control can be used to mitigate these issues.

[0247] *Modeling Stress* Study of microvia reliability in ULK dielectrics: Using the FEA model discussed above, the polymer dielectric candidates were simulated to determine their reliability for 1 μm RDL fabrication. Two via geometries with vias angles of 80° and 90° were simulated to study the effect of via angle. Via diameter was kept constant at 2 μm. The material properties used for dielectric candidates are shown in Table 4.2. All other assumptions and conditions were the same as discussed earlier.

Table 4.2: Material properties of ULK dielectric candidates

Dielectric	Elastic modulus (GPa)	CTE (ppm/K)
BCB	2.9	42
Dielectric J	1.5	65
Parylene HT	2.55	36

[0248] Fig. 16A shows the TSR values obtained from the simulations for 90°-vias. TSR increases with an increase in the via height. Alternatively, it can be said that TSR increases with the aspect ratio as the diameter of the via is constant at 2μm. For both 80°- and 90°-via geometries, Parylene-HT has the lowest strain. For 80°-vias, Dielectric J has the highest strain, while for 90°-vias, BCB has the highest strain. This is attributed to the differences in their CTE and modulus. At a smaller via angle, the effect of CTE seems to dominate as there is more stress concentration due to the effect of geometry. For 90° via geometry, TSR values are significantly lower than that of 80°. Clearly, perfectly vertical vias, e.g., vias with zero taper, are more reliable, as has been reported earlier. In summary, it is the combined effect of elastic modulus, CTE and via geometry that causes the strain in the vias. Low aspect ratio and vertical vias (90°) are more reliable, while dielectrics having low CTE and modulus provide better reliability. Among the three dielectric candidates, Parylene-HT is the most reliable because of its low CTE and elastic modulus.

[0249] *Microvia scaling limitations:* Microvias can sustain a thousand thermal cycles as per the JEDEC standard for passing the reliability criteria. With the reduction in microvia diameter, the strain in the via increases, and thus fatigue life decreases. At a certain point, the total strain range is too high for the via to be reliable. The FEA model described herein was utilized to determine the via diameter at which via reliability hits the limits.

[0250] Conventional laser-drilled microvias have a taper due to the Gaussian distribution of laser power. Thus, the maximum possible via angle with laser drilling is about 80°. For this modeling study, a via geometry with 80°-via angle and an aspect ratio of 1 was considered. This via geometry represents the best case of conventional laser-drilled via. Polymer dielectric properties included CTE = 35 ppm/K, elastic modulus = 2.5 GPa. These properties represent the best-case properties for an epoxy-based dielectric commonly used in substrate packaging. These design and material parameters were used for simulating the total strain range and the results are shown in Fig. 16B.

[0251] *Polymer Reliability.* Polymer cracking in RDL occurs at the copper-polymer interfaces, especially at the corners and the edges of copper features. The stresses developed in the region surrounding the copper traces were evaluated using an FEA model. The effect of RDL L/S and aspect ratio on stress is shown in Fig. 17A. As the RDL dimensions are reduced, the stress in the dielectric increases. Also, stress increases with an increase in the aspect ratio of wires. ULK polymer dielectric candidates were simulated to determine their reliability for 1 μm RDL. The results are shown in Fig. 17B. The effect of elastic modulus and CTE of polymer is apparent from the stress values. Parylene-HT shows the lowest stress because of its low CTE and modulus. As discussed in the previous chapter, the cracking in polymer dielectrics is due to fatigue. However, the fatigue models can be determined empirically. Therefore, the stress in polymers is represented as the ratio of the tensile strength. The probability of fatigue failure should be low as the stress is about 30% of the tensile strength. Therefore, all three dielectric candidates seem reliable in terms of polymer cracking reliability.

[0252] *Adhesion Reliability.* Fig. 18A shows the effect of the Cu deposition rate on adhesion. For the study, the Ti deposition rate was kept constant at 200 A°/min. As the deposition rate is increased, the sputtering voltage increases which increases the energy of sputtered atoms. Therefore, adhesion strength improves as more copper atoms diffuse in bulk, causing better mechanical/chemical interlocking. After 1000 A°/min, the atomic flux of sputtered atoms is too high, resulting in the aggregation of copper atoms. This results in lower adhesion strength.

[0253] Fig. 18B shows the effect of the Ti deposition rate on adhesion. In the study, the Cu deposition rate was kept constant at 200A° /min. With the increase in deposition rate, the sputtering current increases, which increases the atomic flux of sputtered atoms. Therefore, adhesion strength decreases as more copper atoms aggregate rather than diffuse in the bulk. After 800 A° /min, the energy of sputtered atoms is too high, resulting in the diffusion of copper atoms inside bulk, leading to better mechanical/chemical interlocking. This was observed to provide results with higher adhesion strength.

[0254] *Pre-sputtering process for enhanced adhesion.* As described herein, plasma processing before metal deposition can affect the metal-polymer interactions. The conventional pre-sputtering process involves argon plasma treatment followed by Ti – Cu seed sputtering. Embodiments of the present disclosure include a modified pre-sputtering developed to enhance the adhesion of metal seed with the polymer [P. Nimbalkar, C. Blancher, M. Kathaperumal, M. Swaminathan, and R. Tummala, "Effect of titanium-polymer interactions on adhesion of polymer-copper redistribution layers in advanced packaging," IEEE Transactions on Device and Materials Reliability, pp. 1-1, 2022]. In an example embodiment, the sequence of steps is as follows- argon plasma etch → oxygen plasma etch → pre-bake in vacuum → Ti and Cu seed sputtering → electroplating of Cu. However, the present disclosure contemplates that these steps can be performed in different orders, different numbers of times, and/or with additional intervening steps.

[0255] *Materials and methods.* Six different polymer dielectrics with different polymer chemistries were used in this study. The dielectrics are labeled ABF, BCB, P-C (Parylene-C), PHT (Parylene-HT), Diel-J, and Diel-1. ABF-GX92 (Ajinomoto Build-up Film) is a commercially available polymer dielectric widely used in the electronics industry. ABF is a silica-filled dielectric with epoxy as the polymer matrix. BCB (Benzocyclobutene) polymer was obtained from Dow (Trade name: BCB Cyclotene 6505). BCB is a photo-initiated dielectric used in the electronics industry for a variety of applications. Parylene-C and Parylene-HT are commercially available polymer coatings developed by Specialty Coating Systems (SCS). Parylene is the name for a group of polymers based on poly(para-xylylene). Parylene-C is chlorine-substituted, while Parylene-HT is a fluorine-substituted version. Diel-J and Diel-1 are research-grade polymer dielectrics.

[0256] Polymer dielectrics were applied onto 4-inch silicon or FR4 substrates for the study. ABF and Diel-1 were laminated using Meiki vacuum laminator. Parylene-C was vapor deposited using SCS Labcoater PDS 2010. ParyleneHT coated samples were received from

SCS inc. BCB and Diel-1 were spin-coated on silicon wafers. Polymer dielectrics were subjected to two types of pre-sputtering plasma processes. The first process (denoted as-Ar) involved standard argon plasma treatment (150 W, 50 sccm, 8.5 mins) using Oxford End-point RIE. The second process (denoted as Ar-O_2-bake) involved Argon plasma followed by oxygen plasma (200 W, 40sccm, 2 mins) followed by baking (125°C at 5 mTorr for 30 mins) in a vacuum oven (Heraeus vacuum oven).

[0257] Adhesion samples were deposited with 50 nm titanium seed followed by a 200 nm copper seed layer by DC sputtering (Unifilm sputterer). It was followed by electroplating of 20-25µm copper at a plating current of 1-1.5A/dm^2. Copper was electroplated under galvanostatic conditions using Atotech's Cupracid TP electrolyte solution. Samples with electroplated copper were annealed at 200°C for 1 hour under a nitrogen environment. For XPS experiments, samples pre-treated with two plasma processes (Ar and Ar-O_2-bake) were deposited with 10 nm of titanium seed-layer. For roughness measurements and FTIR scans, pre-treated samples were used without any further processing.

[0258] *Characterization.* The interfacial adhesion between the dielectric and copper was quantified using a 90°C peel tester (Testing Machines Inc.). Peel-tests were performed on 1-cm wide metal strips at a peel-rate of 30.5 cm/min. The substrates were carefully taped onto the base metal plate to ensure that the substrate warpage did not influence the measured peel strength.

[0259] Roughness measurements were carried out on the Veeco Dektak 150 profilometer. Samples pre-treated with Ar and Ar-O_2-bake processes were used for roughness measurements. To ensure comparability of data, all samples were characterized with the same scan parameters (scan length: 1000μm, duration: 60 s, resolution: 0.006μm, max load: 5 mg). X-ray photoelectron spectroscopy studies were performed using Thermo K-Alpha XPS.

[0260] For studying Ti-polymer interactions, Ar and Ar-O_2-bake treated dielectrics were deposited with 10 nm of titanium. The effect of plasma on polymer surfaces is temporary and disappears within a few hours after the plasma. Ti deposition was carried out immediately after the pre-treatment processes to preserve its effectiveness. XPS scans were performed after a short in-situ Ar etching process (ion energy: 1000 eV, duration: 2 mins). Depth profiling was carried out using the same in-situ Ar etching by varying the etch duration.

[0261] To study the effects of plasma processes on different dielectrics, FTIR spectroscopy was performed using a Thermo Scientific Nicolet iS50 FTIR spectrometer in

attenuated total reflection (ATR) mode. Ar and Ar-O_2-bake treated dielectrics were analyzed using an FTIR spectrometer within one hour after finishing the processes.

[0262] *Characterization Results.* Fig. 19A summarizes the results of adhesion strength measurements of six dielectrics investigated in the study. It can be seen that the Ar-O_2-bake process resulted in a significant increase in the adhesion strength compared to the Ar plasma process for five of the six dielectrics. The highest increase in mean adhesion strength was observed for Diel-1 from 0.25 N/cm with Ar to 11.2 N/m with Ar-O_2-bake. Similarly, ABF showed an increase in mean adhesion strength from 8.9 N/cm to 10.8 N/cm. ABF also showed the highest maximum adhesion strength of 17.7 N/cm. BCB and Diel-J showed poor adhesion strength of 0.25 N/cm with Ar treatment. Here, 0.25 N/cm corresponds to the minimum measurable adhesion using the peel tester. Ar- O_2-bake treatment resulted in a slight increase in adhesion for both BCB and Diel-1. P-HT showed an increase in adhesion from 2.7 N/cm to 8.4 N/cm. P-C showed a minimal increase in mean adhesion strength from 5.4 N/cm to 5.4 N/cm.

[0263] The study showed that the increase in adhesion strength was independent of the chemistry of the dielectric. As discussed earlier, there can be two main mechanisms of adhesion- mechanical and chemical. Mechanical bonding involves physical interlocking of two adhesive surfaces due to the roughness of the interfaces. Chemical bonding involves chemical interaction between the deposited metal and polymer. In order to elucidate the contribution of the mechanical component, roughness measurements were performed. Fig. 19B shows the roughness values (Ra) measured for all dielectrics for both pre-treatment processes. BCB, Diel-J, and P-C showed higher roughness after the Ar process than Ar-O_2-bake process. While P-HT, Diel-1, and ABF showed slightly higher roughness values with ArO_2-bake than with Ar process. For P-HT, there was a marginal difference in roughness values. Additional oxygen plasma step in Ar-O_2-bake is expected to result in slightly higher roughness values. However, the baking step after Ar and O_2 plasma, possibly leads to smoothening of the polymer surface because of softening due to elevated temperature. Nevertheless, the differences in the roughness values are insignificant and don't explain the higher adhesion values for Ar-O_2-bake process. Usually, a significant increase in surface roughness is necessary to observe the kind of adhesion enhancement observed in this study. Therefore in these results, the contribution of mechanical bonding to adhesion enhancement is expected to be minimal. In order to understand the reasons for adhesion enhancement, detailed XPS analyses are presented in the next section.

[0264] X-ray photoelectron spectroscopy analysis In order to find out the contribution of chemical interactions to adhesion, X-ray photoelectron spectroscopy (XPS) was employed.

[0265] ABF was selected for detailed analyses as it is widely used in the electronics industry. Fig. 20A shows the XPS C-1s spectra of Ti-deposited ABF dielectric treated with Ar plasma and Ar-O_2-bake. It was observed that Ar-O_2-bake treated surface showed lower intensity compared to Ar-treated surface. Though there are numerous factors affecting the intensity of the XPS signal, the lower intensity of Ar-O_2-bake samples can be partly attributed to the broken polymer bonds. Breaking of the polymer backbone would result in numerous unsaturated sites leading to overall fewer bonds present on the polymer surface. A sharp increase in the intensity of the peak around 282 eV was also observed. This peak corresponds to Ti-C bonding [K. W. Paik, H. S. Cole, R. J. Saia, and J. J. Chera, "Studies on metal/benzocyclobutene (bcb) interface and adhesion," Journal of Adhesion Science and Technology, vol. 7, no. 5, pp. 403-415, 1993; S. Freilich and F. Ohuchi, "Reactions at the polyimide-metal interface," Polymer, vol. 28, no. 11, pp. 1908-1914, 1987; F. S. Ohuchi and S. C. Freilich, "Metal polyimide interface: A titanium reaction mechanism," Journal of Vacuum Science & Technology A, vol. 4, no. 3, pp. 10391045, 1986; M. Du, R. Opila, and C. Case, "Interface formation between metals (cu, ti) and low dielectric constant organic polymer (flare™ 1.0)," Journal of Vacuum Science & Technology A: Vacuum, Surfaces, nd Films, vol. 16, no. 1, pp. 155-162, 1998] and the increased intensity is due to the higher number of Ti-C bonds present.

[0266] Fourier Transform Infrared spectroscopy analysis Fig. 20B shows the FTIR spectra of pristine, Ar-treated, and Ar-O_2-bake treated ABF in 1300-1800 cm^{-1} range. The absorbance peaks around 1500 cm^{-1} correspond to the stretching mode of carbon-carbon double bonds. Whereas the peak around 1730 cm^{-1} corresponds to the stretching of carbonyl bonds. It can be clearly seen that there are significant differences in absorbance values. Pristine ABF surface shows the highest absorbance as all polymer bonds are intact in the absence of any pre-treatment. A decrease in absorbance was observed for Ar-treated and Ar-O_2-bake treated samples on account of broken polymer bonds. ABF treated with Ar-O_2-bake process showed the lowest absorbance, signifying the highest number of broken polymer bonds. Fig. 20C shows the FTIR spectra in the 2700-3100 cm^{-1} range. The spectrum on the right of 3000 cm^{-1} corresponds to alkyl C-H bonding, while the spectrum on the left corresponds to aromatic C-H bonding. Similar to Fig. 20B, a reduction in absorbance is seen, confirming the breakage of both aromatic and alkyl C-H bonds.

[0267] Fig. 21A and Fig. 21B show the fitted XPS C-1s spectra of Ti-deposited ABF for Ar and Ar-O_2-bake respectively. ABF-GX92 is an epoxy dielectric with a phenol hardener. Based on the reported chemistry of ABF [Y. Nishimura, "Advanced insulating film for next-generation smartphone performance requirements," Presented at ECTC, 2019], the presence of C-C, C=C, and C-O bonds is expected. In Fig. 21A, the C-C component has the highest contribution, followed by C=C and C-O. At 282.3 eV, a small shoulder corresponding to Ti-C bonding is also present. This confirms the interaction between the titanium seed-layer and the polymer backbone of ABF. In Fig. 21B, the most obvious difference is the presence of a strong Ti-C component at 281.6 eV. C-C components show a higher contribution than the Ar-treated surface. There is a significant reduction in the contribution of C=C component and a slight reduction in the C-O component. This is attributed to the higher breakage of C=C bonds during the Ar-O_2-bake process than the Ar treatment. Partially broken C = C bonds might be responsible for the stronger C-C component. The breakage of C-O bonds might also be a contributing factor to the C-C component. FTIR spectra in Fig. 20B and Fig. 20C confirm that after ArO_2-bake process, there is higher breakage of polymer bonds. The higher adhesion strength achieved with Ar-O_2-bake process is attributed to the higher number of Ti - C bonds due to the increased titanium-polymer interaction.

[0268] Comparing Fig. 21A and Fig. 21B, it is observed that there is a shift in the positions of C=C and Ti-C components towards lower binding energies. C=C component shifted from 284.1 eV (Ar) to 282.7 eV (Ar-O_2-bake). While the Ti-C component shifted from 282.3 eV (Ar) to 281.6 eV (Ar-O_2-bake). This is again attributed to the higher titanium-polymer interactions. The Ti-C component has lower binding energy, while C=C has higher binding energy. Therefore, as more C=C bonds are broken and Ti-C bonds are formed, a lowering of the binding energy of C-1 s electrons is expected. The significant shift in C=C denotes higher breakage of the polymer backbone and formation of Ti-C bonds.

[0269] As discussed earlier, Argon plasma provides physical breakage of polymer bonds and provides a rough surface for adhesion. Oxygen plasma further provides a larger number of broken bonds by chemical breakage by reacting with carbon atoms from the polymer backbone. Adsorption of oxygen ions during the oxygen plasma step is also expected to play some role. However, just the oxygen plasma process or Ar-O_2without baking did not result in a significant increase in adhesion. It is hypothesized that the baking step after ArO_2 plasma temporarily stabilizes the broken polymer bonds and adsorbed oxygen ions on the polymer surface. Furthermore, Ti-C bond formation is expected to be assisted through Ti-O-C intermediate formation [J. F. Friedrich, I. Koprinarov, R. Giebler, A. Lippitz,

and W. E. S. Unger, "Reactions and intermediates at the metal-polymer interface as observed by xps and nexafs spectroscopy," The Journal of Adhesion, vol. 71, no. 2-3, pp. 297-321, 1999; J. M. Burkstrand, "Metal-polymer interfaces: Adhesion and x-ray photoemission studies," Journal of Applied Physics, vol. 52, no. 7, pp. 4795-4800, 1981; T. P. Nguyen, A. Lahmar, and P. Jonnard, "Adhesion improvement of poly(phenylenevinylene) substrates induced by argon-oxygen plasma treatment," The Journal of Adhesion, vol. 66, no. 1-4, pp. 303-317, 1998; M. Du, R. Opila, and C. Case, "Interface formation between metals (cu, ti) and low dielectric constant organic polymer (flare^{TM} 1.0)," Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films, vol. 16, no. 1, pp. 155-162, 1998].

[0270] Since oxygen can form two bonds, it can act as a bridge between titanium and carbon atoms, leading to the formation of a crosslinking structure. The temporary Ti-O-C bonds may then completely convert to Ti − C and Ti-O bonds [J. F. Friedrich, I. Koprinarov, R. Giebler, A. Lippitz, and W. E. S. Unger, "Reactions and intermediates at the metal-polymer interface as observed by xps and nexafs spectroscopy," The Journal of Adhesion, vol. 71, no. 2-3, pp. 297-321, 1999; S. Freilich and F. Ohuchi, "Reactions at the polyimide-metal interface," Polymer, vol. 28, no. 11, pp. 1908-1914, 1987; F. S. Ohuchi and S. C. Freilich, "Metal polyimide interface: A titanium reaction mechanism," Journal of Vacuum Science & Technology A, vol. 4, no. 3, pp. 10391045, 1986. eprint: https://doi.org/10.1116/1.573450]. A strong Ti-O bonding was also detected in the Ti-2p spectra of the samples studied. Formation of Ti-C and Ti-O interlayer between titanium and polymers has been reported earlier [Y. Oh, E. J. Kim, Y. Kim, K. Choi, W. B. Han, H.-S. Kim, and C. S. Yoon, "Adhesion of sputter-deposited cu/ti film on plasma-treated polymer substrate," Thin Solid Films, vol. 600, pp. 90-97, 2016].

[0271] Fig. 22 shows the depth profiles of Ti-deposited, Ar-O_2-bake processed ABF. The presence of Ti-C and Ti-O peaks is clearly seen in the Ti-2p profile. With increasing etch depth, both Ti-C and Ti-O peaks diminish in intensity. The same observation can be made from C-1's and O-1's profiles. Strong Ti-C and Ti-O components are present at shallow depths closer to the top surface. Both C-1s and O-1s profiles show a shift towards higher binding energies, signifying organic carbon and oxygen bonding in the polymer. Ti-2p profile shows strong spectra even at larger depths denoting diffusion of titanium atoms inside the bulk polymer. Since the effects of pre-deposition plasma processing are limited to the polymer surface, the presence of strong Ti-C and Ti-O peaks near the top surface is reasonable. This also denotes that a large part of titanium atoms inside bulk polymer may remain unreacted. F. Faupel, V. Zaporojtchenko, A. Thran, T. Strunskus, and M. Kiene, "7 -

metal diffusion in polymers and on polymer surfaces," in Diffusion Processes in Advanced Technological Materials, D. Gupta, Ed., Norwich, NY: William Andrew Publishing, 2005, pp. 333-363, ISBN: 978-0-8155-1501-2; F. Faupel, R. Willecke, and A. Thran, "Diffusion of metals in polymers," Materials Science and Engineering: R: Reports, vol. 22, no. 1, pp. 1-55, 1998]. Therefore, pre-deposition plasma processing can enhance chemical interactions.

[0272] ABF, BCB, Diel-J, and Diel-1 contain oxygen atoms in the polymer structure, which may assist in Ti-C formation through an oxygenated intermediate. In the case of P-C and P-HT, there are no oxygen atoms present in the polymer backbone. However, there was still an increase in adhesion strength. This can be attributed to the adsorbed oxygen from the plasma process. Also, oxygen can be present inside the sputtering chamber even at very low base pressures. Oxygen pick-up from the background is a possibility and could be partly responsible for the increased adhesion strength [M. Du, R. Opila, and C. Case, "Interface formation between metals (cu, ti) and low dielectric constant organic polymer (flare ^{TM}1.0)," Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films, vol. 16, no. 1, pp. 155-162, 1998].

[0273] Table 4.3 shows the percentages of Ti-C components extracted from the fitted C-1s spectra of all dielectrics under study. Ar-O_2-bake process showed a higher percent of Ti-C component compared to Ar process. ABF and Diel-1 show a significantly higher Ti-C percent consistent with their high adhesion strength values. Diel-J showed a lower adhesion improvement and a smaller increase in Ti-C percent. BCB showed the highest increase of 16.6% and yet showed lower adhesion values. This may be due to the poor chemical reactivity of BCB towards titanium [K. W. Paik, H. S. Cole, R. J. Saia, and J. J. Chera, "Studies on metal/benzocyclobutene (bcb) interface and adhesion," Journal of Adhesion Science and Technology, vol. 7, no. 5, pp. 403-415, 1993. eprint: https://doi.org/10.1163/156856193X00295]. As these are relative percentages of components and not absolute amounts, it is possible that 16.6% increase in Ti-C component may not be sufficient for proportional adhesion enhancement. Furthermore, adhesion strength can be dependent on the strength of polymer bonds. Increased titanium interactions wouldn't necessarily result in high adhesion in a polymer with weaker bonds or lower tensile strength. This is supported by the fact that P-C and P-HT have high tensile strength due to their highly crystalline nature. This can be the reason for their higher adhesion values, even with a relatively low increase in Ti-C percent. Either of these factors can lead to lower adhesion observed for BCB.

Table 4.3: Ti-C component percentage in XPS C-1s spectra

Dielectric	**Process**	
	Ar	**Ar-O_2-bake**
ABF	13.1	25
BCB	6.3	22.9
Diel-J	16.5	18.7
Diel-1	12.7	28.3
P-C	5.1	10.1
P-HT	20.64	28.8

[0274] **Contact angle studies**

[0275] Fig. 23 shows contact angle measurements for the dielectrics treated with Ar plasma and Ar-O_2-bake processes. Ar-treated dielectrics showed very low contact angles with water, denoting the hydrophilic nature of the surfaces. However, Ar-O_2-bake processed dielectrics showed significantly higher contact angles, denoting a reduction in hydrophilicity. The hydrophilicity after Ar plasma might be due to the adsorbed Ar^+ ions on dielectric surfaces. The adsorbed Ar^+ might play a role in preventing metal-polymer interactions. $Ar - O_2$-bake treatment may reduce the number of Ar^+ ions on dielectric surfaces, thereby making the polymer surface more reactive and facilitating Ti-polymer interactions.

[0276] The interactions between titanium seed and polymer dielectrics were studied for a variety of commercial dielectrics. The effects of two pre-deposition plasma processes on adhesion and chemical interactions were investigated. Ar-O_2-bake process resulted in a significant adhesion enhancement without an appreciable increase in roughness. From XPS study of ABF dielectric, it was found that a larger Ti-C component was responsible for the adhesion enhancement. A higher percentage of Ti-C component in XPS C-1s spectra was observed for all dielectrics under study. Broken polymer bonds play a crucial role in chemical interactions. FTIR scans confirmed a larger number of broken polymer bonds in Ar-O_2-bake samples. Ti-C formation may occur through Ti-O-C intermediate formation using oxygen from plasma treatment. Thus, the study further demonstrates process optimization for achieving high polymer-RDL adhesion.

[0277] DESIGN, MATERIALS, AND PROCESSES FOR MULTI-LAYER RDL

[0278] *ULK dielectric material selection for High Bandwidth and Reliability.* Selection of ULK dielectrics for low capacitance RDL is challenging due to the conflicting nature of the fundamental physical properties of polymers. Traditional epoxy-based dielectrics used in package substrates have silica fillers that compensate for the poor mechanical properties of polymer matrix but result in an increased dielectric constant (D_k). ULK dielectrics don't have silica fillers leading to lower Dk but poor mechanical stability. Thus, the selection of polymer dielectrics for RDL applications needs to be carried out with several considerations that include- thermal and mechanical stability, moisture sensitivity, processability and chemical inertness. Dielectric constant (D_k) and Dissipation factor (D_f) need to be as low as possible to minimize RDL capacitance and dissipation losses. In the instant study, $D_k < 2.7$ was targeted. The processability of polymers is an important factor in being able to build a multilayer structure consisting of RDL routing with vias. It is critical to control the thickness of the dielectric to achieve the desired via dimensions. For targeting a microvia dimension of 2 μm diameter, it is important to have dielectric thickness lower than 5 μm. Dry film dielectrics conventionally used in package substrates are not available with less than 5 μm thickness. That leaves only liquid or vapor deposited dielectric. Another reason for desiring thin dielectrics is that a lower aspect ratio of vias gives better thermomechanical reliability. Liquid dielectrics can be difficult to process on panels as they need to be spin-coated. The uniformity and planarity of spin-coated dielectrics are poor, especially on multi-layered substrates. Furthermore, for impedance matching, very fine thickness control (<1 μm) is desired. Vapor-deposited polymers are thus very attractive due to sub-micrometer thickness control. Young's modulus and CTE of polymers play crucial roles in the thermomechanical reliability of microvias. A low Young's modulus (<7 GPa) is desired to lower the stresses induced in RDL. A very high modulus makes the polymer less pliable and cannot accommodate the expansion of copper. On the other hand, CTE value needs to be as low as possible, preferably <60 ppm/K. Tensile strength and elongation to failure are also critical to prevent polymer cracking. Polymers become viscous and more flowable above the glass transition temperature. Therefore, to prevent RDL failure, the glass transition temperature should be above the solder reflow temperature of 250°C, i.e., the maximum temperature encountered by the package substrate during processing. Moisture absorption in polymers leads to ionic migration under the influence of electrical bias. Therefore, moisture absorption needs to be <0.5% with ideally zero ionic content. Several ULK polymer dielectrics were considered in the instant study. Based on the requirements,

BCB (Dow Cyclotene 3035), Parylene-HT and Dielectric-J (R&D grade polymer from an industry partner) were the potential dielectric candidates in the study. Parylene-HT was identified as the best candidate and used for further evaluations.

[0279] *RDL Resistance and Capacitance.* RDL capacitance has a major effect on the maximum signal speed that can be transferred through the channel thereby affecting the bandwidth. A low capacitance RDL is desired to reduce RC losses and crosstalk between the adjacent lines. RC losses and crosstalk cause an increase in latency and a reduction in signal amplitudes. These two factors affect the readability of the signal described in the latter part of this section. At higher data rates, the losses become excessive leading to non-readability of the signal. For this reason, to achieve higher bandwidths, lower capacitance RDL is desired.

[0280] Fig. 24A shows the effect of the aspect ratio and L/S on RDL resistance. Specifically, Fig. 24A shows the effect of RDL aspect ratio on DC resistance of a single copper line of 1 mm length. Clearly, a higher aspect ratio leads to lower resistance due to increased cross-sectional area. At current generation operating frequencies, the skin depth is proportional to the minimum RDL dimensions. For example, at 1 GHz, the skin depth in Cu is 2.06 μm. However, with higher data rates, the skin depth reduces and becomes considerably smaller than the Cu trace widths. At 10 GHz, the skin depth in Cu is 0.65 μm.

[0281] In this case, most of the current in RDL flows through the periphery of the conductor lines. Larger conductor widths, therefore, provide no benefit. Due to the skin depth phenomena, at higher frequencies, it becomes critical to maximize the perimeter of the RDL wires instead of the cross-sectional area. In other words, finer pitch traces with higher aspect ratio traces provide additional benefits at >10 GHz.

[0282] Fig. 24B shows the effect of aspect ratio on total capacitance (self-capacitance + mutual capacitance) of an RDL line with 1 μm width. SiO_2 dielectric used in back-end packaging results in a very high capacitance compared to all polymer dielectrics shown. Parylene-HT has the lowest Dk among all dielectrics under evaluation and thus can result in up to 44% reduction in capacitance compared to SiO_2.

[0283] *Electrical performance.* The primary motivation for choosing RDL materials with low Dk is their potential to signal at higher data rates while maintaining signal integrity. This along with fine-pitch routing lines can increase the overall bandwidth. An eye diagram is a graphical tool that is indicative of signal integrity and electrical performance. It can be used to measure the signal amplitude, latency, jitter, signal-to-noise ratio and distortions in an electrical signal. Usually, a threshold value is set by the designer to denote the readability of the signal as per the required specifications.

[0284] Fig. 26, subpanel A and Fig. 26, subpanel B show insertion and return losses, respectively, in 1 μm striplines with Parylene-HT and SiO_2 as dielectrics. Parylene-HT shows significantly lower losses compared to SiO_2 mainly due to the lower D_k and D_f. At 50 GHz, Parylene-HT showed 2.73 dB loss as compared to 3.04 dB loss for SiO_2. The loss is for a 1 mm long transmission line whereas, in actual applications, the die-to-die channel length is 3-5 mm. Fig. 26, subpanel C shows a Far-end crosstalk in 1 μm stripline with Parylene-HT and SiO2 as dielectric. Fig. 26, subpanel D shows Near-end crosstalk in 1 μm stripline with Parylene-HT and SiO_2 as dielectric.

[0285] Fig 27 shows schematic used to analyze the reflection loss in 1 μm stripline with Parylene-HT and SiO_2 as dielectric. Fig. 27 also shows simulated stripline parameters for SiO_2 and Parylene-HT. In this analysis, a coupled stripline transmission line of length 1 mm was analyzed using a channel simulation.

[0286] For the simulation of eye diagrams, a PRBS input source was used for a rise time of 10 ps, with V_{high} of 1V. The connector was terminated at 50 to minimize reflection loss.

[0287] A crosstalk driver was used that models both synchronous and random crosstalk which inherited properties from the source. A threshold value of 20% of the V_{high} was used to determine eye-closure. At 25 Gbps, the eye-height for the SiO_2 is below 0.8V while Parylene-HT is at 0.84V. This suggests that there is potential to signal at higher data rates when we use an ultra-low D_k material. Fig. 25 shows the simulated eye diagrams at data rate = 25 Gbps, rise time = 10 ps, BER = $1e^{-12}$. Fig. 25 also compares the various eye parameters obtained for SiO2 and Parylene-HT.

[0288] To summarize, the crosstalk between coupled striplines was simulated. Analysis of the eye diagrams was carried out to determine the maximum data rate possible for Parylene-HT and SiO2. The results indicate that there is a significant reduction in crosstalk with a lower dielectric constant as compared to SiO_2. These losses and crosstalk are expected to increase with longer routing wires. The maximum data rate for signaling using Parylene-HT was estimated to be around 25 Gbps which overcomes the limitations faced by conventional high-d_k epoxy and BEOL alternatives. This study highlighted the benefits of using ULK dielectrics for high-bandwidth computing applications.

[0289] **Discussion**

[0290] Conventional polymer dielectrics used in package substrates induce thermal and curing stresses on the wafer/panel substrates. Vapor deposition of polymers with spontaneous curing on substrates at ambient conditions reduces the thermal and curing

stresses, thereby improving the ease of processing. Lower stresses also lead to lower warpage and improved thermomechanical reliability of package substrates. This enables larger body size package substrates for heterogeneous integration.

[0291] The example embodiments of the present disclosure described herein include the vapor deposition of polymers with spontaneous polymerization on substrates at ambient conditions reduces the thermal and curing stresses, thereby improving the ease of processing. Lower stresses also lead to lower warpage and improved thermomechanical reliability of package substrates. This enables larger body size package substrates for heterogeneous integration.

[0292] The exemplary system and method can include multiple benefits, including (i) capabilities to work with larger panel and body sizes possible with lower stresses and warpage, (ii) providing lower D_k as compared to inorganic dielectrics leading to lower capacitive losses, (iii) providing lower temperature processing compared to inorganic dielectrics, (iv) employing fewer thermal processing steps reduce the manufacturing costs, (v) being scalable to large panel formats, and (vi) providing thinner dielectric layers and overall thinner package substrates compared to traditional polymer-based package substrates.

[0293] In some embodiments of the present disclosure, the device includes a polymer dielectric deposited on a large wafer/panel package substrate such that it polymerizes on the substrate during the application/deposition so that further curing of the polymer is unnecessary. The deposition/polymerization may take place at ambient temperatures, leading to minimal/zero thermal stresses.

[0294] Fig. 25A shows an example conventional semi-additive process flow, e.g., used in package substrates, using vacuum lamination or liquid spin coating. Conventional vapor deposition pressures typically are $<10^{-5}$ Torr. As shown in Fig. 10, the polymer dielectrics are cured as a part of the application process – the curing can induce stresses in the substrate due to curing shrinkage associated with these dielectrics. The shrinkages can occur due to the presence of solvent in these dielectrics. The curing stresses thus can cause warping of the substrates, especially when the panel sizes or package/substrate sizes are considerably large. Conventional polymer dielectrics often can be cured before undergoing any further processing due to the inadequate mechanical stability of uncured dielectrics. The trend in semiconductor packaging is towards larger body/package/substrate sizes. Therefore, low-stress polymer dielectrics can be used for large body/package/substrate sizes with minimum warpage. Fig. 25B also shows size effects associated with larger and thinner wafers that can aggravate wafer warpage.

[0295] The curing processes can add significant costs to the conventional package substrates due to the multiple curing steps required for each layer of dielectric. Curing stresses can also cause cracking of fragile substrate materials such as glass. In contrast, the exemplary spontaneous polymerization reduces the chances of such cracking due to zero curing stresses.

[0296] Free-standing parylene films are also available in the market. These free-standing films can be applied to the substrates by applying heat and pressure and they would not require curing. However, these films won't adhere well to the substrate. Additionally, they won't be able to flow and fill the fine spaces between high-density wiring and micro-scale interconnect structures.

[0297] In contrast, the exemplary system and method In some embodiments of the present disclosure, the device includes a package substrate with multiple polymer and metal layers where polymer build-up layers are deposited on a substrate in such a way that the polymer polymerizes on the substrate during deposition.

[0298] **Conclusion**

[0299] Although example embodiments of the present disclosure are explained in some instances in detail herein, it is to be understood that other embodiments are contemplated. Accordingly, it is not intended that the present disclosure be limited in its scope to the details of construction and arrangement of components set forth in the following description or illustrated in the drawings. The present disclosure is capable of other embodiments and of being practiced or carried out in various ways.

[0300] In some embodiments, embodiments of the present disclosure can include a glass wafer or panel substrate with a polymer dielectric applied in such a way that the dielectric polymerizes on the glass substrate during deposition.

[0301] The exemplary system and method can be employed for packaged semiconductor devices that can be used in computing applications. As some non-limiting examples, embodiments of the present disclosure can be used for large semiconductor wafers configured for high-performance computing (e.g., data centers, artificial intelligence, 5G, mm-wave, base stations).

[0302] In some embodiments of the present disclosure, the package substrate can include a polymer dielectric as described herein conformally deposited onto the various RF components, followed by the deposition of a thin layer of a conductive material, metal, high-k dielectric and/or a composite for electromagnetic interference shielding.

[0303] It must also be noted that, as used in the specification and the appended claims, the singular forms "a," "an," and "the" include plural referents unless the context clearly dictates otherwise. Ranges may be expressed herein as from "about" or "approximately" one particular value and/or to "about" or "approximately" another particular value. When such a range is expressed, other exemplary embodiments include from the one particular value and/or to the other particular value.

[0304] By "comprising" or "containing" or "including" is meant that at least the name compound, element, particle, or method step is present in the composition or article or method, but does not exclude the presence of other compounds, materials, particles, method steps, even if the other such compounds, material, particles, method steps have the same function as what is named.

[0305] In describing example embodiments, terminology will be resorted to for the sake of clarity. It is intended that each term contemplates its broadest meaning as understood by those skilled in the art and includes all technical equivalents that operate in a similar manner to accomplish a similar purpose. It is also to be understood that the mention of one or more steps of a method does not preclude the presence of additional method steps or intervening method steps between those steps expressly identified. Steps of a method may be performed in a different order than those described herein without departing from the scope of the present disclosure. Similarly, it is also to be understood that the mention of one or more components in a device or system does not preclude the presence of additional components or intervening components between those components expressly identified.

[0306] The term "about," as used herein, means approximately, in the region of, roughly, or around. When the term "about" is used in conjunction with a numerical range, it modifies that range by extending the boundaries above and below the numerical values set forth. In general, the term "about" is used herein to modify a numerical value above and below the stated value by a variance of 10%. In one aspect, the term "about" means plus or minus 10% of the numerical value of the number with which it is being used. Therefore, about 50% means in the range of 45%-55%. Numerical ranges recited herein by endpoints include all numbers and fractions subsumed within that range (e.g., 1 to 5 includes 1, 1.5, 2, 2.75, 3, 3.90, 4, 4.24, and 5).

[0307] Similarly, numerical ranges recited herein by endpoints include subranges subsumed within that range (e.g., 1 to 5 includes 1-1.5, 1.5-2, 2-2.75, 2.75-3, 3-3.90, 3.90-4, 4-4.24, 4.24-5, 2-5, 3-5, 1-4, and 2-4). It is also to be understood that all numbers and fractions thereof are presumed to be modified by the term "about."

[0308] Unless otherwise expressly stated, it is in no way intended that any method set forth herein be construed as requiring that its steps be performed in a specific order. Accordingly, where a method claim does not actually recite an order to be followed by its steps or it is not otherwise specifically stated in the claims or descriptions that the steps are to be limited to a specific order, it is no way intended that an order be inferred, in any respect. This holds for any possible non-express basis for interpretation, including: matters of logic with respect to arrangement of steps or operational flow; plain meaning derived from grammatical organization or punctuation; the number or type of embodiments described in the specification.

[0309] While the methods and systems have been described in connection with certain embodiments and specific examples, it is not intended that the scope be limited to the particular embodiments set forth, as the embodiments herein are intended in all respects to be illustrative rather than restrictive.

[0310] The following patents, applications, and publications, as listed below and throughout this document, are hereby incorporated by reference in their entirety herein.

References

[1] R. Tummala, B. Deprospo, S. Dwarakanath, S. Ravichandran, P. Nimbalkar, N. Nedumthakady, and M. Swaminathan, "Glass panel packaging, as the most leadingedge packaging: Technologies and applications," in 2020 Pan Pacific Microelectronics Symposium (Pan Pacific), 2020, pp. 1-5.

[2] C. Nair, "Modeling, design, materials, processes and reliability of multi-layer redistribution wiring layers on glass substrates for next generation of high-performance computing applications," Ph.D. dissertation, Georgia Institute of Technology, 2019.

[3] B. DeProspo, "Modeling, design and demonstration of 1 m wide low resistance panel redistribution layer technology for high performance computing applications," Ph.D. dissertation, Georgia Institute of Technology, 2020.

[4] D. Opp, D. Skinner, and R. Wiktorek, "A model for polymer fatigue," Polymer Engineering & Science, vol. 9, no. 2, pp. 121-130, 1969.

[5] J. Williams, "A model of fatigue crack growth in polymers," Journal of Materials Science, vol. 12, no. 12, pp. 2525-2533, 1977.

[6] H. F. Mark, Encyclopedia of polymer science and technology, concise. John Wiley & Sons, 2013.

[7] R. W. Hertzberg, H. Nordberg, and J. Manson, "Fatigue crack propagation in polymeric materials," Journal of Materials Science, vol. 5, no. 6, pp. 521-526, 1970.

[8] J. Sauer and G. Richardson, "Fatigue of polymers," International journal of fracture, vol. 16, no. 6, pp. 499-532, 1980.

[9] J. Sauer and M. Hara, "Effect of molecular variables on crazing and fatigue of polymers," in Crazing in Polymers Vol. 2, Springer, 1990, pp. 69-118.

[10] S. Hegde, R. V. Pucha, and S. K. Sitaraman, "Enhanced reliability of high density wiring (hdw) substrates through new dielectric and base substrate materials," in ASME International Mechanical Engineering Congress and Exposition, vol. 36487, 2002, pp. 283-290.

[11] S. Mahalingam, S. Hegde, G. Ramakrishna, R. V. Pucha, and S. K. Sitaraman, "Material interaction effects in the reliability of high density interconnect (hdi) boards," in ASME International Mechanical Engineering Congress and Exposition, vol. 37149, 2003, pp. 165-170.

[12] S. Mahalingam, S. Hegde, J. Ahmad, R. V. Pucha, V. Sundaram, F. Liu, G. White, R. Tummala, and S. K. Sitaraman, "Materials, processes and reliability of mixedsignal substrates for sop technology," in 2004 Proceedings. 54th Electronic Components and Technology Conference (IEEE Cat. No. 04CH37546), IEEE, vol. 2, 2004, pp. 1630-1635.

[13] S. S. Manson, Behavior of materials under conditions of thermal stress. National Advisory Committee for Aeronautics, 1953, vol. 2933.

[14] S. S. Manson and T. Dolan, Thermal stress and low cycle fatigue, 1966.

[15] W. Engelmaier, "Fatigue life of leadless chip carrier solder joints during power cycling," IEEE transactions on components, hybrids, and manufacturing technology, vol. 6, no. 3, pp. 232-237, 1983.

[16] K. Yamanaka, T. Fujisaki, M. Ichinose, and T. Ooyoshi, "Effect of geometry and dielectric material on thermo-mechanical strain on micro-vias in build-up substrates," Journal of Materials Science: Materials in Electronics, vol. 21, no. 9, pp. 943-949, 2010.

[17] G. Ramakrishna, F. Liu, and S. Sitaraman, "Experimental and numerical investigation of microvia reliability," in ITherm 2002. Eighth Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (Cat. No. 02CH37258), IEEE, 2002, pp. 932-939.

[18] F. Su, R. Mao, J. Xiong, K. Zhou, Z. Zhang, J. Shao, and C. Xie, "On thermomechanical reliability of plated-through-hole (pth)," Microelectronics Reliability, vol. 52, no. 6, pp. 1189-1196, 2012.

[19] G. Ramakrishna, F. Liu, and S. K. Sitaraman, "Role of dielectric material and geometry on the thermo-mechanical reliability of microvias," in 52nd Electronic Components and Technology Conference 2002.(Cat. No. 02CH37345), IEEE, 2002, pp. 439 – 445.

[20] S. Mahalingam, S. Hegde, G. Ramakrishna, R. V. Pucha, and S. K. Sitaraman, "Material interaction effects in the reliability of high density interconnect (hdi) boards," in ASME International Mechanical Engineering Congress and Exposition, vol. 37149, 2003, pp. 165-170.

[21] Y. Ning, M. H. Azarian, and M. Pecht, "Influence of plating quality on reliability of microvias," IPC APEX Expo, 2015.

[22] P. Nimbalkar, F. Liu, A. Watanabe, D. Weyers, M. Kathaperumal, C. P. Lin, F. Naohito, T. Makita, N. Watanabe, A. Kubo, M. Swaminathan, and R. Tummala, "Fabrication and reliability demonstration of 5 m redistribution layer using lowstress dielectric dry film," in 2020 IEEE 70th Electronic Components and Technology Conference (ECTC), 2020, pp. 62-67.

[23] D. Kovach, N. Amirgulyan, C.-P. CHIEN, and M. Tanielian, "Minimizing stress in cu/polyimide processes for large format mcm manufacturing," The International journal of microcircuits and electronic packaging, vol. 23, no. 1, pp. 70-77, 2000.

[24] S. Chen, C. Yang, F. Faupel, and P. Ho, "Stress relaxation during thermal cycling in metal/polyimide layered films," Journal of applied physics, vol. 64, no. 12, pp. 6690-6698, 1988.

[25] S. Lagrange, S. Brongersma, M. Judelewicz, A. Saerens, I. Vervoort, E. Richard, R. Palmans, and K. Maex, "Self-annealing characterization of electroplated copper films," Microelectronic Engineering, vol. 50, no. 1-4, pp. 449-457, 2000.

[26] T. Hara, H. Toida, and Y. Shimura, "The self-annealing phenomenon in copper interconnection," Electrochemical and Solid State Letters, vol. 6, no. 7, G98, 2003.

[27] H. Matsuyama, T. Suzuki, T. Nakamura, M. Shiozu, H. Ehara, M. Oshima, T. Soeda, H. Hosoi, and K. Yamabe, "Voiding generation in copper interconnect under room temperature storage in 12 years," Japanese Journal of Applied Physics, vol. 56, no. 7S2, 07KG01, 2017.

[28] H. Matsuyama, T. Suzuki, M. Shiozu, H. Ehara, T. Soeda, H. Hosoi, M. Oshima, and K. Yamabe, "Verification of copper stress migration under low temperature long time stress," in 2019 IEEE International Reliability Physics Symposium (IRPS), IEEE, 2019, pp. 1-5.

[29] C. Zhu, W. Ning, G. Xu, and L. Luo, "Stress evolution during thermal cycling of copper/polyimide layered structures," Materials science in semiconductor processing, vol. 27, pp. 819-826, 2014.

[30] M. Horiuchi, T. Yamasaki, and Y. Shimizu, "Metallization technologies on a smooth resin surface for the next generation of flip chip packaging," Transactions of The Japan Institute of Electronics Packaging, vol. 3, no. 1, pp. 110-115, 2010.

[31] K. Inoue, K. Matsui, M. Watanabe, and H. Honma, "Surface modification of polyimide using uv light and formation of circuit patterns," Journal of The Surface Finishing Society of Japan, vol. 59, no. 1, pp. 47-47, 2008.

[32] Y. Oh, E. J. Kim, Y. Kim, K. Choi, W. B. Han, H.-S. Kim, and C. S. Yoon, "Adhesion of sputter-deposited cu/ti film on plasma-treated polymer substrate," Thin Solid Films, vol. 600, pp. 90-97, 2016.

[33] J. F. Friedrich, I. Koprinarov, R. Giebler, A. Lippitz, and W. E. S. Unger, "Reactions and intermediates at the metal-polymer interface as observed by xps and nexafs spectroscopy," The Journal of Adhesion, vol. 71, no. 2-3, pp. 297-321, 1999. eprint: https://doi.org/10.1080/00218469908014853.

[34] S. H. Kim, S. W. Na, N.-E. Lee, Y. W. Nam, and Y.-H. Kim, "Effect of surface roughness on the adhesion properties of cu/cr films on polyimide substrate treated by inductively coupled oxygen plasma," Surface and Coatings Technology, vol. 200, no. 7, pp. 2072-2079, 2005.

[35] S. H. Kim, S. H. Cho, N.-E. Lee, H. M. Kim, Y. W. Nam, and Y.-H. Kim, "Adhesion properties of cu/cr films on polyimide substrate treated by dielectric barrier discharge plasma," Surface and Coatings Technology, vol. 193, no. 1, pp. 101-106, 2005, Asian-European International Conference on Plasma Surface Engineering 2003.

[36] K. W. Paik, H. S. Cole, R. J. Saia, and J. J. Chera, "Studies on metal/benzocyclobutene (bcb) interface and adhesion," Journal of Adhesion Science and Technology, vol. 7, no. 5, pp. 403-415, 1993. eprint: https://doi.org/10.1163/156856193X00295.

[37] S. Freilich and F. Ohuchi, "Reactions at the polyimide-metal interface," Polymer, vol. 28, no. 11, pp. 1908-1914, 1987.

[38] F. S. Ohuchi and S. C. Freilich, "Metal polyimide interface: A titanium reaction mechanism," Journal of Vacuum Science & Technology A, vol. 4, no. 3, pp. 10391045, 1986. eprint: https://doi.org/10.1116/1.573450.

[39] J. M. Burkstrand, "Metal-polymer interfaces: Adhesion and x-ray photoemission studies," Journal of Applied Physics, vol. 52, no. 7, pp. 4795-4800, 1981. eprint: https://doi.org/10.1063/1.329320.

[40] K. L. Mittal, "Adhesion aspects of metallization of organic polymer surfaces," Journal of Vacuum Science and Technology, vol. 13, no. 1, pp. 19-25, 1976. eprint: https://doi.org/10.1116/1.568850.

[41] Y. Nakamura, Y. Suzuki, and Y. Watanabe, "Effect of oxygen plasma etching on adhesion between polyimide films and metal," Thin Solid Films, vol. 290-291, pp. 367-369, 1996, Papers presented at the 23rd International Conference on Metallurgical Coatings and Thin Films.

[42] S. B. Lee and Y.-K. Kim, "Adhesion improvement of polyimide/metal interface by he/o2/nf3 atmospheric pressure plasma," Plasma Processes and Polymers, vol. 6, no. S1, S525-S529, 2009. eprint: https://onlinelibrary.wiley.com/doi/pdf/10.1002/ ppap. 200931111.

[43] T. P. Nguyen, A. Lahmar, and P. Jonnard, "Adhesion improvement of poly(phenylenevinylene) substrates induced by argon-oxygen plasma treatment," The Journal of Adhesion, vol. 66, no. 1-4, pp. 303-317, 1998. eprint: https://doi.org/10.1080/ 00218469808009971.

[44] F. D. Egitto and L. J. Matienzo, "Plasma modification of polymer surfaces for adhesion improvement," IBM Journal of Research and Development, vol. 38, no. 4, pp. 423-439, 1994.

[45] M. M. R. Howlader, T. Suga, A. Takahashi, K. Saijo, S. Ozawa, and K. Nanbu, "Surface activated bonding of lcp/cu for electronic packaging," Journal of Materials Science, vol. 40, pp. 3177-3184, 2005.

[46] F. Faupel, V. Zaporojtchenko, A. Thran, T. Strunskus, and M. Kiene, "7 - metal diffusion in polymers and on polymer surfaces," in Diffusion Processes in Advanced Technological Materials, D. Gupta, Ed., Norwich, NY: William Andrew Publishing, 2005, pp. 333-363, ISBN: 978-0-8155-1501-2.

[47] F. Faupel, R. Willecke, and A. Thran, "Diffusion of metals in polymers," Materials Science and Engineering: R: Reports, vol. 22, no. 1, pp. 1-55, 1998.

[48] J. H. Das and J. E. Morris, "Metal diffusion in polymers," IEEE Transactions on Components, Packaging, and Manufacturing Technology: Part B, vol. 17, no. 4, pp. 620-625, 1994.

[49] H. Kudo, T. Takano, M. Tanaka, R. Kasai, J. Suyama, M. Akazawa, M. Takeda, H. Mawatari, T. Sasao, Y. Okazaki, et al., "A characterized redistribution layer architecture for advanced packaging technologies," in 2016 IEEE 66th Electronic Components and Technology Conference (ECTC), IEEE, 2016, pp. 2063-2067.

[50] D. Okamoto, Y. Shibasaki, D. Shibata, T. Hanada, F. Liu, M. Kathaperumal, and R. R. Tummala, "Fabrication and reliability demonstration of 3μm diameter photo vias at 15μm pitch in thin photosensitive dielectric dry film for 2.5 d glass interposer applications," in 2019 IEEE 69th Electronic Components and Technology Conference (ECTC), IEEE, 2019, pp. 2112-2116.

[51] C. Nair, B. DeProspo, H. Hichri, M. Arendt, F. Liu, V. Sundaram, and R. Tummala, "Reliability studies of excimer laser-ablated microvias below 5 micron diameter in dry film polymer dielectrics for next generation, panel-scale 2.5 d interposer rdl," in 2018 IEEE 68th Electronic Components and Technology Conference (ECTC), IEEE, 2018, pp. 1005-1009.

[52] Y. Oka and N. Koizumi, "Effects of impurity ions on electrical properties of poly (vinylidene fluoride)," Polymer Journal, vol. 14, no. 11, pp. 869-876, 1982.

[53] M. Egginger and R. Schwoediauer, "Analysis of mobile ionic impurities in polyvinylalcohol thin films by thermal discharge current and dielectric impedance spectroscopy," AIP Advances, vol. 2, no. 4, p. 042 152, 2012.

[54] E. Bumiller and C. Hillman, "A review of models for time-to-failure due to metallic migration mechanisms," in White paper issued by DfR Solutions, 2009.

[55] D. Lambert, R. Gannamani, and R. Blish, "Dendrite fuse re-growth kinetics on organic substrates for microprocessors," in 2004 IEEE International Reliability Physics Symposium. Proceedings, IEEE, 2004, pp. 543-546.

[56] S.-A. Kim, D.-S. Ahn, Y.-H. Eum, D.-H. Kim, and Y.-B. Kim, "Case study of copper dendrite growth under hast test," in 2008 15th International Symposium on the Physical and Failure Analysis of Integrated Circuits, IEEE, 2008, pp. 1-3.

[57] D. S. Peck, "Comprehensive model for humidity testing correlation," in 24th International Reliability Physics Symposium, IEEE, 1986, pp. 44-50.

[58] G. DiGiacomo, "Metal migration (ag, cu, pb) in encapsulated modules and timeto-fail model as a function of the environment and package properties," in 20th International Reliability Physics Symposium, IEEE, 1982, pp. 27-33.

[59] Polymer-Database. (2022). "Dielectric strength of polymers."

[60] C.-K. Hu, L. Gignac, E. Liniger, B. Herbst, D. Rath, S. Chen, S. Kaldor, A. Simon, and W.-T. Tseng, "Comparison of cu electromigration lifetime in cu interconnects coated with various caps," Applied Physics Letters, vol. 83, no. 5, pp. 869-871, 2003.

[61] C.-K. Hu, D. Canaperi, S. Chen, L. Gignac, B. Herbst, S. Kaldor, M. Krishnan, E. Liniger, D. Rath, D. Restaino, et al., "Effects of overlayers on electromigration reliability improvement for cu/low k interconnects," in 2004 IEEE International Reliability Physics Symposium. Proceedings, IEEE, 2004, pp. 222-228.

[62] H. Ono, T. Nakano, and T. Ohta, "Diffusion barrier effects of transition metals for cu/m/si multilayers (m = cr, ti, nb, mo, ta, w)," Applied Physics Letters, vol. 64, no. 12, pp. 1511-1513, 1994.

[63] T. Kanki, J. Ikeda, Y. Kobayashi, S. Suda, Y. Nakata, and T. Nakamura, "Development of highly reliable cu wiring of $1/s = 1/1\mu m$ for chip to chip interconnection," in 2012 IEEE International Interconnect Technology Conference, IEEE, 2012, pp. 13 .

[64] Scs parylene properties, Specialty Coating Systems (SCS), 2016.

[65] A. Pizzagalli, "Lithography technology and trends for advanced packaging," in 2016 China Semiconductor Technology International Conference (CSTIC), IEEE, 2016, pp. 1-3.

[66] M. Lapedus, Lithography challenges for fan-out.

[67] M. Griot, "Introduction to laser technology," Technical Guide, pp. 10-6, 2009.

[68] B. Matuskova, B. Považay, R. Holly, F. Bügelsack, T. Zenger, T. Uhrmann, and B. Thallner, "Maskless lithography optimized for heterogeneous and chiplet integration," in 2020 International Wafer Level Packaging Conference (IWLPC), IEEE, 2020, pp. $01 - 06$.

[69] P. Nimbalkar, P. Bhaskar, C. Blancher, M. Kathaperumal, M. Swaminathan, and R. Tummala, "Novel zero side-etch process for; $1\mu m$ package redistribution layers," in 2022 IEEE 72nd Electronic Components and Technology Conference (ECTC), IEEE, 2022, pp. 2168-2173.

[70] R. Iannuzzelli, "Predicting plated-through-hole reliability in high temperature manufacturing processes," in 1991 Proceedings 41st Electronic Components & Technology Conference, IEEE, 1991, pp. 410-421.

[71] P. Nimbalkar, M. Kathaperumal, F. Liu, M. Swaminathan, and R. Tummala, "Reliability modeling of micro-vias in high-density redistribution layers," in 2021 IEEE 71st Electronic Components and Technology Conference (ECTC), 2021, pp. 983988 .

[72] P. Nimbalkar, C. Blancher, M. Kathaperumal, M. Swaminathan, and R. Tummala, "Effect of titanium-polymer interactions on adhesion of polymer-copper redistribution layers in advanced packaging," IEEE Transactions on Device and Materials Reliability, pp. 1-1, 2022.

[73] M. Du, R. Opila, and C. Case, "Interface formation between metals (cu, ti) and low dielectric constant organic polymer (flare ™1.0)," Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films, vol. 16, no. 1, pp. 155-162, 1998.

[74] Y. Nishimura, "Advanced insulating film for next-generation smartphone performance requirements," Presented at ECTC, 2019.

CLAIMS

What is claimed is:

1. A method of fabricating an interconnect, the method comprising:

formation of a metal layer on a base substrate;

formation of copper pillars on at least a portion of the first metal layer;

vaporizing a source material at a first temperature and a first pressure to form a vapor dimer of the source material;

heating the vapor dimer in an inert environment to a second temperature to form a vapor monomer at a second pressure, wherein the second temperature is higher than the first temperature, and wherein the second pressure is lower than the first pressure; and

introducing the vapor monomer to a chamber having a workpiece for an interconnect having an exposed surface and plurality of metal pillars to spontaneously deposit and polymerize the vapor monomer to form a first layer of a conformal layer of a polymer on at least the exposed surface of the workpiece and surrounding the plurality of metal pillars;

planarizing or over-planarizing the polymer to expose a plurality of top surfaces of the plurality of metal pillars;

forming additional metal layers, including a second metal layer having metal pillars, on the polymer and the exposed top surfaces of the plurality of metal pillars;

introducing additional vapor monomer to the chamber to spontaneously deposit and polymerize the additional vapor monomer to form an additional layer, including a second layer, of a conformal layer of the polymer on at least the second layer;

planarizing or over-planarizing the polymer of each of the additional layers, including the second layer, to expose respective top surfaces of the plurality of metal pillars of the additional metal layers; and

forming a top metal layer on a top polymer layer having the exposed plurality of top surfaces to form the interconnect.

2. The method of claim 1, comprising:

a) depositing a metal seed layer on a base substrate;

b) forming a first metal layer on the metal seed layer;

c) applying a layer of a photoresist on a top surface of the first metal layer and patterning the photoresist, followed by forming the plurality of metal pillars at predetermined locations on the first metal layer;

d) removing the photoresist layer and exposed portions of the metal seed layer;

e) conformally depositing an inorganic barrier layer on metal structures and exposed top surface portions of a base substrate to form the first layer;

f) conformally depositing an overburden layer of a polymer dielectric on the inorganic barrier layer and underlying metal structures;

g) planarizing or over-planarizing the polymer dielectric to expose the top surfaces of the plurality of metal pillars; and

h) forming a metal layer connected to the exposed top surfaces of the plurality of metal pillars.

3. The method of claim 1 or 2, wherein the metal seed layer is deposited on the base substrate using electroless, physical vapor deposition (PVD), chemical vapor deposition (CVD), or a sputtering process.

4. The method of claim 2, wherein the inorganic barrier layer is made from a material comprising SiO2, Si3N4, SiC, MgO, ZrO2, or tungsten nitride. SiOx, AlOx, SiNx, TiOx, TaNx, WNx, Ta, Ti where 'x' is the stoichiometric coefficient ranging from 0.01 to 10.

5. The method of claim 2, wherein the overburden layer of the polymer dielectric is formed by a spontaneous polymerization or chemical vapor deposition (CVD) process.

6. The method of claim 2, wherein the polymer dielectric is a poly-para-xylylene, an acrylic, an epoxy, a polyurethane, a silicone, a poly(tetrafluoroethylene), a polyimide, a fluoropolymer, or any combination thereof.

7. The method of claim 1, further comprising:

i) completing steps b) through h) again.

8. The method of claim 7, wherein steps f), g), h), and i) are completed more than one time.

9. A bridge die, an interposer, or a package substrate prepared by a process according to any one of claims 1-8.

10. An electronic device comprising a bridge die, an interposer, or a package substrate according to claim 9.

11. A device comprising:

a high-density interconnect wiring structure comprising:

high-density metal wiring, including a first wire and a second wire;

a dielectric layer formed between the first metal wire and the second metal wire, wherein the dielectric layer is conformally applied and spontaneously deposited.

12. The device of claim 11, wherein the high-density interconnect wiring structure has a high aspect ratio metal traces having its cross-sectional dimensions in a range from 0.1 micrometers to 100 micrometers

13. The device of claim 11 further comprising a plurality of metal pillars having a high aspect ratio metal traces having its cross-sectional dimensions in a range from 0.1 micrometers to 100 micrometers

14. The device of claim 13, wherein the plurality of pillars or high-density interconnect wiring structure are surrounded by a low-k dielectric material having a dielectric constant less than 3.

15. The device of any one of claims 1 - 14, wherein the ratio of (i) a height to width or (ii) a width to height has a range from 0.1 to 10.

16. The device of any one of claims 11 – 15, comprising:

one or more chips, chiplets, dies, devices, components, passive components, and/or active components,

wherein the one or more chips, chiplets, dies, devices, components, passive components, and/or active components are connected to another component by the first wire and the second wire.

17. The device of any one of claims 11 – 16, wherein the high-density interconnect wiring structure forms an asymmetric interconnect structure having multiple layers of polymer and metal disposed on to a base substrate on either side of the base substrate.

18. The device of any one of claims 11 – 17, wherein the metal wiring has an interface layer comprising roughened copper, roughened inorganic material, roughened organic material, or a combination thereof.

19. The device of any one of claims 11 – 18, wherein the metal wiring has an interface layer comprising nano-roughened copper, a silane coupling agent, siloxane or a chemical compound containing Si, O, H, C and organic molecule.

20. The device of claim 19, wherein the silane coupling agent comprises 3-Methacryloxypropyltrimethoxysilane.

21. The device of any one of claims 11 – 20, wherein the base substrate has an area having a percentage covered by metal of at least 10%.

22. The device of any one of claims 11 - 21, further comprising:

embedded substrate having cavities, including (i) a first cavity with a first depth value and (ii) a second cavity with a second depth value.

23. The device of any one of claims 11- 22, comprising a silane or siloxane coupling agent deposited on copper, polymer, dielectric, glass, substrate material or a combination of these.

24. The device of any one of claims 11 – 23, comprising:

metal pillars or underlying metal structures having an average variation in thickness or height in the range from 1% to 50%.

25. The device of claim 24, wherein the metal pillars are substantially perpendicular to the underlying metal layer.

26. The device of any one of claims 11 – 25, wherein the dielectric layer either (i) has a melting point higher than 250 °C or (ii) has a step coverage of at least 50%.

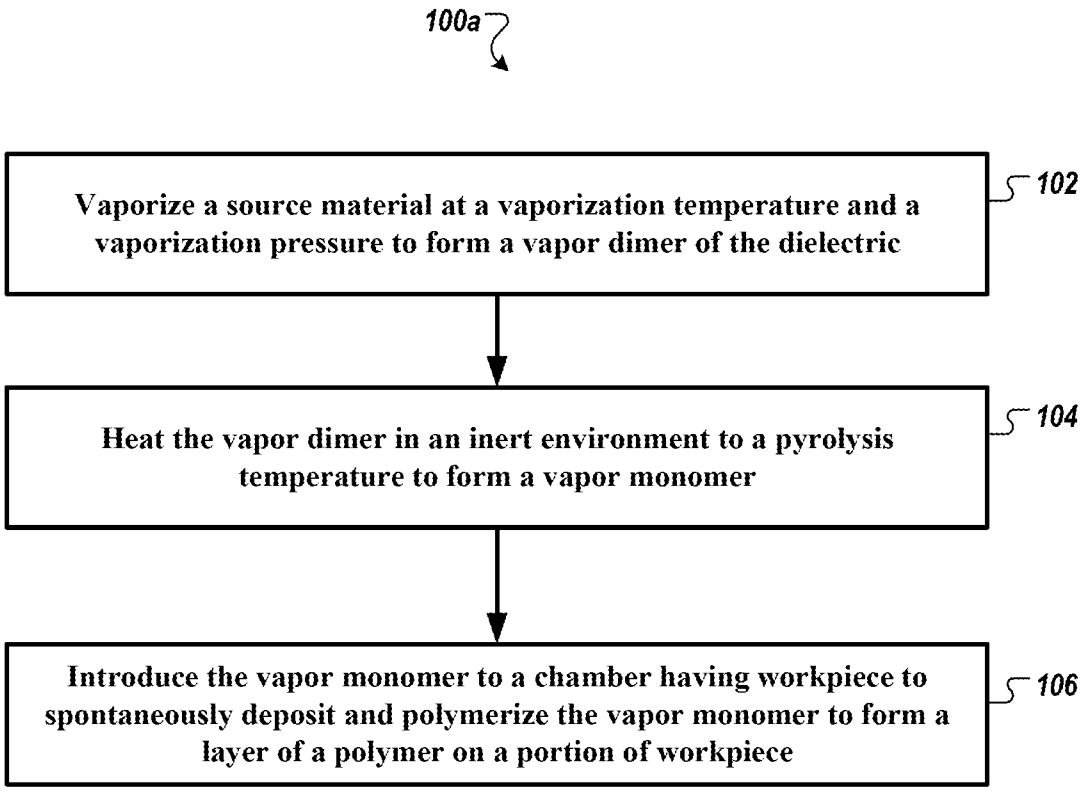

100a
Vaporize a source material at a vaporization temperature and a vaporization pressure to form a vapor dimer of the dielectric
102
Heat the vapor dimer in an inert environment to a pyrolysis temperature to form a vapor monomer
104
Introduce the vapor monomer to a chamber having workpiece to spontaneously deposit and polymerize the vapor monomer to form a layer of a polymer on a portion of workpiece
106

FIG. 1A

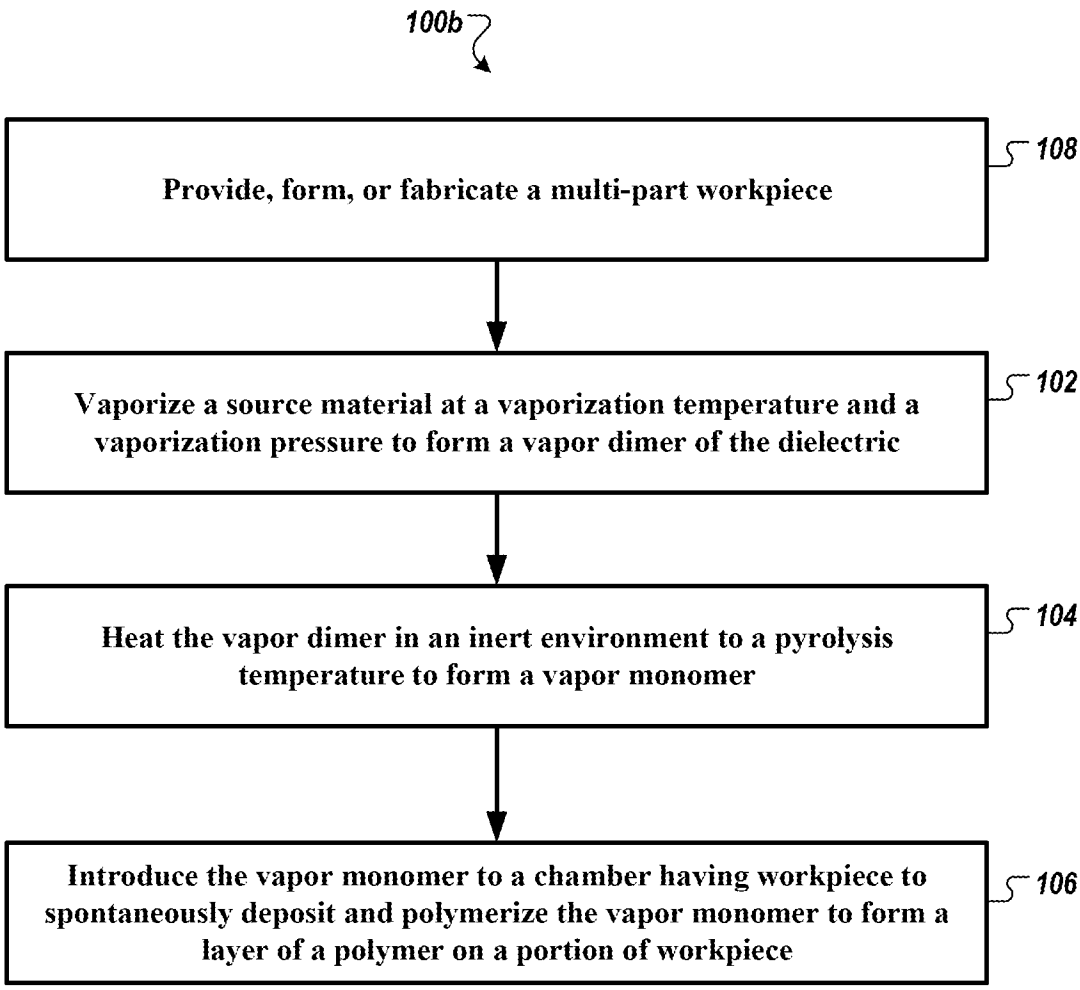

100b
Provide, form, or fabricate a multi-part workpiece
108
Vaporize a source material at a vaporization temperature and a vaporization pressure to form a vapor dimer of the dielectric
102
Heat the vapor dimer in an inert environment to a pyrolysis temperature to form a vapor monomer
104
Introduce the vapor monomer to a chamber having workpiece to spontaneously deposit and polymerize the vapor monomer to form a layer of a polymer on a portion of workpiece
106

FIG. 1B

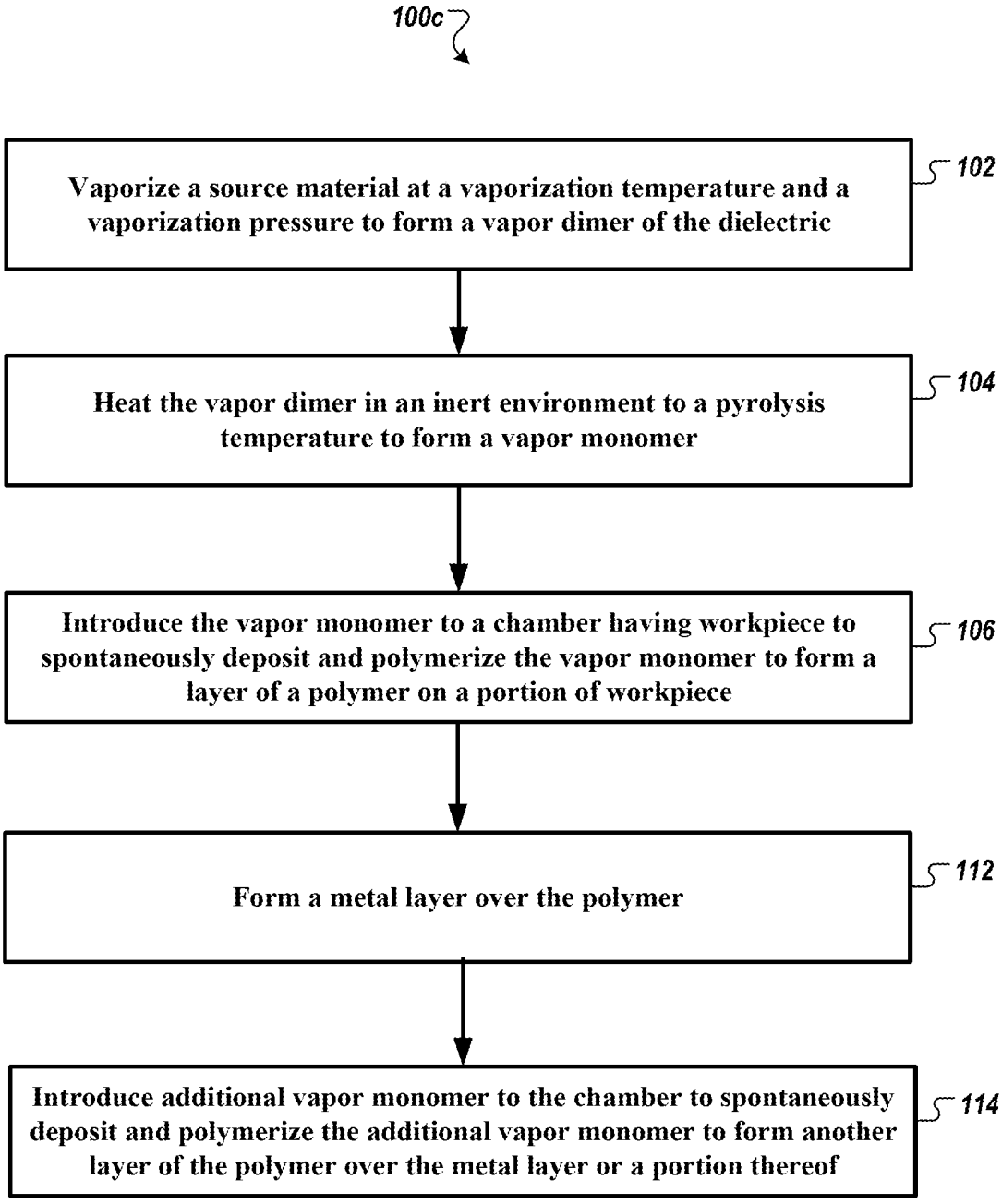

100c
Vaporize a source material at a vaporization temperature and a vaporization pressure to form a vapor dimer of the dielectric
102
Heat the vapor dimer in an inert environment to a pyrolysis temperature to form a vapor monomer
104
Introduce the vapor monomer to a chamber having workpiece to spontaneously deposit and polymerize the vapor monomer to form a layer of a polymer on a portion of workpiece
106
Form a metal layer over the polymer
112
Introduce additional vapor monomer to the chamber to spontaneously deposit and polymerize the additional vapor monomer to form another layer of the polymer over the metal layer or a portion thereof
114

FIG. 1C

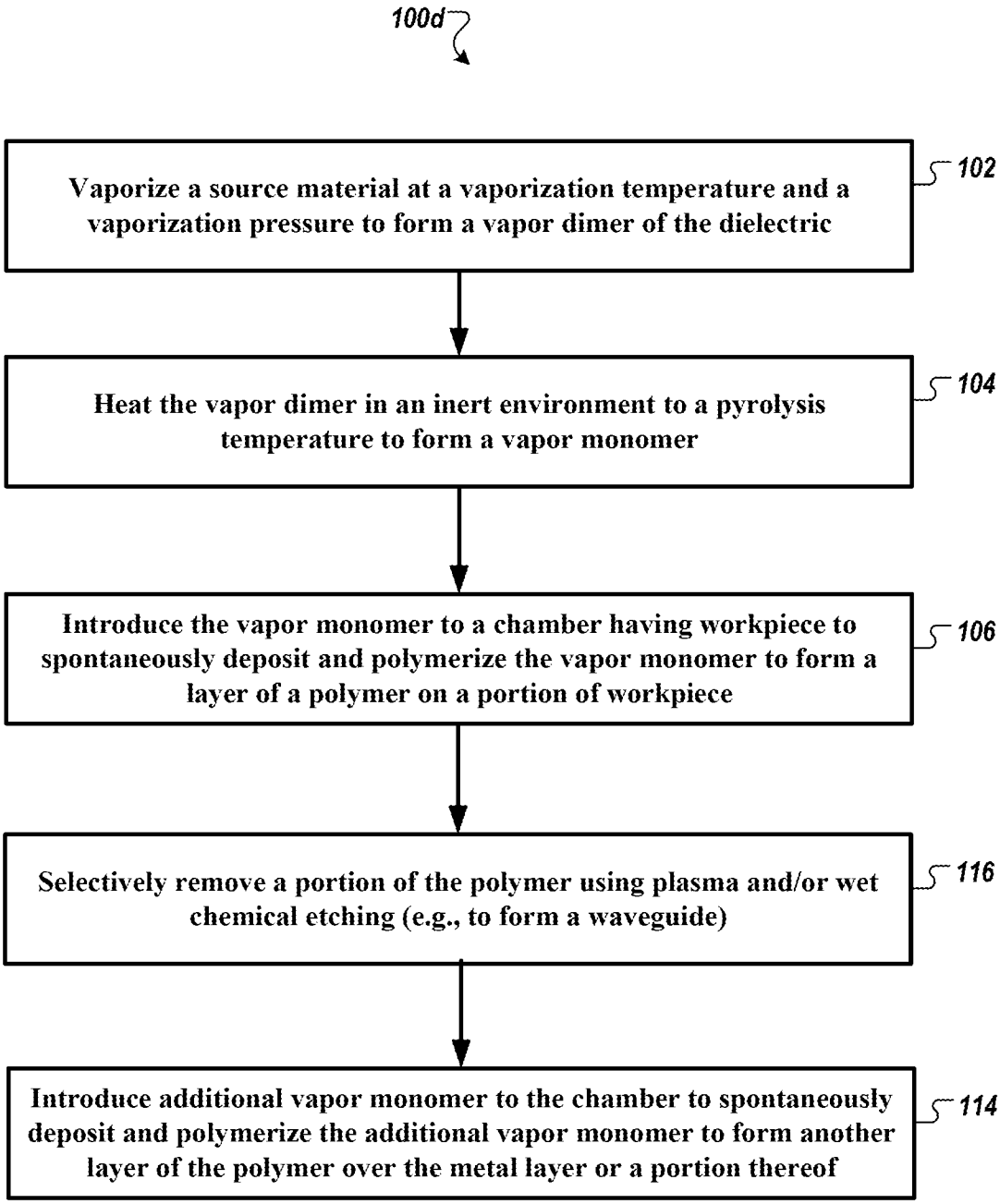

100d
Vaporize a source material at a vaporization temperature and a vaporization pressure to form a vapor dimer of the dielectric
102
Heat the vapor dimer in an inert environment to a pyrolysis temperature to form a vapor monomer
104
Introduce the vapor monomer to a chamber having workpiece to spontaneously deposit and polymerize the vapor monomer to form a layer of a polymer on a portion of workpiece
106
Selectively remove a portion of the polymer using plasma and/or wet chemical etching (e.g., to form a waveguide)
116
Introduce additional vapor monomer to the chamber to spontaneously deposit and polymerize the additional vapor monomer to form another layer of the polymer over the metal layer or a portion thereof
114

FIG. 1D

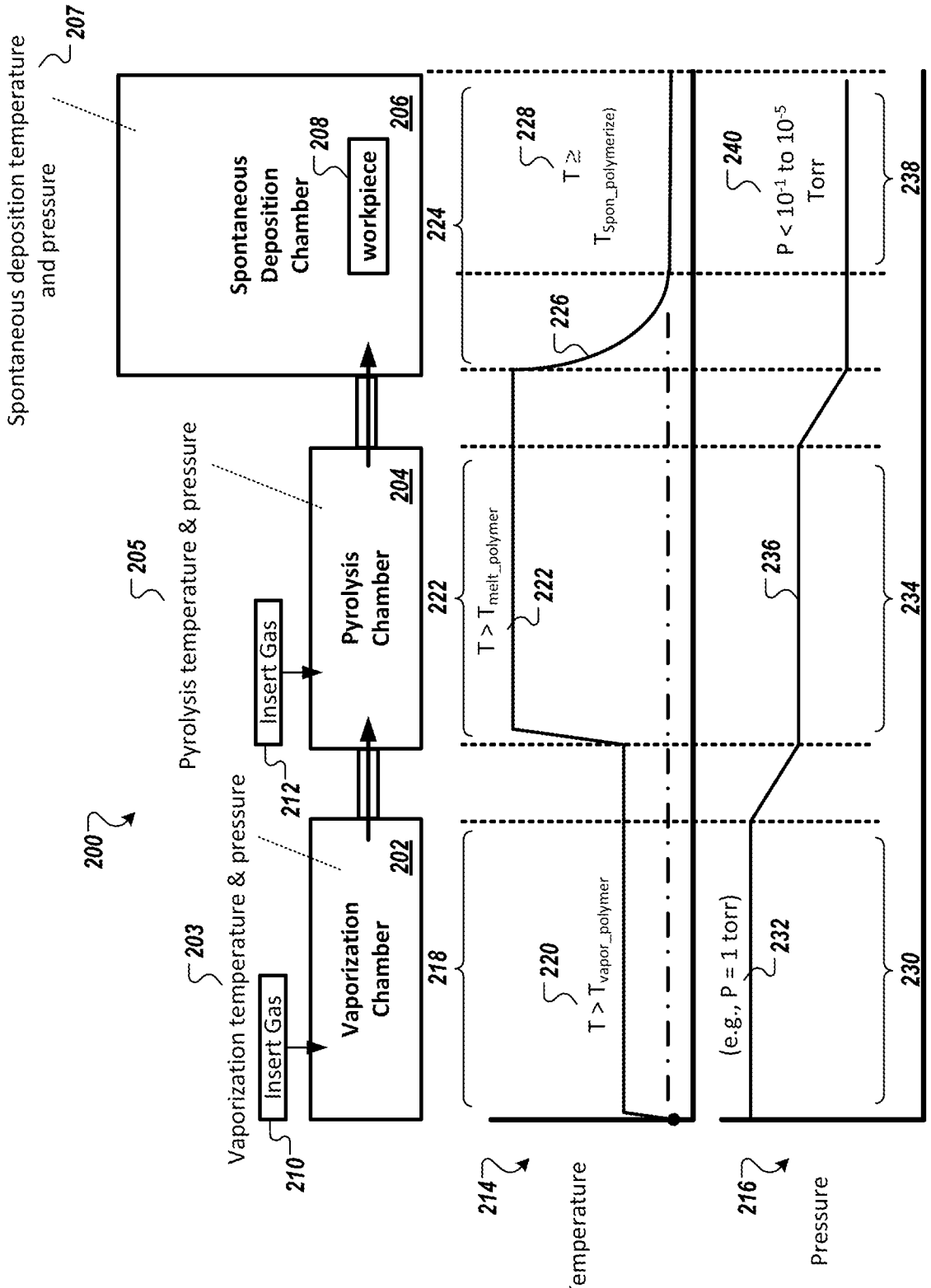

Spontaneous deposition temperature and pressure
207
Spontaneous Deposition Chamber
208
workpiece
206
Pyrolysis temperature & pressure
205
Pyrolysis Chamber
204
Insert Gas
212
Vaporization temperature & pressure
203
Vaporization Chamber
202
Insert Gas
210
200
224
228
T ≥ T_Spon_polymerize)
226
240
P < 10^-1 to 10^-5 Torr
238
222
T > T_melt_polymer
222
236
234
218
220
T > T_vapor_polymer
(e.g., P = 1 torr)
232
230
214
Temperature
216
Pressure

FIG. 2A

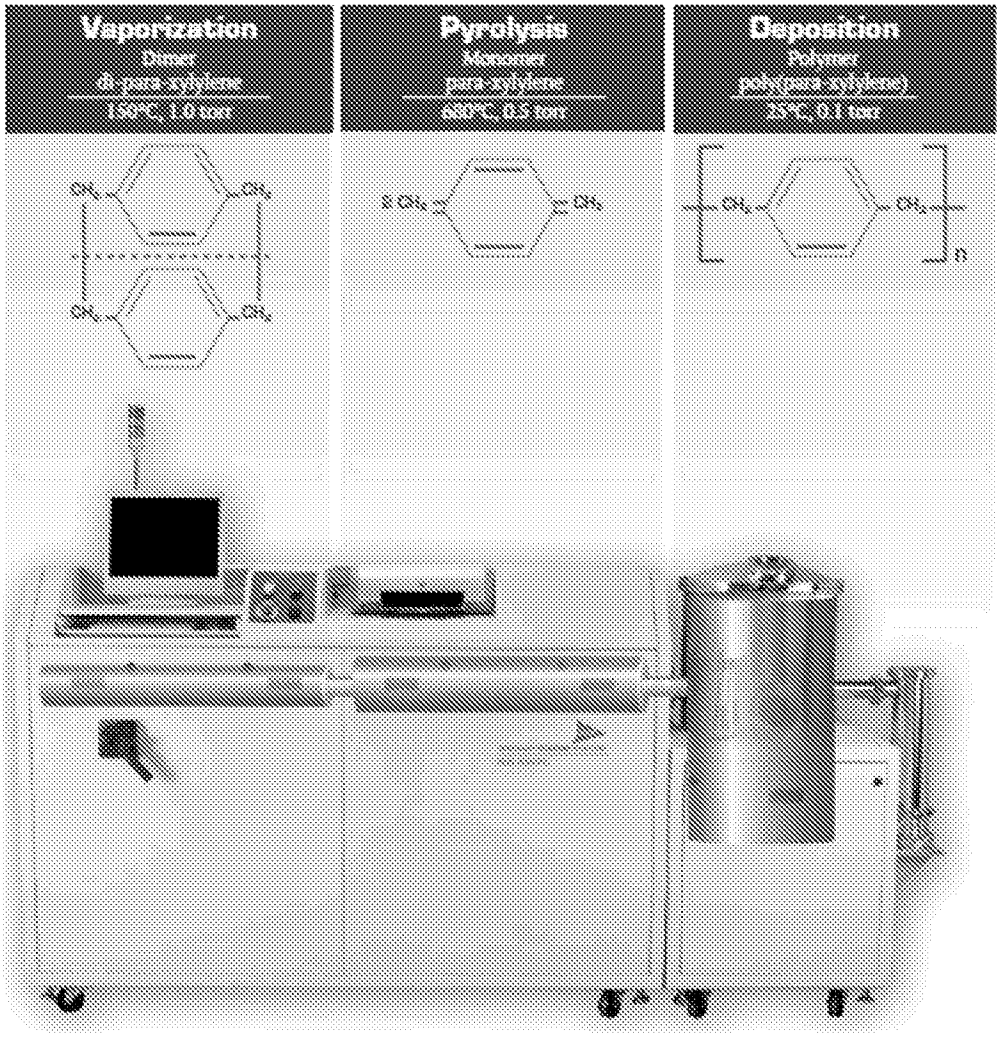

Vaporization
Dimer
di-para-xylylene
135°C, 1.0 torr
Pyrolysis
Monomer
para-xylylene
690°C, 0.5 torr
Deposition
Polymer
poly(para-xylylene)
25°C, 0.1 torr

FIG. 2B

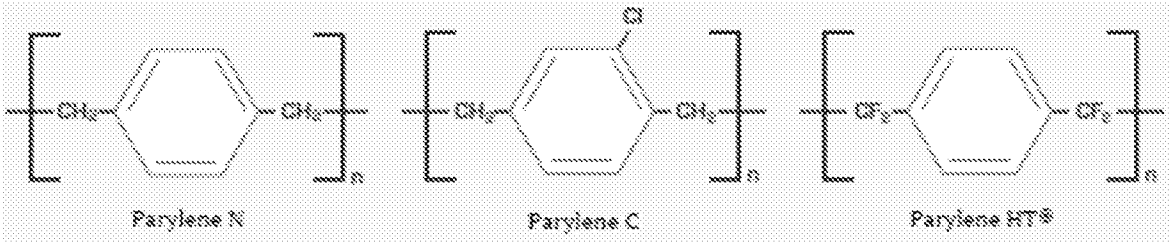

Parylene N
Parylene C
Parylene HT®

FIG. 2C

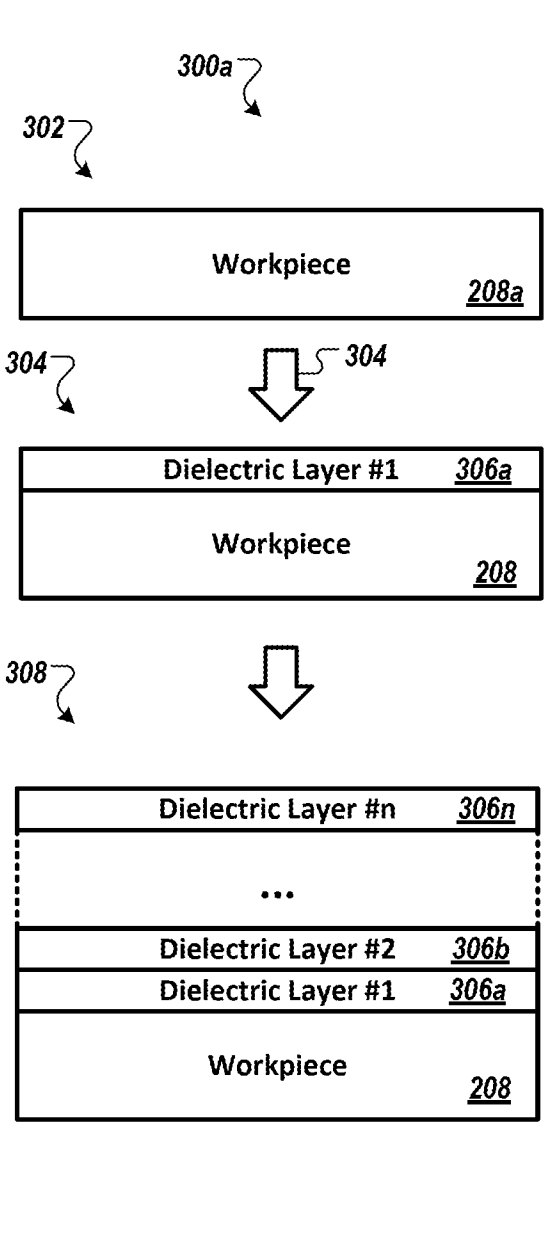

300a
302
Workpiece
208a
304
304
Dielectric Layer #1
306a
Workpiece
208
308
Dielectric Layer #n
306n
...
Dielectric Layer #2
306b
Dielectric Layer #1
306a
Workpiece
208

FIG. 3A

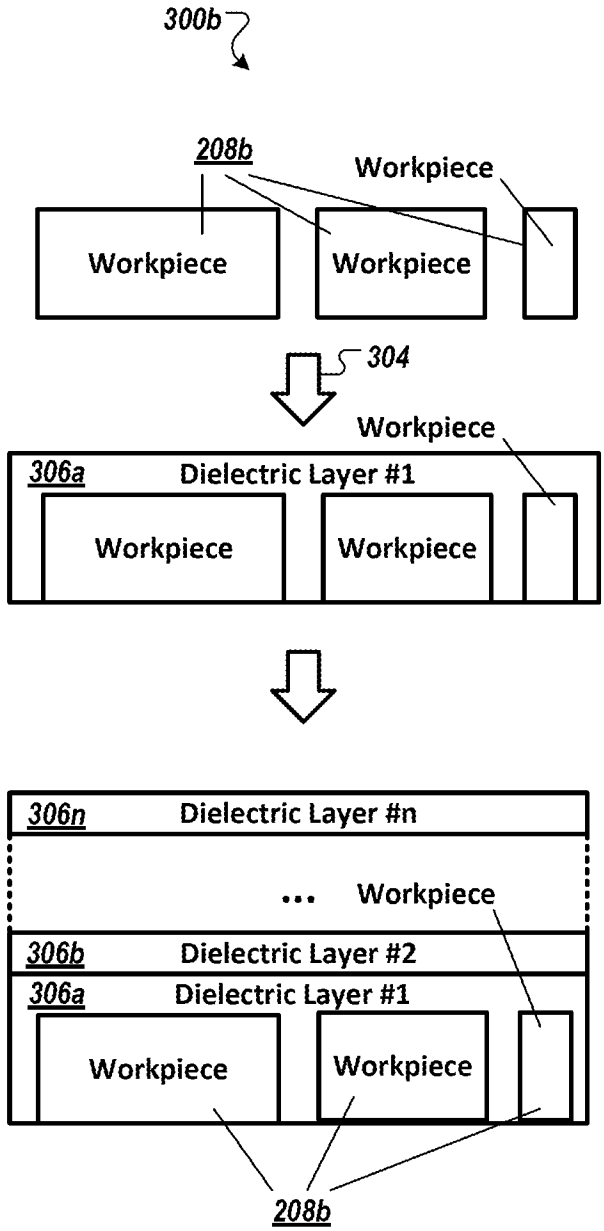

300b
208b
Workpiece
Workpiece
Workpiece
304
Workpiece
306a
Dielectric Layer #1
Workpiece
Workpiece
306n
Dielectric Layer #n
...
Workpiece
306b
Dielectric Layer #2
306a
Dielectric Layer #1
Workpiece
Workpiece
208b

FIG. 3B

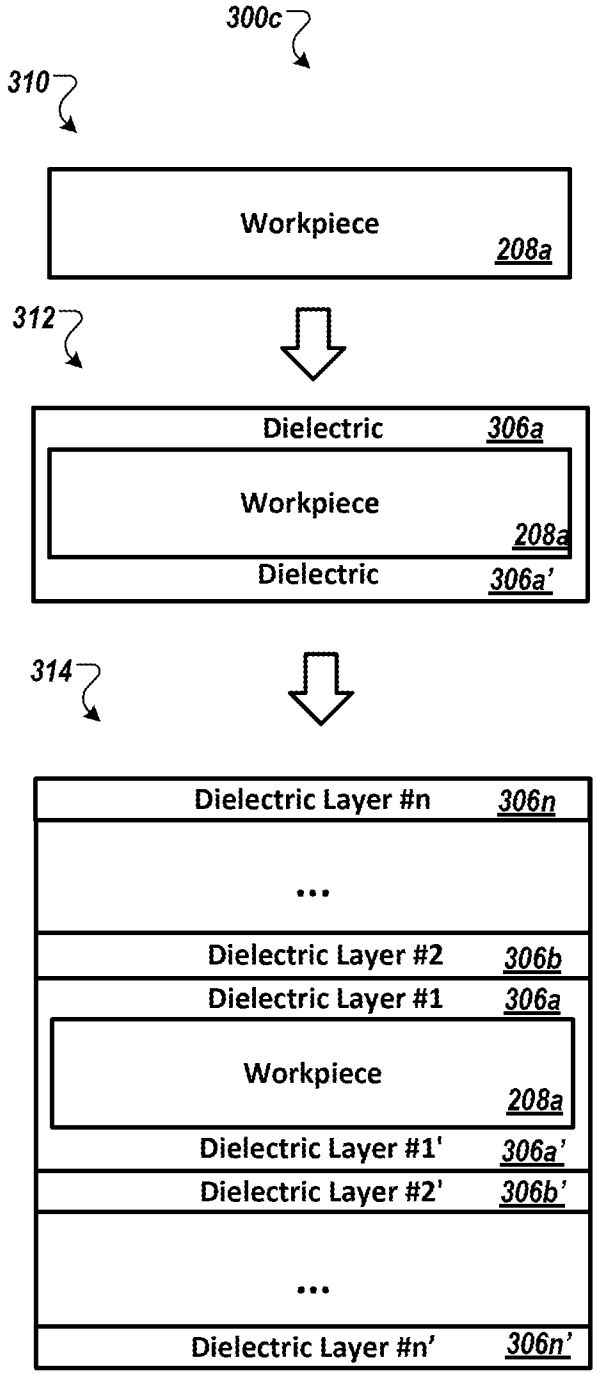

300c
310
Workpiece
208a
312
Dielectric
306a
Workpiece
208a
Dielectric
306a'
314
Dielectric Layer #n
306n
...
Dielectric Layer #2
306b
Dielectric Layer #1
306a
Workpiece
208a
Dielectric Layer #1'
306a'
Dielectric Layer #2'
306b'
...
Dielectric Layer #n'
306n'

FIG. 3C

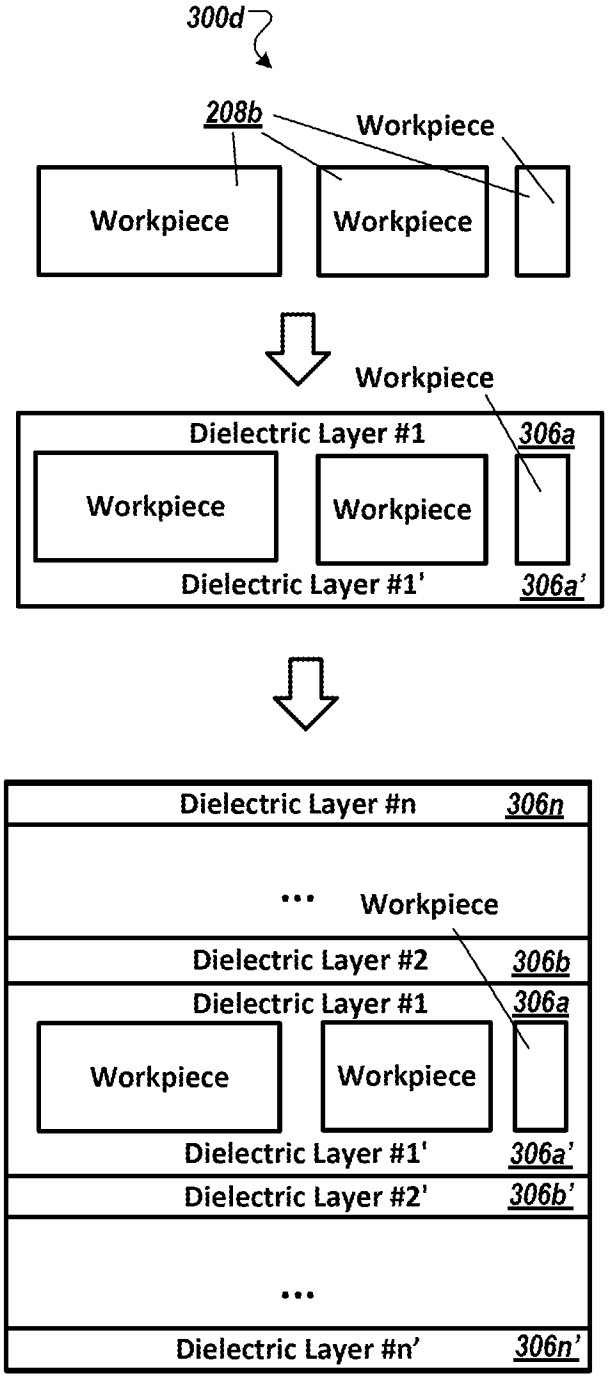

300d
208b
Workpiece
Workpiece
Workpiece
Workpiece
Dielectric Layer #1
306a
Workpiece
Workpiece
Dielectric Layer #1'
306a'
Dielectric Layer #n
306n
...
Workpiece
Dielectric Layer #2
306b
Dielectric Layer #1
306a
Workpiece
Workpiece
Dielectric Layer #1'
306a'
Dielectric Layer #2'
306b'
...
Dielectric Layer #n'
306n'

FIG. 3D

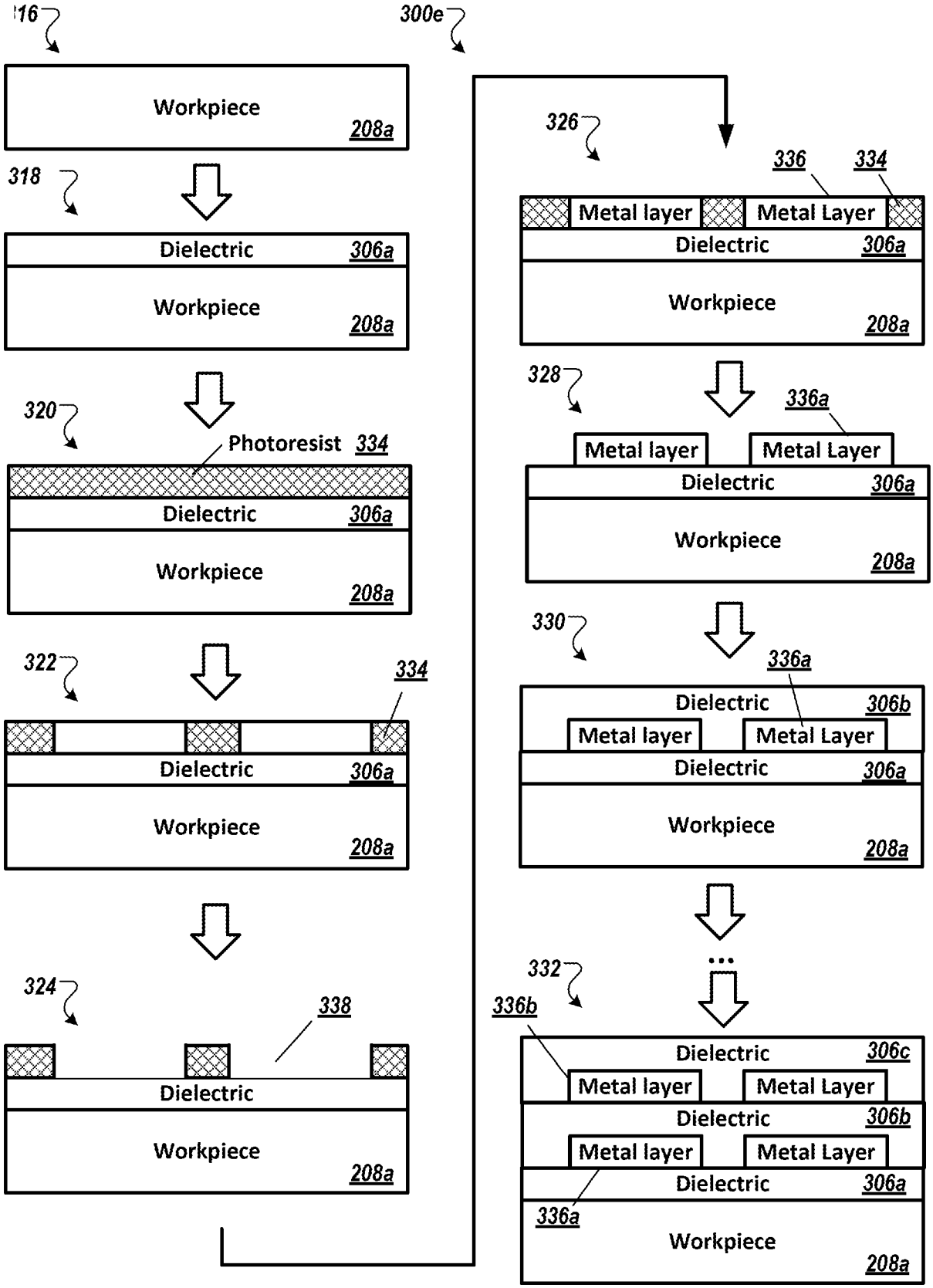

316
Workpiece
208a
318
Dielectric
306a
Workpiece
208a
320
Photoresist
334
Dielectric
306a
Workpiece
208a
322
334
Dielectric
306a
Workpiece
208a
324
338
Dielectric
Workpiece
208a
300e
326
336
334
Metal layer
Metal Layer
Dielectric
306a
Workpiece
208a
328
336a
Metal layer
Metal Layer
Dielectric
306a
Workpiece
208a
330
336a
Dielectric
306b
Metal layer
Metal Layer
Dielectric
306a
Workpiece
208a
332
336b
Dielectric
306c
Metal layer
Metal Layer
Dielectric
306b
Metal layer
Metal Layer
Dielectric
306a
336a
Workpiece
208a

FIG. 3E

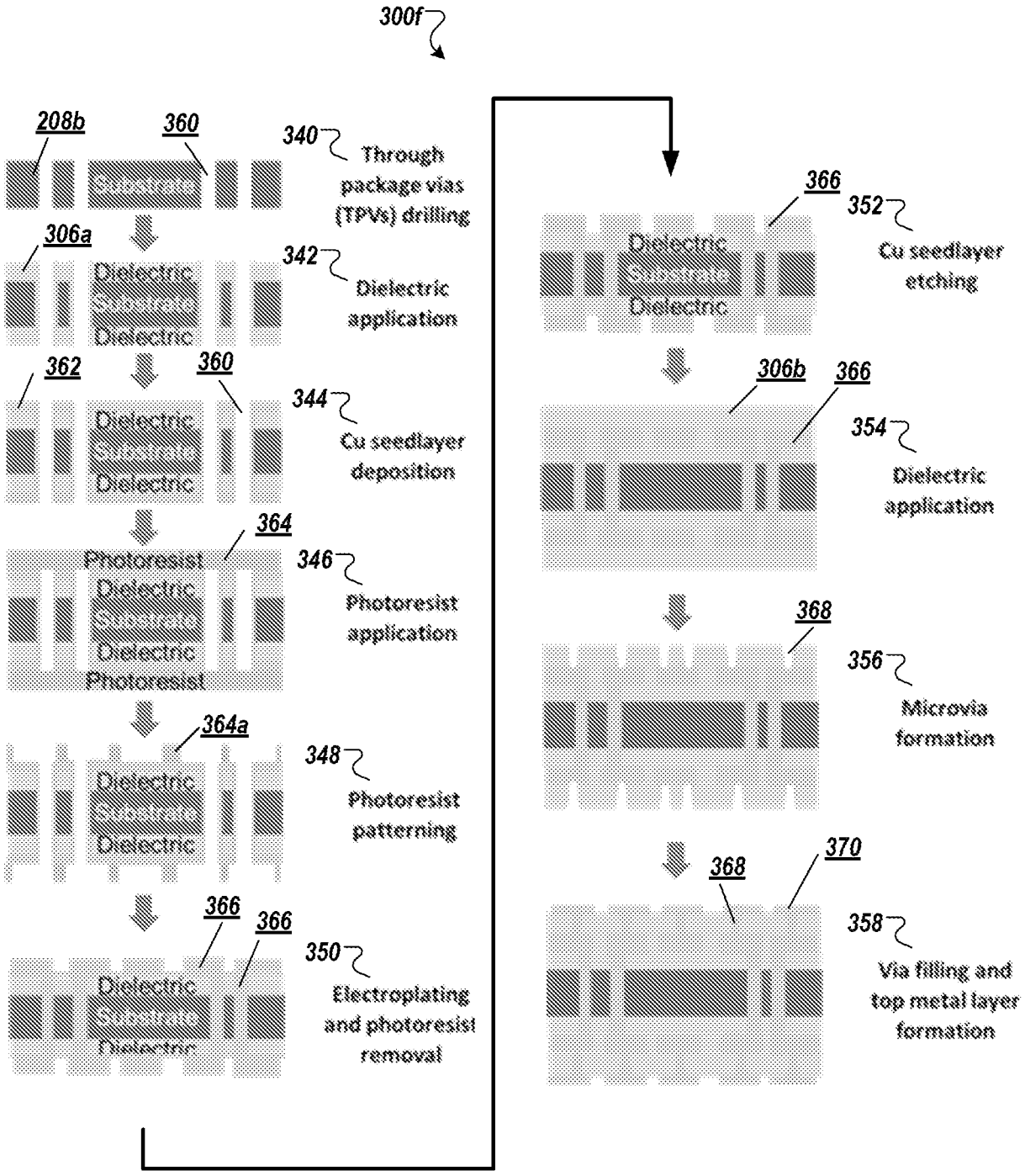

300f
208b
360
340
Through package vias (TPVs) drilling
Substrate
306a
342
Dielectric application
Dielectric
Substrate
Dielectric
362
360
344
Cu seedlayer deposition
364
346
Photoresist application
Photoresist
364a
348
Photoresist patterning
366
366
350
Electroplating and photoresist removal
366
352
Cu seedlayer etching
306b
366
354
Dielectric application
368
356
Microvia formation
368
370
358
Via filling and top metal layer formation

FIG. 3F

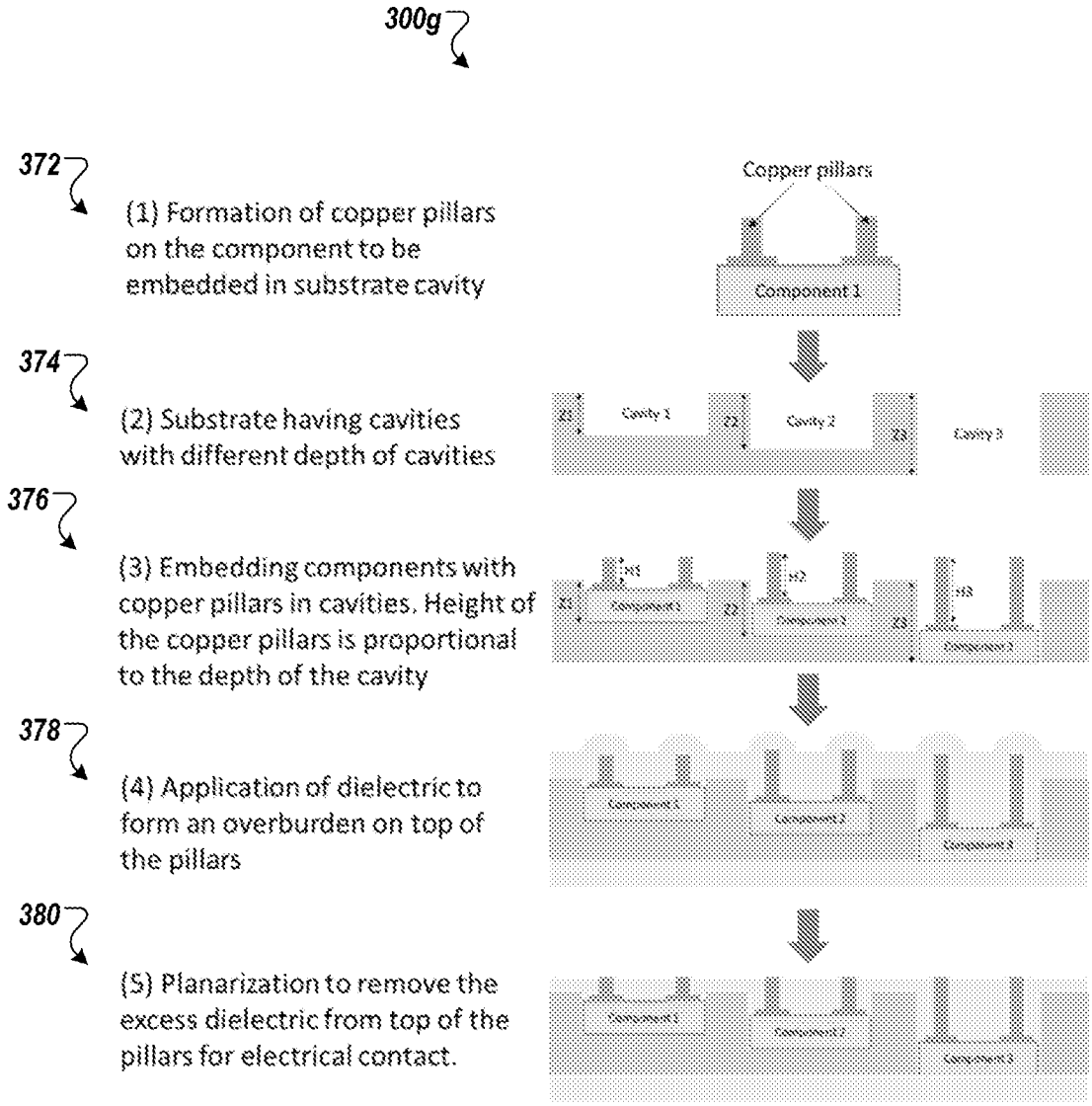

300g
372
(1) Formation of copper pillars on the component to be embedded in substrate cavity
Copper pillars
Component 1
374
(2) Substrate having cavities with different depth of cavities
Cavity 1
Cavity 2
Cavity 3
376
(3) Embedding components with copper pillars in cavities. Height of the copper pillars is proportional to the depth of the cavity
378
(4) Application of dielectric to form an overburden on top of the pillars
380
(5) Planarization to remove the excess dielectric from top of the pillars for electrical contact.

FIG. 3G

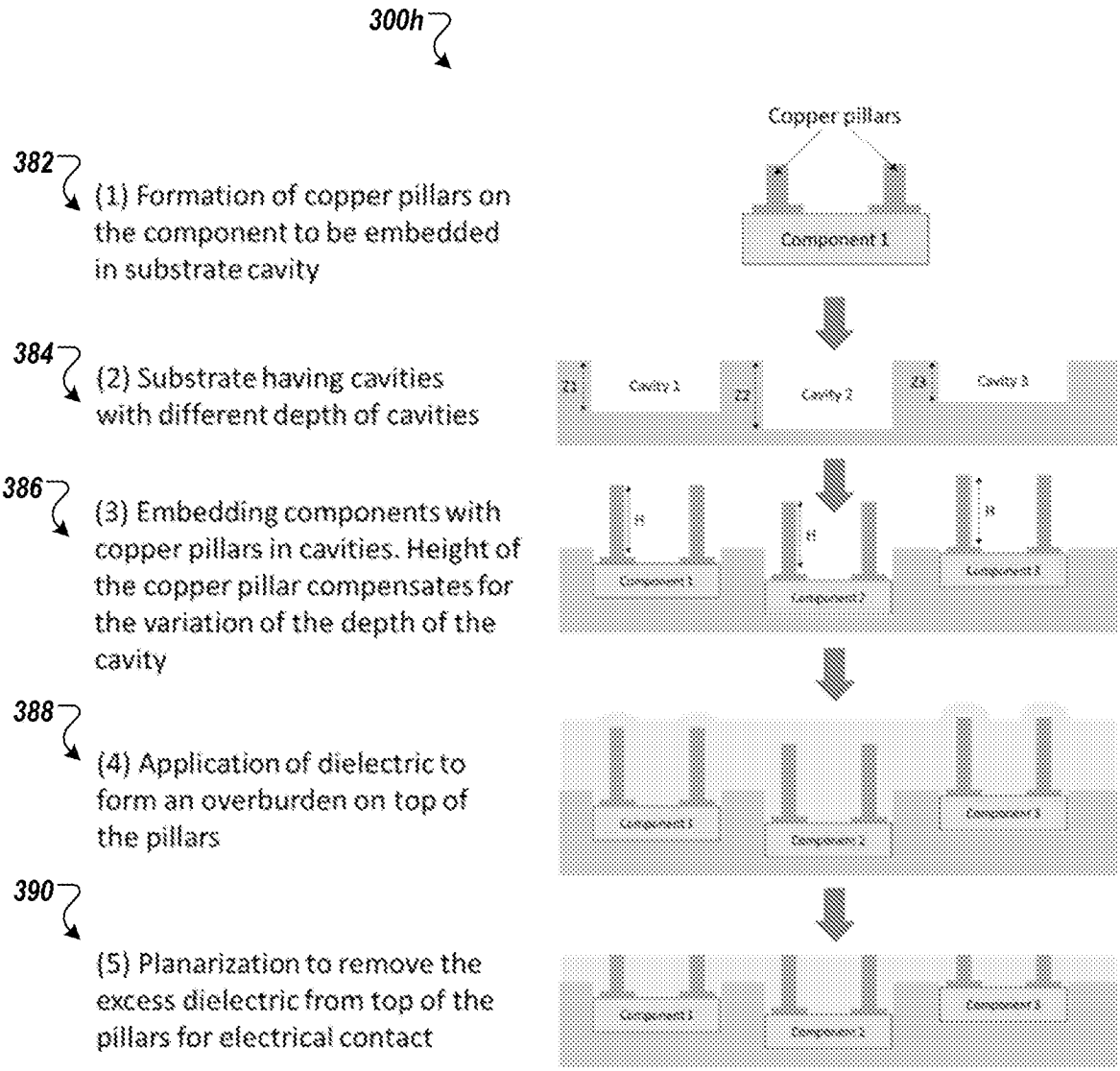

300h
382
(1) Formation of copper pillars on the component to be embedded in substrate cavity
384
(2) Substrate having cavities with different depth of cavities
386
(3) Embedding components with copper pillars in cavities. Height of the copper pillar compensates for the variation of the depth of the cavity
388
(4) Application of dielectric to form an overburden on top of the pillars
390
(5) Planarization to remove the excess dielectric from top of the pillars for electrical contact
Copper pillars
Component 1
Cavity 1
Cavity 2
Cavity 3

FIG. 3H

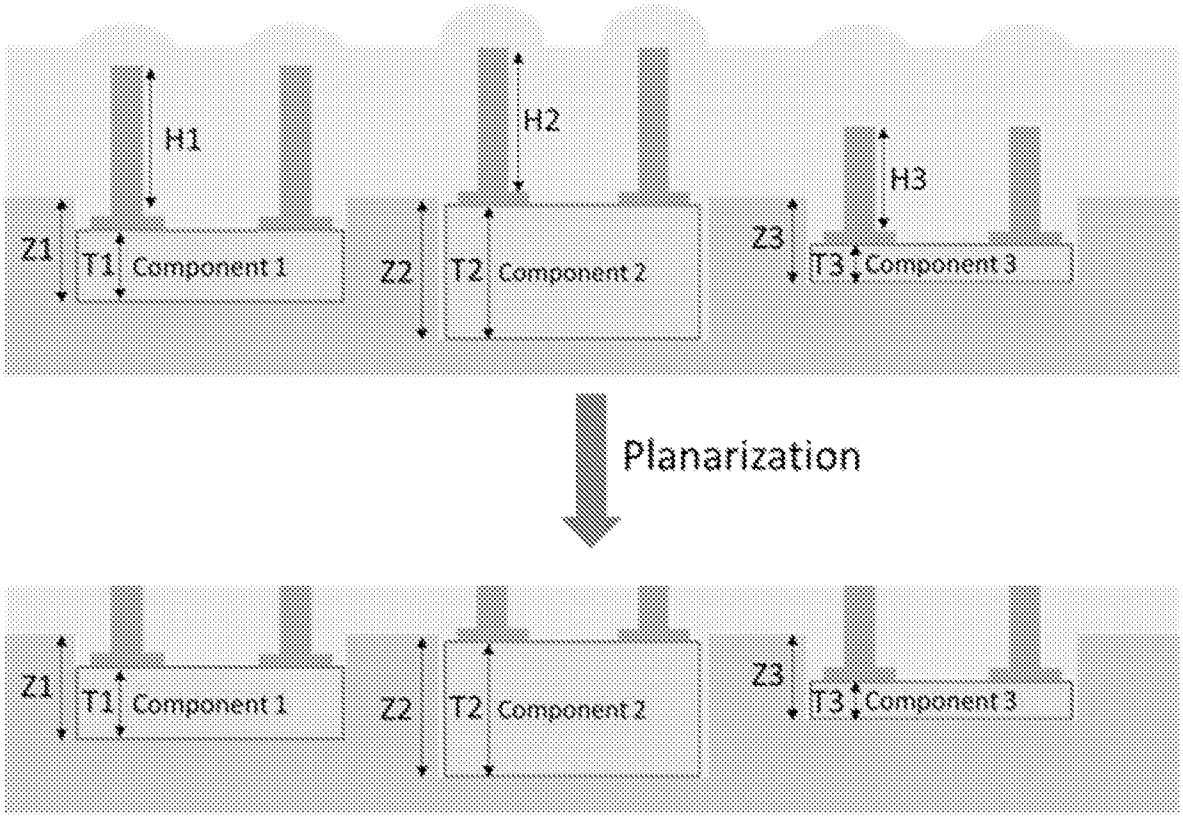

H1
H2
H3
Z1
T1
Component 1
Z2
T2
Component 2
Z3
T3
Component 3
Planarization
Z1
T1
Component 1
Z2
T2
Component 2
Z3
T3
Component 3

FIG. 3I

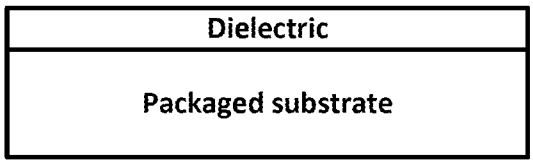


FIG. 4A

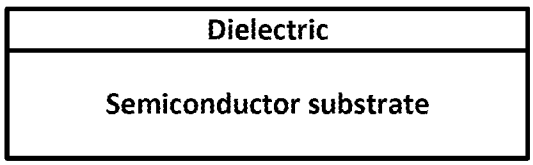


FIG. 4B

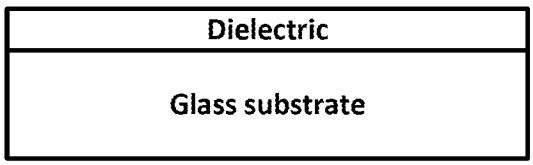


FIG. 4C

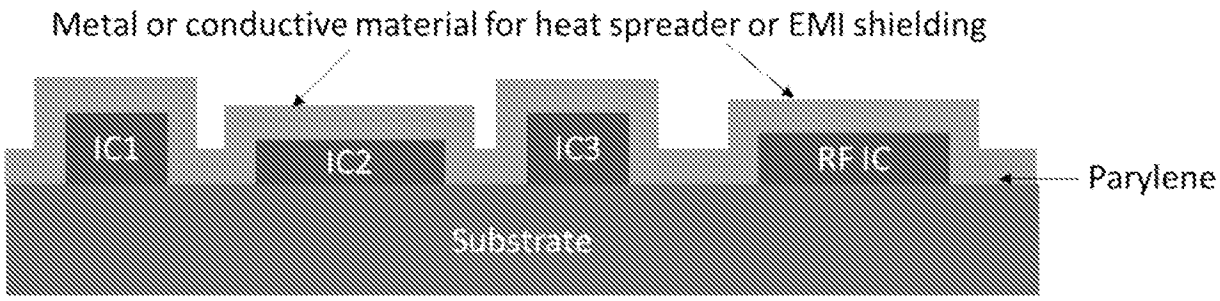


FIG. 4D

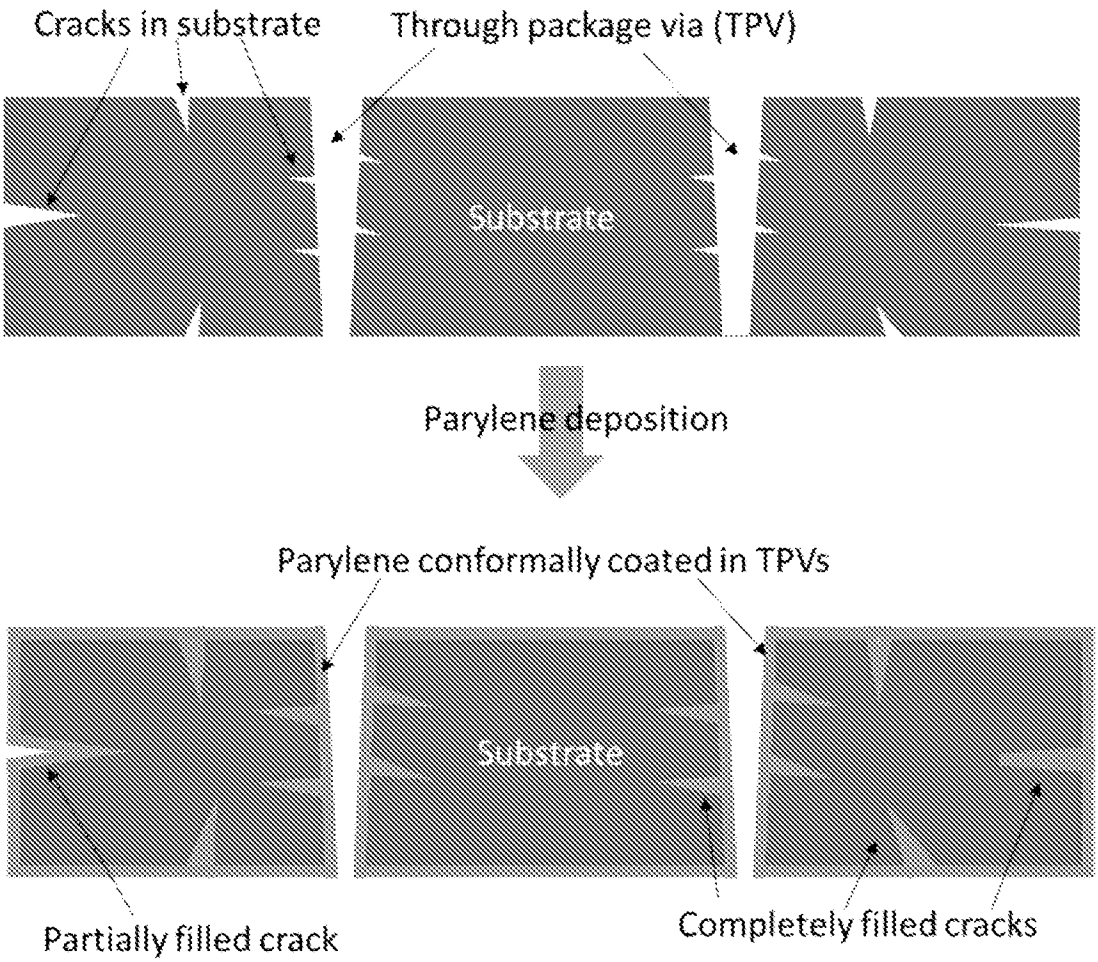

Cracks in substrate
Through package via (TPV)
Substrate
Parylene deposition
Parylene conformally coated in TPVs
Substrate
Partially filled crack
Completely filled cracks

FIG. 4E

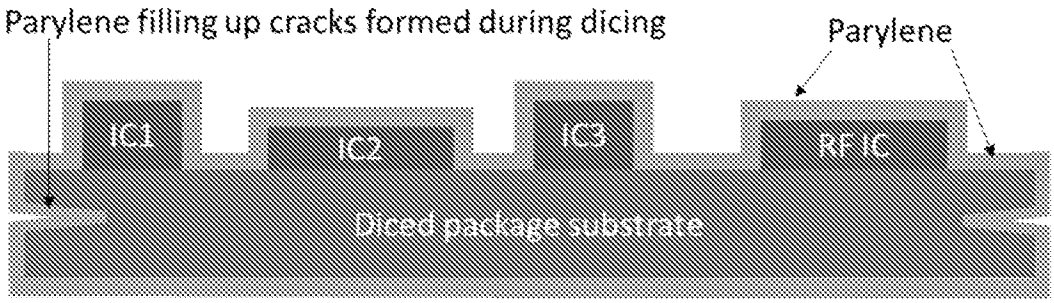

Parylene filling up cracks formed during dicing
Parylene
IC1
IC2
IC3
RF IC
Diced package substrate

FIG. 4F

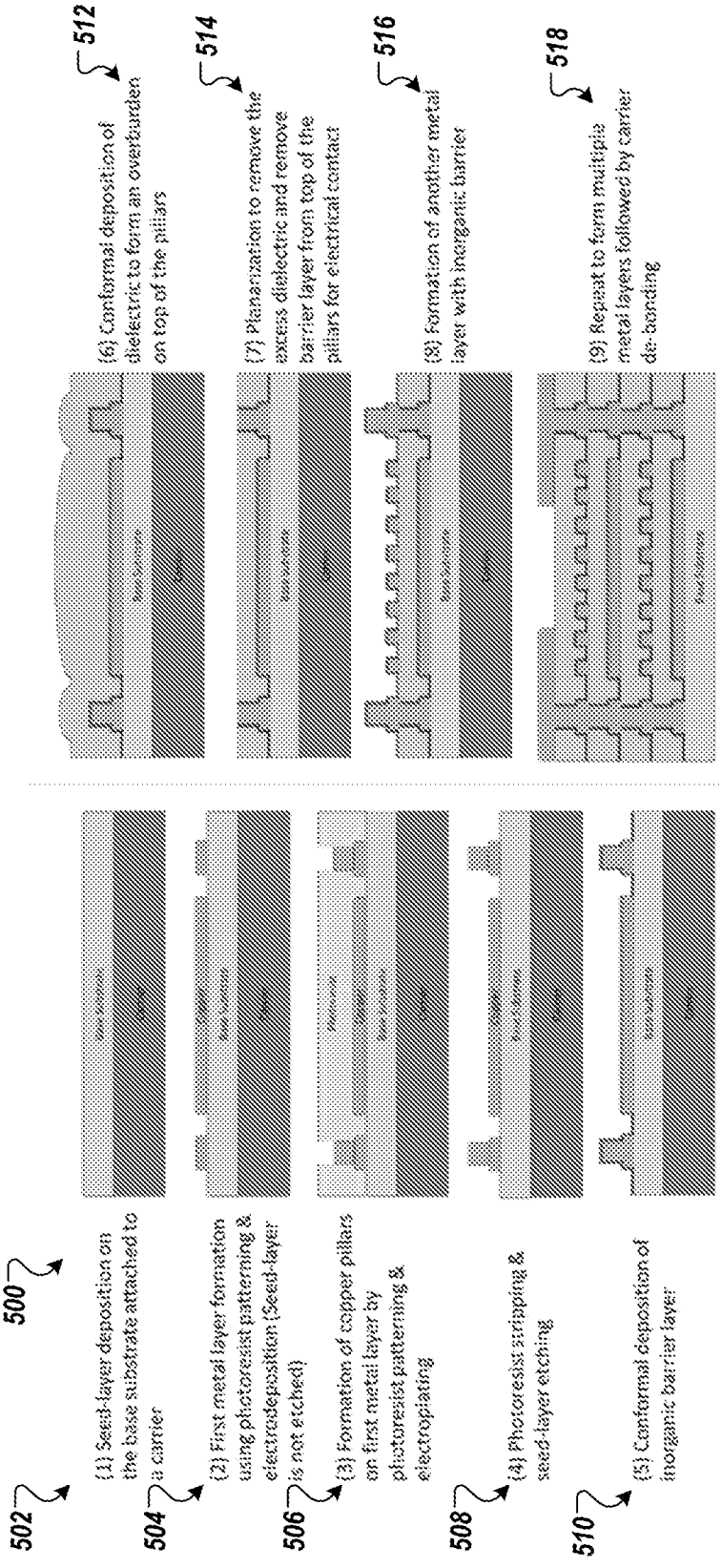

500
502
(1) Seed-layer deposition on the base substrate attached to a carrier
504
(2) First metal layer formation using photoresist patterning & electrodeposition (Seed-layer is not etched)
506
(3) Formation of copper pillars on first metal layer by photoresist patterning & electroplating
508
(4) Photoresist stripping & seed-layer etching
510
(5) Conformal deposition of inorganic barrier layer
512
(6) Conformal deposition of dielectric to form an overburden on top of the pillars
514
(7) Planarization to remove the excess dielectric and remove barrier layer from top of the pillars for electrical contact
516
(8) Formation of another metal layer with inorganic barrier
518
(9) Repeat to form multiple metal layers followed by carrier de-bonding

FIG. 5A

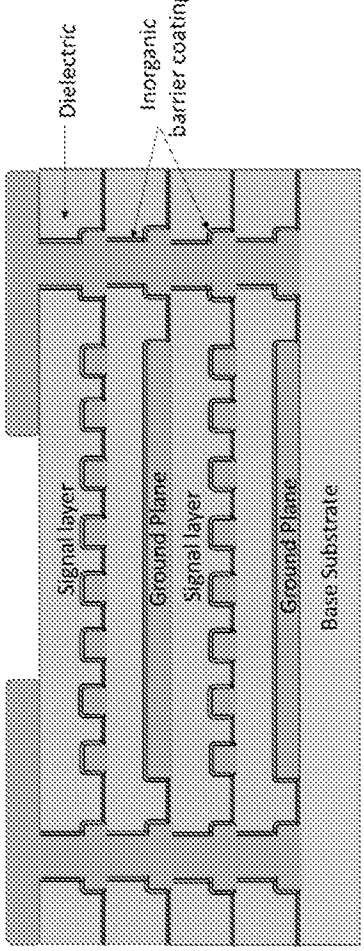

Dielectric
Inorganic barrier coating
Signal layer
Ground Plane
Signal layer
Ground Plane
Base Substrate

FIG. 5B

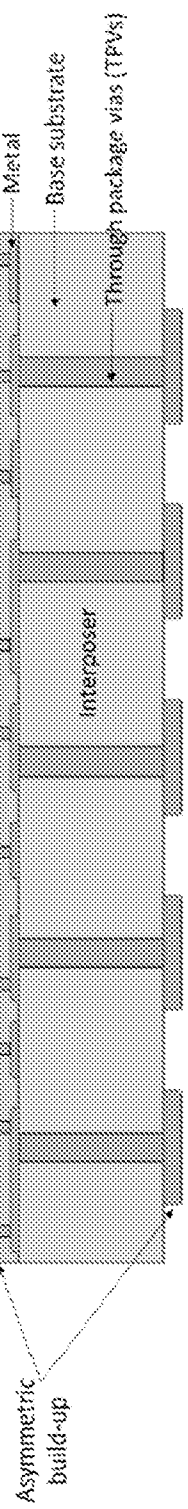

Dielectric
Metal
Base substrate
Through package vias (TPVs)
Interposer
Asymmetric build-up

FIG. 5C

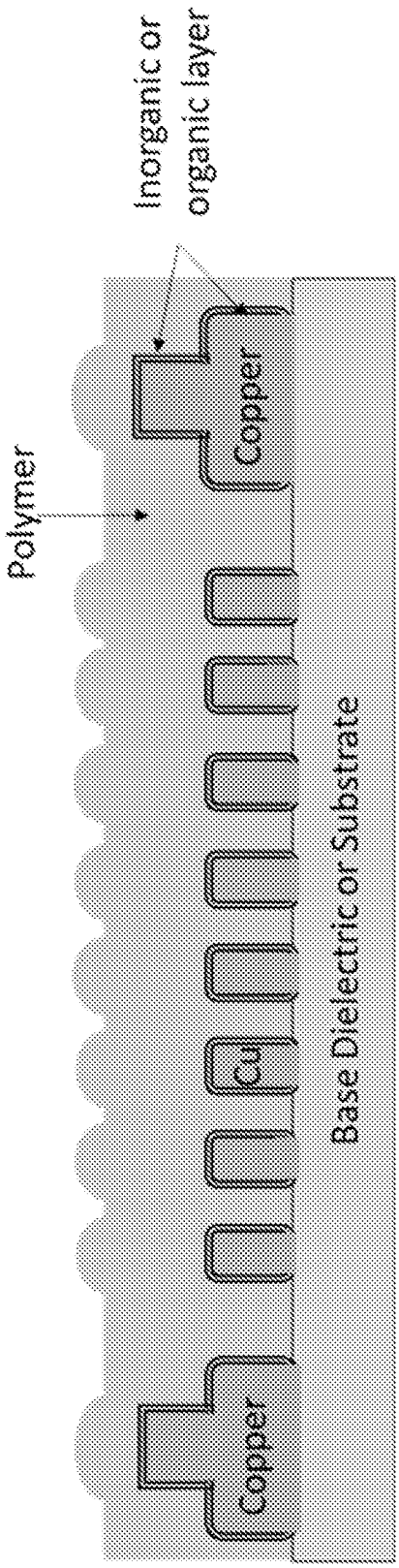

Inorganic or organic layer
Polymer
Copper
Cu
Base Dielectric or Substrate
Copper

FIG. 5D

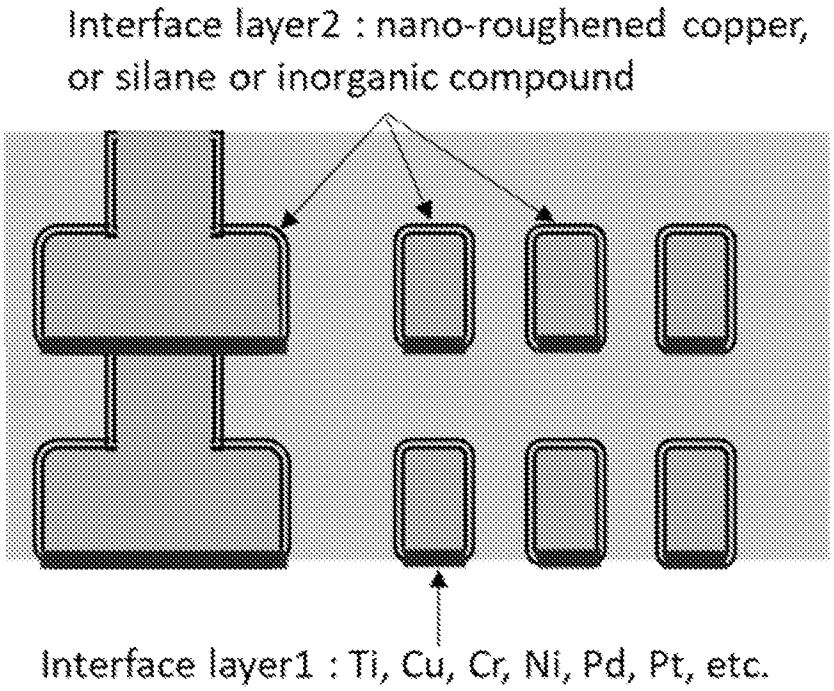

Interface layer2 : nano-roughened copper,
or silane or inorganic compound
Interface layer1 : Ti, Cu, Cr, Ni, Pd, Pt, etc.

FIG. 5E

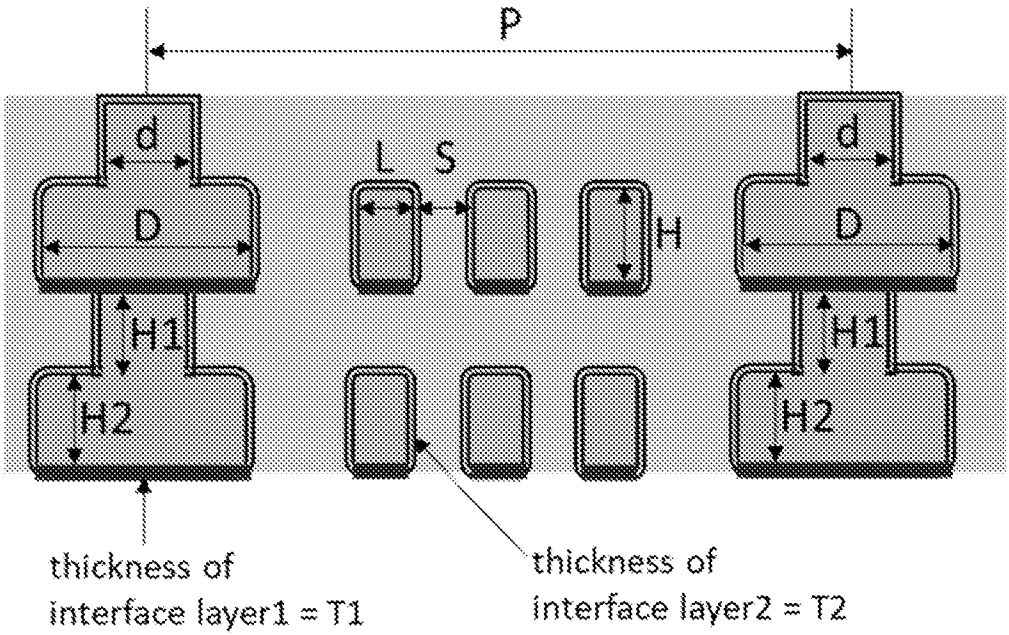

P
d
D
L
S
H
H1
H2
thickness of
interface layer1 = T1
thickness of
interface layer2 = T2

FIG. 5F

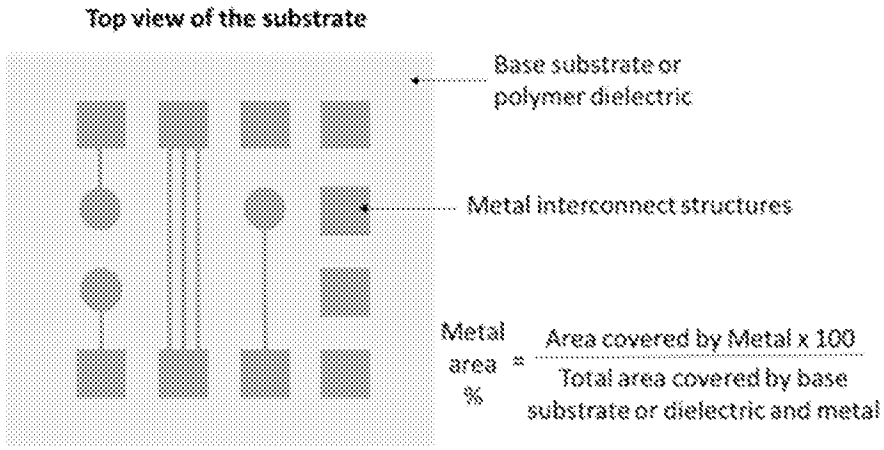

Top view of the substrate
Base substrate or polymer dielectric
Metal interconnect structures
Metal area % = Area covered by Metal x 100 / Total area covered by base substrate or dielectric and metal

FIG. 6A

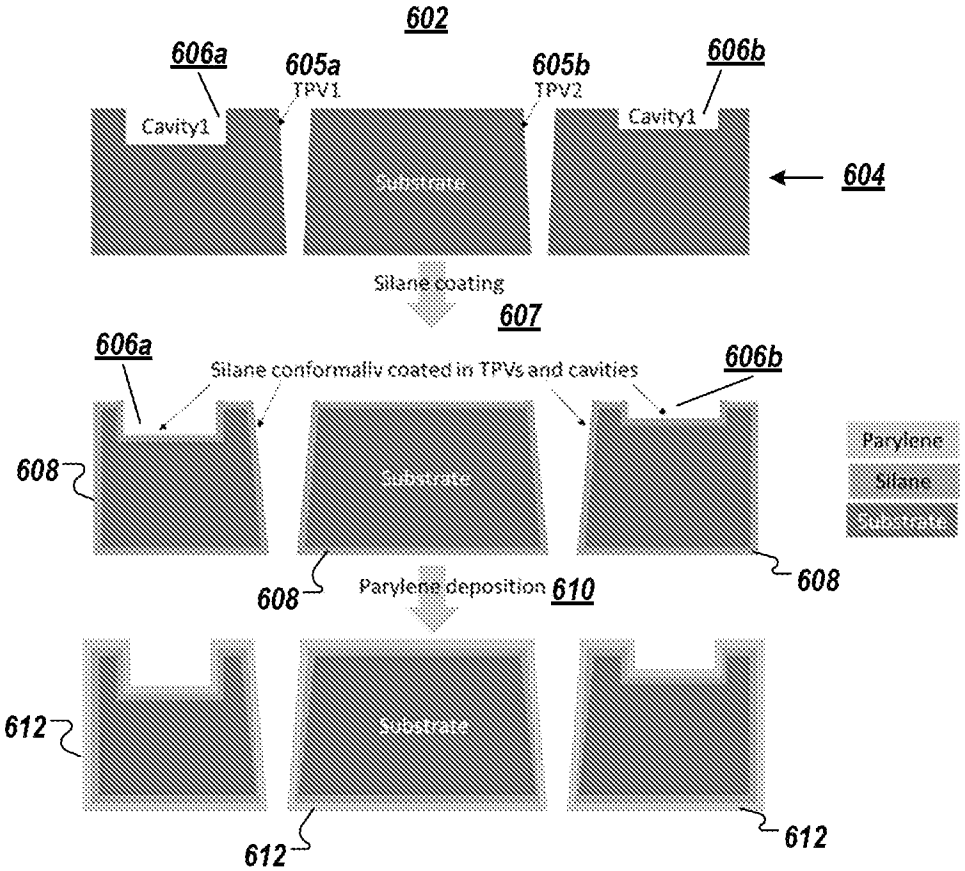

602
606a
605a
TPV1
605b
TPV2
606b
Cavity1
Cavity1
Substrate
604
Silane coating
607
606a
Silane conformally coated in TPVs and cavities
606b
608
Substrate
Parylene
Silane
608
608
Parylene deposition 610
612
Substrate
612
612

FIG. 6B

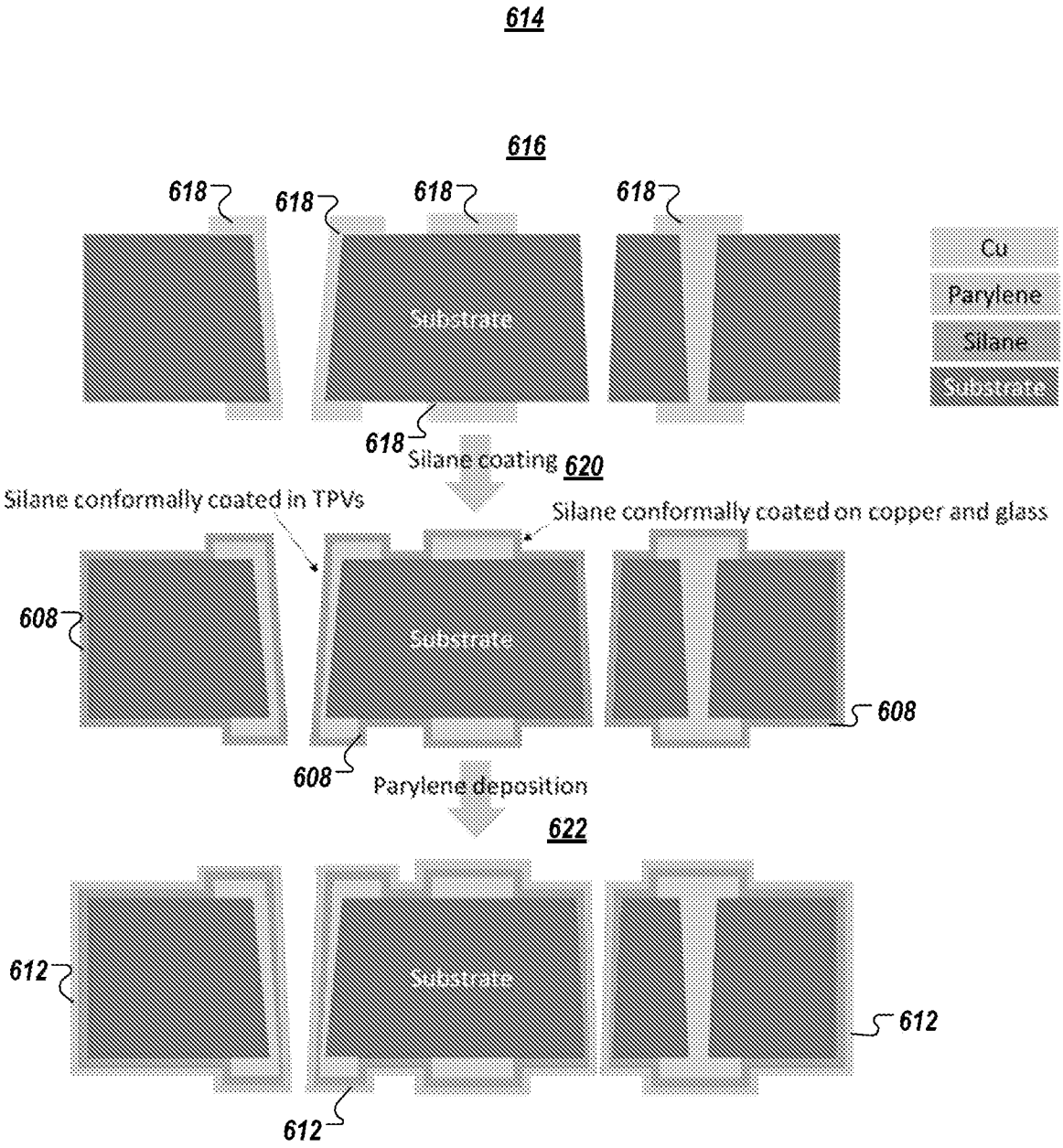

614
616
618
618
618
618
Substrate
Cu
Parylene
Silane
Substrate
618
Silane coating 620
Silane conformally coated in TPVs
Silane conformally coated on copper and glass
608
Substrate
608
608
Parylene deposition
622
612
Substrate
612
612

FIG. 6C

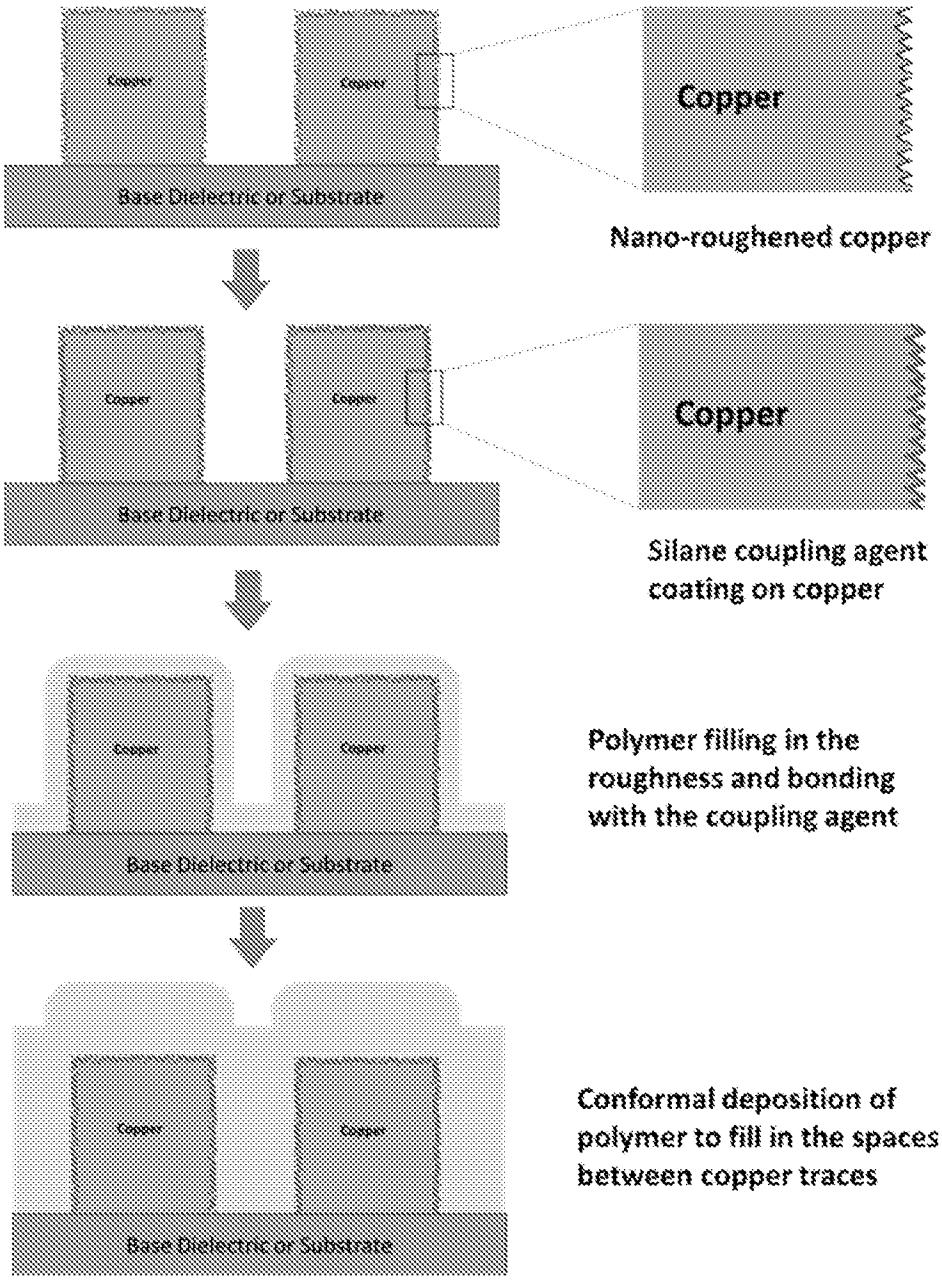

Copper
Copper
Base Dielectric or Substrate
Copper
Nano-roughened copper
Copper
Copper
Base Dielectric or Substrate
Copper
Silane coupling agent coating on copper
Copper
Copper
Base Dielectric or Substrate
Polymer filling in the roughness and bonding with the coupling agent
Copper
Copper
Base Dielectric or Substrate
Conformal deposition of polymer to fill in the spaces between copper traces

FIG. 6D

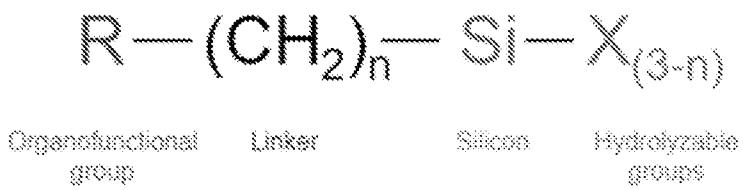

R—(CH2)n— Si—X(3-n)
Organofunctional group
Linker
Silicon
Hydrolyzable groups

FIG. 6E

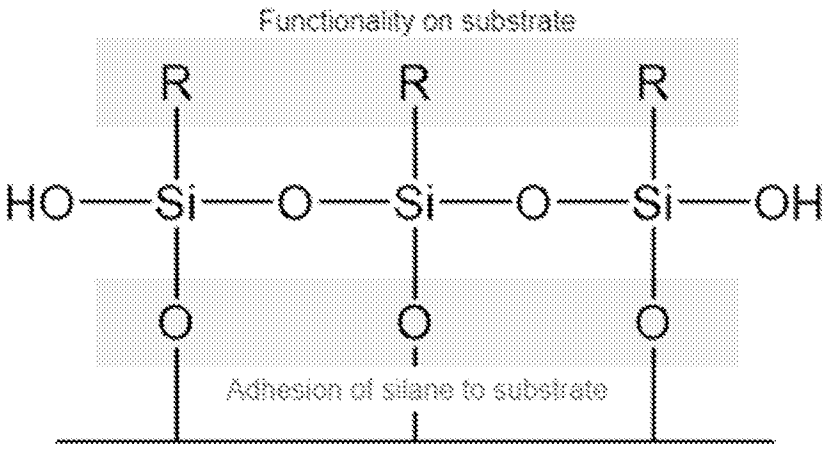

Functionality on substrate
R
R
R
HO—Si—O—Si—O—Si—OH
O
O
O
Adhesion of silane to substrate

FIG. 6F

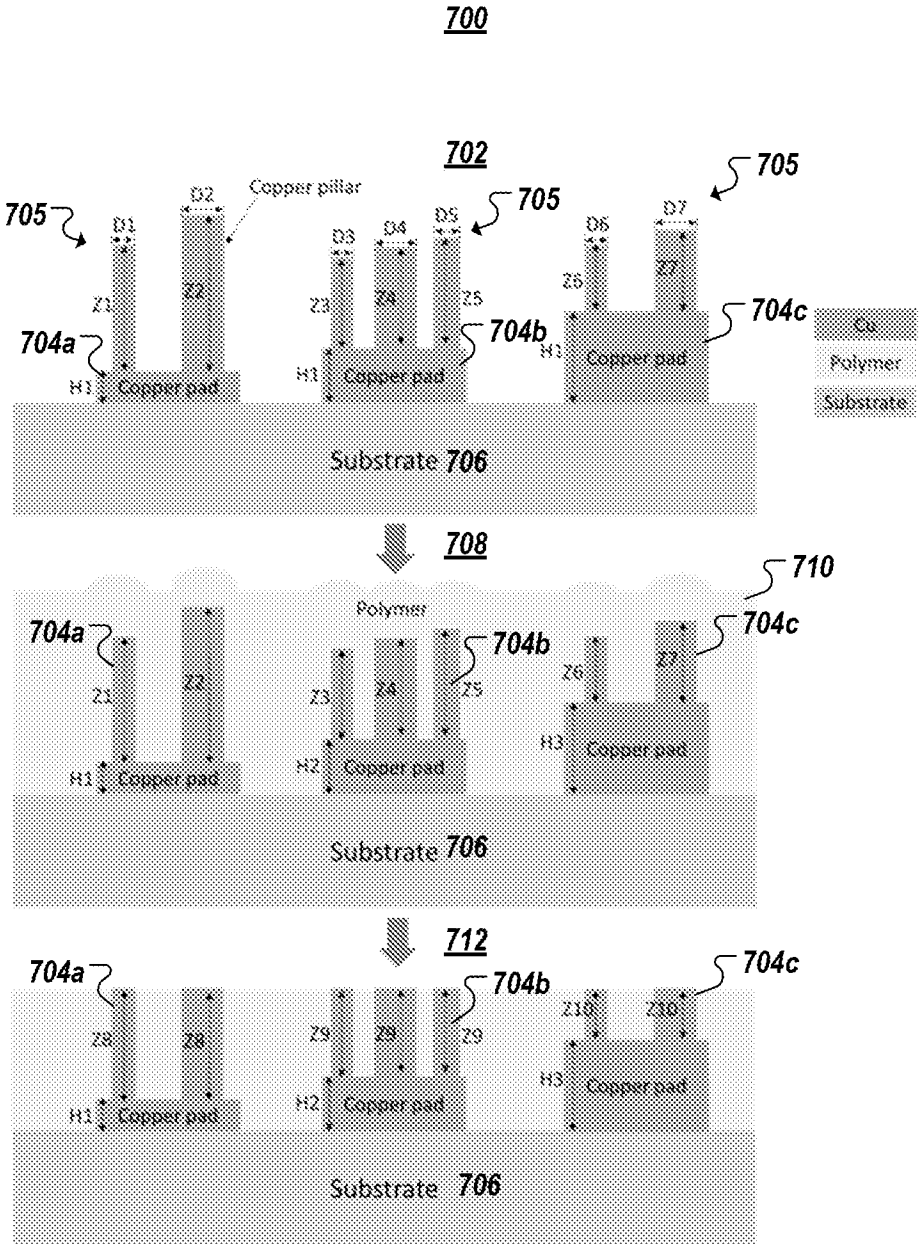

700
702
705
705
705
Copper pillar
D1
D2
D3
D4
D5
D6
D7
Z1
Z2
Z3
Z4
Z5
Z6
Z7
704a
704b
704c
H1
Copper pad
Cu
Polymer
Substrate
Substrate 706
708
710
Polymer
704a
704b
704c
Z1
Z2
Z3
Z4
Z5
Z6
Z7
H1
H2
H3
Copper pad
Substrate 706
712
704a
704b
704c
Z8
Z8
Z9
Z9
Z9
Z10
Z10
H1
H2
H3
Copper pad
Substrate 706

FIG. 7

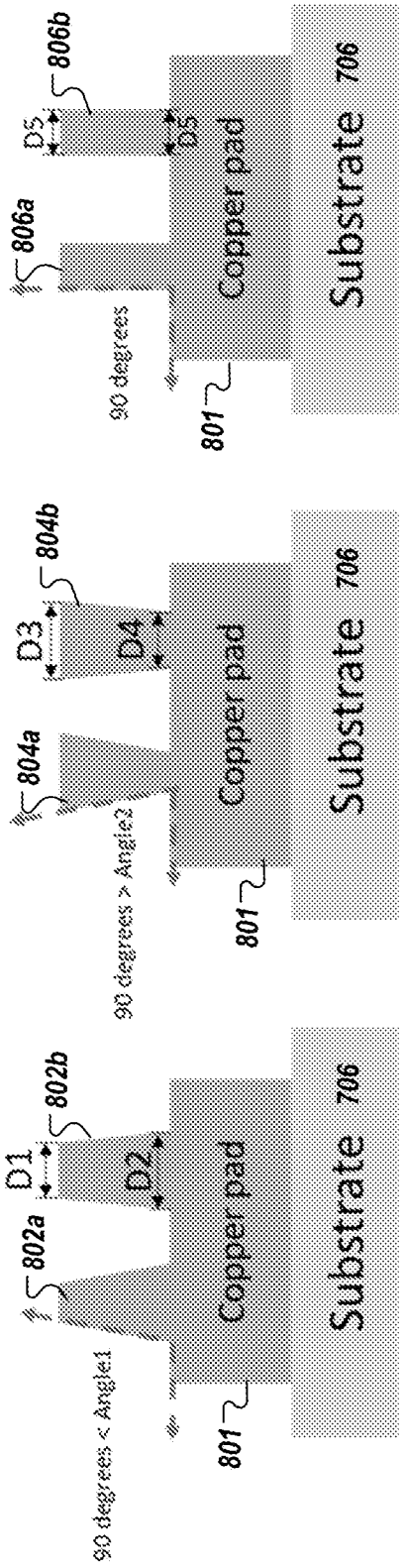

802a
802b
D1
D2
90 degrees < Angle1
Copper pad
Substrate 706
801
804a
804b
D3
D4
90 degrees > Angle2
Copper pad
Substrate 706
801
806a
806b
D5
D5
90 degrees
Copper pad
Substrate 706
801

FIG. 8

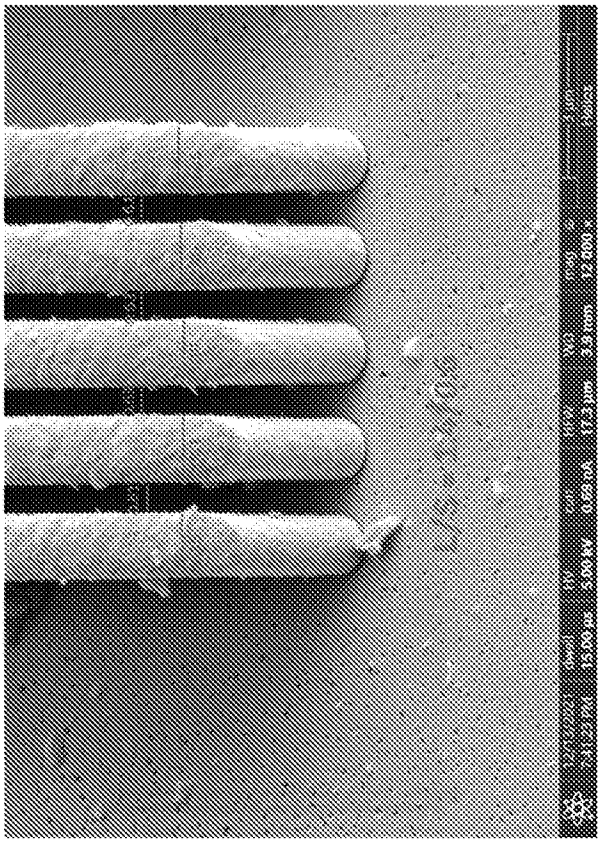


FIG. 9

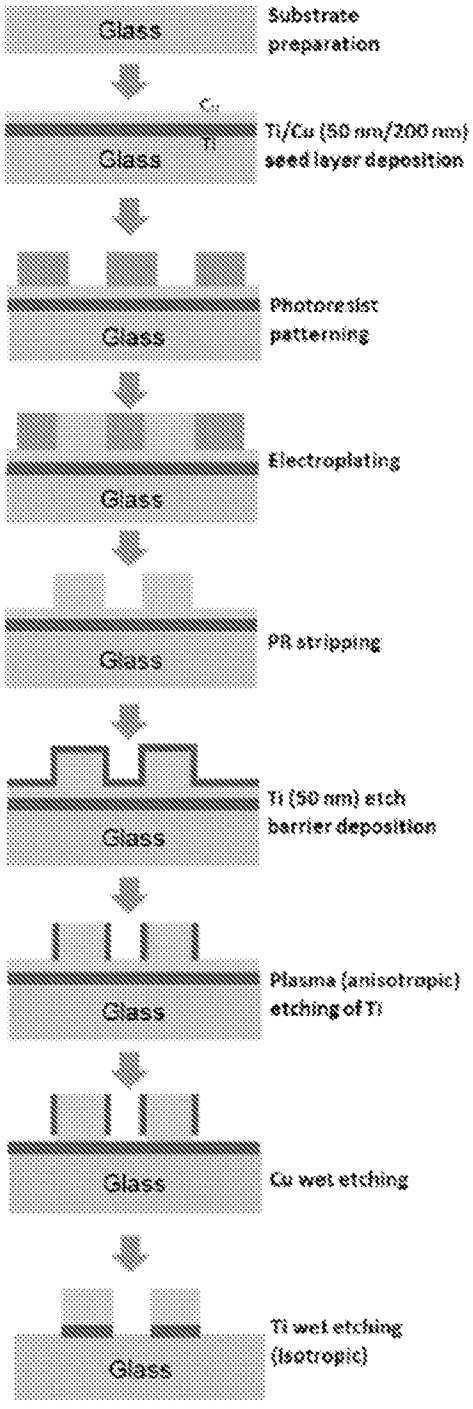

Glass
Substrate preparation
Cu
Ti
Glass
Ti/Cu (50 nm/200 nm) seed layer deposition
Glass
Photoresist patterning
Glass
Electroplating
Glass
PR stripping
Glass
Ti (50 nm) etch barrier deposition
Glass
Plasma (anisotropic) etching of Ti
Glass
Cu wet etching
Glass
Ti wet etching (isotropic)

FIG. 10

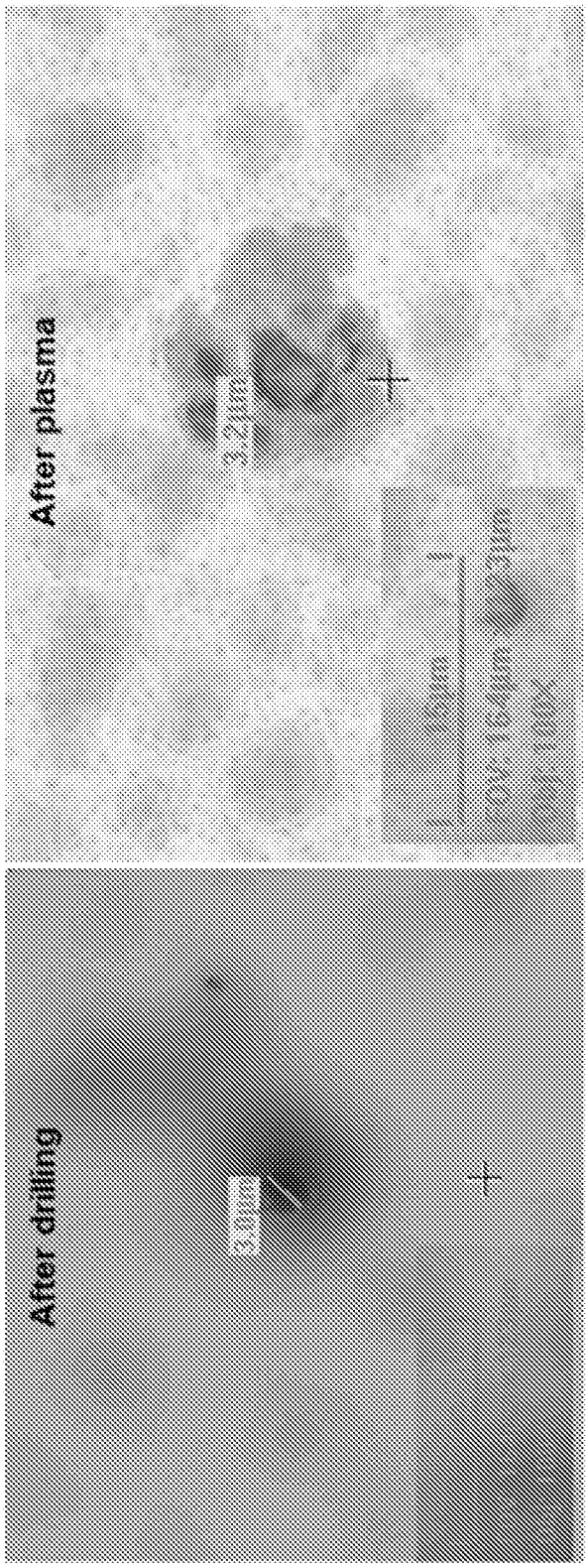


FIG. 11

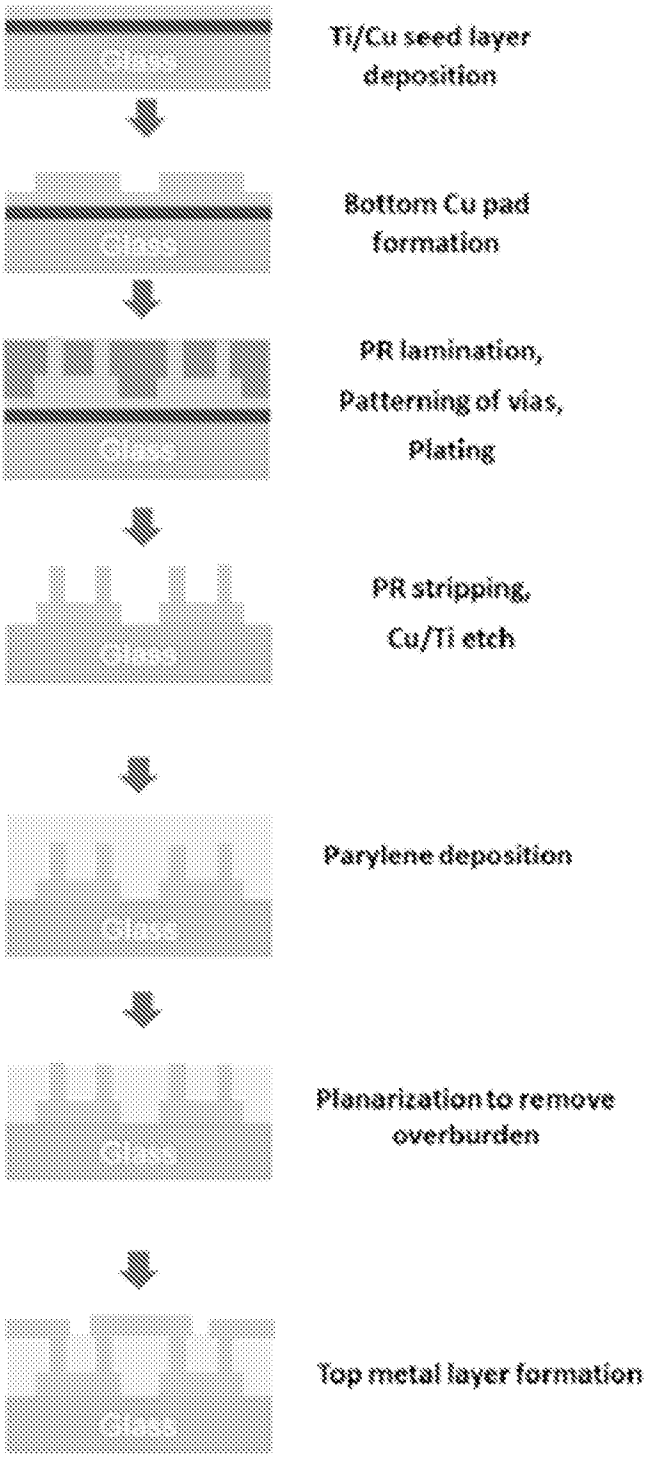

Glass
Ti/Cu seed layer deposition
Glass
Bottom Cu pad formation
Glass
PR lamination, Patterning of vias, Plating
Glass
PR stripping, Cu/Ti etch
Glass
Parylene deposition
Glass
Planarization to remove overburden
Glass
Top metal layer formation

FIG. 12

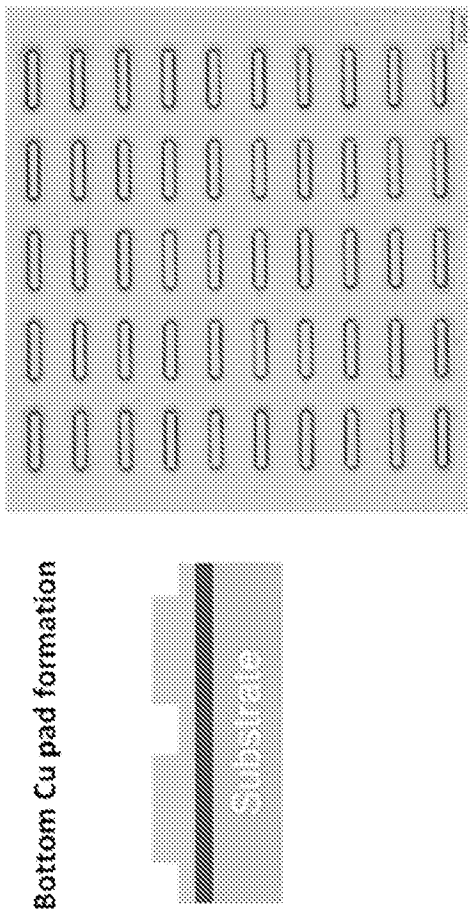


FIG. 13A

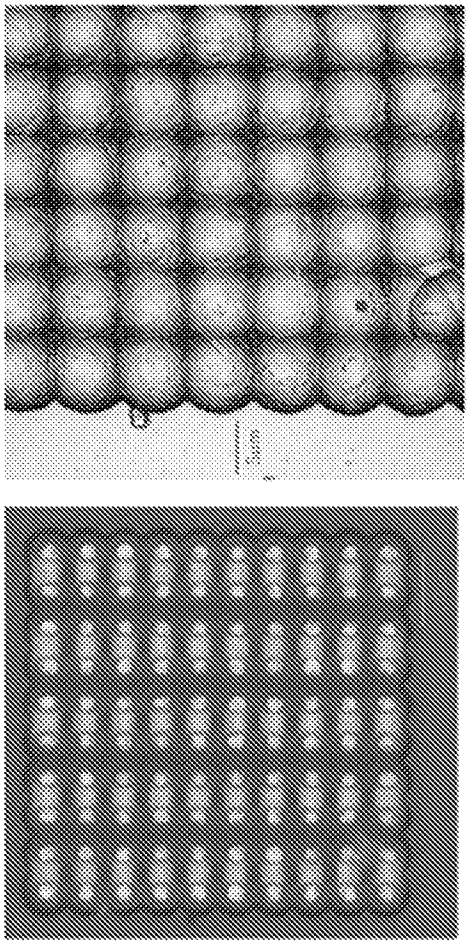


FIG. 13B

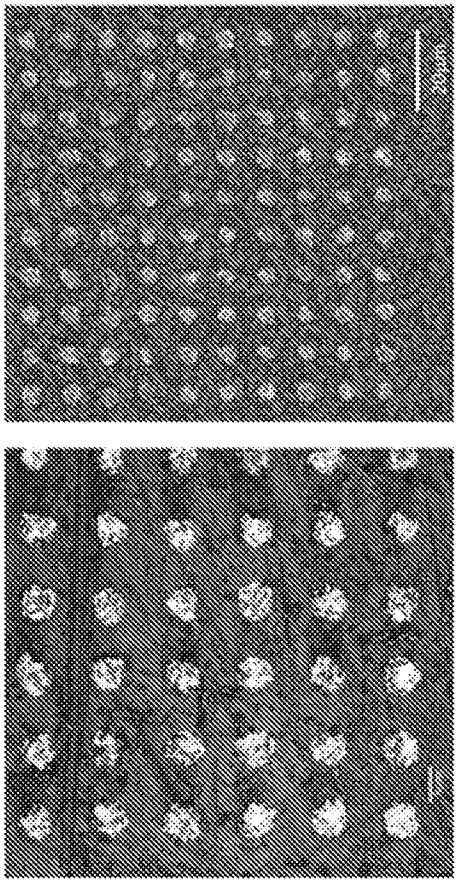


FIG. 13C

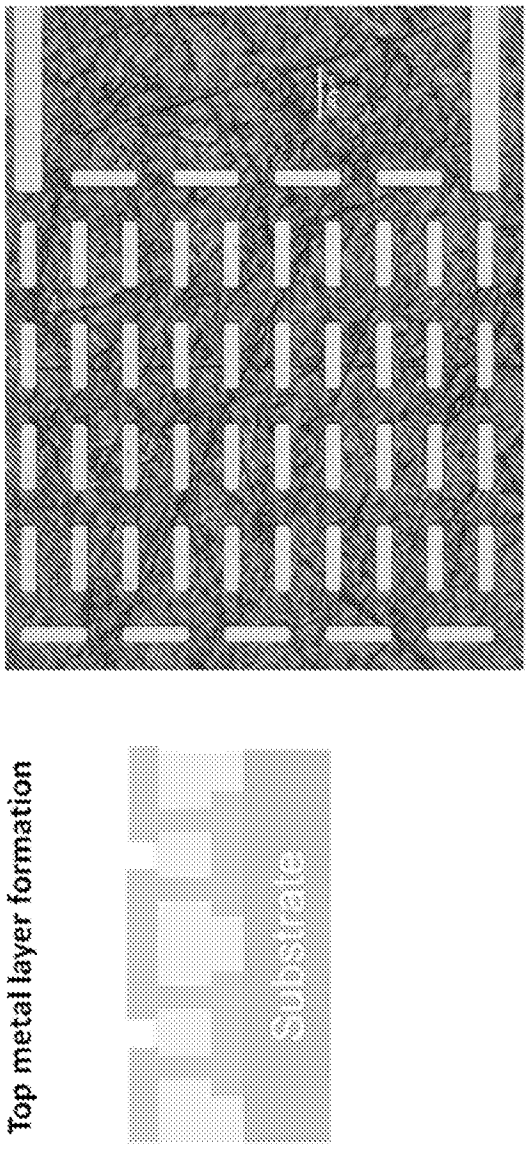


FIG. 13D

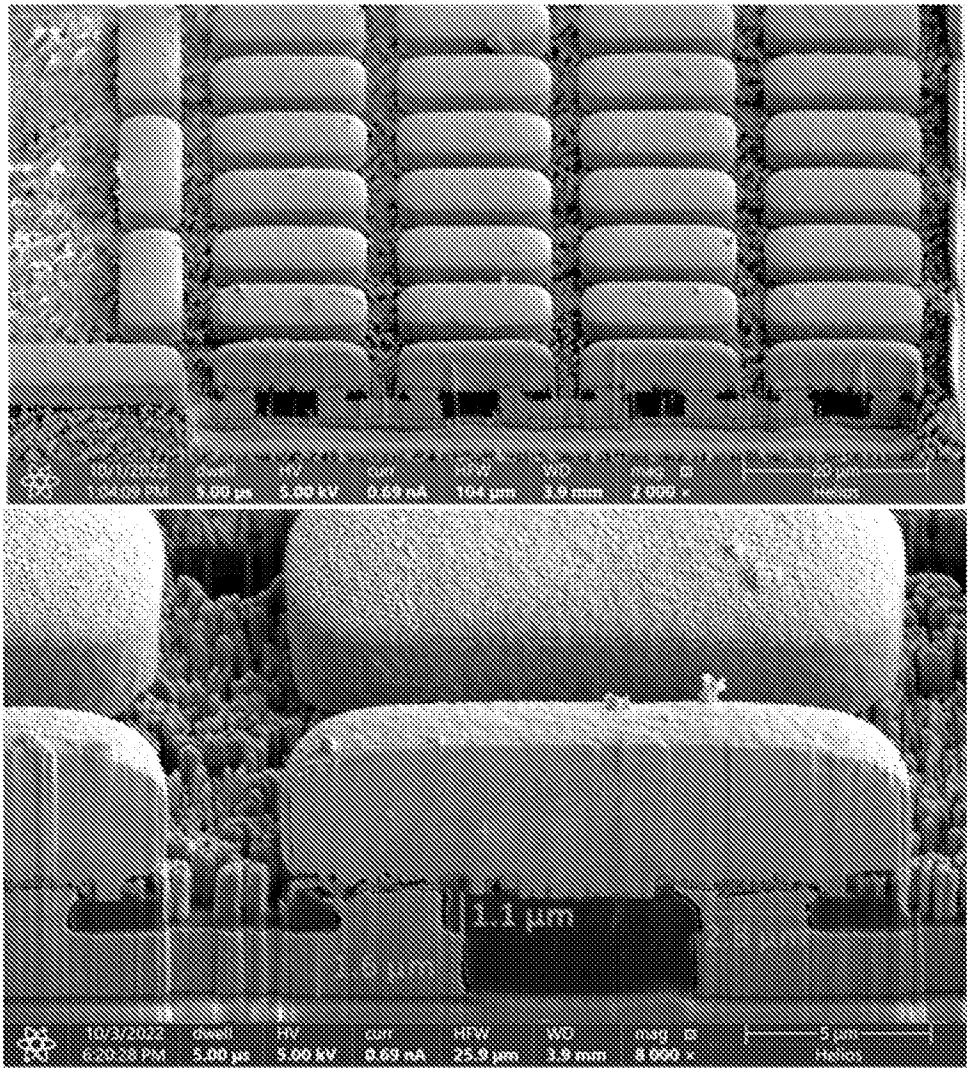


FIG. 14

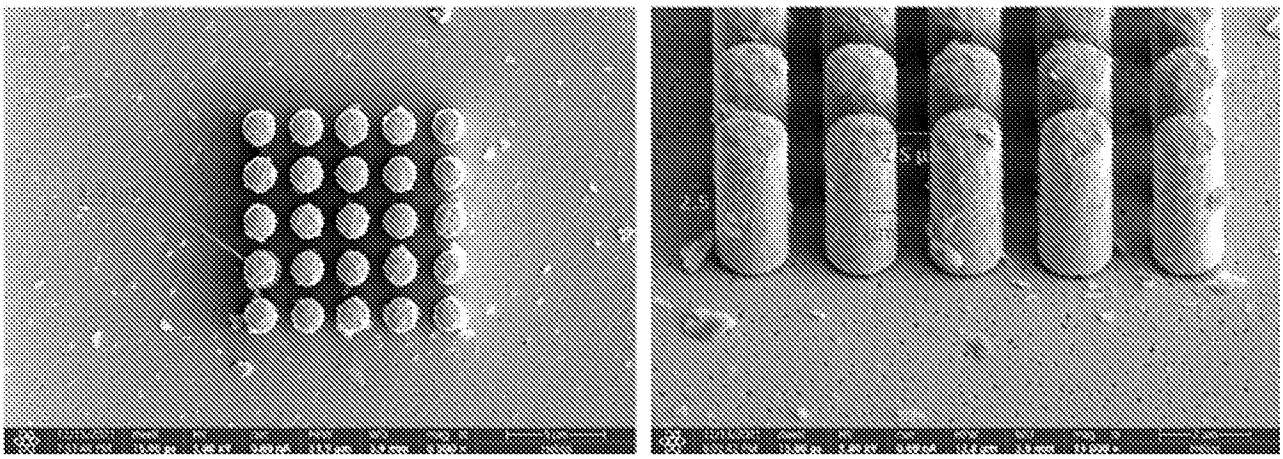


FIG. 15

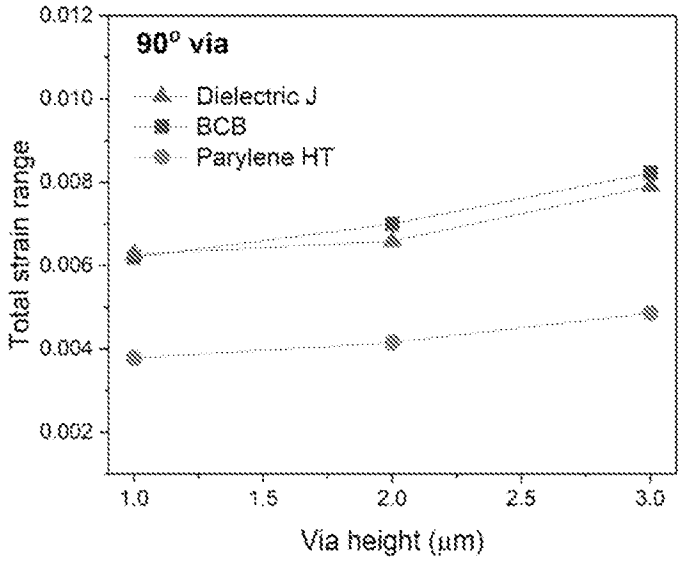


FIG. 16A

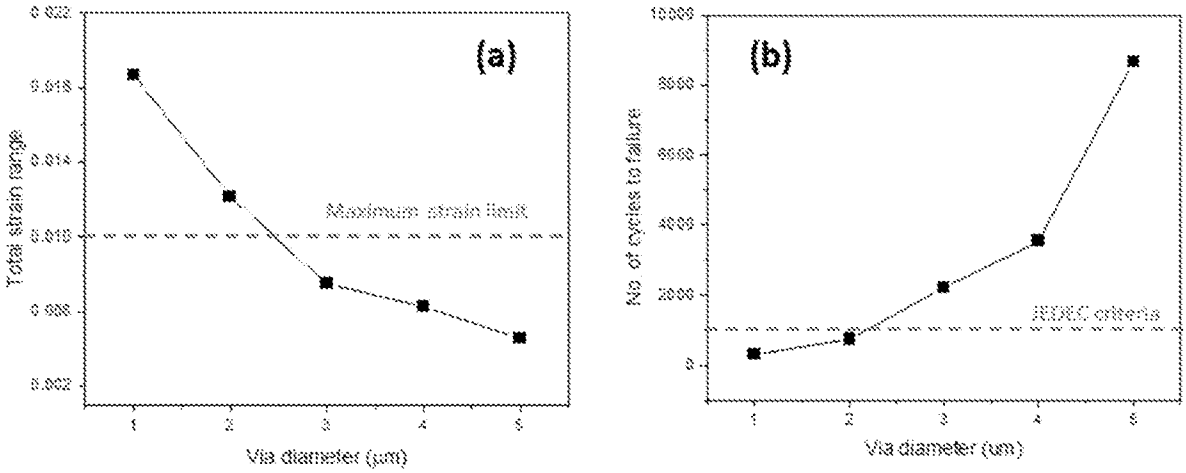


FIG. 16B

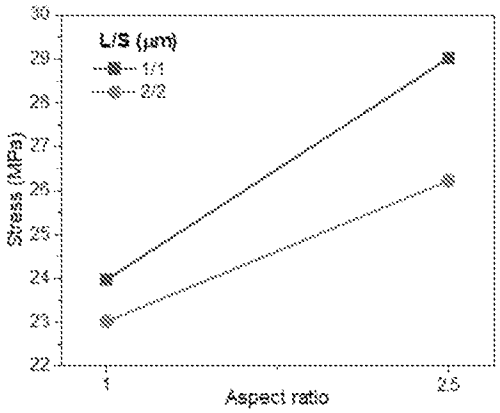


FIG. 17A

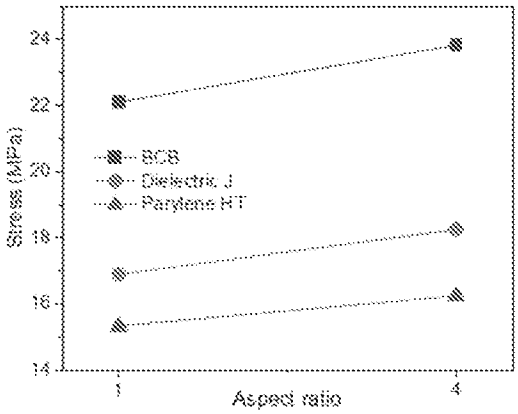


FIG. 17B

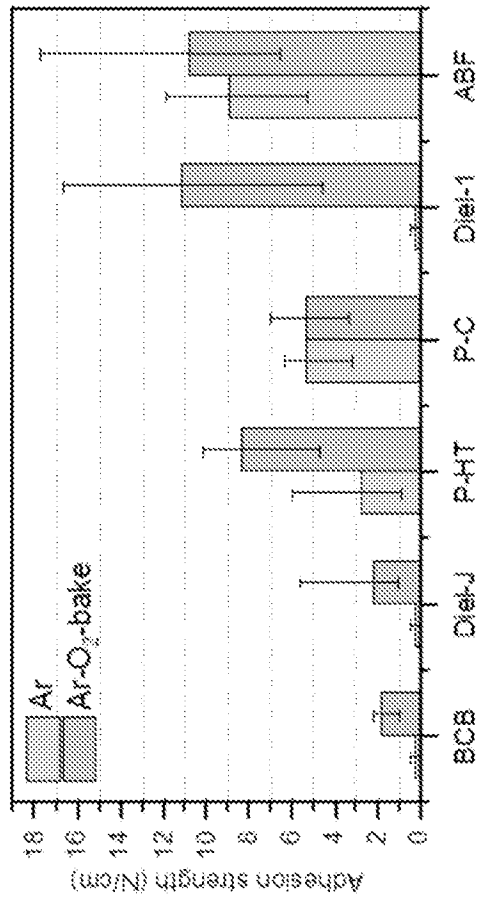


FIG. 19A

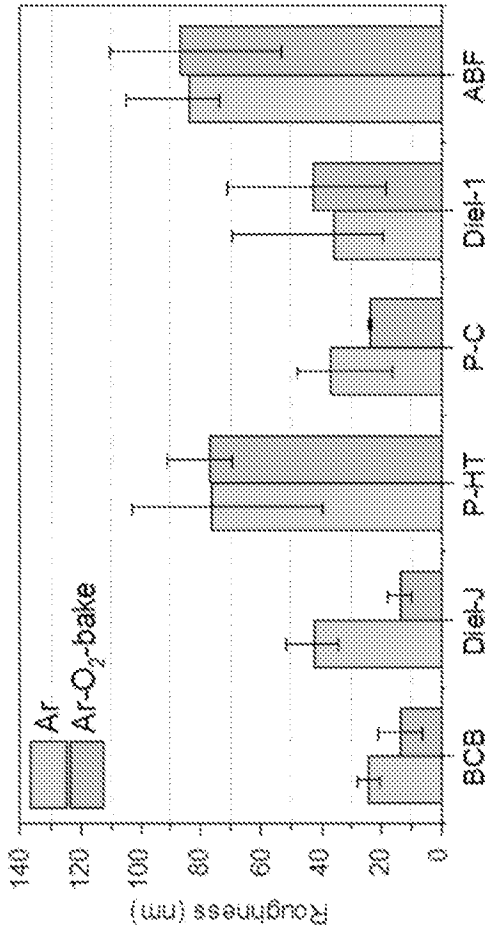


FIG. 19B

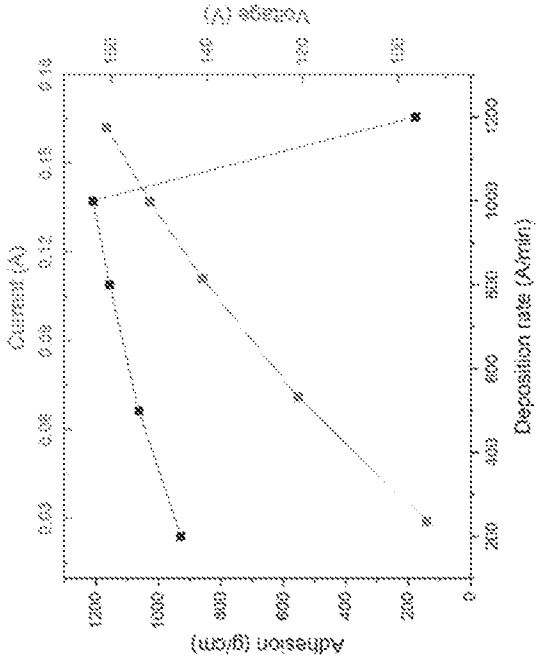


FIG. 18A

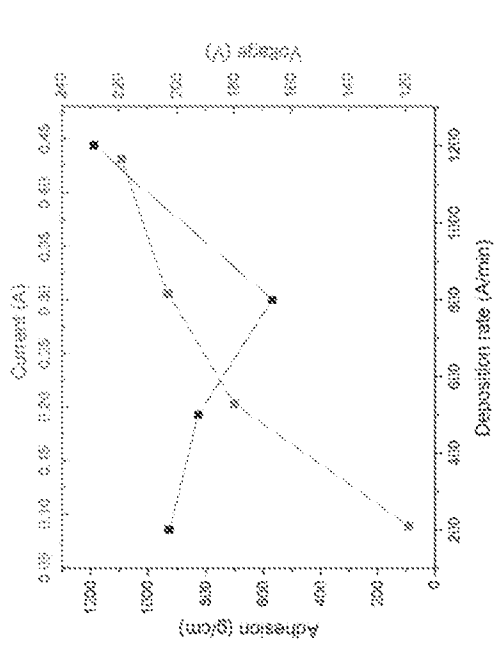


FIG. 18B

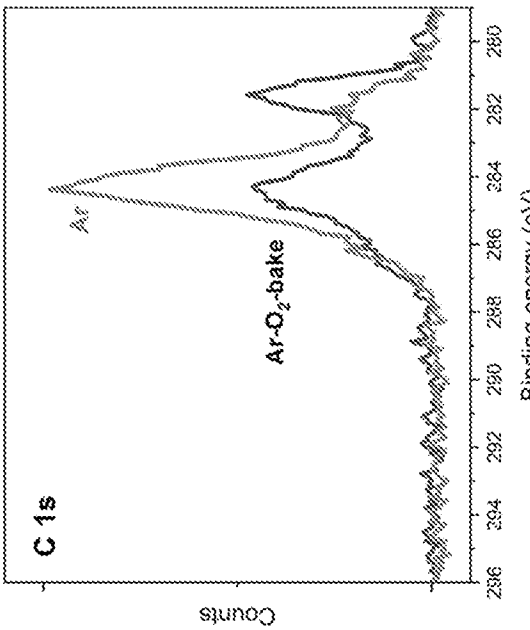


FIG. 20A

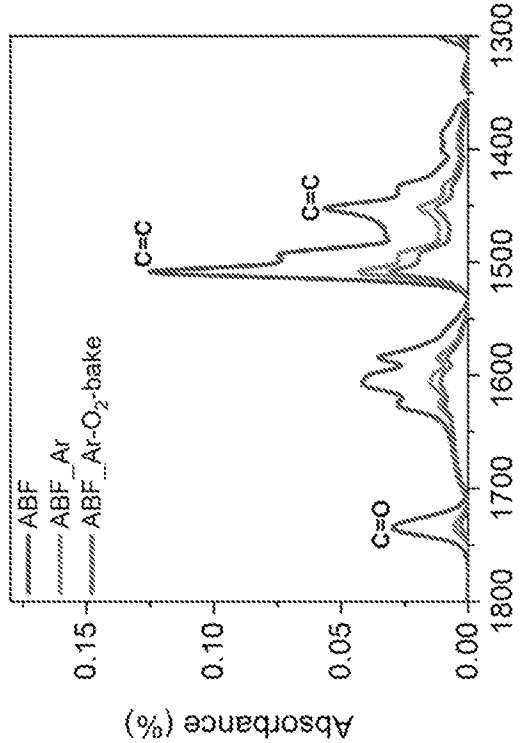


FIG. 20B

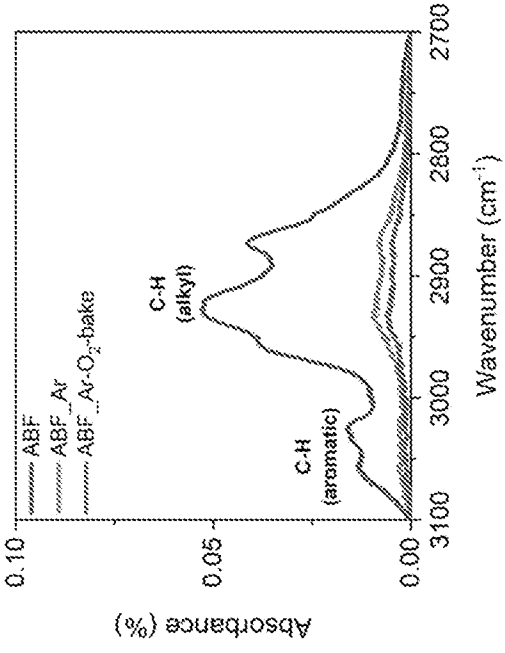


FIG. 20C

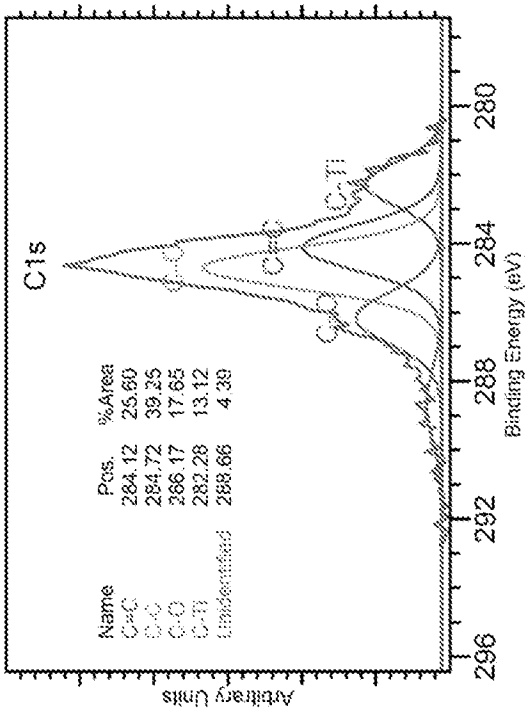


FIG. 21A

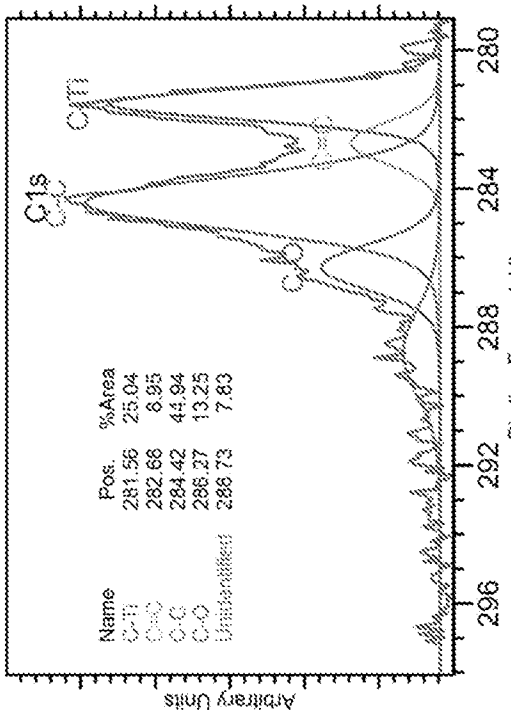


FIG. 21B

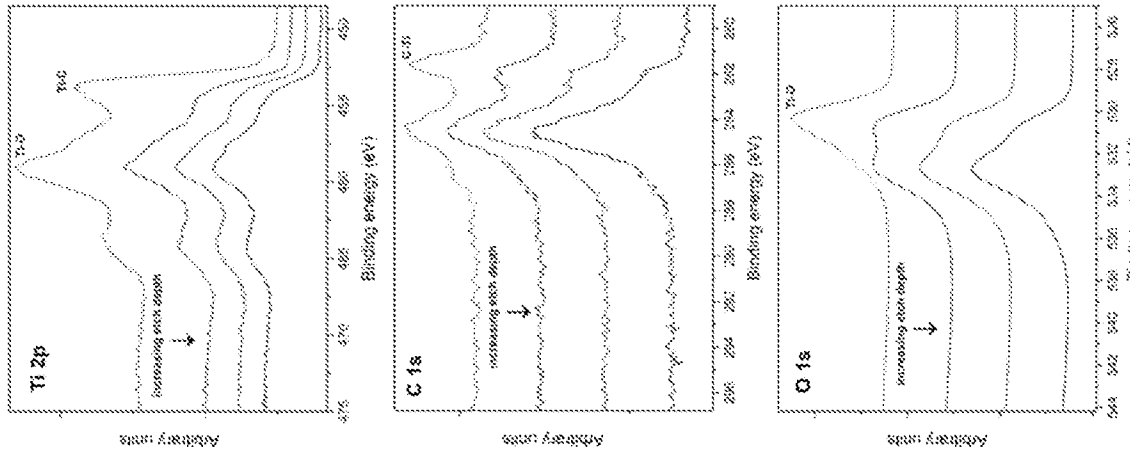


FIG. 22

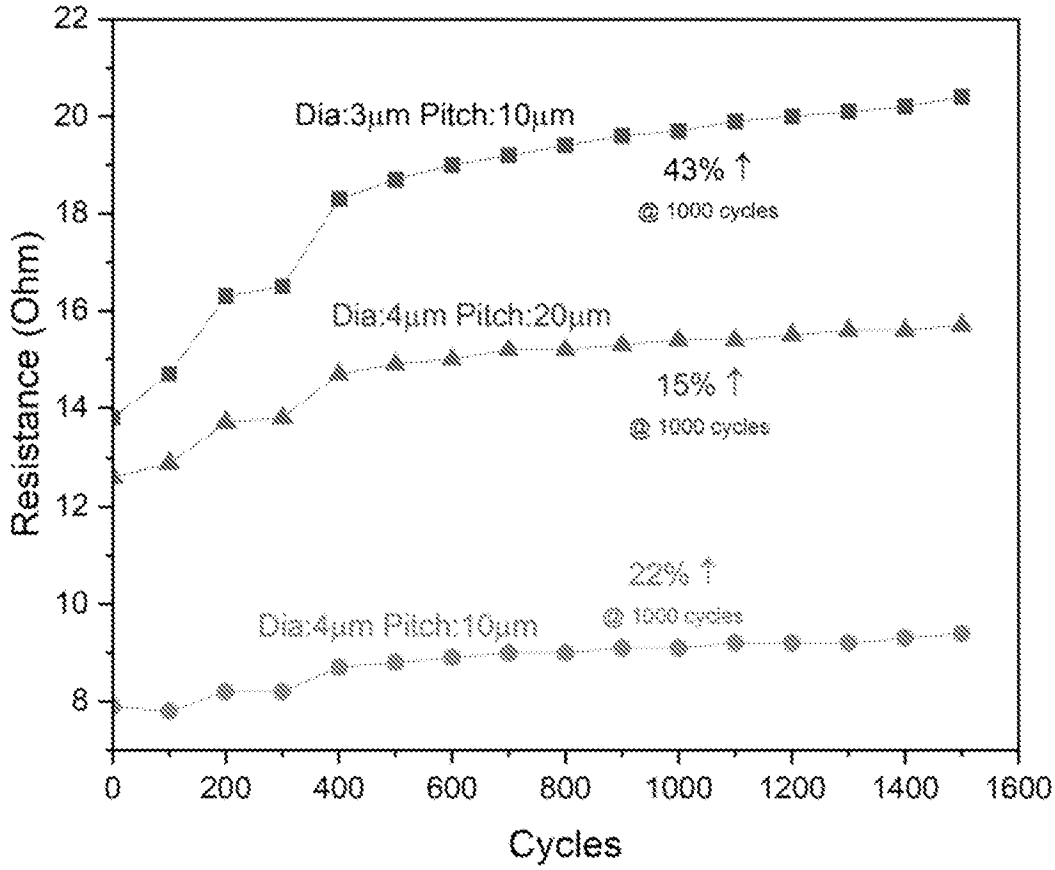

Resistance (Ohm)
Cycles
Dia:3μm Pitch:10μm
43% ↑
@ 1000 cycles
Dia:4μm Pitch:20μm
15% ↑
@ 1000 cycles
Dia:4μm Pitch:10μm
22% ↑
@ 1000 cycles
22
20
18
16
14
12
10
8
0
200
400
600
800
1000
1200
1400
1600

FIG. 23

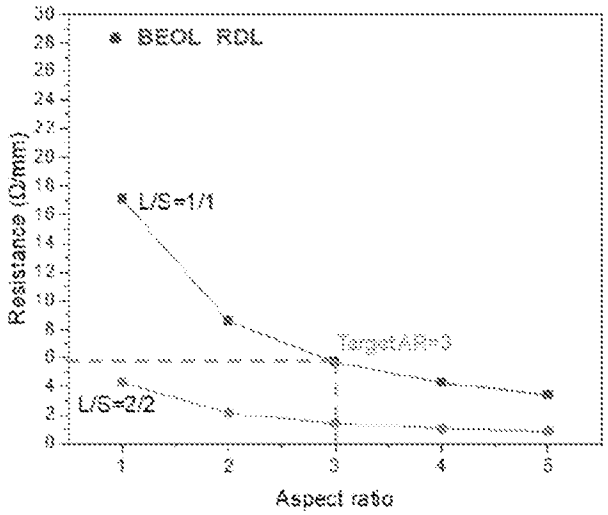


FIG. 24A

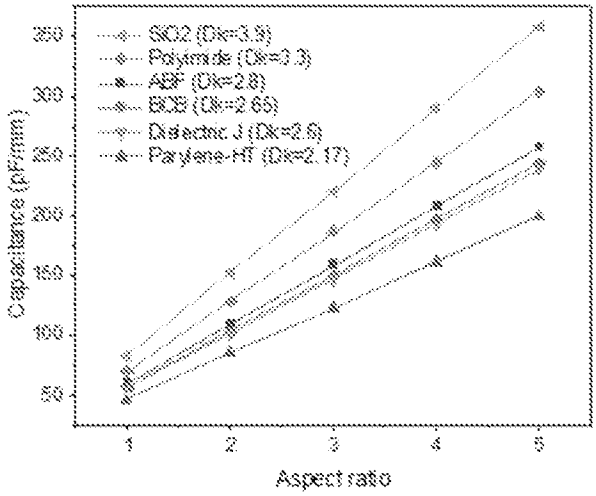
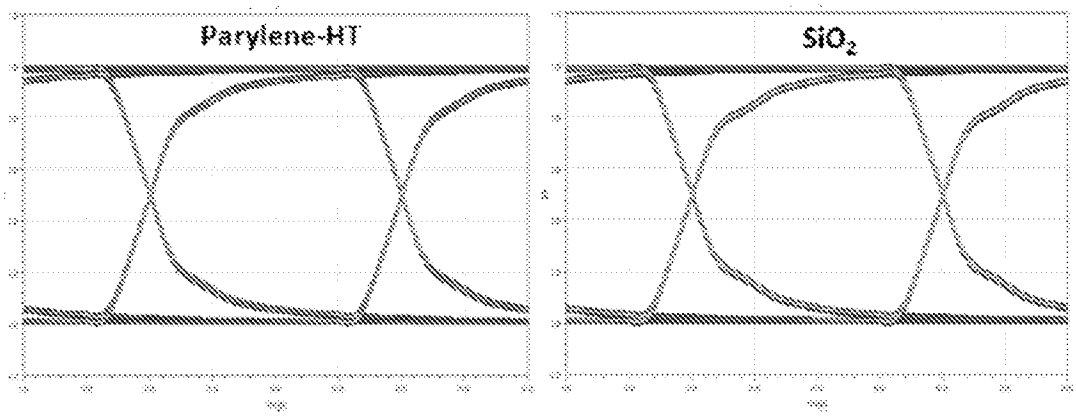


FIG. 24B



Parameter	SiO_2	Parylene-HT
Eye Level Zero	0.0055	0.0019
Eye Level One	0.9886	0.9928
Eye Amplitude	0.9831	0.9909
Eye Height	0.8067	0.8432
Eye Signal To Noise	16.7160 (SI)	20.1186 (SI)
Eye Opening Factor	0.9402 (SI)	0.9503 (SI)
Eye Width	0.9474	0.9549
Eye Jitter P2P	0.0739	0.0599
Eye Jitter RMS	0.0088	0.0075
Min Eye Width	0.9321	0.9461
Min Eye Height	0.7482	0.806

FIG. 25

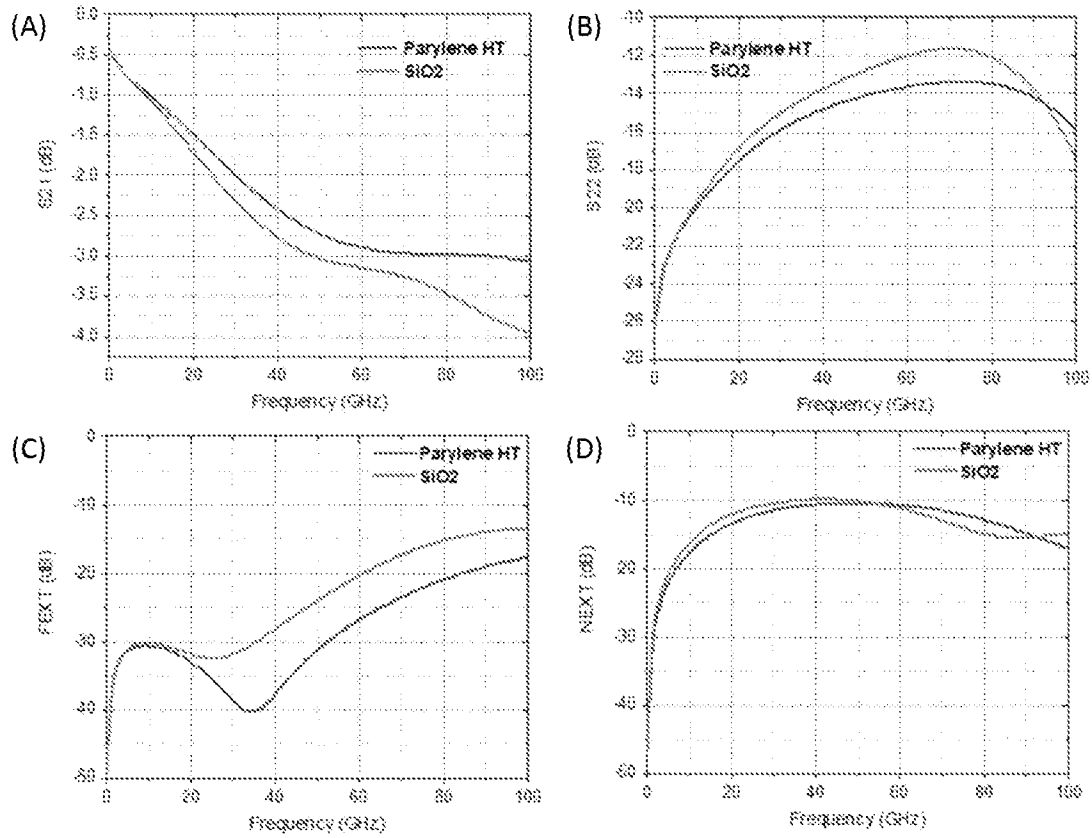
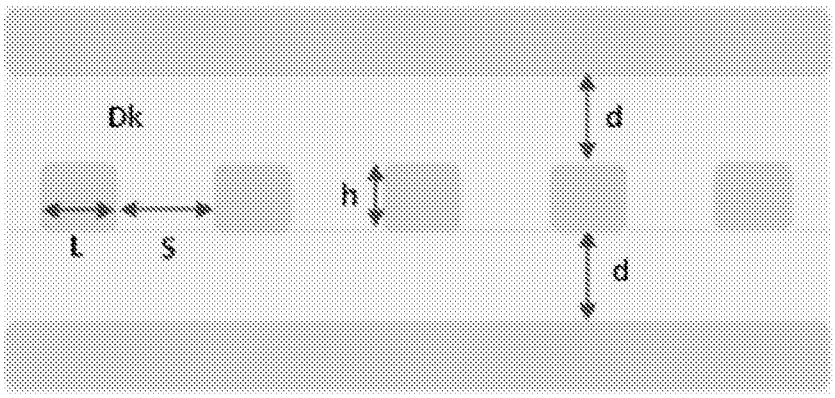


FIG. 26



Simulated Parameters	SiO_2	Parylene-HT
Dielectric constant (D_k)	3.9	2.17
Dielectric loss (D_f)	0.001	0.001
Linewidth and Spacing (L/S)	1/1	1/1
Trace Height (h)	3.5	3.5
Dielectric Thickness (d)	1.3	0.8

FIG. 27

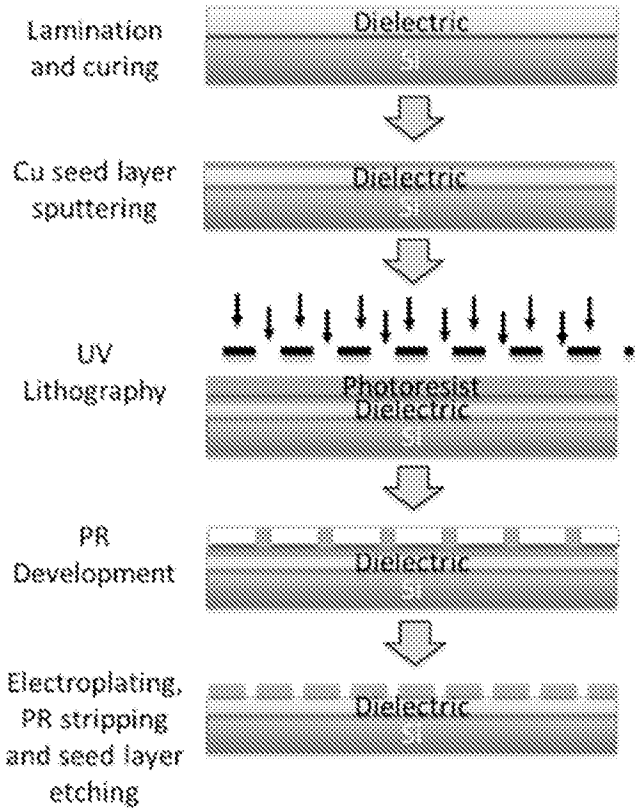


FIG. 28A
(prior art)

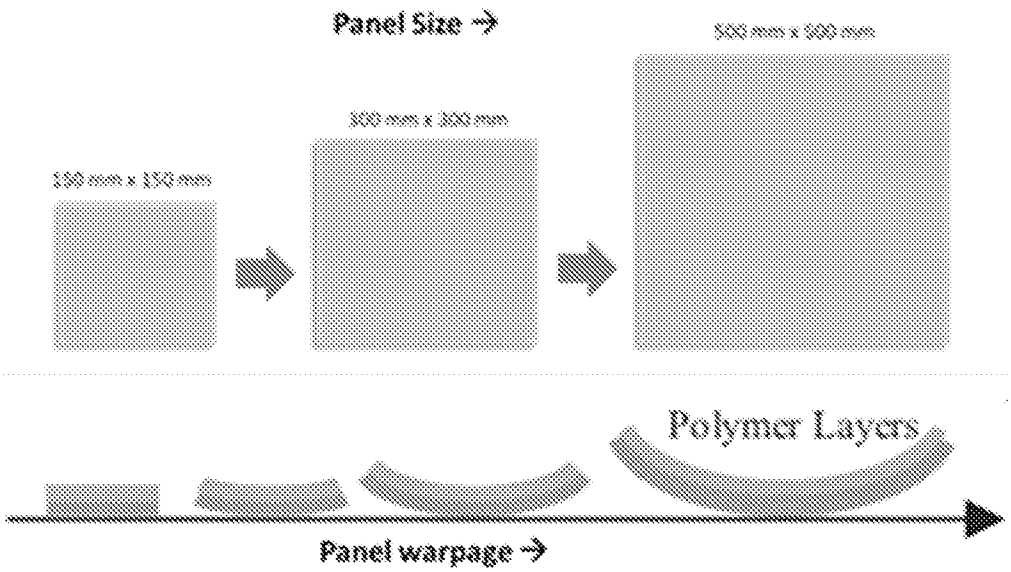


FIG. 28B

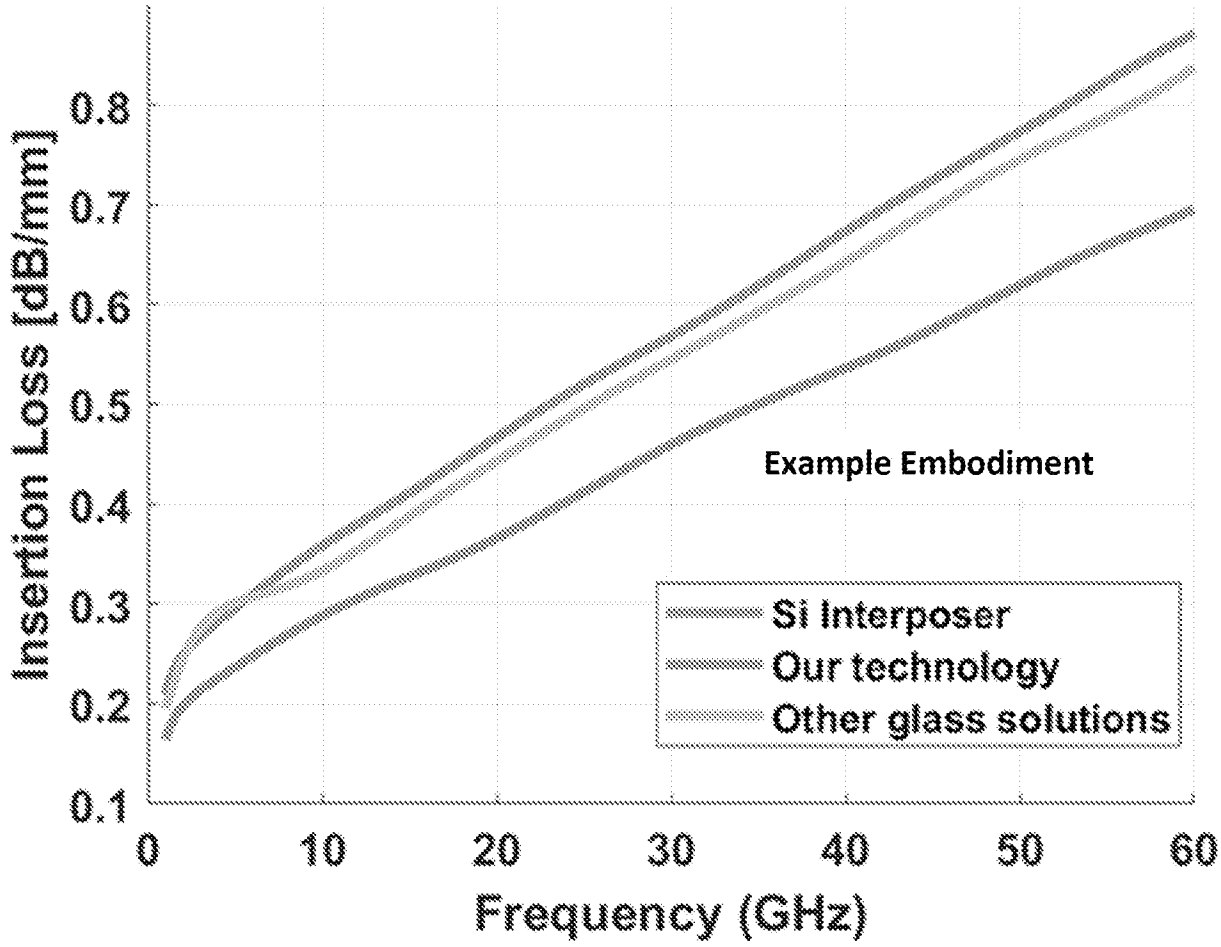

Insertion Loss [dB/mm]
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
10
20
30
40
50
60
Frequency (GHz)
Example Embodiment
Si Interposer
Our technology
Other glass solutions

FIG. 29

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2024/041939

A. CLASSIFICATION OF SUBJECT MATTER

IPC: ***H01L 21/768*** (2024.01); ***H01L 23/528*** (2024.01); *H01L 29/66* (2024.01)

CPC: ***H01L 21/768; H01L 23/528;*** *H01L 29/66*

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

See Search History Document

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

See Search History Document

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

See Search History Document

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
	CN 1216407 C (WINBOND ELECTRONICS) 24 August 2005 (24.08.2005)	
X	see machine translation	11
Y	see machine translation	12-14
	US 2021/0312114 A1 (ICOMETRUE COMPANY LTD.) 07 October 2021 (07.10.2021)	
Y	entire document	12-14
A	entire document	1-8
	US 2011/0252637 A1 (ENDO et al.) 20 October 2011 (20.10.2011)	
A	entire document	1-8
	US 2015/0380302 A1 (LAM RESEARCH CORPORATION) 31 December 2015 (31.12.2015)	
A	entire document	1-8, 11-14
	US 2021/0398991 A1 (TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY LIMITED) 23 December 2021 (23.12.2021)	
A	entire document	1-8, 11-14

☑ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"D" document cited by the applicant in the international application
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
18 September 2024 (18.09.2024)	**04 October 2024 (04.10.2024)**

Name and mailing address of the ISA/US	Authorized officer
Mail Stop PCT, Attn: ISA/US **Commissioner for Patents** **P.O. Box 1450, Alexandria, VA 22313-1450**	**MATOS** **TAINA**
Facsimile No. **571-273-8300**	Telephone No. **571-272-4300**

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2024/041939

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☑ Claims Nos.: **9, 10, 15-26**
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2024/041939

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2022/0238323 A1 (TOKYO ELECTRON LIMITED) 28 July 2022 (28.07.2022) entire document	1-8, 11-14