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Applicant: N.V. Philips' Gloeilampenfabrieken  
Groenewoudseweg 1  
NL-5621 BA Eindhoven(NL)

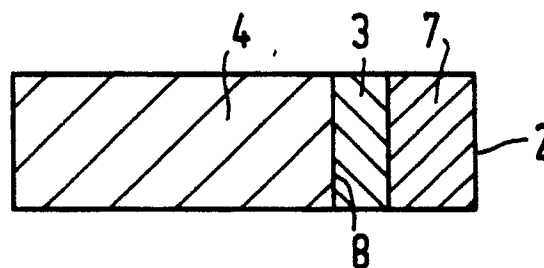
Inventor: Van Gorkom, Gerardus Gegorius  
Petrus  
c/o INT. OCTROOIBUREAU B.V., Prof.  
Holstlaan 6  
NL-5656 AA Eindhoven(NL)  
Inventor: Van Gorkum, Aart Adrianus  
c/o INT. OCTROOIBUREAU B.V., Prof.  
Holstlaan 6

NL-5656 AA Eindhoven(NL)  
Inventor: Van de Walle, Gerjan Franciscus  
Arthur  
c/o INT. OCTROOIBUREAU B.V., Prof.  
Holstlaan 6  
NL-5656 AA Eindhoven(NL)  
Inventor: Van der Heide, Petrus Arthur Marie  
c/o INT. OCTROOIBUREAU B.V., Prof.  
Holstlaan 6  
NL-5656 AA Eindhoven(NL)  
Inventor: Hoeberechts, Arthur Marie Eugène  
c/o INT. OCTROOIBUREAU B.V., Prof.  
Holstlaan 6  
NL-5656 AA Eindhoven(NL)

Representative: Raap, Adriaan Yde et al  
INTERNATIONAAL OCTROOIBUREAU B.V.  
Prof. Holstlaan 6  
NL-5656 AA Eindhoven(NL)

Semiconductor device for generating an electron current.

The efficiency of semiconductor cathodes based on avalanche breakdown is enhanced by using "δ-doping" structures. The quantisation effects introduced thereby decrease the effective work function.



**FIG.4**

### Semiconductor device for generating an electron current.

The invention relates to a semiconductor device for generating an electron current, comprising a cathode having a semiconductor body with at least an n-type semiconductor region and a first p-type semiconductor region, in which electrons leaving the semiconductor body at a surface can be generated in said body by giving the n-type region a positive bias with respect to the p-type region.

The invention also relates to a pick-up tube and a display device provided with such a semiconductor device.

Semiconductor devices of the type described in the opening paragraph are known from Netherlands Patent Application 7905470 (PHN 9532) in the name of the Applicant.

They are used, inter alia, in cathode ray tubes in which they replace the conventional thermionic cathode in which electron emission is generated by heating. In addition they are used in, for example, apparatus for electron microscopy. In addition to the high energy consumption for the purpose of heating, thermionic cathodes have the drawback that they are not immediately ready for operation because they have to be heated sufficiently before emission occurs. Moreover, the cathode material is eventually lost due to evaporation, so that these cathodes have a limited lifetime.

In order to avoid the heating source which is troublesome in practice and also to mitigate the other drawbacks, research has been done in the field of cold cathodes.

The cold cathodes known from the above-mentioned Patent Application are based on the emission of electrons from the semiconductor body when a pn junction is operated in the reverse direction in such a manner that avalanche multiplication occurs. Some electrons may then obtain as much kinetic energy as is required to exceed the electron work function; these electrons are then liberated on the surface and thus supply an electron current.

Moreover, the cathodes described in said Patent Application are provided with an acceleration or gate electrode.

In this type of cathodes the aim is to have a maximum possible efficiency, which can be achieved, inter alia, by a minimum possible work function for the electrons. The latter is realised, for example, by providing the surface of the cathode with a layer of material which decreases the work function. Cesium is preferably used for this purpose because it produces a maximum decrease of the electron work function.

However, the use of cesium may have drawbacks. For example, cesium is very sensitive

to the presence (in its ambience) of oxidising gases (water vapour, oxygen, CO<sub>2</sub>). Moreover, cesium is fairly volatile, which may be detrimental in those uses in which substrates or compounds are present in the vicinity of the cathode such as may be the case, for example, in electron lithography or electron microscopy. The evaporated cesium may then precipitate on these objects.

In order to try and avoid these problems, Netherlands Patent Application no. 8600675 (PHN 11.670) in the name of the Applicant proposes to provide an intrinsic semiconductor layer between the p-type region and the n-type region.

The substantially intrinsic layer introduces in the semiconductor device a region which in the operating condition is completely depleted and in which a maximum field strength prevails substantially throughout this region. As a result, the electrons are generated earlier and at a higher potential energy, while the generated electrons in the intrinsic part undergo a slight scattering of ionised dopant atoms so that the effective free path length is increased.

Since also electron emission is then possible as a result of the tunnel effect, a higher efficiency is achieved.

It is one of the objects of the present invention to enhance the efficiency of such a semiconductor cathode in a different manner.

To this end a semiconductor device according to the invention is characterized in that the n-type region has a thickness of at most 4 nanometers. This thickness is preferably smaller than 2 nanometers.

The invention is based, inter alia, on the recognition that quantisation effects occur at such a small thickness (one or several atomic layers) so that the effective work function is decreased.

It is also based on the recognition that the factor  $e^{-d/\lambda}$  ( $\lambda$ : free path length) which also influences the efficiency becomes considerably larger due to a smaller thickness.

The use of such regions with a thickness of one or several atomic layers is possible by providing so-called "δ-doping" or "Planar Doping" structures. Such an n-type (or p-type) layer may comprise a partly intrinsic top layer due to the special way of providing the structures. Where this Application refers to thin n-type or p-type layers, such a double layer of an n-type or p-type layer and a thin intrinsic layer is also included. An intrinsic layer is then understood to mean a ν-type or π-type layer with a doping of at most  $5 \cdot 10^{16}$  atoms/cm<sup>3</sup>.

To enhance the efficiency to a further extent, the thin n-type layer may also be deliberately sep-

arated from the p-type region by an intrinsic semiconductor layer, similarly as described in Netherlands Patent Application no. 8600675 (PHN 11.670) in the name of the Applicant.

The above-mentioned quantisation effects also occur if the thin n-type layer is present between two p-type regions.

A preferred embodiment of the invention is therefore characterized in that the n-type region is present between the first p-type region and a second p-type surface region.

This second p-type surface region has preferably also a thickness of at most 4 nanometers. An additional advantage of such a device is that, notably for silicon, the distance between the bottom of the conduction band and the vacuum level at some distance from the surface is lower for p-type silicon than for n-type silicon. The second p-type surface region preferably has a thickness of at most 2 micrometers, for example, by forming it again as a "Planar Doping" structure. A part of the first p-type region may also be realised in such a manner.

Another preferred embodiment of a semiconductor device according to the invention is characterized in that the surface has an electrically insulating layer in which at least one aperture is provided, while at least one acceleration electrode is arranged on the insulating layer at the edge of the aperture, and the semiconductor structure, at least within the aperture, locally has a lower breakdown voltage than the other part of the semiconductor structure.

Similar advantages (electron beams with a narrow energy spectrum, lens action) as described in Netherlands Patent Application no. 7905470 can be obtained by providing the semiconductor structure with such an acceleration electrode. For electron-optical functions the acceleration electrode may be split up or, if necessary, an extra electrode may be arranged around the acceleration electrode.

A cathode according to the invention may be advantageously used in a pick-up tube, while there are also various uses for a display device comprising a semiconductor cathode according to the invention. One use is, for example, a display tube having a fluorescent screen which is activated by the electron current originating from the semiconductor device.

Some embodiments of the invention will now be described in greater detail by way of example with reference to the accompanying drawing in which

Fig. 1 diagrammatically shows a comparison between the structure of a semiconductor device according to the invention and that of the device described in Netherlands Patent Application no. 7905470.

Fig. 2 diagrammatically shows a comparison

of the associated prevailing field strength in the semiconductor body,

Fig. 3 shows diagrammatically the associated energy diagrams, while

Fig. 4 shows diagrammatically another structure of a semiconductor device according to the invention, and

Fig. 5 shows some energy diagrams associated with the semiconductor device of Fig. 4.

The Figures are shown diagrammatically and are not to scale, in which for the sake of clarity particularly the dimensions in the direction of thickness have been greatly exaggerated. Semiconductor zones of the same conductivity type are generally shaded in the same direction; corresponding parts in the Figures are generally indicated by the same reference numerals.

The advantages of a semiconductor device according to the invention will now be described with reference to Figs. 1 to 3 and compared with those as described in Netherlands Patent Application no. 7905470. The device described in this Application (Fig. 1a) comprises at a main surface 2 of a semiconductor body 1 an n-type surface region 3 constituting a pn junction 8 with a p-type region 4. The regions 3 and 4 may be biased in the reverse direction with respect to each other so that avalanche multiplication occurs. A part of the electrons which are then liberated may then obtain as much energy as is required to be emitted from the semiconductor body.

In a first device according to the invention (Fig. 1b) the n-type surface region 3 has a thickness of at most 4 nanometers (for example, 2 nanometers). For the sake of the example it has been assumed for the device of Fig. 1 that the p-type region 4 is completely depleted during use. The p-type regions are possibly contacted via a p<sup>+</sup> region 5.

Fig. 2 shows diagrammatically the variation of the field strength for the two devices. For the devices of Fig. 1 a maximum field occurs at the area of the pn junction 8, which field decreases to the value of zero on both sides of the junction at the edges of the depletion zone (line a, b). Such a field variation leads to an electron energy diagram as is shown by means of drawn lines in Fig. 3a for the device of Fig. 1a. Viewed from the surface 2, the electron work function is initially zero until it increases in the depletion zone to a value of approximately 0.8 volt (in silicon) at the area of the pn junction. Since it holds that

$$E = - \frac{dV}{dx}$$

and the field E decreases from this point (see Fig. 2, line a), the curve a in Fig. 3a increases less and less steeply from this point until the electron work function remains constant from the edge of the depletion zone.

A similar curve for the device of Fig. 1b differs

from that of Fig. 3a in that the electron work function will steeply increase at approximately 2 nanometers from the surface (see Fig. 3b) due to the small thickness of the n-type region 3.

To be able to reach the vacuum, the electrons must have an energy which is at least equal to the emission energy  $\phi$ . For an electron which has a potential energy which is equal to or higher than this emission energy  $\phi$  at a distance  $x$  from the surface, the chance of emission is given by  $P = Ae^{-x/\lambda}$ , where  $A$  is a standardising constant and  $\lambda$  is an effective free path length.

For the electrons of the devices described it holds that this chance of electrons just having this potential energy is given by

$$P_a = Ae^{-d_a/\lambda_a}$$

and

$$P_b = Ae^{-d_b/\lambda_b}$$

respectively.

Since  $d_b$  in the device according to the invention is small with respect to the thickness  $d_a$  in the device of Fig. 1, it holds that  $d_b < d_a$ , while  $\lambda_a \approx \lambda_b$  so that  $P_b > P_a$ .

Moreover, due to the small thickness of the layer 3 quantisation effects occur, which are shown as discrete levels 6 in the energy diagram of Fig. 3b. This results in a decrease of the effective emission energy  $\phi$  (distance between the bottom of the conduction band and the vacuum level). Since the total efficiency of the device is determined by  $\eta = Ae^{-x/\lambda} \cdot e^{-\phi/kT}$ , this leads to a further increase of the efficiency. The efficiency can be even further increased by replacing the p-type region 4 by an intrinsic semiconductor region similarly as described in Netherlands Patent Application no. 8600675. The associated energy diagrams are denoted by broken lines in Fig. 3. In this case the effective work function is even further reduced because the quantisation effects cause a more favourable division of the levels 6.

The effect of these quantisation effects can be used to great advantage in the device of Fig. 4 in which a thin n-type region 3 is present between a p-type region 4 and a p-type surface region 7. The n-type region 3 is only several atomic layers thick so that quantisation effects occur of the energy levels and the (quasi) Fermi level comes above the bottom of the conduction band of the n-type region 3 (Fig. 5a). If the p-type surface region 7 (and hence indirectly the n-type region 3) is given a positive bias with respect to the p-type region 4, so

that avalanche multiplication occurs, the electron work function in the region 3 increases until the quasi Fermi level coincides with the bottom of the conduction band of the (preferably highly doped) p-type surface region 7.

Electrons which are generated by simultaneous occurrence of avalanche breakdown of the pn junction 8 fill up the energy levels and cross, as it were, the p-type surface region. To cause a minimum loss of electrons, a small layer thickness ( $< 4$  nanometers) and a high doping is preferably chosen for this p-type region.

An additional advantage is that the effective work function ( $\phi'$  in Fig. 5b) for electrons in p-type silicon is lower than that for electrons in n-type silicon ( $\phi$ , Fig. 5a).

Similarly as the region 3, the p<sup>+</sup>-type surface layer 7 may alternatively be provided by means of techniques resulting in "δ-doping" or "Planar Doping" structures, i.e. techniques which in addition to other suitable techniques (molecular beam epitaxy) can also be used for manufacturing the n-type surface layer 3 in the device of Fig. 1b. In this respect it may be advantageous to manufacture the p-type layer 4 and/or possible intermediate intrinsic layers by means of this technique.

As stated in the opening paragraph, a semiconductor cathode according to the invention may have an insulating layer at its surface 2 on which acceleration electrodes are arranged around apertures for the purpose of emission; the possible forms of the emitting regions and the acceleration electrodes have been described in greater detail in the above-mentioned Netherlands Patent Application no. 7905470. For example, the aperture may be slit-shaped or circular with a gap width or circle diameter of the same order of magnitude as the thickness of the insulating layer. The semiconductor structure usually has a lower breakdown voltage at the area of such apertures. The acceleration electrode (of, for example polycrystalline silicon) may be split up in different manners in which, for example, a part is located inside and another part is located outside a circular gap. Moreover, the surface may be coated, if desired, with a work function-decreasing material such as cesium or barium. Instead of silicon it is alternatively possible to choose an A3-B5 semiconductor material (gallium arsenic).

Semiconductor cathodes according to the invention can be used in pick-up tubes as well as display tubes, but also, for example in electron microscopy.

## Claims

1. A semiconductor device for generating an

electron current, comprising a cathode having a semiconductor body with at least an n-type semiconductor region and a first p-type semiconductor region, in which electrons leaving the semiconductor body at a surface can be generated in said body by giving the n-type region a positive bias with respect to the p-type region, characterized in that the n-type region has a thickness of at most 4 nanometers.

2. A semiconductor device as claimed in Claim 1, characterized in that the thickness of the n-type region is at most 2 nanometers.

3. A semiconductor device as claimed in Claim 1 or 2, characterized in that a substantially intrinsic semiconductor region is present between the first p-type region and the n-type region.

4. A semiconductor device as claimed in Claim 3, characterized in that the substantially intrinsic semiconductor region is of the  $\pi$ -type or the  $\nu$ -type with a maximum impurity concentration of  $5 \cdot 10^{16}$  atoms/cm<sup>3</sup>.

5. A semiconductor device as claimed in Claim 1, 2, 3 or 4, characterized in that the n-type region is present between the first p-type semiconductor region and a second p-type surface region.

6. A semiconductor device as claimed in Claim 5, characterized in that the p-type surface region is highly doped and has a thickness of at most 4 nanometers.

7. A semiconductor device as claimed in Claim 6, characterized in that the thickness of the p-type surface region is at most 2 nanometers.

8. A semiconductor device as claimed in any one of the preceding Claims, characterized in that the first p-type semiconductor region is at least partly highly doped over a thickness of at most 4 nanometers.

9. A semiconductor device as claimed in any one of Claims 1 to 8, characterized in that the surface has an electrically insulating layer in which at least one aperture is provided, while at least one acceleration electrode is arranged on the insulating layer at the edge of the aperture, and the semiconductor structure, at least within the aperture, locally has a lower breakdown voltage than the other part of the semiconductor structure.

10. A semiconductor device as claimed in Claim 9, characterized in that the aperture is slit-shaped or circular with a gap width or a circle diameter which is of the same order of magnitude as the thickness of the insulating layer.

11. A semiconductor device as claimed in Claim 9 or 10, characterized in that the acceleration electrode consists of two or more sub-electrodes.

12. A semiconductor device as claimed in Claim 11, characterized in that the aperture constitutes a substantially annular gap, one sub-electrode being present within the annular gap and one

sub-electrode being present outside the annular gap.

13. A semiconductor device as claimed in Claim 12, characterized in that the centre line of the annular gap constitutes a circle.

14. A semiconductor device as claimed in any one of Claims 9 to 13, characterized in that a second electrode which substantially entirely surrounds the acceleration electrode is provided on the electrically insulating layer.

15. A semiconductor device as claimed in Claims 1 to 14, characterized in that the surface of the semiconductor body is coated with an electron work function-decreasing material at least at the area of the emitting surface.

16. A semiconductor device as claimed in Claim 15, characterized in that the work function-decreasing material is a material from the group of cesium and barium.

17. A semiconductor device as claimed in any one of Claims 1 to 16, characterized in that the semiconductor body consists of silicon or an A3-B5 material.

18. A semiconductor body as claimed in any one of the preceding Claims, characterized in that the acceleration electrode comprises polycrystalline silicon.

19. A pick-up tube provided with means for driving an electron beam, which electron beam scans a charge image, characterized in that the electron beam is generated by means of a semiconductor device as claimed in any one of Claims 1 to 18.

20. A display device provided with means for driving an electron beam, which electron beam produces an image, characterized in that the electron beam is generated by means of a semiconductor device as claimed in any one of Claims 1 to 18.

21. A display device as claimed in Claim 20, characterized in that said display device has a fluorescent screen which is present in vacuo at a few millimeters from the semiconductor device and which is activated by the electron beam originating from the semiconductor device.

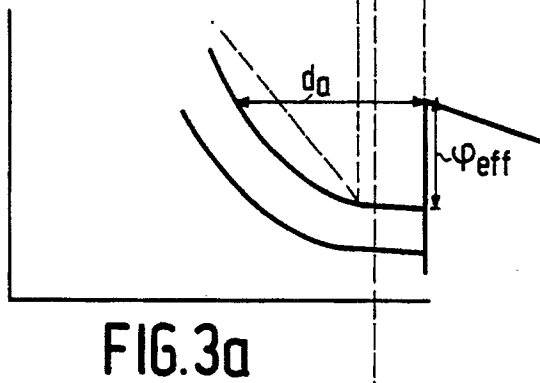
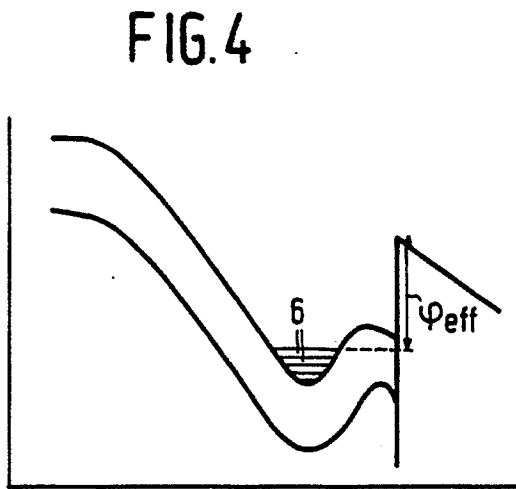
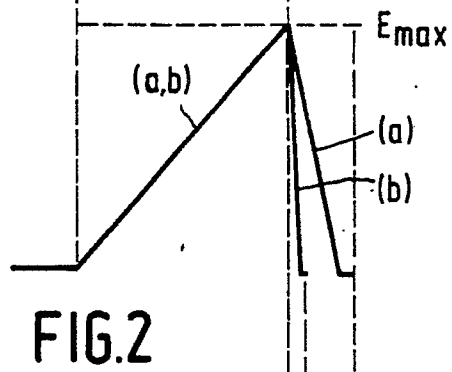
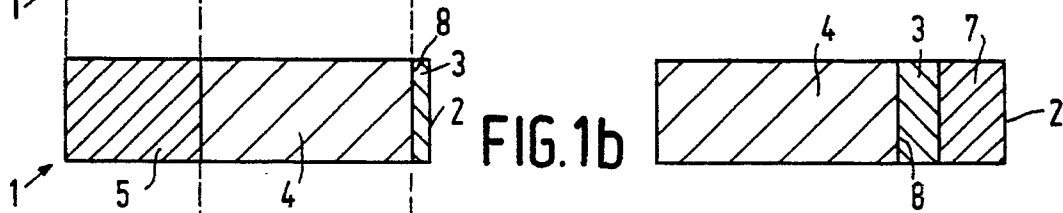
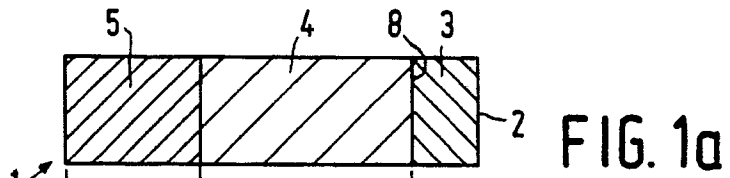


FIG. 5a

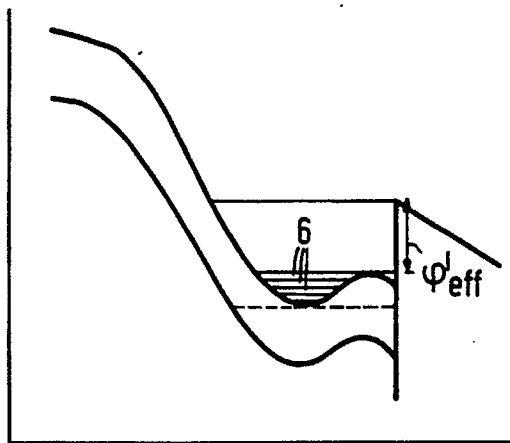
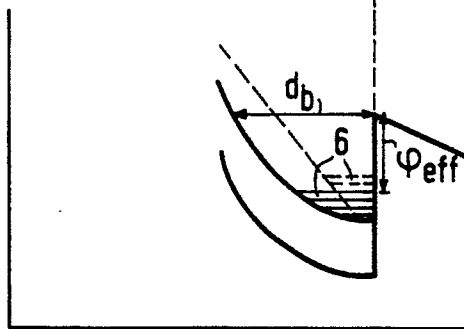


FIG. 3b

FIG. 5b



DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
A	EP-A-0 241 956 (PHILIPS) * Page 3, lines 30-34; page 5, lines 15-17; figure 1 *	1-4, 9, 15, 16	H 01 J 01/30 H 01 L 29/66
A	EP-A-0 257 460 (CANON) * Page 6, lines 7-9; page 14, line 8 - page 15, line 2; page 17, lines 10-18; page 20, lines 15-23; figures 4, 5 *	1, 4, 11, 15, 16	
			TECHNICAL FIELDS SEARCHED (Int. Cl.5)
			H 01 J 1/00
The present search report has been drawn up for all claims			
Place of search <b>THE HAGUE</b>		Date of completion of the search <b>26-09-1990</b>	Examiner <b>ROWLES K. E. G.</b>
<b>CATEGORY OF CITED DOCUMENTS</b> X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document		T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons ..... & : member of the same patent family, corresponding document	