



(51) International Patent Classification:

H01L 27/115 (2017.01) H01L 21/8239 (2006.01)

(21) International Application Number:

PCT/CN2018/104834

(22) International Filing Date:

10 September 2018 (10.09.2018)

(25) Filing Language:

English

(26) Publication Language:

English

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(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN,

(54) Title: MEMORY DEVICE USING COMB-LIKE ROUTING STRUCTURE FOR REDUCED METAL LINE LOADING

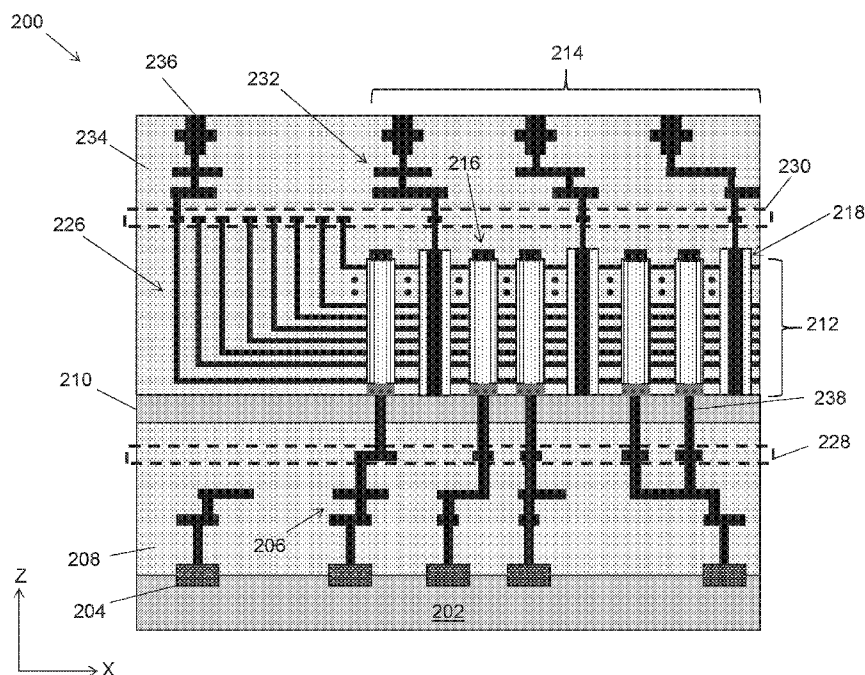


FIG. 2

(57) Abstract: Embodiments of three-dimensional memory device architectures and fabrication methods therefor are disclosed. In an example, the memory device includes a substrate and one or more peripheral devices on the substrate. The memory device also includes one or more interconnect layers and a semiconductor layer disposed over the one or more interconnect layers. A layer stack having alternating conductor and insulator layers is disposed above the semiconductor layer. A plurality of structures extend vertically through the layer stack. A first set of conductive lines are electrically coupled with a first set of the plurality of structures and a second set of conductive lines are electrically coupled with a second set of the plurality of structures different from the first set. The first and second sets of conductive lines are vertically distanced from opposite ends of the plurality of structures.

HR, HU, ID, IL, IN, IR, IS, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (*unless otherwise indicated, for every kind of regional protection available*): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— with international search report (Art. 21(3))

MEMORY DEVICE USING COMB-LIKE ROUTING STRUCTURE FOR REDUCED METAL LINE LOADING

BACKGROUND

[0001] Embodiments of the present disclosure relate to three-dimensional (3D) memory devices and fabrication methods thereof.

[0002] Flash memory devices have undergone rapid development. Flash memory devices can store data for a considerably long time without powering (i.e., they are a form of non-volatile memory), and have advantages such as high integration level, fast access, easy erasing, and rewriting. To further improve the bit density and reduce cost of flash memory devices, three-dimensional NAND flash memory devices have been developed.

[0003] A three-dimensional NAND flash memory device includes a stack of gate electrodes arranged over a substrate, with a plurality of semiconductor channels through and intersecting word lines, into the p- and/or n-type implanted substrate. The bottom/lower gate electrodes function as bottom/lower selective gates (BSG). The top/upper gate electrodes function as top/upper selective gates (TSG). Back-End-of Line (BEOL) Metal plays the role of Bit-Lines (BLs). The word lines/gate electrodes between the top/upper selective gate electrodes and the bottom/lower gate electrodes function as word lines (WLs). The intersection of a word line and a semiconductor channel forms a memory cell. WLs and BLs are typically laid perpendicular to each other (e.g., in an X-direction and a Y-direction), and TSGs are laid in a direction perpendicular to both the WLs and BLs (e.g., in a Z-direction.)

BRIEF SUMMARY

[0004] Embodiments of three-dimensional memory device architectures and fabrication methods therefore are disclosed herein. The disclosed structures and methods provide a staggered fabrication for various metal lines, such as the bit lines, to reduce the density of the metal lines on the same plane. Reducing the metal line density leads to reduced cross-talk between the lines and faster program speeds.

- [0005] In some embodiments, a memory device includes a substrate and one or more peripheral devices on the substrate. The memory device also includes one or more interconnect layers electrically coupled with the one or more peripheral devices, and a semiconductor layer disposed over the one or more interconnect layers. A layer stack having alternating conductor and insulator layers is disposed above the semiconductor layer. A plurality of structures extend vertically through the layer stack. The memory device also includes a first set of conductive lines electrically coupled with a first set of the plurality of structures and a second set of conductive lines electrically coupled with a second set of the plurality of structures different from the first set. The first set of conductive lines are vertically distanced from one end of the plurality of structures and the second set of conductive lines are vertically distanced from an opposite end of the plurality of structures.
- [0006] In some embodiments, the memory device further includes one or more second interconnect layers, the one or more second interconnect layers being electrically coupled to the second set of conductive lines.
- [0007] In some embodiments, the one or more second interconnect layers comprises conductive pads configured to provide electrical connection to external devices.
- [0008] In some embodiments, the plurality of structures includes one or more NAND memory strings.
- [0009] In some embodiments, the one or more NAND strings each includes a plurality of layers surrounding a core insulating material, wherein the plurality of layers includes a blocking layer, a storage layer, a tunneling layer, and a channel layer.
- [0010] In some embodiments, the plurality of structures comprises one or more conductive contacts.
- [0011] In some embodiments, the first set of the plurality of structures includes only the NAND memory strings and the second set of the plurality of structures includes only the conductive contacts.
- [0012] In some embodiments, the second set of conductive lines are located on an opposite side of the semiconductor layer from the first set of conductive lines.
- [0013] In some embodiments, the first semiconductor structure further includes a plurality of conductive pads configured to provide electrical connection to external devices.

- [0014] In some embodiments, the memory device further includes further includes vias extending through a thickness of the semiconductor layer, where the vias electrically contact the first set of conductive lines and the first set of the plurality of structures.
- [0015] In some embodiments, a memory device includes a substrate, a dielectric material disposed on a first surface of the substrate, a semiconductor layer disposed on the dielectric material, and a layer stack having alternating conductor and insulator layers disposed on the semiconductor layer. The memory device also includes a plurality of structures extending vertically through the layer stack. The memory device also includes a first set of conductive lines electrically coupled with a first set of the plurality of structures and a second set of conductive lines electrically coupled with a second set of the plurality of structures different from the first set. The first set of conductive lines are vertically distanced from one end of the plurality of structures and the second set of conductive lines are vertically distanced from an opposite end of the plurality of structures. The memory device also includes one or more peripheral devices formed on a second surface of the substrate, the second surface being opposite to the first surface.
- [0016] In some embodiments, the plurality of structures includes one or more NAND memory strings.
- [0017] In some embodiments, the one or more NAND strings each includes a plurality of layers surrounding a core insulating material, wherein the plurality of layers includes a blocking layer, a storage layer, a tunneling layer, and a channel layer.
- [0018] In some embodiments, the plurality of structures comprises one or more conductive contacts.
- [0019] In some embodiments, the first set of the plurality of structures includes only the NAND memory strings and the second set of the plurality of structures includes only the conductive contacts.
- [0020] In some embodiments, the second set of conductive lines are located on an opposite side of the semiconductor layer from the first set of conductive lines.
- [0021] In some embodiments, the first set of conductive lines are disposed in the dielectric material.
- [0022] In some embodiments, the memory device includes one or more interconnect layers coupled to the one or more peripheral devices.

- [0023] In some embodiments, the memory device further includes further includes vias extending through a thickness of the substrate, where the vias electrically contact the first set of conductive lines and the one or more interconnect layers.
- [0024] In some embodiments, the one or more interconnect layers includes conductive pads designed to provide electrical connection to external devices.
- [0025] In some embodiments, a method to form a memory device includes forming one or more peripheral devices on a substrate and one or more interconnect layers over the one or more peripheral devices. The one or more interconnect layers are electrically coupled with the one or more peripheral devices. The method also includes forming a first set of conductive lines electrically coupled with the one or more interconnect layers, and forming a semiconductor layer over the first set of conductive lines. The method includes forming vias through a thickness of the semiconductor layer where the vias are electrically coupled to the first set of conductive lines. The method also includes forming, on the semiconductor layer, a layer stack having alternating conductor and insulator layers. The method includes forming a plurality of structures each extending vertically through the layer stack. A first set of the plurality of structures is electrically coupled to the first set of conductive lines using the vias. The method also includes forming a second set of conductive lines over an end vertically distanced from the plurality of structures. The second set of conductive lines is electrically coupled to a second set of the plurality of structures different from the first set.
- [0026] In some embodiments, a method to form a memory device includes forming a first set of conductive lines over a first surface of a substrate, the first set of conductive lines being surrounded by a dielectric layer on the first surface of the substrate. The method also includes forming a semiconductor layer over the first set of conductive lines, and forming vias through a thickness of the semiconductor layer. The vias are electrically coupled to the first set of conductive lines. The method also includes forming, on the semiconductor layer, a layer stack having alternating conductor and insulator layers. The method includes forming a plurality of structures each extending vertically through the layer stack. A first set of the plurality of structures is electrically coupled to the first set of conductive lines using the vias. The method also includes forming a second set of conductive lines over an end vertically distanced from the plurality of structures. The

second set of conductive lines are electrically coupled to a second set of the plurality of structures different from the first set. The method also includes forming one or more peripheral devices on a second surface of the substrate opposite from the first surface.

[0027] The three-dimensional memory devices provided by the present disclosure include bit lines and other metal routing lines that are provided at different heights above (or below) the substrate such that they are not densely packed on the same plane.

BRIEF DESCRIPTION OF THE DRAWINGS

[0028] Aspects of the present disclosure are best understood from the following detailed description when reading with the accompanying figures. It is noted that, in accordance with the common practice in the industry, various features are not drawn to scale. In fact, the dimensions of the various features may be arbitrarily increased or reduced for clarity of illustration and discussion.

[0029] FIG. 1 is an illustration of a three-dimensional memory device.

[0030] FIG. 2 illustrates a cross-section view of a three-dimensional memory device, according to some embodiments.

[0031] FIG. 3 illustrates a cross-section view of another three-dimensional memory device, according to some embodiments.

[0032] FIGs. 4A-4H illustrate side views of a three-dimensional memory structure at different stages of an exemplary fabrication process, according to some embodiments.

[0033] FIGs. 5A – 5E illustrate side views of another three-dimensional memory structure at different stages of an exemplary fabrication process, according to some embodiments.

[0034] FIG. 6 is an illustration of a fabrication process for forming a three-dimensional memory structure, according to some embodiments.

[0035] FIG. 7 is an illustration of another fabrication process for forming a three-dimensional memory structure, according to some embodiments.

DETAILED DESCRIPTION

- [0036] Although specific configurations and arrangements are discussed, it should be understood that this is done for illustrative purposes only. A person skilled in the pertinent art will recognize that other configurations and arrangements can be used without departing from the spirit and scope of the present disclosure. It will be apparent to a person skilled in the pertinent art that the present disclosure can also be employed in a variety of other applications.
- [0037] It is noted that references in the specification to “one embodiment,” “an embodiment,” “an example embodiment,” “some embodiments,” etc., indicate that the embodiment described may include a particular feature, structure, or characteristic, but every embodiment may not necessarily include the particular feature, structure, or characteristic. Moreover, such phrases do not necessarily refer to the same embodiment. Further, when a particular feature, structure or characteristic is described in connection with an embodiment, it would be within the knowledge of a person skilled in the pertinent art to effect such feature, structure or characteristic in connection with other embodiments whether or not explicitly described.
- [0038] In general, terminology may be understood at least in part from usage in context. For example, the term “one or more” as used herein, depending at least in part upon context, may be used to describe any feature, structure, or characteristic in a singular sense or may be used to describe combinations of features, structures or characteristics in a plural sense. Similarly, terms, such as “a,” “an,” or “the,” again, may be understood to convey a singular usage or to convey a plural usage, depending at least in part upon context.
- [0039] It should be readily understood that the meaning of “on,” “above,” and “over” in the present disclosure should be interpreted in the broadest manner such that “on” not only means “directly on” something but also includes the meaning of “on” something with an intermediate feature or a layer therebetween, and that “above” or “over” not only means the meaning of “above” or “over” something but can also include the meaning it is “above” or “over” something with no intermediate feature or layer therebetween (i.e., directly on something).

[0040] Further, spatially relative terms, such as “beneath,” “below,” “lower,” “above,” “upper,” and the like, may be used herein for ease of description to describe one element or feature’s relationship to another element(s) or feature(s) as illustrated in the figures. The spatially relative terms are intended to encompass different orientations of the device in use or operation in addition to the orientation depicted in the figures. The apparatus may be otherwise oriented (rotated 90 degrees or at other orientations) and the spatially relative descriptors used herein may likewise be interpreted accordingly.

[0041] As used herein, the term “substrate” refers to a material onto which subsequent material layers are added. The substrate itself can be patterned. Materials added on top of the substrate can be patterned or can remain unpatterned. Furthermore, the substrate can include a wide array of semiconductor materials, such as silicon, germanium, gallium arsenide, indium phosphide, etc. Alternatively, the substrate can be made from an electrically non-conductive material, such as a glass, a plastic, or a sapphire wafer.

[0042] As used herein, the term “layer” refers to a material portion including a region with a thickness. A layer can extend over the entirety of an underlying or overlying structure, or may have an extent less than the extent of an underlying or overlying structure. Further, a layer can be a region of a homogeneous or inhomogeneous continuous structure that has a thickness less than the thickness of the continuous structure. For example, a layer can be located between any pair of horizontal planes between, or at, a top surface and a bottom surface of the continuous structure. A layer can extend horizontally, vertically, and/or along a tapered surface. A substrate can be a layer, can include one or more layers therein, and/or can have one or more layer thereupon, thereabove, and/or therebelow. A layer can include multiple layers. For example, an interconnect layer can include one or more conductor and contact layers (in which contacts, interconnect lines, and/or vias are formed) and one or more dielectric layers.

[0043] As used herein, the term “nominal/nominally” refers to a desired, or target, value of a characteristic or parameter for a component or a process operation, set during the design phase of a product or a process, together with a range of values above and/or below the desired value. The range of values can be due to slight variations in manufacturing processes or tolerances. As used herein, the term “about” indicates the value of a given quantity that can vary based on a particular technology node associated

with the subject semiconductor device. Based on the particular technology node, the term “about” can indicate a value of a given quantity that varies within, for example, 10–30% of the value (e.g., $\pm 10\%$, $\pm 20\%$, or $\pm 30\%$ of the value).

[0044] As used herein, the term “3D memory device” refers to a semiconductor device with vertically oriented strings of memory cell transistors (referred to herein as “memory strings,” such as NAND strings) on a laterally-oriented substrate so that the memory strings extend in the vertical direction with respect to the substrate. As used herein, the term “vertical/vertically” means nominally perpendicular to the lateral surface of a substrate.

[0045] In the present disclosure, for ease of description, “tier” is used to refer to elements of substantially the same height along the vertical direction. For example, a word line and the underlying gate dielectric layer can be referred to as “a tier,” a word line and the underlying insulating layer can together be referred to as “a tier,” word lines of substantially the same height can be referred to as “a tier of word lines” or similar, and so on.

[0046] Any of the memory devices described herein can be used in an electronic system, such as, for example, portable electronics, computers, or wearable electronics.

[0047] FIG. 1 illustrates a portion of a three-dimensional NAND flash memory device 100. The flash memory device 100 includes a substrate 101, an insulating layer 103 over substrate 101, a tier of lower selective gate electrodes 104 over the insulating layer 103, and a plurality of tiers of control gate electrodes 107 stacking on top of bottom selective gate electrodes 104 to form an alternating conductor/dielectric stack. The flash memory device also includes a tier of upper selective gate electrodes 109 over the stack of control gate electrodes 107, doped source line regions 120 in portions of substrate 101 between adjacent lower selective gate electrodes 104, and NAND strings 114 through upper selective gate electrodes 109, control gate electrodes 107, lower selective gate electrodes 104, and insulating layer 103. NAND strings 114 includes a memory film 113 over the inner surface of NAND strings 114 and a core filling film 115 surrounded by memory film 113. The flash memory device 100 further includes a plurality of bit lines 111 connected to NAND strings 114 over upper selective gate electrodes 109 and a plurality of metal interconnects 119 connected to the gate electrodes through a plurality of metal

contacts 117. Insulating layers between adjacent tiers of gate electrodes are not shown in FIG. 1 for clarity. The gate electrodes include upper selective gate electrodes 109, control gate electrodes 107 (e.g., also referred to as the word lines), and lower selective gate electrodes 104.

[0048] In FIG. 1, for illustrative purposes, three tiers of control gate electrodes 107-1, 107-2, and 107-3 are shown together with one tier of upper selective gate electrodes 109 and one tier of lower selective gate electrodes 104. Each tier of gate electrodes have substantially the same height over substrate 101. The gate electrodes of each tier are separated by gate line slits 108-1 and 108-2 through the stack of gate electrodes. Each of the gate electrodes in a same tier is conductively connected to a metal interconnect 119 through a metal contact 117. That is, the number of metal contacts formed on the gate electrodes equals the number of gate electrodes (i.e., the sum of all upper selective gate electrodes 109, control gate electrodes 107, and lower selective gate electrodes 104). Further, the same number of metal interconnects is formed to connect to each metal contact via. In some arrangements, additional metal contacts are formed to connect to other structures beyond the gate electrodes, such as, for example, dummy structures.

[0049] When forming NAND strings 114, other vertical structures may also be formed that extend through the tiers of control gate electrodes 107-1, 107-2, and 107-3 down to substrate 101. Examples of other vertical structures include through array contacts (TACs) that may be used to make electrical connection with components above and/or below the tiers of gate electrodes. These other vertical structures are not illustrated in FIG. 1 for clarity.

[0050] For illustrative purposes, similar or same parts in a three-dimensional NAND device are labeled using same element numbers. However, element numbers are merely used to distinguish relevant parts in the Detailed Description and do not indicate any similarity or difference in functionalities, compositions, or locations. Structure 200 illustrated in FIG. 2 provides a side view of a three-dimensional NAND memory device, according to some embodiments. Structure 300 illustrated in FIG. 3 provides a side view of another three-dimensional NAND memory device, according to some embodiments. FIGs. 4A – 4H illustrate an example fabrication process for forming the three-dimensional NAND memory device illustrated in FIG. 2, according to some

embodiments. FIGs. 5A – 5E illustrate an example fabrication process for forming the three-dimensional NAND memory device illustrated in FIG. 3, according to some embodiments. Other parts of the memory devices are not shown for ease of description. Although using three-dimensional NAND devices as examples, in various applications and designs, the disclosed structures can also be applied in similar or different semiconductor devices to, e.g., reduce the density of metal connections or wiring. The specific application of the disclosed structures should not be limited by the embodiments of the present disclosure. For illustrative purposes, word lines and gate electrodes are used interchangeably to describe the present disclosure.

[0051] FIG. 2 illustrates an exemplary memory device 200, according to some embodiments. Memory device 200 includes a substrate 202. Substrate 202 can provide a platform for forming subsequent structures. Such subsequent structures are formed on a front (e.g., top) surface of substrate 202. And such subsequent structures are said to be formed in a vertical direction (e.g., orthogonal to the front surface of substrate 202.) In FIG. 2, and for all subsequent illustrated structures, the X and Y directions are along a plane parallel to the front and back surfaces of substrate 202, while the Z direction is in a direction orthogonal to the front and back surfaces of substrate 202.

[0052] In some embodiments, substrate 202 includes any suitable material for forming the three-dimensional memory device. For example, substrate 202 can include silicon, silicon germanium, silicon carbide, silicon on insulator (SOI), germanium on insulator (GOI), glass, gallium nitride, gallium arsenide, and/or other suitable III-V compound.

[0053] Substrate 202 can include one or more peripheral devices 204. Peripheral devices 204 can be formed “on” substrate 202, in which the entirety or part of the peripheral device 204 is formed in substrate 202 (e.g., below the top surface of substrate 202) and/or directly on substrate 202. Any of peripheral devices 204 can include transistors formed on substrate 202. Doped regions to form source/drain regions of the transistors can be formed in substrate 202 as well, as would be understood to one skilled in the relevant art.

[0054] In some embodiments, peripheral devices 204 can include any suitable digital, analog, and/or mixed-signal peripheral circuits used for facilitating the operation of memory device 200. For example, peripheral devices 204 can include one or more of a page buffer, a decoder (e.g., a row decoder and a column decoder), a sense amplifier, a

driver, a charge pump, a current or voltage reference, or any active or passive components of the circuits (e.g., transistors, diodes, resistors, or capacitors). In some embodiments, peripheral devices 204 are formed on substrate 202 using complementary metal-oxide-semiconductor (CMOS) technology (also known as a “CMOS chip”).

[0055] One or more peripheral interconnect layers 206 can be included above peripheral devices 204 to transfer electrical signals to and from peripheral devices 204. Peripheral interconnect layers 206 can include one or more contacts and one or more interconnect conductor layers each including one or more interconnect lines and/or vias. As used herein, the term “contact” can broadly include any suitable types of interconnects, such as middle-end-of-line (MEOL) interconnects and back-end-of-line (BEOL) interconnects, including vertical interconnect accesses (e.g., vias) and lateral lines (e.g., interconnect lines). Peripheral interconnect layers 206 can further include one or more interlayer dielectric (ILD) layers, generally represented by dielectric material 208. The contacts and the conductor layers in peripheral interconnect layers 206 can include conductor materials including, but not limited to, tungsten (W), cobalt (Co), copper (Cu), aluminum (Al), silicides, or any combination thereof. Dielectric material 208 can include silicon oxide, silicon nitride, silicon oxynitride, doped silicon oxide, or any combination thereof.

[0056] A semiconductor layer 210 is disposed over dielectric material 208 and peripheral interconnect layers 206, according to some embodiments. Semiconductor layer 210 can be epitaxially grown silicon or any other epitaxially grown semiconducting material. Semiconductor layer 210 can also be deposited using well-known vapor deposition techniques such as chemical vapor deposition (CVD) or physical vapor deposition (PVD) techniques.

[0057] A layer stack 212 that includes alternating conductor and insulator layers is disposed on semiconductor layer 210. Any number of alternating conductor/insulator layers may be used in layer stack 212. The conductor layers can each have the same thickness or have different thicknesses. Similarly, the insulator layers can each have the same thickness or have different thicknesses. The conductor layers can include conductor materials including, but not limited to, W, Co, Cu, Al, doped silicon, silicides, or any combination thereof. The insulator layers can include dielectric materials including, but

not limited to, silicon oxide, silicon nitride, silicon oxynitride, or any combination thereof. In some embodiments, the insulator layers represent empty space (e.g., vacuum).

[0058] Extending vertically through layer stack 212, and over semiconductor layer 210, is a plurality of structures 214. Plurality of structures 214 can include any number of NAND memory strings 216 and/or conductive contacts 218. Each of NAND memory strings 216 provides a plurality of memory bit locations controlled by voltage applied to corresponding word lines (e.g., the conductor layers of layer stack 212). One or both of the conductive top and bottom portions of each of NAND memory strings 216 can be coupled to bit lines that control current flow through a channel layer of each NAND memory string 216.

[0059] Conductive contacts 218 can be through array contacts (TAC). Conductive contacts 218 can extend through layer stack 212 and deliver signals to conductive layers or pads disposed both above and below layer stack 212.

[0060] According to some embodiments, memory device 200 includes two different levels of contact lines for making contact with each of plurality of structures 214. For example, a first set of conductive lines 228 can be located on one side of plurality of structures 214 (in the z direction), and a second set of conductive lines 230 can be located on an opposite side of plurality of structures 214 (in the z direction). Each of first and second sets of conductive lines 228 and 230 can include bit lines coupled to one or more of NAND memory strings 216, word lines coupled to the conductive layers of layer stack 212 using conductive vias 226, and other contact lines coupled to conductive contacts 218. By splitting such conductive lines between separate locations, the density of the lines in a single location is decreased, leading to reduced cross-talk and faster operation speeds of memory device 200.

[0061] The various conductive lines may be staggered between first set of conductive lines 228 and second set of conductive lines 230 in any fashion. The staggering of the conductive lines can create a comb-like arrangement of the conductive lines. In one example, each of conductive contacts 218 is connected to a corresponding conductive line in second set of conductive lines 230, and each of NAND memory strings 216 is connected to a corresponding bit line in first set of conductive lines 228. Each of NAND memory strings 216 can be connected to a corresponding bit line in first set of conductive

lines 228 using vias 238 through a thickness of semiconductor layer 210. In another example, the conductive lines alternate between being located in either first set of conductive lines 228 or second set of conductive lines 230 along the x-direction for each of plurality of structures 214. In yet another example, the bit lines connected to NAND memory strings 216 are staggered such that the bit lines alternate between being located in first set of conductive lines 228 and second set of conductive lines 230 along the x-direction for each of NAND memory strings 216. Any other arrangements are possible as well, so long as the conductive lines coupled to each of plurality of structures 214 are not all located along the same plane.

[0062] In some embodiments, any first set of structures of plurality of structures 214 can be coupled to conductive lines in the first set of conductive lines 228, and any second set of structures of plurality of structures 214 can be coupled to conductive lines in the second set of conductive lines 230. In some embodiments, the first set of structures can include all NAND memory strings 216 and the second set of structures can include all conductive contacts 218. The first set of structures can be different than the second set of structures. Furthermore, in some embodiments, the first set of structures includes entirely different structures than the second set of structures. In some embodiments, second set of conductive lines 230 are disposed over an opposite side of semiconductor layer 210 in the z-direction compared to first set of conductive lines 228.

[0063] Memory device 200 includes one or more interconnect layers 232 having substantially the same properties as peripheral interconnect layers 206. Interconnect layers 232 can further include one or more interlayer dielectric (ILD) layers, generally represented by dielectric material 234. Dielectric material 234 can be similar to dielectric material 208. Interconnect layers 232 can include conductive pads 236 at a top surface of semiconductor device 200. Conductive pads 236 can be used to provide electrical connection to external devices and their use would be well understood to a person skilled in the relevant art.

[0064] FIG. 3 illustrates another example of a memory device 300, according to some embodiments. Memory device 300 is similar to memory device 200 and includes many of the same components, the details of which are not repeated in the description of memory device 300. However, the location and orientation of certain components are different

between memory device 200 and memory device 300. The various components of memory device 200 are each disposed over one surface of substrate 202, while the various components of memory device 300 can be disposed on either surface of substrate 302. Substrate 302 can have similar properties as substrate 202. In some embodiments, substrate 302 is thinner than substrate 202.

[0065] Over a first surface of substrate 302, memory device 300 includes a dielectric material 306 followed by semiconductor layer 210. The formation of the memory array above semiconductor layer 210 is similar to that described in memory device 200.

[0066] Memory device 300 similarly includes two levels of contact lines for making contact with each of plurality of vertical structures 214. For example, a first set of conductive lines 303 can be located on one side of plurality of structures 214 (in the z direction), and a second set of conductive lines 304 can be located on an opposite side of plurality of structures 214 (in the z direction). The first set of conductive lines 303 can be located within dielectric material 306. First set of conductive lines 303 and second set of conductive lines 304 can be connected to various ones of plurality of structures 214 as described above for memory device 200.

[0067] Memory device 300 includes one or more peripheral devices 204 formed on a second surface of substrate 302 that is opposite from the first surface. One or more peripheral devices can be electrically coupled with peripheral interconnect layers 206 surrounded by dielectric material 208 as described above for memory device 200. Additionally, one or more of peripheral devices 204 can be electrically coupled to one or more of the first set of conductive lines 303 using vias 308 passing through a thickness of substrate 302.

[0068] Peripheral interconnect layers 206 can include conductive pads 310 at a top surface of semiconductor device 300. Conductive pads 310 can be used to provide electrical connection to external devices and their use would be well understood to a person skilled in the relevant art.

[0069] FIGs. 4A – 4H illustrate an example fabrication process for forming memory device 200. FIG. 4A illustrates the formation of peripheral devices 204 on substrate 202. Peripheral devices 204 can include a plurality of transistors formed on substrate 202. The transistors can be formed by a plurality of processing steps including, but not limited to,

photolithography, dry/wet etch, thin film deposition, thermal growth, implantation, chemical mechanical polishing (CMP), or any combination thereof. In some embodiments, doped regions are formed in substrate 202, which function, for example, as source regions and/or drain regions of the transistors. In some embodiments, isolation regions, such as shallow trench isolation (STI), is also formed in substrate 202. These particular features are not explicitly illustrated as they are well understood structures to a person skilled in the relevant art. Any arrangement of transistors or electrically passive devices (e.g., capacitors, resistors, etc.) may be provided on substrate 202.

[0070] FIG. 4B illustrates the formation of a first interconnect layer above peripheral devices 204. The first interconnect layer includes one or more contacts 402 and patterned conductor layers 404. Contacts 402 can be provided to contact either patterned features of peripheral devices 204 or portions of substrate 202. Conductor layers 404 represent conductive traces that extend into and out of the page. Contacts 402 and patterned conductor layers 404 can include conductor materials deposited by one or more thin film deposition processes including, but not limited to, CVD, PVD, ALD, electroplating, electroless plating, or any combination thereof. Fabrication processes to form the contacts and conductor layers can also include photolithography, CMP, wet/dry etch, or any combination thereof.

[0071] One or more deposited dielectric layers are represented by dielectric material 208. Dielectric material 208 can represent any number of deposited dielectric layers that include materials deposited by one or more thin film deposition processes including, but not limited to, CVD, PVD, ALD, or any combination thereof.

[0072] FIG. 4C illustrates the formation of one or more additional interconnect layers to form peripheral interconnect layers 206. Any number of interconnect layers may be formed each having vias connecting different levels of conductor layers. Additional dielectric layers are also deposited to increase a total thickness of dielectric material 208. A top surface 406 of dielectric material 208 can be planarized using a polishing technique, such as chemical mechanical polishing (CMP), according to some embodiments.

[0073] FIG. 4D illustrates the formation of semiconductor layer 210 over peripheral interconnect layers 206. Semiconductor layer 210 can be silicon that is epitaxially grown or any other semiconducting material that can be epitaxially grown. Semiconductor layer

210 can also be deposited using well-known vapor deposition techniques such as chemical vapor deposition (CVD) or physical vapor deposition (PVD) techniques.

According to some embodiments, one or more conductive vias 238 are formed through a thickness of semiconductor layer 210. Conductive vias 238 can be electrically coupled with one or more layers of peripheral interconnect layers 206.

[0074] FIG. 4E illustrates the formation of a layer stack 408 having alternating sacrificial layers 410 and dielectric layers 412 formed over semiconductor layer 210, according to some embodiments.

[0075] The formation of layer stack 408 can involve depositing sacrificial layers 410 to each have the same thickness or to have different thicknesses. Example thicknesses of sacrificial layers 410 can range from 10 nm to 60 nm. Similarly, dielectric layers 412 can each have the same thickness or have different thicknesses. Example thicknesses of dielectric layers 412 can range from 10 nm to 60 nm.

[0076] The dielectric material of sacrificial layers 410 is different from the dielectric material of dielectric layers 412, according to some embodiments. For example, each of sacrificial layers 410 can be silicon nitride while each of dielectric layers 412 can be silicon dioxide. Other example materials for each of sacrificial layers 410 include poly-crystalline silicon, poly-crystalline germanium, and poly-crystalline germanium-silicon. The dielectric materials used for any of dielectric layers 412 or sacrificial layers 410 can include silicon oxide, silicon nitride, silicon oxynitride, or any combination thereof. It should be understood that any number of dielectric layers may be included in layer stack 408.

[0077] Layer stack 408 includes a portion having a staircase structure where each of at least sacrificial layers 410 terminate at a different length in the horizontal 'X' direction. This staircase structure allows for electrical contacts to connect each of the word lines of the memory device, as will be shown later.

[0078] FIG. 4F illustrates the formation of vertical structures 214 through layer stack 408, according to some embodiments. Vertical structures 214 includes both NAND memory strings 216 and conductive contacts 218.

[0079] In some embodiments, NAND memory strings 216 include a plurality of memory layers 414 and a core insulator material 416 that extend between an epitaxially grown

material 420 on semiconductor layer 210 and a top conductive material 418. Epitaxially grown material 420 can include epitaxially grown silicon, and may extend into a portion of semiconductor layer 210. Top conductive material 418 may include doped polysilicon or any other conductive material.

[0080] Plurality of memory layers 414 of each NAND memory string 216 can include a semiconductor channel layer, such as amorphous silicon, polysilicon, or single crystalline silicon. Plurality of memory layers 414 can also include a tunneling layer, a storage layer (also known as “charge trap/storage layer”), and a blocking layer. The blocking layer, the storage layer, the tunneling layer, and the semiconductor channel layer are arranged over one another on the sidewalls in the order listed (with the blocking layer deposited first and the semiconductor channel layer deposited last), according to some embodiments. The tunneling layer can include silicon oxide, silicon nitride, or any combination thereof. The blocking layer can include silicon oxide, silicon nitride, high dielectric constant (high-k) dielectrics, or any combination thereof. The storage layer can include silicon nitride, silicon oxynitride, silicon, or any combination thereof. In some embodiments, plurality of memory layers 414 includes silicon oxide/silicon nitride/silicon oxide (ONO) dielectrics (e.g., a tunneling layer including silicon oxide, a storage layer including silicon nitride, and a blocking layer including silicon oxide). Core insulator 416 can be any dielectric material, such as oxide, for example. In some embodiments, plurality of memory layers 414 surround core insulator 416. A diameter of NAND memory strings 216 can be between about 100 nm and 200 nm.

[0081] In some embodiments, the formation of NAND memory strings 216 includes etching a plurality of openings through layer stack 408 and into a portion of semiconductor layer 210. Epitaxially grown material 420 is then formed at the bottom of the plurality of openings, followed by deposition of plurality of memory layers 414 and deposition of core insulator 416, such that plurality of memory layers 414 surround core insulator 416. Top conductive material 418 can be formed over plurality of memory layers 414 and core insulator 416, and may be formed after etching a top portion of memory layers 414 and core insulator 416. Each of the various layers of plurality of memory layers 414 can be formed using any suitable deposition technique, such as sputtering, evaporation, or chemical vapor deposition (CVD). Example CVD techniques

include plasma-enhanced CVD (PECVD), low pressure CVD (LPCVD), and atomic layer deposition (ALD). Similarly, core insulator 416 can be formed using any of the techniques described above.

[0082] In some embodiments, NAND memory strings 216 are electrically coupled to corresponding bit lines in first set of conductive lines 228 using vias 238 extending through a thickness of semiconductor layer 210. Not every structure of vertical structures 214 includes a connection to a conductive line in first set of conductive lines 228. According to some embodiments, only NAND memory strings 216 are connected to corresponding conductive lines in first set of conductive lines 228.

[0083] Conductive contacts 218 can be TACs that each include a conductive core 424 surrounding by an insulating material 422. Conductive core 424 can include conductor materials including, but not limited to, tungsten (W), cobalt (Co), copper (Cu), aluminum (Al), silicides, or any combination thereof. Insulating material 422 can include silicon oxide, silicon nitride, silicon oxynitride, doped silicon oxide, or any combination thereof. Conductive core 424 and insulating material 422 can each be formed using any suitable deposition technique, such as sputtering, evaporation, or chemical vapor deposition (CVD). Example CVD techniques include plasma-enhanced CVD (PECVD), low pressure CVD (LPCVD), and atomic layer deposition (ALD).

[0084] According to some embodiments, a chemical mechanical polishing process (CMP) can be performed to planarize a top surface 425 of the semiconductor structure following the formation of plurality of vertical structures 214.

[0085] FIG. 4G illustrates additional fabricated structures and layers of memory device 200. According to some embodiments, sacrificial layers 410 of layer stack 408 are removed and replaced with conductor layers 426 to form layer stack 212 having alternating conductor layers 426 and dielectric layers 412. Conductor layers 426 can act as word lines for each of NAND memory strings 216. Sacrificial layers 410 can be removed by a suitable etching process, e.g., an isotropic dry etch or a wet etch. The etching process can have sufficiently high etching selectivity of the material of sacrificial layers 410 over the materials of other parts of the structure, such that the etching process can have minimal impact on the other parts of the structure. In some embodiments, sacrificial layers 410 include silicon nitride and the etchant of the isotropic dry etch

includes one or more of CF_4 , CHF_3 , C_4F_8 , C_4F_6 , and CH_2F_2 . The radio frequency (RF) power of the isotropic dry etch can be lower than about 100 W and the bias can be lower than about 10 V. In some embodiments, sacrificial layers 410 include silicon nitride and the etchant of the wet etch includes phosphoric acid. In some embodiments, dielectric layers 412 can be removed such that empty space (vacuum) exists between conductor layers 426. The vacuum space between conductor layers 426 acts as an insulating layer and may help reduce parasitic capacitance.

[0086] Conductor layers 426 can include conductor materials including, but not limited to, W, Co, Cu, Al, doped silicon, silicides, or any combination thereof. Each of conductor layers 426 can be deposited into the regions left behind by the removal of sacrificial layers 410 using a suitable deposition method such as CVD, sputtering, MOCVD, and/or ALD.

[0087] Contact is made to each of conductor layers 426 using vias 226 extending through dielectric material 234. A second set of conductive lines 230 are formed to make electrical contact with one or more of the word lines and to one or more of conductive contacts 218. Not every structure of vertical structures 214 includes a connection to a conductive line in second set of conductive lines 230. According to some embodiments, only conductive contacts 218 are connected to corresponding conductive lines in second set of conductive lines 230.

[0088] FIG. 4H illustrates the formation of one or more interconnect layers 232 making electrical connection with one or more of second set of conductive lines 230, according to some embodiments. Any number of interconnect layers may be formed with each having vias connecting different levels of conductor layers. Additional dielectric layers are also deposited to increase a total thickness of dielectric material 234.

[0089] According to some embodiments, conductive pads 236 are formed at a top surface of memory device 200. Conductive pads 236 can be used to provide electrical connection to external devices and their use would be well understood to a person skilled in the relevant art.

[0090] FIGS. 5A – 5E illustrate an example fabrication process for forming memory device 300. FIG. 5A illustrates the formation of dielectric material 306 over a first

surface of substrate 302. A first set of conductive lines 303 is formed within dielectric material 306.

- [0091] A semiconductor layer 210 is subsequently formed over dielectric material 306. One or more vias 238 are formed through a thickness of semiconductor layer 210 and can make electrical connection with one or more of the conductive lines in first set of conductive lines 303.
- [0092] FIG. 5B illustrates the formation of plurality of vertical structures 214 through layer stack 212. Additionally, second set of conductive lines 304 is formed over plurality of vertical structures 214, and connections are made using conductive vias between conductive contacts 218 and corresponding conductive lines of second set of conductive lines 304, according to some embodiments. One or more interconnect layers 232 are formed having electrical connection with one or more conductive lines in second set of conductive lines 304. The details of the formation of these components is the same as described above for FIGs. 4E – 4H.
- [0093] Each of NAND memory strings 216 is electrically connected to a corresponding bit line of first set of conductive lines 303 using vias 238, according to some embodiments. According to some embodiments, only NAND memory strings 216 are electrically connected to bit lines in first set of conductive lines 303 and only conductive contacts 218 are electrically connected to conductive lines in second set of conductive lines 304.
- [0094] FIG. 5C illustrates the thinning of substrate 302 and subsequent formation of peripheral devices 204 on a second surface of substrate 302 opposite from the first surface, according to some embodiments. The formation of peripheral devices 204 is the same as described above for FIG. 4A.
- [0095] FIG. 5D illustrates the formation of dielectric material 208 over peripheral devices 204, and the formation of a first interconnect level within dielectric material 208. The first interconnect level provides electrical contact to peripheral devices 204 and also to one or more bit lines of first set of conductive lines 303 using vias 308 that extend through a thickness of the thinned substrate 302.
- [0096] FIG. 5E illustrates the formation of the remainder of peripheral interconnect layers 206 making electrical connection with peripheral devices 204 and one or more bit

lines of first set of conductive lines 303. The formation of peripheral interconnect layers 206 is the same as described above in FIG. 4C. According to some embodiments, conductive pads 310 are formed at a top surface of memory device 300. Conductive pads 310 can be used to provide electrical connection to external devices and their use would be well understood to a person skilled in the relevant art.

[0097] FIG. 6 is a flowchart of an exemplary method 600 for forming a NAND memory device, according to the first embodiment. The operations of method 600 are generally illustrated in FIGs. 4A – 4H. It should be understood that the operations shown in method 600 are not exhaustive and that other operations can be performed as well before, after, or between any of the illustrated operations. In various embodiments of the present disclosure, the operations of method 600 can be performed in a different order and/or vary.

[0098] In operation 602, peripheral devices are formed on a substrate. The peripheral devices can include a plurality of transistors formed on the substrate. The peripheral devices can include any arrangement of transistors or electrically passive devices (e.g., capacitors, resistors, etc.) The transistors can be formed by a plurality of processing steps including, but not limited to, photolithography, dry/wet etch, thin film deposition, thermal growth, implantation, chemical mechanical polishing (CMP), or any combination thereof. In some embodiments, doped regions are formed in the substrate, which function, for example, as source regions and/or drain regions of the transistors. In some embodiments, isolation regions, such as shallow trench isolation (STI), is also formed in the substrate.

[0099] In operation 604, one or more interconnect layers are formed over the peripheral devices. Any number of interconnect layers may be formed each having vias connecting different levels of conductor layers. A dielectric material can be deposited to surround the one or more interconnect layers.

[0100] In operation 606, a first set of conductive lines is formed and are electrically coupled to the one or more interconnect layers. The first set of conductive lines can also be considered to be one layer of the one or more interconnect layers.

[0101] In operation 608, a semiconductor layer is formed over the one or more interconnect layers. The semiconductor layer can also be formed over the first set of conductive lines. The semiconductor layer can be deposited using well-known vapor

deposition techniques such as chemical vapor deposition (CVD) or physical vapor deposition (PVD) techniques. In some embodiments the semiconductor layer is epitaxially grown silicon.

[0102] In operation 610, one or more vias are formed through a thickness of the semiconductor layer. The one or more vias make electrical contact with the first set of conductive lines, according to some embodiments.

[0103] In operation 612, a layer stack having alternating conductor and insulator layers is formed on the semiconductor layer. The formation of the layer stack can involve first depositing alternating types of dielectric materials (e.g., sacrificial layers alternating with dielectric layers). The layers of the alternating dielectric stack can include materials including, but not limited to, silicon oxide, silicon nitride, silicon oxynitride, or any combination thereof. The layers of the alternating dielectric stack can include dielectric materials deposited by one or more thin film deposition processes including, but not limited to, CVD, PVD, ALD, or any combination thereof. At a later time, the sacrificial layers can be removed and replaced by conductor layers to form the alternating conductor and insulator layers. The insulator layers may be dielectric layers, or may be regions of vacuum between the conductor layers.

[0104] In operation 614, a plurality of vertical structures are formed through the layer stack. The vertical structures can include one or more NAND memory strings having a plurality of memory layers surrounding a core insulator. Forming the plurality of memory layers may include depositing a semiconductor channel layer, such as amorphous silicon, polysilicon, or single crystalline silicon, a tunneling layer, a storage layer (also known as “charge trap/storage layer”), and a blocking layer. The blocking layer, the storage layer, the tunneling layer, and the semiconductor channel layer may each be deposited in the order listed on the sidewalls of the one or more first openings, according to some embodiments. The tunneling layer can include silicon oxide, silicon nitride, or any combination thereof. The blocking layer can include silicon oxide, silicon nitride, high dielectric constant (high-k) dielectrics, or any combination thereof. The storage layer can include silicon nitride, silicon oxynitride, silicon, or any combination thereof. In some embodiments, the plurality of memory layers includes silicon oxide/silicon nitride/silicon oxide (ONO) dielectrics (e.g., a tunneling layer including silicon oxide, a storage layer

including silicon nitride, and a blocking layer including silicon oxide). The one or more NAND memory strings can be formed above the vias formed in operation 610, such that only the one or more NAND memory strings are electrically connected to corresponding bit lines in the first set of conductive lines using the vias.

[0105] Other vertical structures can include conductive contacts such as TACs that include a core conductive material that extends vertically through the layer stack.

[0106] According to some embodiments, any first set of the vertical structures can be coupled to corresponding conductive lines in the first set of conductive lines using the vias.

[0107] In operation 616, a second set of conductive lines is formed that is coupled to a second set of the vertical structures. The second set of vertical structures is different from the first set of vertical structures, though some of the vertical structures may be in both the first and second sets. According to some embodiments, the second set of vertical structures can include any number of NAND strings and vertical conductive contacts. In one example, the second set of vertical structures includes only the vertical conductive contacts.

[0108] According to some embodiments, the second set of conductive lines are formed on a different plane than the first set of conductive lines either above or below the plurality of vertical structures. The second set of conductive lines can be formed over an opposite end vertically distanced from the plurality of vertical structures compared to the first set of conductive lines. By staggering the position of the various conductive lines on two different planes, the density of conductive lines on a given plane is reduced.

[0109] FIG. 7 is a flowchart of an exemplary method 700 for forming a NAND memory device, according to the first embodiment. The operations of method 700 are generally illustrated in FIGs. 5A – 5E. It should be understood that the operations shown in method 700 are not exhaustive and that other operations can be performed as well before, after, or between any of the illustrated operations. In various embodiments of the present disclosure, the operations of method 700 can be performed in a different order and/or vary.

- [0110] In operation 702, a first set of conductive lines are formed over a first surface of a substrate. The first set of conductive lines can be formed within a dielectric material deposited first over the first surface of the substrate.
- [0111] In operation 704, a semiconductor layer is formed over the first set of conductive lines in the dielectric material. The semiconductor layer can be deposited using well-known vapor deposition techniques such as chemical vapor deposition (CVD) or physical vapor deposition (PVD) techniques. In some embodiments the semiconductor layer is epitaxially grown silicon.
- [0112] In operation 706, one or more vias are formed through a thickness of the semiconductor layer. The one or more vias make electrical contact with the first set of conductive lines, according to some embodiments.
- [0113] In operation 708, a layer stack having alternating conductor and insulator layers is formed on the semiconductor layer. The formation of the layer stack can involve first depositing alternating types of dielectric materials (e.g., sacrificial layers alternating with dielectric layers). The layers of the alternating dielectric stack can include materials including, but not limited to, silicon oxide, silicon nitride, silicon oxynitride, or any combination thereof. The layers of the alternating dielectric stack can include dielectric materials deposited by one or more thin film deposition processes including, but not limited to, CVD, PVD, ALD, or any combination thereof. At a later time, the sacrificial layers can be removed and replaced by conductor layers to form the alternating conductor and insulator layers. The insulator layers may be dielectric layers, or may be regions of vacuum between the conductor layers.
- [0114] In operation 710, a plurality of vertical structures are formed through the layer stack. The vertical structures can include one or more NAND memory strings having a plurality of memory layers surrounding a core insulator. Forming the plurality of memory layers may include depositing a semiconductor channel layer, such as amorphous silicon, polysilicon, or single crystalline silicon, a tunneling layer, a storage layer (also known as “charge trap/storage layer”), and a blocking layer. The blocking layer, the storage layer, the tunneling layer, and the semiconductor channel layer may each be deposited in the order listed on the sidewalls of the one or more first openings, according to some embodiments. The tunneling layer can include silicon oxide, silicon nitride, or any

combination thereof. The blocking layer can include silicon oxide, silicon nitride, high dielectric constant (high-k) dielectrics, or any combination thereof. The storage layer can include silicon nitride, silicon oxynitride, silicon, or any combination thereof. In some embodiments, the plurality of memory layers includes silicon oxide/silicon nitride/silicon oxide (ONO) dielectrics (e.g., a tunneling layer including silicon oxide, a storage layer including silicon nitride, and a blocking layer including silicon oxide). The one or more NAND memory strings can be formed above the vias formed in operation 706, such that only the one or more NAND memory strings are electrically connected to corresponding bit lines in the first set of conductive lines using the vias.

[0115] Other vertical structures can include conductive contacts such as TACs that include a core conductive material that extends vertically through the layer stack.

[0116] According to some embodiments, any first set of the vertical structures can be coupled to corresponding conductive lines in the first set of conductive lines using the vias.

[0117] In operation 712, a second set of conductive lines is formed over an opposite end of the vertical structures from the first set of conductive lines. The second set of conductive lines is coupled to a second set of the vertical structures. The second set of vertical structures is different from the first set of vertical structures, though some of the vertical structures may be in both the first and second sets. According to some embodiments, the second set of vertical structures can include any number of NAND strings and vertical conductive contacts. In one example, the second set of vertical structures includes only the vertical conductive contacts.

[0118] According to some embodiments, the second set of conductive lines are formed on a different plane than the first set of conductive lines either above or below the plurality of vertical structures. The second set of conductive lines can be formed over an opposite end vertically distanced from the plurality of vertical structures compared to the first set of conductive lines. By staggering the position of the various conductive lines on two different planes, the density of conductive lines on a given plane is reduced.

[0119] In operation 714, peripheral devices are formed on a second surface of the substrate opposite from the first surface. In some embodiments, the substrate is thinned before the formation of the peripheral devices. The peripheral devices are formed in the

same way as described above in operation 602, and may also include one or more interconnect layers connected to the peripheral devices. The one or more interconnect layers can also make electrical connection with one or more of the bit lines in the first set of conductive lines using conductive vias passing through a thickness of the substrate.

[0120] The present disclosure describes various embodiments of three-dimensional memory devices and methods of making the same. In some embodiments, a memory device includes substrate and one or more peripheral devices on the substrate. The memory device also includes one or more interconnect layers electrically coupled with the one or more peripheral devices, and a semiconductor layer disposed over the one or more interconnect layers. A layer stack having alternating conductor and insulator layers is disposed above the semiconductor layer. A plurality of structures extend vertically through the layer stack. The memory device also includes a first set of conductive lines electrically coupled with a first set of the plurality of structures and a second set of conductive lines electrically coupled with a second set of the plurality of structures different from the first set. The first set of conductive lines are vertically distanced from one end of the plurality of structures and the second set of conductive lines are vertically distanced from an opposite end of the plurality of structures.

[0121] In some embodiments, a memory device includes a substrate, a dielectric material disposed on a first surface of the substrate, a semiconductor layer disposed on the dielectric material, and a layer stack having alternating conductor and insulator layers disposed on the semiconductor layer. The memory device also includes a plurality of structures extending vertically through the layer stack. The memory device also includes a first set of conductive lines electrically coupled with a first set of the plurality of structures and a second set of conductive lines electrically coupled with a second set of the plurality of structures different from the first set. The first set of conductive lines are vertically distanced from one end of the plurality of structures and the second set of conductive lines are vertically distanced from an opposite end of the plurality of structures. The memory device also includes one or more peripheral devices formed on a second surface of the substrate, the second surface being opposite to the first surface.

[0122] In some embodiments, a method to form a memory device includes forming one or more peripheral devices on a substrate and one or more interconnect layers over the

one or more peripheral devices. The one or more interconnect layers are electrically coupled with the one or more peripheral devices. The method also includes forming a first set of conductive lines electrically coupled with the one or more interconnect layers, and forming a semiconductor layer over the first set of conductive lines. The method includes forming vias through a thickness of the semiconductor layer where the vias are electrically coupled to the first set of conductive lines. The method also includes forming, on the semiconductor layer, a layer stack having alternating conductor and insulator layers. The method includes forming a plurality of structures each extending vertically through the layer stack. A first set of the plurality of structures is electrically coupled to the first set of conductive lines using the vias. The method also includes forming a second set of conductive lines over an end vertically distanced from the plurality of structures. The second set of conductive lines is electrically coupled to a second set of the plurality of structures different from the first set.

[0123] In some embodiments, a method to form a memory device includes forming a first set of conductive lines over a first surface of a substrate, the first set of conductive lines being surrounded by a dielectric layer on the first surface of the substrate. The method also includes forming a semiconductor layer over the first set of conductive lines, and forming vias through a thickness of the semiconductor layer. The vias are electrically coupled to the first set of conductive lines. The method also includes forming, on the semiconductor layer, a layer stack having alternating conductor and insulator layers. The method includes forming a plurality of structures each extending vertically through the layer stack. A first set of the plurality of structures is electrically coupled to the first set of conductive lines using the vias. The method also includes forming a second set of conductive lines over an end vertically distanced from the plurality of structures. The second set of conductive lines are electrically coupled to a second set of the plurality of structures different from the first set. The method also includes forming one or more peripheral devices on a second surface of the substrate opposite from the first surface.

[0124] The foregoing description of the specific embodiments will so fully reveal the general nature of the present disclosure that others can, by applying knowledge within the skill of the art, readily modify and/or adapt for various applications such specific embodiments, without undue experimentation, without departing from the general

concept of the present disclosure. Therefore, such adaptations and modifications are intended to be within the meaning and range of equivalents of the disclosed embodiments, based on the disclosure and guidance presented herein. It is to be understood that the phraseology or terminology herein is for the purpose of description and not of limitation, such that the terminology or phraseology of the present specification is to be interpreted by the skilled artisan in light of the disclosure and guidance.

[0125] Embodiments of the present disclosure have been described above with the aid of functional building blocks illustrating the implementation of specified functions and relationships thereof. The boundaries of these functional building blocks have been arbitrarily defined herein for the convenience of the description. Alternate boundaries can be defined so long as the specified functions and relationships thereof are appropriately performed.

[0126] The Summary and Abstract sections may set forth one or more but not all exemplary embodiments of the present disclosure as contemplated by the inventor(s), and thus, are not intended to limit the present disclosure and the appended claims in any way.

[0127] The breadth and scope of the present disclosure should not be limited by any of the above-described exemplary embodiments, but should be defined only in accordance with the following claims and their equivalents.

WHAT IS CLAIMED IS:

1. A memory device, comprising:

a substrate;

one or more peripheral devices formed on the substrate;

one or more interconnect layers disposed above the one or more peripheral devices and electrically coupled with the one or more peripheral devices;

a semiconductor layer disposed over the one or more interconnect layers;

a layer stack having alternating conductor and insulator layers disposed above the semiconductor layer;

a plurality of structures extending vertically through the layer stack;

a first set of conductive lines electrically coupled with a first set of the plurality of structures and with the one or more interconnect layers, the first set of conductive lines being vertically distanced from one end of the plurality of structures; and

a second set of conductive lines electrically coupled with a second set of the plurality of structures different from the first set, the second set of conductive lines being vertically distanced from an opposite end of the plurality of structures.

2. The memory device of claim 1, further comprising one or more second interconnect layers, the one or more second interconnect layers being electrically coupled to the second set of conductive lines.
3. The memory device of claim 2, wherein the one or more second interconnect layers comprises conductive pads configured to provide electrical connection to external devices.
4. The memory device of claim 1, wherein the plurality of structures comprises NAND memory strings.

5. The memory device of claim 4, wherein the NAND strings each includes a plurality of layers surrounding a core insulating material, wherein the plurality of layers comprises a blocking layer, a storage layer, a tunneling layer, and a channel layer.
6. The memory device of claim 4, wherein the first set of the plurality of structures includes a first set of the NAND memory strings and the second set of the plurality of structures includes a second set of the NAND memory strings.
7. The memory device of claim 4, wherein the plurality of structures comprises conductive contacts.
8. The memory device of claim 7, wherein the first set of the plurality of structures includes only the NAND memory strings and the second set of the plurality of structures includes only the conductive contacts.
9. The memory device of claim 1, wherein the first set of conductive lines are located on an opposite side of the semiconductor layer from the second set of conductive lines.
10. The memory device of claim 1, further comprising vias extending through a thickness of the semiconductor layer, wherein the vias electrically contact the first set of conductive lines and the first set of the plurality of structures.
11. A memory device, comprising:
 - a substrate;
 - a dielectric material disposed on a first surface of the substrate;
 - a semiconductor layer disposed on the dielectric material;
 - a layer stack having alternating conductor and insulator layers disposed on the semiconductor layer;
 - a plurality of structures extending vertically through the layer stack;

a first set of conductive lines electrically coupled with a first set of the plurality of structures, the first set of conductive lines being vertically distanced from one end of the plurality of structures;

a second set of conductive lines electrically coupled with a second set of the plurality of structures different from the first set, the second set of conductive lines being vertically distanced from an opposite end of the plurality of structures; and

one or more peripheral devices formed on a second surface of the substrate, the second surface being opposite to the first surface.

12. The memory device of claim 11, wherein the plurality of structures comprises one or more NAND memory strings.
13. The memory device of claim 12, wherein the one or more NAND memory strings each includes a plurality of layers surrounding a core insulating material, wherein the plurality of layers comprises a blocking layer, a storage layer, a tunneling layer, and a channel layer.
14. The memory device of claim 12, wherein the first set of the plurality of structures includes a first set of the NAND memory strings and the second set of the plurality of structures includes a second set of the NAND memory strings.
15. The memory device of claim 12, wherein the plurality of structures comprises one or more conductive contacts.
16. The memory device of claim 15, wherein the first set of the plurality of structures includes only the NAND memory strings and the second set of the plurality of structures includes only the conductive contacts.
17. The memory device of claim 11, wherein the first set of conductive lines are located on an opposite side of the semiconductor layer from the second set of conductive lines.
18. The memory device of claim 17, wherein the first set of conductive lines are disposed in the dielectric material.

19. The memory device of claim 11, further comprising one or more interconnect layers coupled to the one or more peripheral devices.
20. The memory device of claim 19, further comprising vias extending through a thickness of the substrate, wherein the vias electrically contact the first set of conductive lines and the one or more interconnect layers.
21. The memory device of claim 19, wherein the one or more interconnect layers comprises conductive pads configured to provide electrical connection to external devices.
22. A method for forming a memory device, comprising:
 - forming one or more peripheral devices on a substrate;
 - forming one or more interconnect layers over the one or more peripheral devices, the one or more interconnect layers being electrically coupled with the one or more peripheral devices;
 - forming a first set of conductive lines electrically coupled with the one or more interconnect layers;
 - forming a semiconductor layer over the first set of conductive lines;
 - forming vias through a thickness of the semiconductor layer, the vias being electrically coupled to the first set of conductive lines;
 - forming, on the semiconductor layer, a layer stack having alternating conductor and insulator layers;
 - forming a plurality of structures each extending vertically through the layer stack, wherein a first set of the plurality of structures are electrically coupled to the first set of conductive lines using the vias; and

forming a second set of conductive lines over an end vertically distanced from the plurality of structures, the second set of conductive lines being electrically coupled to a second set of the plurality of structures different from the first set.

23. The method of claim 22, further comprising forming one or more second interconnect layers over the second set of conductive lines, the one or more second interconnect layers being electrically coupled to the second set of conductive lines.
24. The method of claim 23, further comprising forming one or more conductive pads along a top surface of the memory device, the one or more conductive pads being electrically coupled to the one or more second interconnect layers.
25. The method of claim 22, wherein forming the plurality of structures comprises forming a plurality of NAND strings, wherein forming the plurality of NAND strings comprises:
- depositing a plurality of memory layers comprising a blocking layer, a storage layer, a tunneling layer, and a channel layer; and
- depositing a core insulator material.
26. The method of claim 25, wherein the forming of the plurality of structures comprises forming the first set of the plurality of structures only as the NAND strings.
27. The method of claim 25, wherein the forming of the plurality of structures comprises forming the first set of the plurality of structures as a first set of the NAND strings and forming the second set of the plurality of structures as a second set of the NAND strings different from the first set of the NAND strings.
28. The method of claim 22, wherein forming the plurality of structures comprises forming a plurality of conductive contacts.
29. The method of claim 28, wherein forming the plurality of structures comprises forming the second set of the plurality of structures only as the conductive contacts.
30. A method for forming a memory device, comprising:

forming a first set of conductive lines over a first surface of a substrate, the first set of conductive lines being surrounded by a dielectric layer on the first surface of the substrate;

forming a semiconductor layer over the first set of conductive lines;

forming vias through a thickness of the semiconductor layer, the vias being electrically coupled to the first set of conductive lines;

forming, on the semiconductor layer, a layer stack having alternating conductor and insulator layers;

forming a plurality of structures each extending vertically through the layer stack, wherein a first set of the plurality of structures are electrically coupled to the first set of conductive lines using the vias;

forming a second set of conductive lines over an end vertically distanced from the plurality of structures, the second set of conductive lines being electrically coupled to a second set of the plurality of structures different from the first set; and

forming one or more peripheral devices on a second surface of the substrate opposite from the first surface.

31. The method of claim 30, further comprising forming one or more first interconnect layers over the one or more peripheral devices, the one or more first interconnect layers being electrically coupled with the one or more peripheral devices and with the first set of conductive lines using vias through a thickness of the substrate.
32. The method of claim 31, further comprising forming one or more conductive pads along a surface of the memory device, the one or more conductive pads being electrically coupled to the one or more first interconnect layers.
33. The method of claim 30, further comprising forming one or more second interconnect layers over the second set of conductive lines, the one or more second interconnect layers being electrically coupled to the first set of conductive lines.

34. The method of claim 33, further comprising forming one or more conductive pads along a surface of the memory device, the one or more conductive pads being electrically coupled to the one or more second interconnect layers.
35. The method of claim 30, further comprising thinning a thickness of the substrate before forming the one or more peripheral devices.
36. The method of claim 30, wherein forming the plurality of structures comprises forming a plurality of NAND strings, wherein forming the plurality of NAND strings comprises:
- depositing a plurality of memory layers comprising a blocking layer, a storage layer, a tunneling layer, and a channel layer; and
- depositing a core insulator material.
37. The method of claim 36, wherein forming the plurality of structures comprises forming the first set of the plurality of structures only as the NAND strings.
38. The method of claim 36, wherein the forming of the plurality of structures comprises forming the first set of the plurality of structures as a first set of the NAND strings and forming the second set of the plurality of structures as a second set of the NAND strings different from the first set of the NAND strings.
39. The method of claim 30, wherein forming the plurality of structures comprises forming a plurality of conductive contacts.
40. The method of claim 39, wherein forming the plurality of structures comprises forming the second set of the plurality of structures only as the conductive contacts.

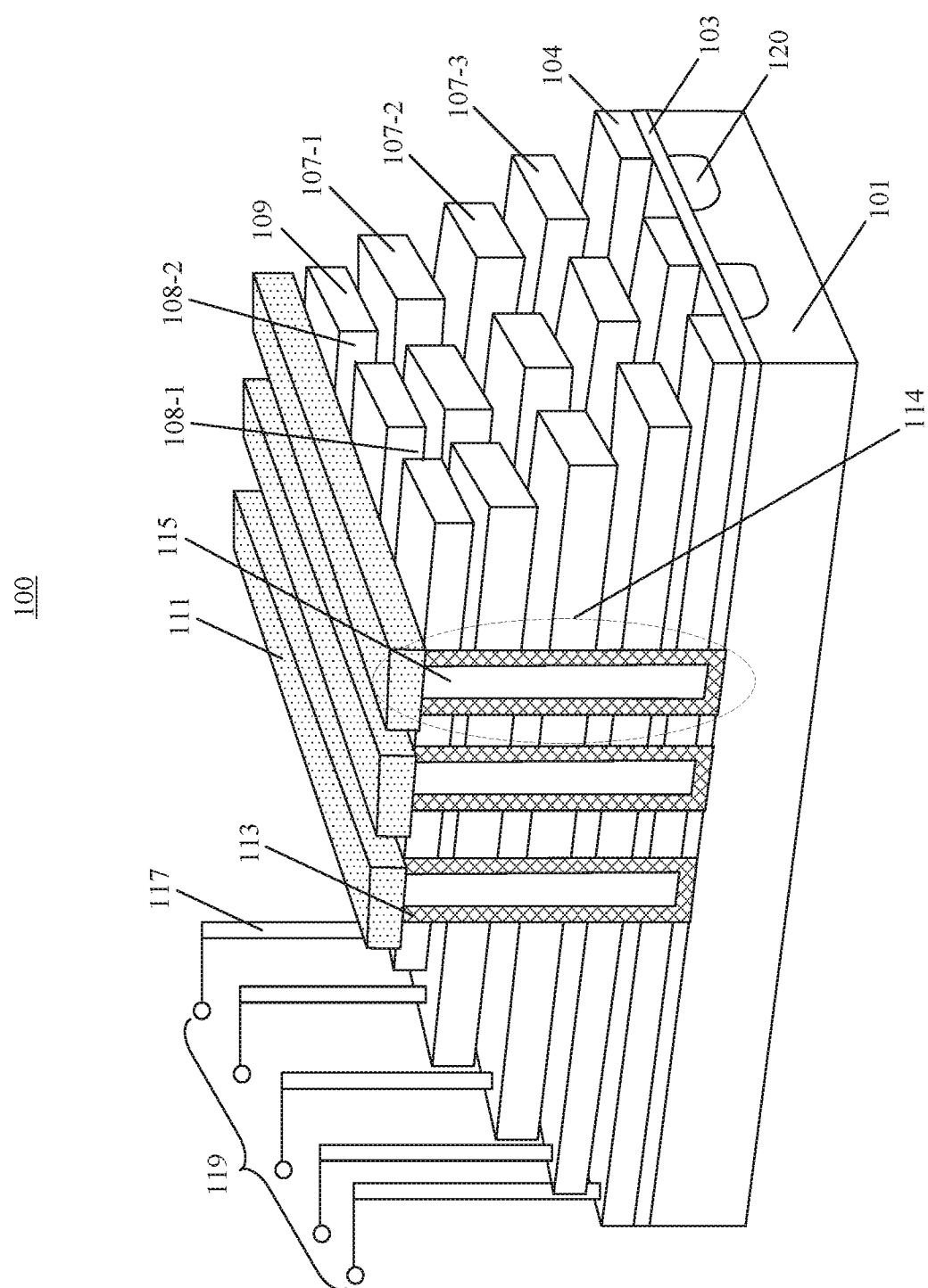
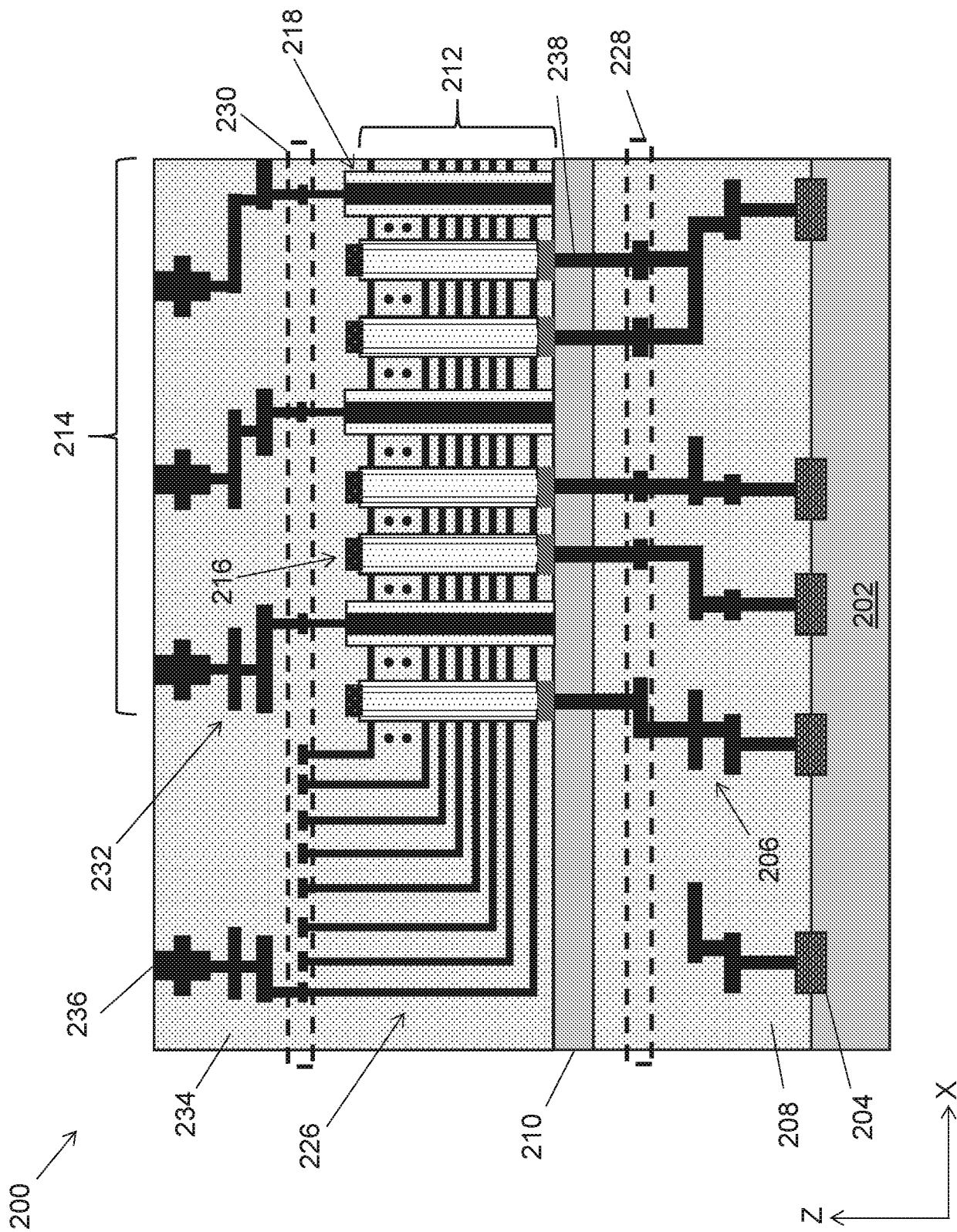


Fig.



2. General

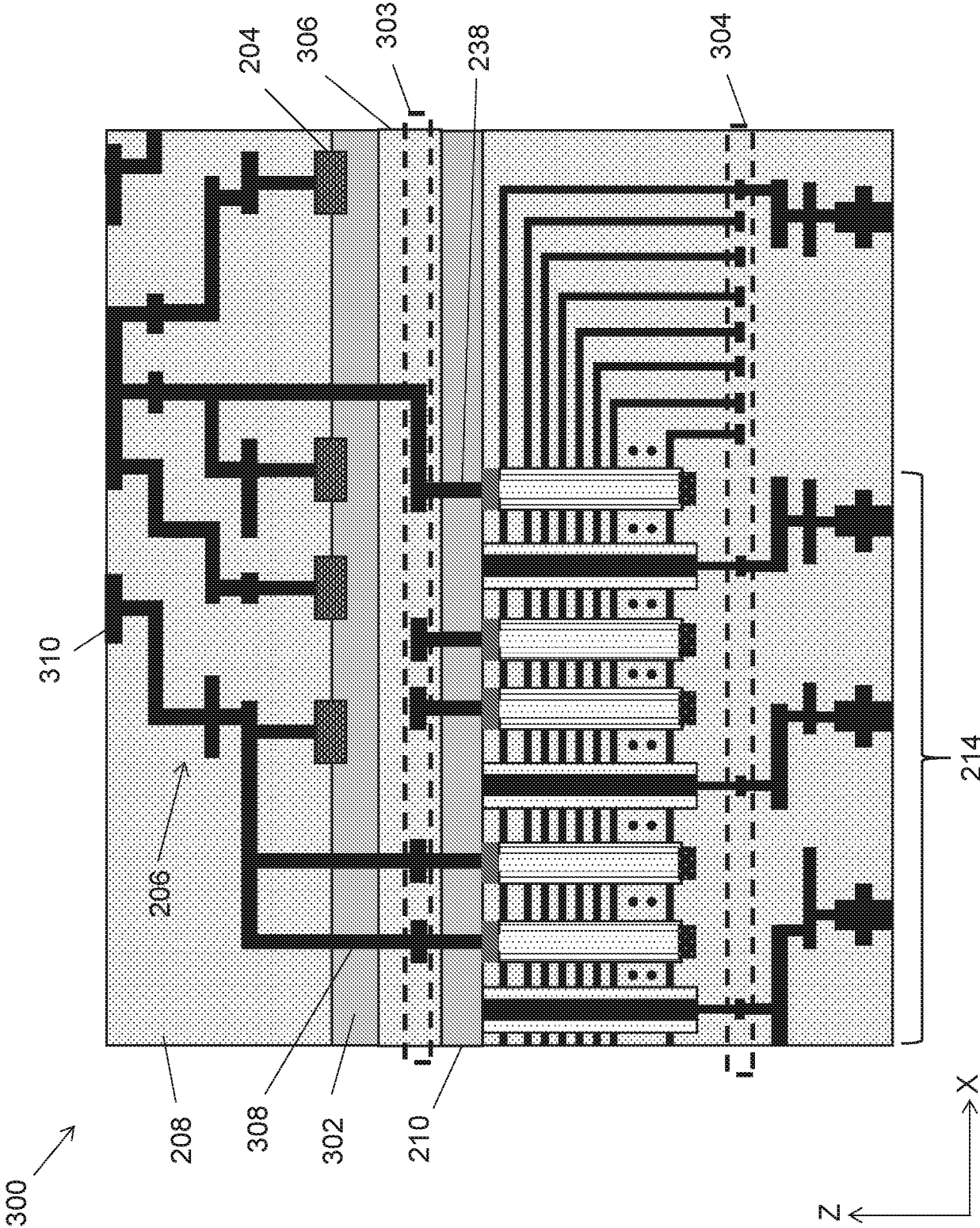


FIG. 3

200

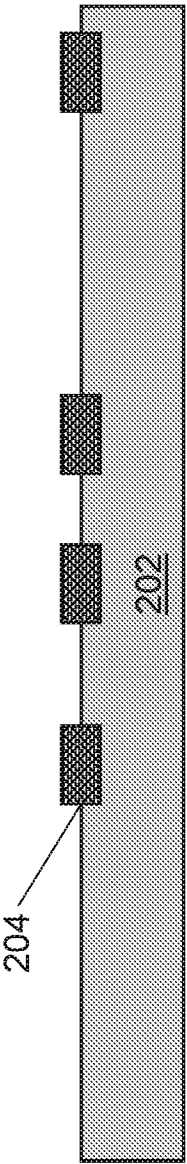


FIG. 4A

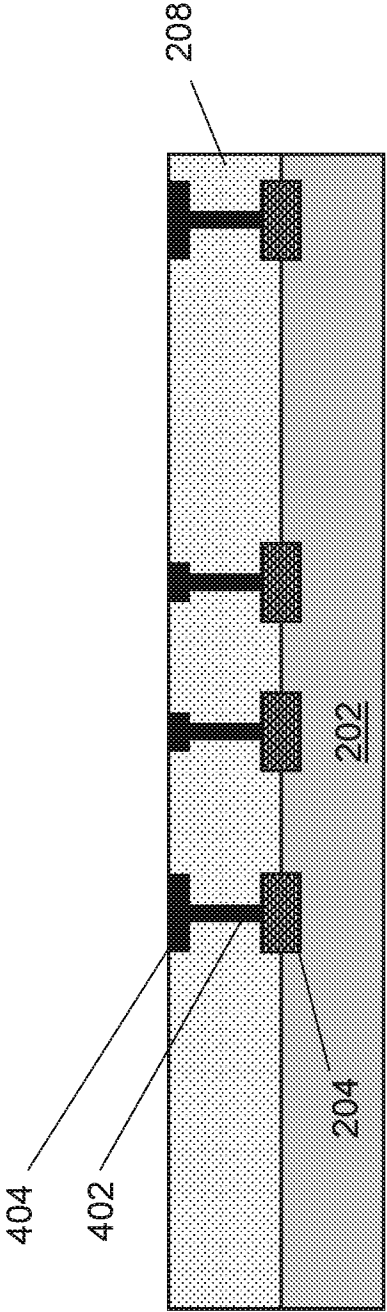
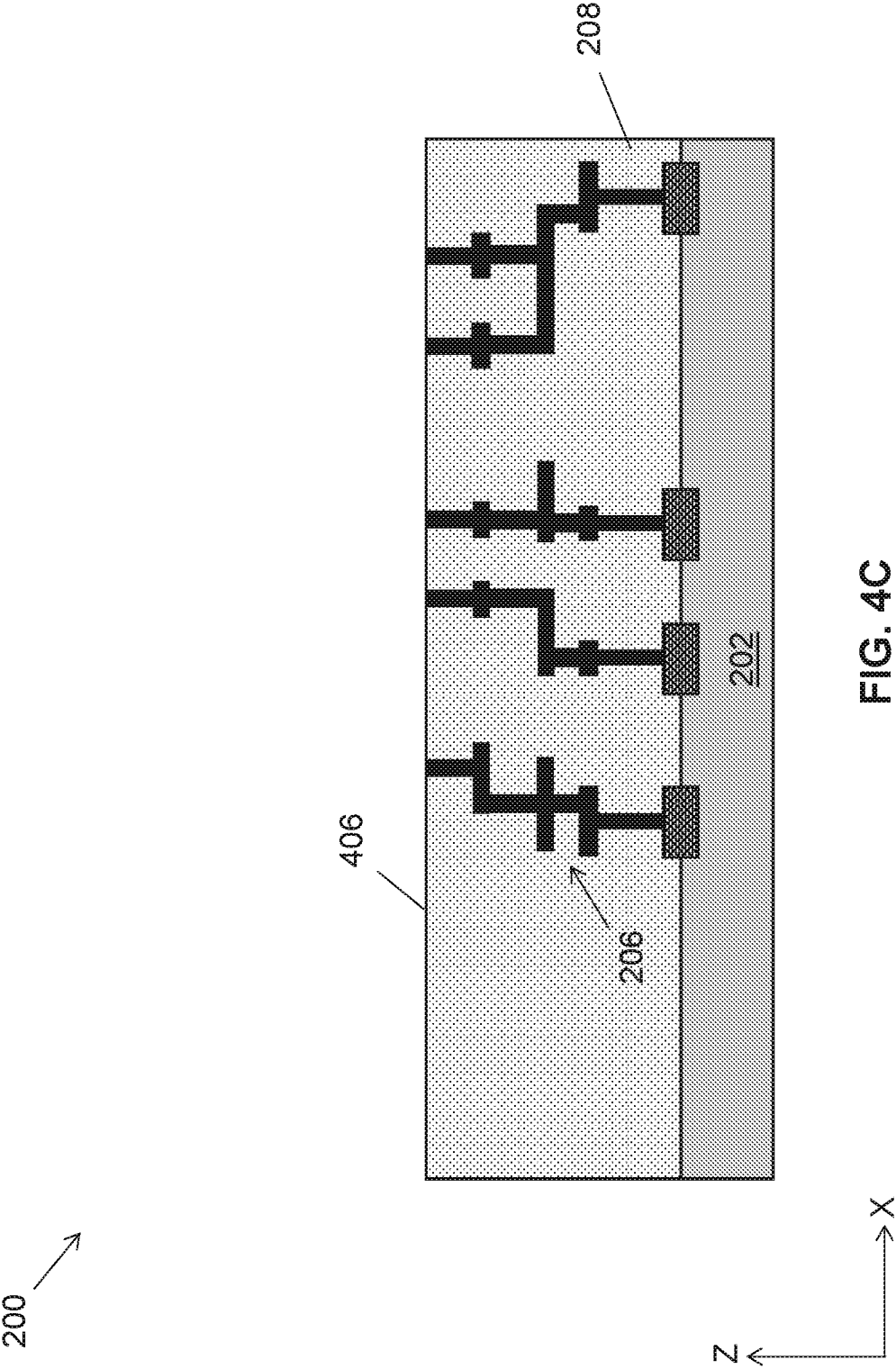


FIG. 4B



200

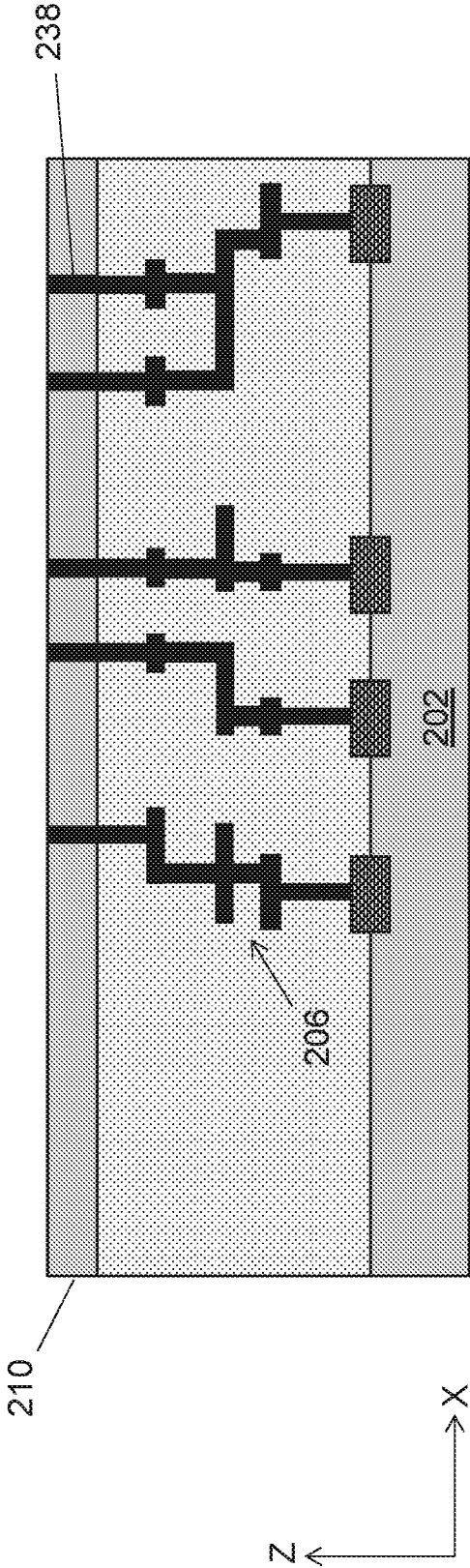


FIG. 4D

200 ↗

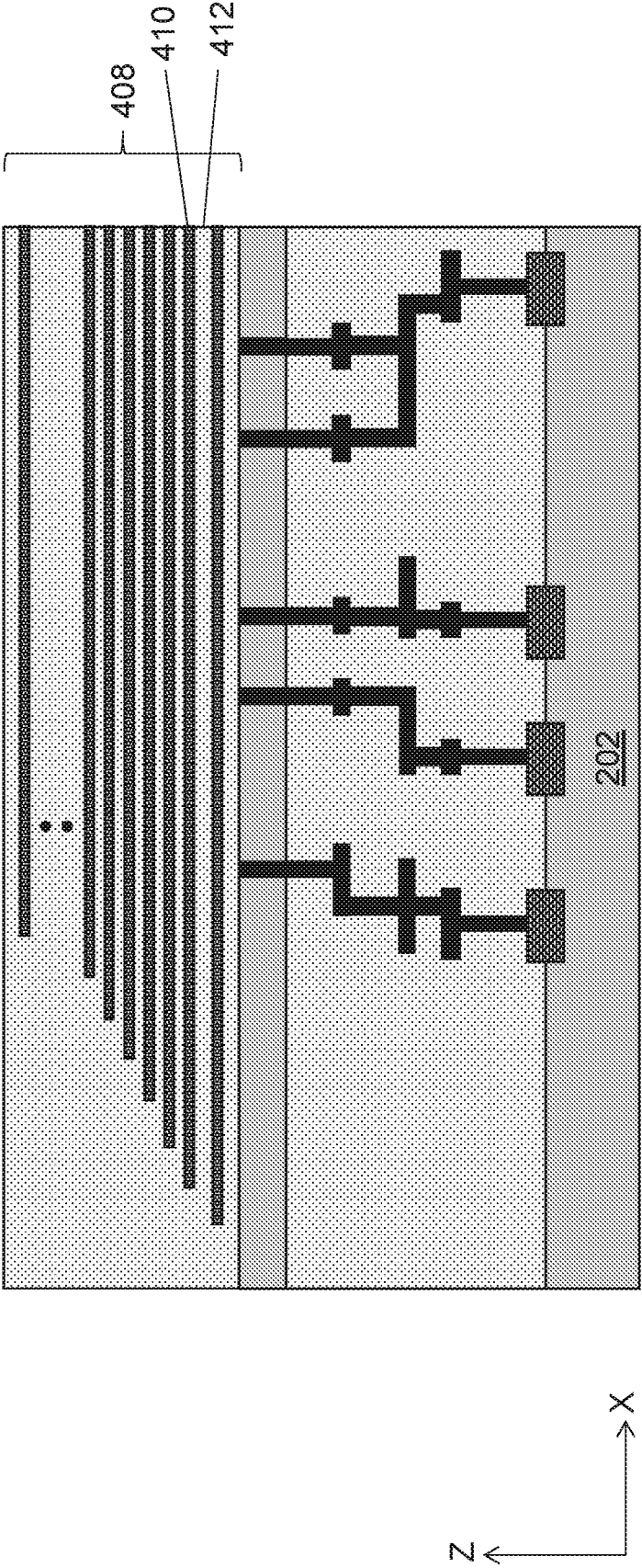


FIG. 4E

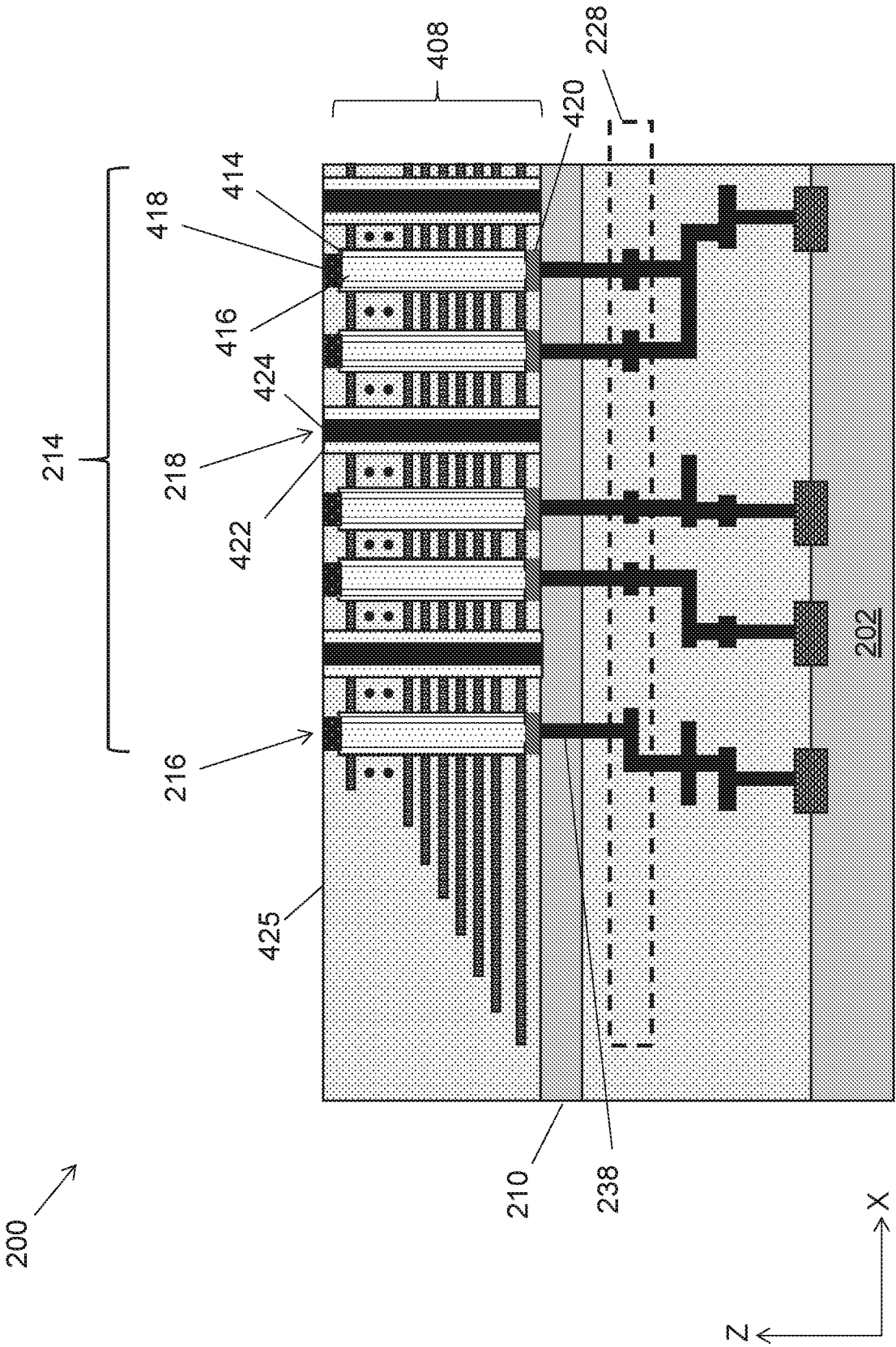


FIG. 4F

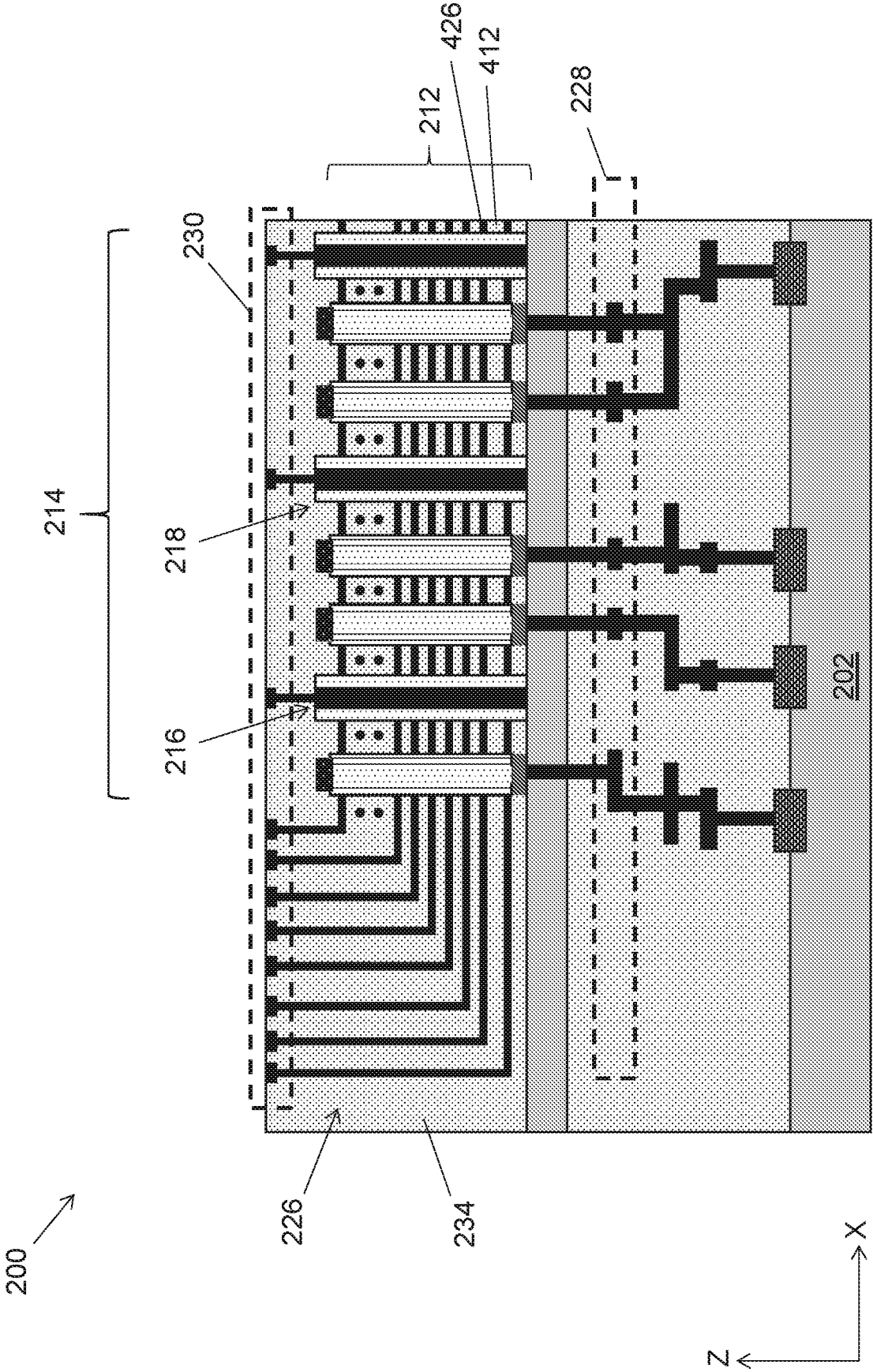


FIG. 4G

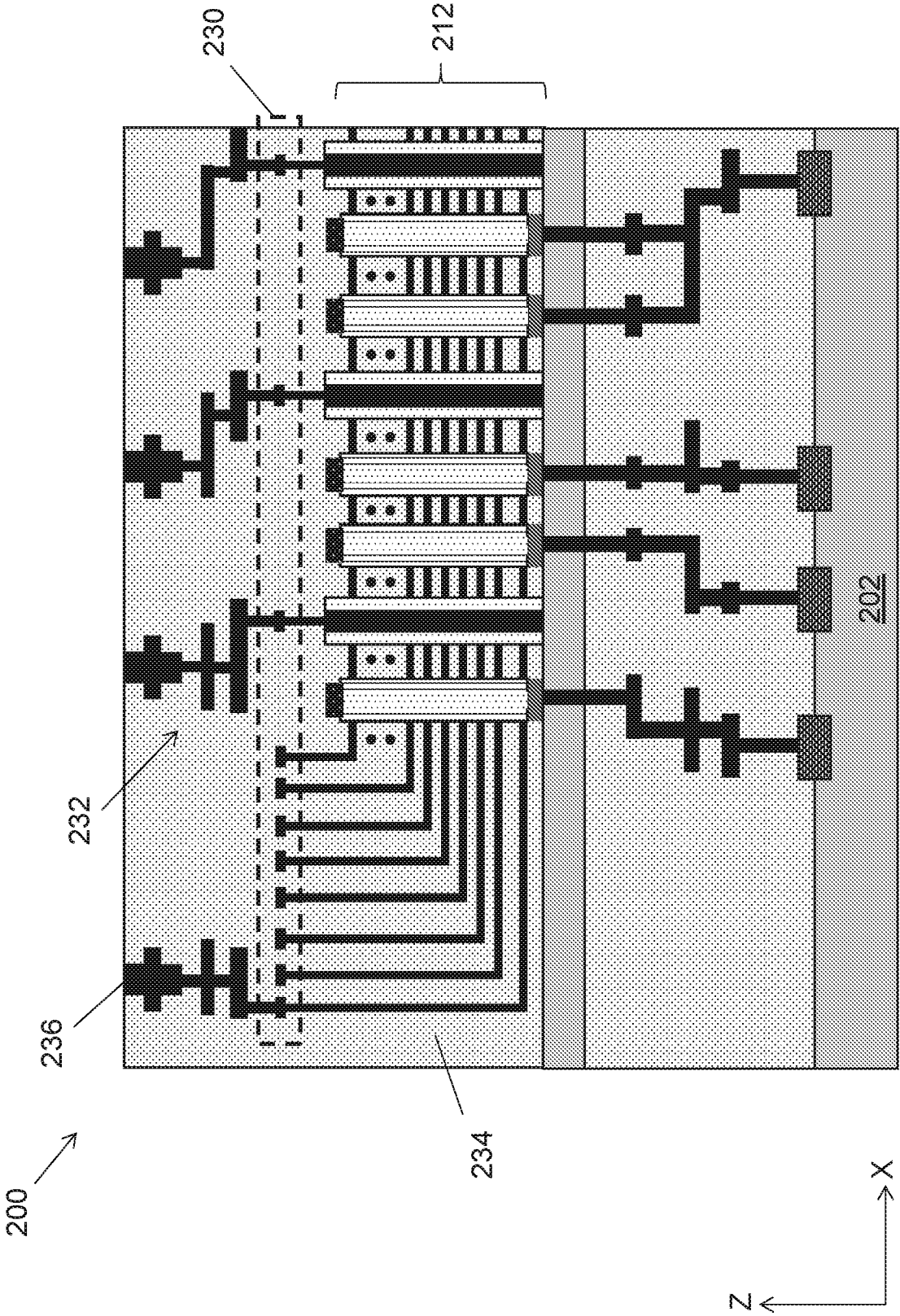


FIG. 4H

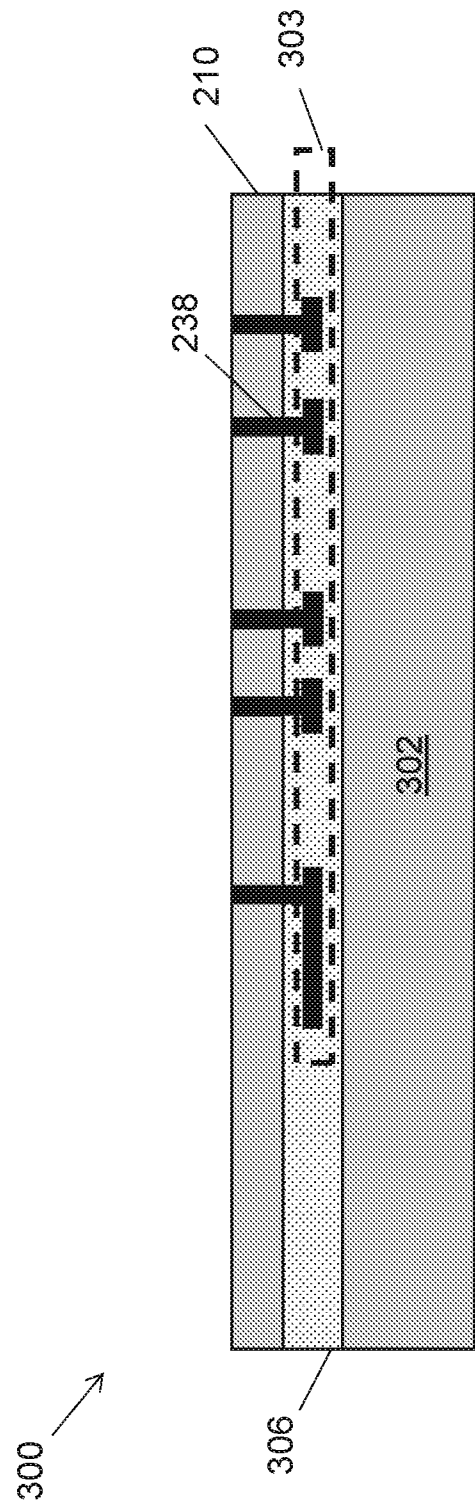
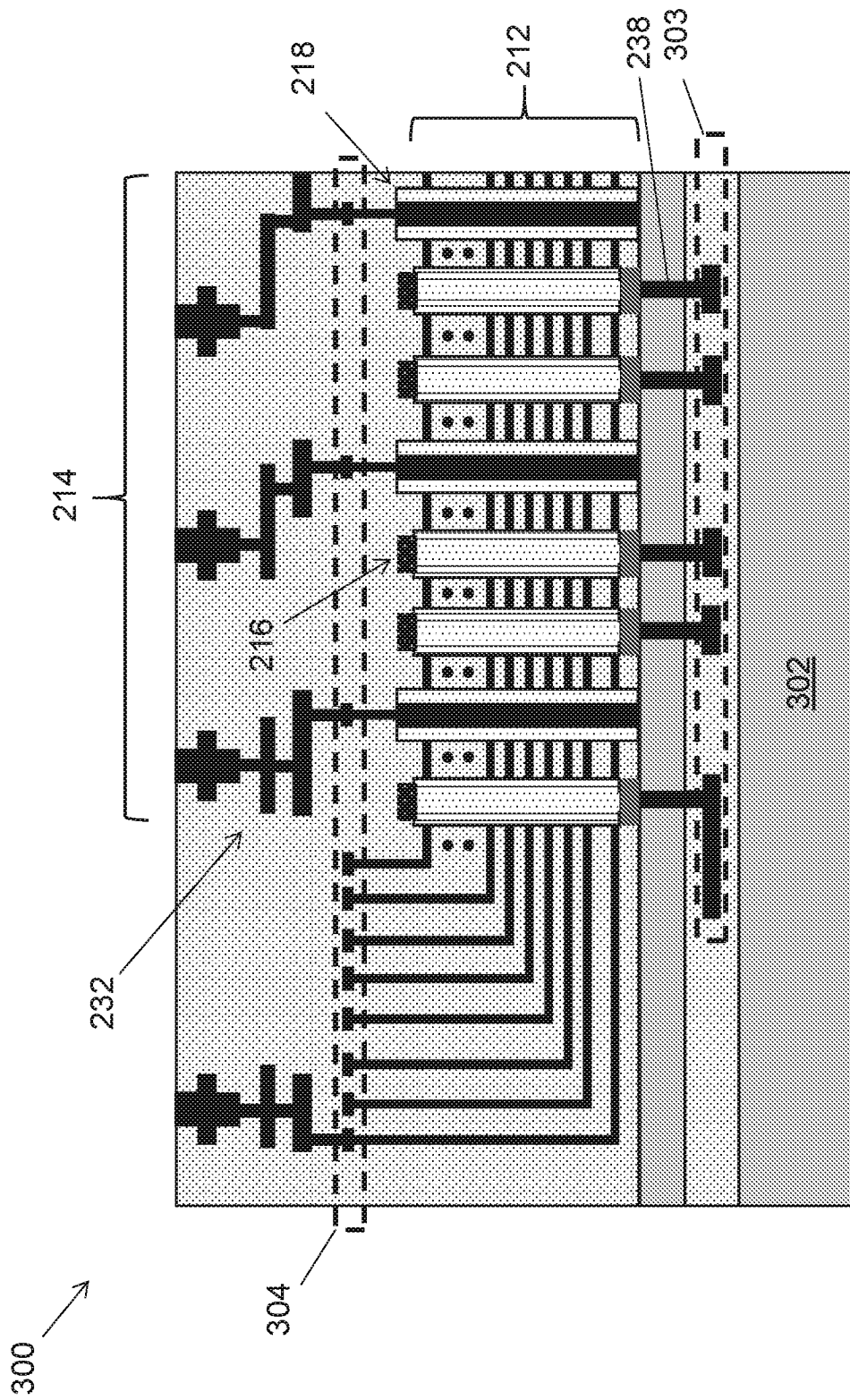


FIG. 5A



MSL

300 ↗

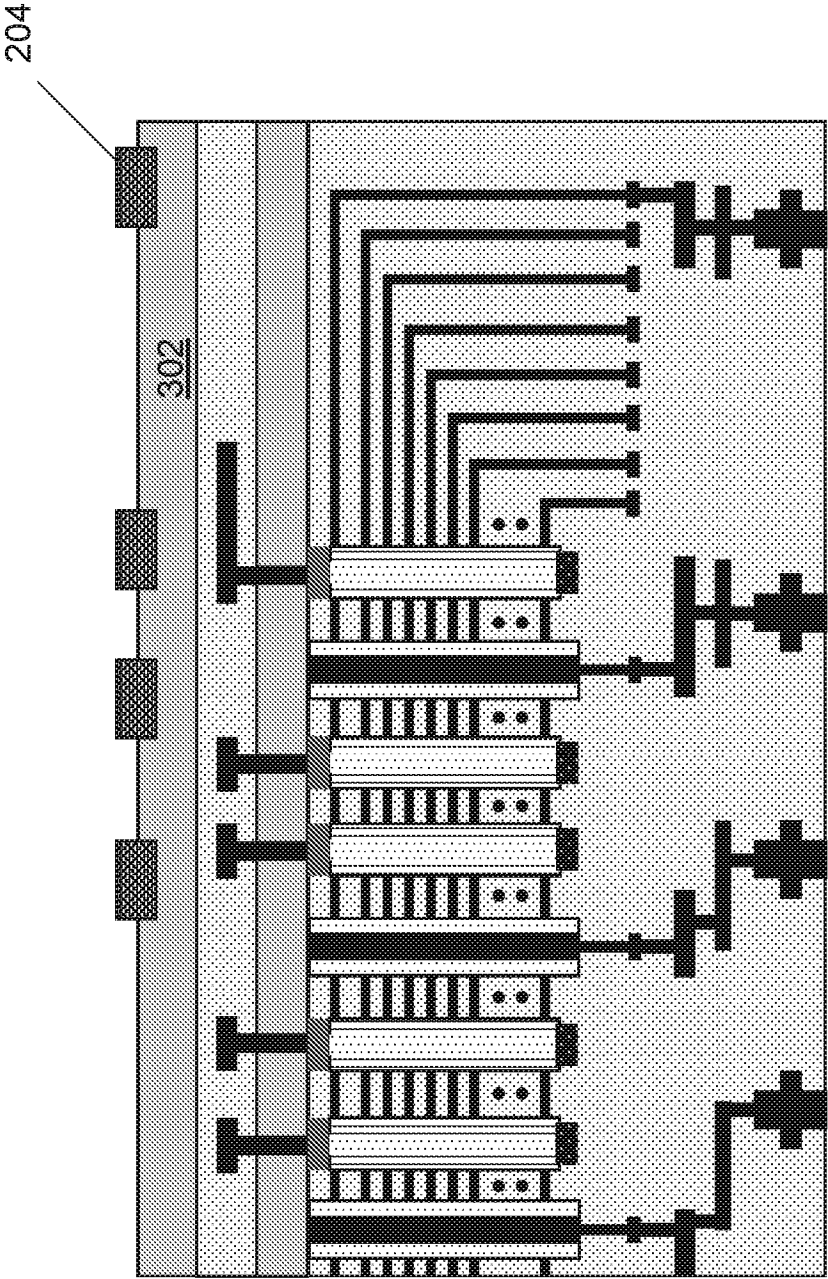


FIG. 5C

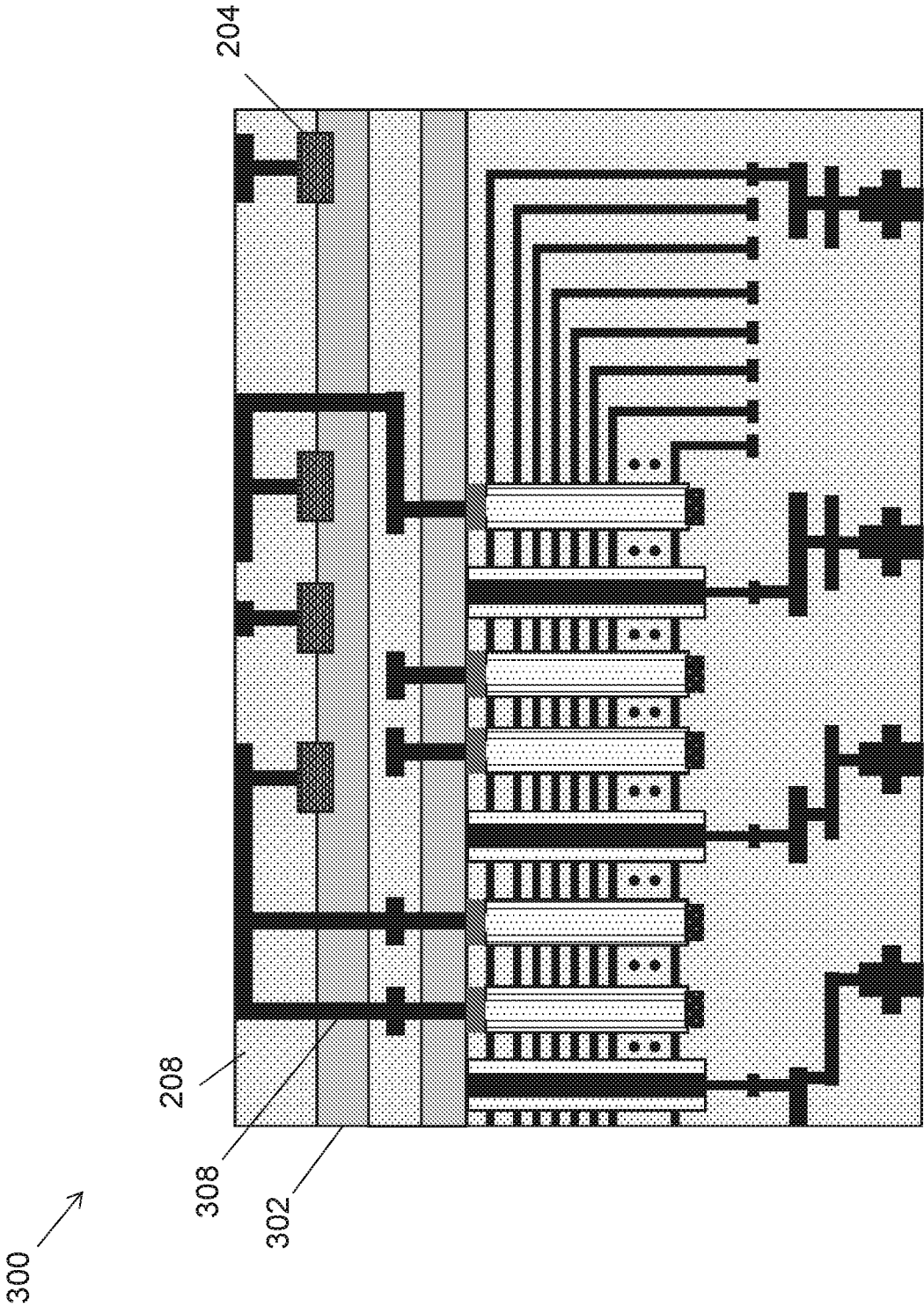


FIG. 5D

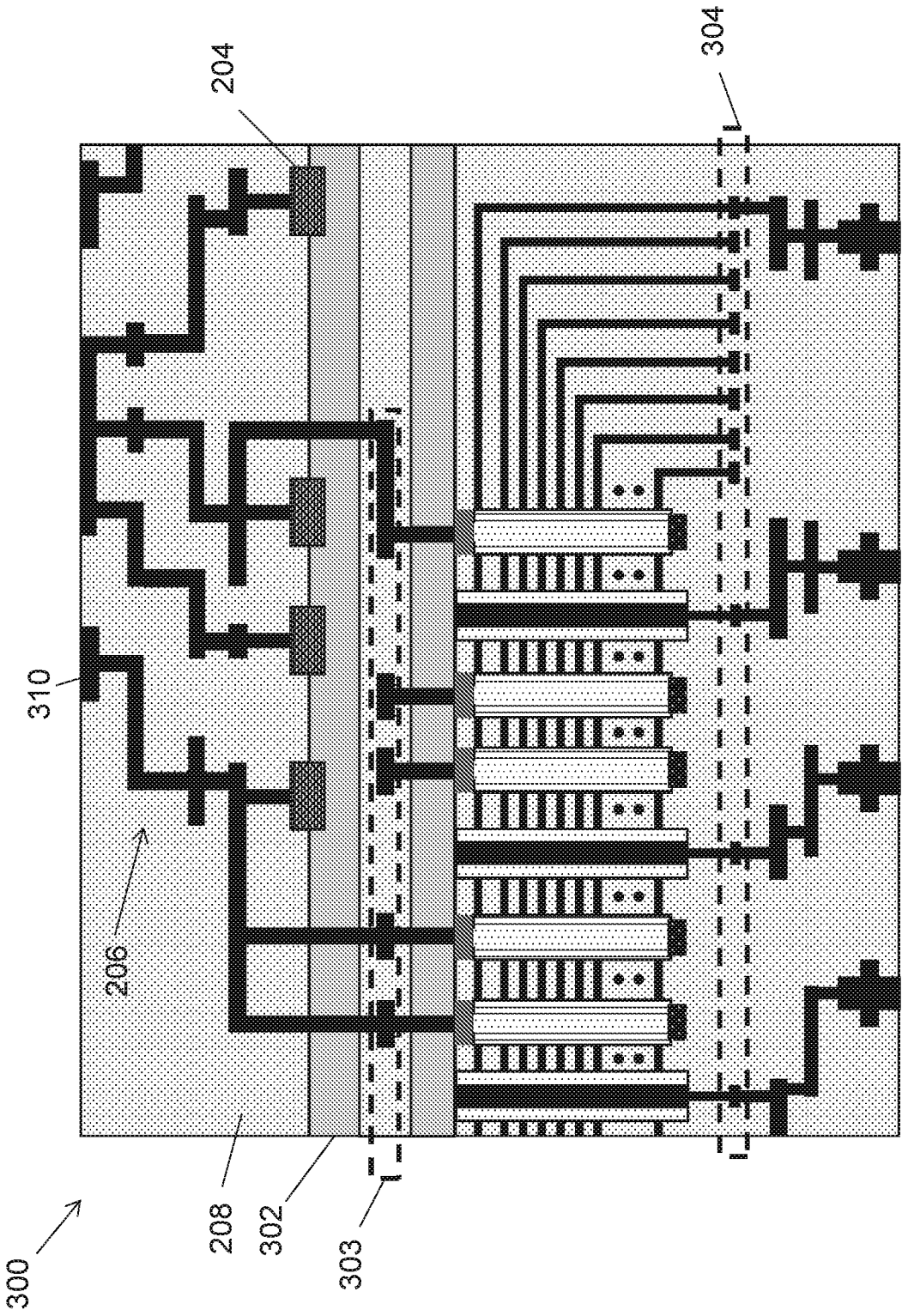
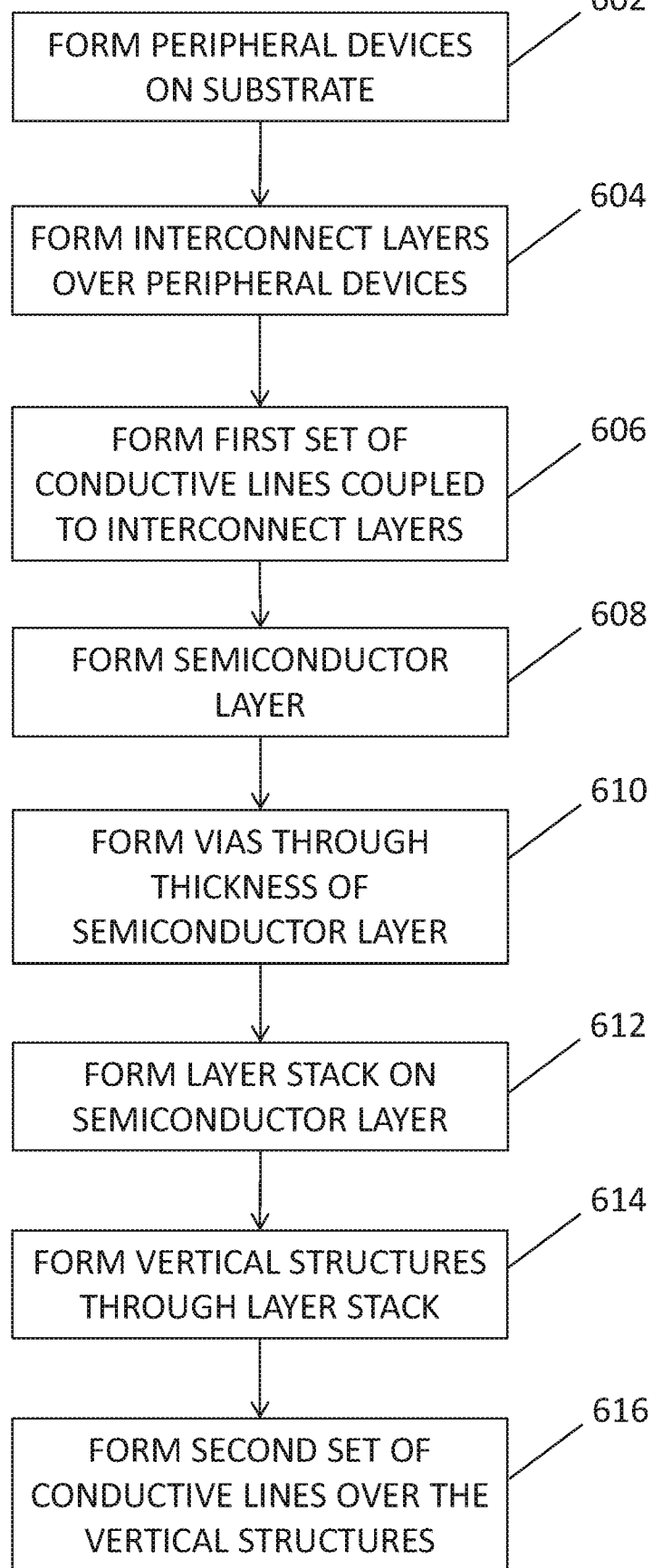
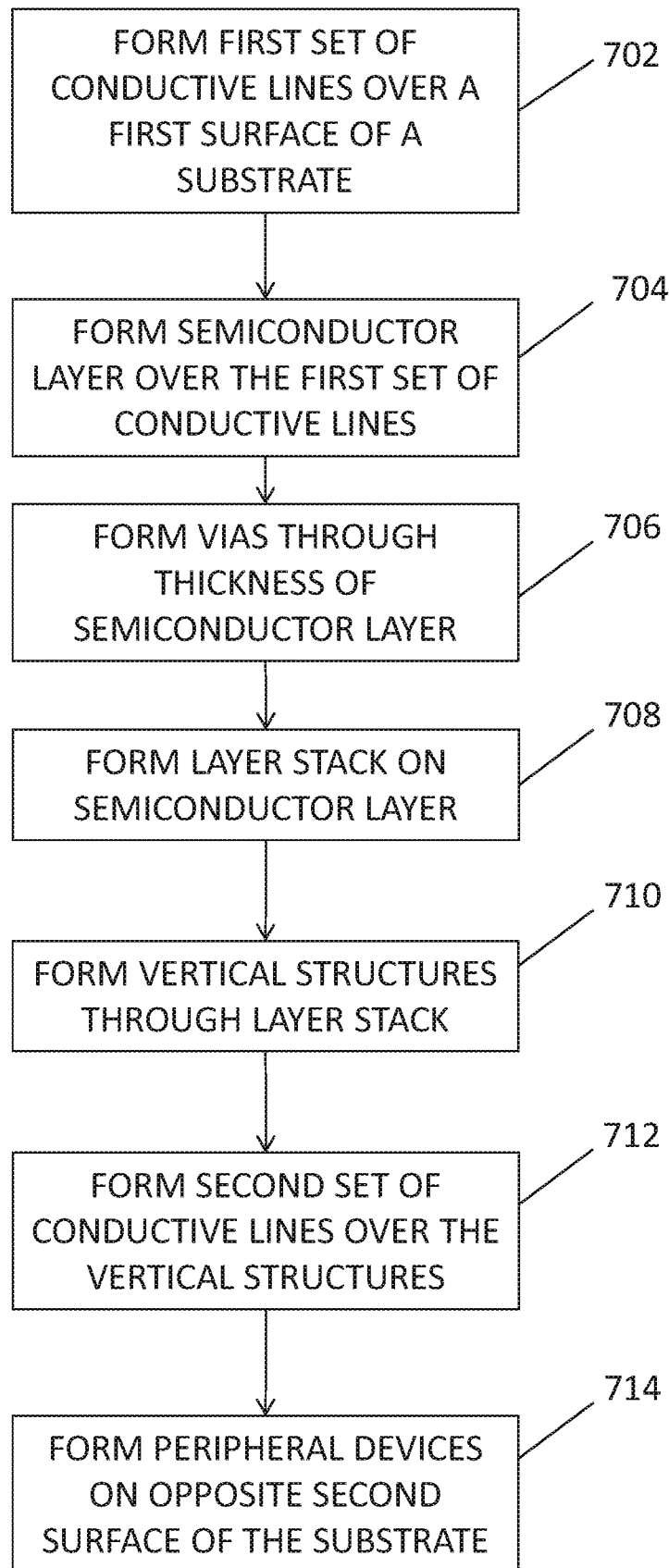


FIG. 5E

600**FIG. 6**

700**FIG. 7**

INTERNATIONAL SEARCH REPORT

International application No.

PCT/CN2018/104834

A. CLASSIFICATION OF SUBJECT MATTER

H01L 27/115(2017.01)i; H01L 21/8239(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L; G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNPAT,CNKI,EPODOC,WPI: memory, three-dimensional, 3D, substrate, dielectric, peripheral, interconnect layer, semiconductor layer, layer stack, conductor layer, insulator layer, vertical, conductive line

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2017186750 A1 (TAIWAN SEMICONDUCTOR MANUFACTURING CO., LTD.) 29 June 2017 (2017-06-29) description, paragraphs [0020]-[0067]	1-40
A	US 2010193861 A1 (SHIM, SUNIL ET AL.) 05 August 2010 (2010-08-05) the whole document	1-40
A	CN 103137625 A (INSTITUTE OF MICROELECTRONICS OF THE CHINESE ACADEMY OF SCIENCES) 05 June 2013 (2013-06-05) the whole document	1-40
A	CN 103295966 A (MACRONIX INTERNATIONAL CO., LTD.) 11 September 2013 (2013-09-11) the whole document	1-40

☐ Further documents are listed in the continuation of Box C.☒ See patent family annex.

* Special categories of cited documents:

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“O” document referring to an oral disclosure, use, exhibition or other means

“P” document published prior to the international filing date but later than the priority date claimed

“T” later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

“X” document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

“Y” document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

“&” document member of the same patent family

Date of the actual completion of the international search

07 May 2019

Date of mailing of the international search report

04 June 2019

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Facsimile No. (86-10)62019451

Telephone No. 86-(10)-53961637

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.

PCT/CN2018/104834

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				TW	201735019	A	01 October 2017
US	2010193861	A1	05 August 2010	CN	101794789	A	04 August 2010
				KR	20100088829	A	11 August 2010
CN	103137625	A	05 June 2013	None			
CN	103295966	A	11 September 2013	None			