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(54) **SEMICONDUCTOR PACKAGE FOR A SEMICONDUCTOR CHIP HAVING CENTRALLY LOCATED BOTTOM BOND PADS**

4,532,419 * 7/1985 Takeda 235/492
4,539,472 * 9/1985 Poetker et al. 235/488
4,722,765 * 2/1988 Ambros et al. 29/846

(List continued on next page.)

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FOREIGN PATENT DOCUMENTS

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39 11 711 * 10/1990 (DE) .
0 198 194 * 10/1986 (EP) .

(List continued on next page.)

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OTHER PUBLICATIONS

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Related U.S. Patent Documents

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Goodenough, Frank: "Mixing Gold and Aluminum Bond Wires on Power ICs Cuts Cost and Ups Reliability"; p. 34; In: Electronic Design, 11, H.19, 1990.*

Bregman, Mark F. and Kovac, Carolin A.; "Plastic for VLSI-Based Computers"; H.6, S.75-80; In: Solid State Technology, Jun. 1968.*

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(62) Division of application No. 08/748,460, filed on Nov. 8, 1996, now Pat. No. Re. 36,097.

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(57) **ABSTRACT**

(51) **Int. Cl.**⁷ **H01L 21/50**; H01L 21/56; H01L 21/60

A semiconductor package having outer leads which are not protruded from the package but only exposed to outside. The semiconductor package comprises a semiconductor chip which is formed with a plurality of bond pads at a central portion of its bottom surface, a lead frame including leads connected to bond pads for input/output of the bond pads respectively and bus bars connected to power supplying pads of the bond pads, insulation adhesives for attaching inner leads of the leads and inner leads of the bus bars to a bottom surface of the semiconductor chip formed with the bond pads, metal wires for electrically connecting the inner leads of the leads and the inner leads of the bus bars to the bond pads respectively, and a molding compound enveloping the semiconductor chip assembly with outer leads of the lead frame exposed to outside. The adhesive tapes are removed after a molding procedure.

(52) **U.S. Cl.** **438/124**; 438/118; 438/123; 438/126; 438/127; 438/977; 29/827; 29/841; 29/856; 264/272.17; 257/691; 257/693; 257/696; 257/787; 174/52.4; 361/773; 361/775; 361/783; 361/813

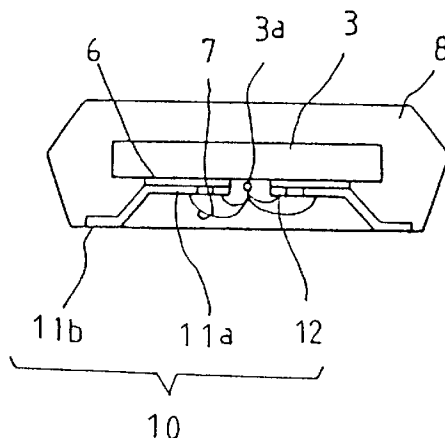
(58) **Field of Search** 438/112, 118, 438/123, 124, 127; 29/827, 841, 855, 856; 264/272.11, 272.15, 272.17; 257/692, 693, 696, 698, 787, 691; 174/52.4; 361/767, 772, 773, 775, 783, 813

(56) **References Cited**

U.S. PATENT DOCUMENTS

3,940,786 * 2/1976 Scheingold et al. 257/773

37 Claims, 5 Drawing Sheets



U.S. PATENT DOCUMENTS

4,937,656	*	6/1990	Kohara	257/676	60183745	9/1985	(JP)	23/4
5,107,325	*	4/1992	Nakayoshi	257/793	60257159	12/1985	(JP)	23/48
5,122,860	*	6/1992	Kikuchi et al.	257/679	61222715	10/1986	(JP)	45/14
5,157,480	*	10/1992	McShane et al.	257/693	622560	1/1987	(JP)	23/48
5,166,866	*	11/1992	Kim et al.	361/767	6276540A	4/1987	(JP)	257/693
5,172,214	*	12/1992	Casto	257/676	62134944	6/1987	(JP)	23/28
5,200,362	*	4/1993	Lin et al.	438/126	62154769	7/1987	(JP)	23/52
5,229,846	*	7/1993	Kozuka	257/678	62249464	10/1987	(JP)	23/48
5,235,207	*	8/1993	Ohi et al.	257/670	62-298146 A	* 12/1987	(JP)	257/692
5,273,938	*	12/1993	Lin et al.	438/127	2298146	12/1987	(JP)	257/692
5,436,500	*	7/1995	Park et al.	257/696	1189149	1/1988	(JP)	
5,474,958	*	12/1995	Djennas et al.	438/124	6367763A	3/1988	(JP)	257/693
5,529,959	*	6/1996	Yamanaka	438/123	63-151058 A	* 6/1988	(JP)	257/692
5,583,375	*	12/1996	Tsubosaki et al.	257/692	3151058	6/1988	(JP)	257/692
5,693,573	*	12/1997	Choi	438/123	63296252	12/1988	(JP)	257/666
					01-161724 A	* 6/1989	(JP)	
					247061	3/1990	(JP)	23/50
					263142	3/1990	(JP)	23/28
					02-170456 A	* 7/1990	(JP)	257/692
					2246125	10/1990	(JP)	21/60
					03-131059 A	* 6/1991	(JP)	257/692
					05166964	7/1993	(JP)	257/693
					06132453	5/1994	(JP)	257/693
					06236956	8/1994	(JP)	257/693

FOREIGN PATENT DOCUMENTS

0 465 143	*	1/1992	(EP)					
0 501 830	*	9/1992	(EP)					
51-016701 A	*	2/1976	(JP)					
57-176751 A	*	10/1982	(JP)					
5811198		1/1983	(JP)	15/2				
6015786		1/1985	(JP)					
6068488		4/1985	(JP)					

* cited by examiner

FIG. 1A
PRIOR ART

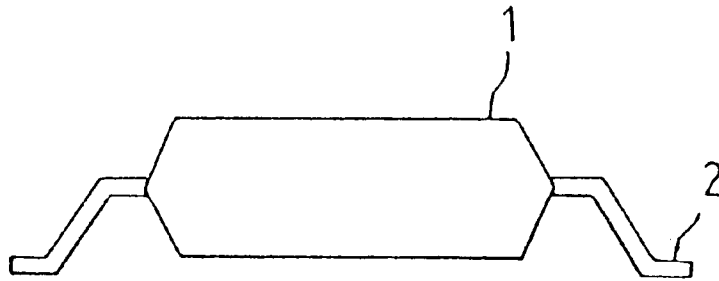


FIG. 1B
PRIOR ART

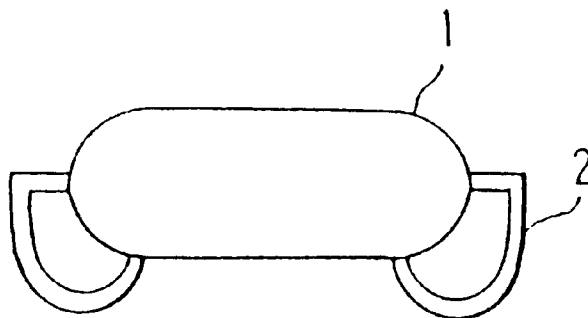


FIG. 2
PRIOR ART

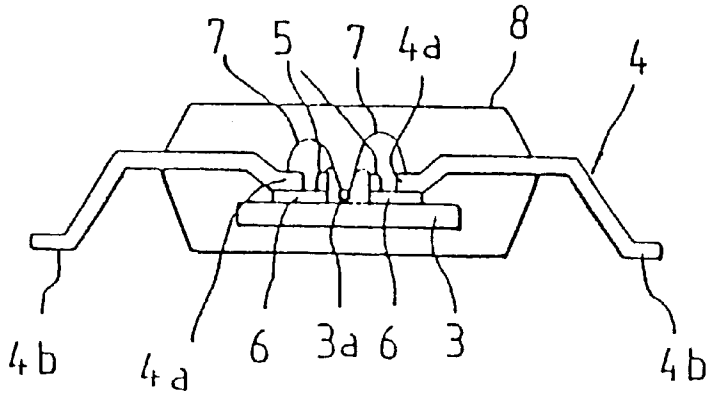


FIG. 3
PRIOR ART

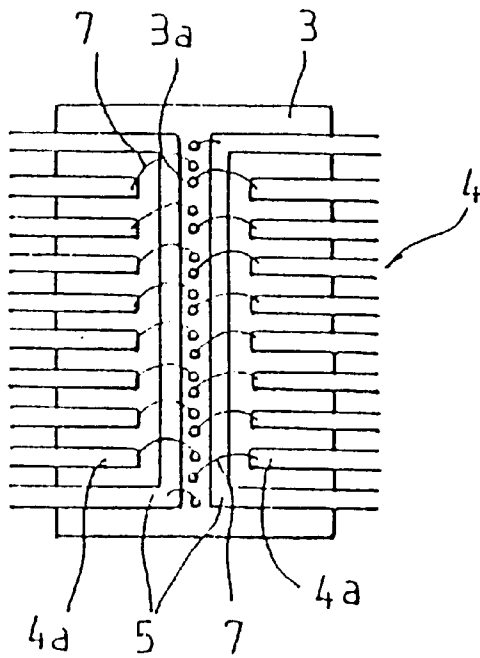


FIG. 4

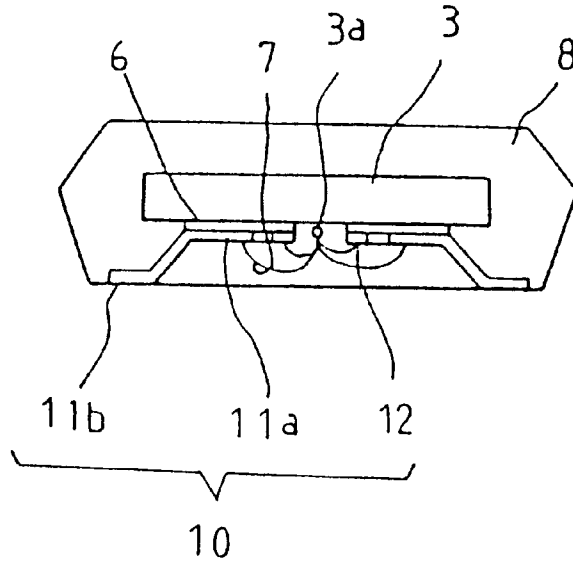


FIG. 5

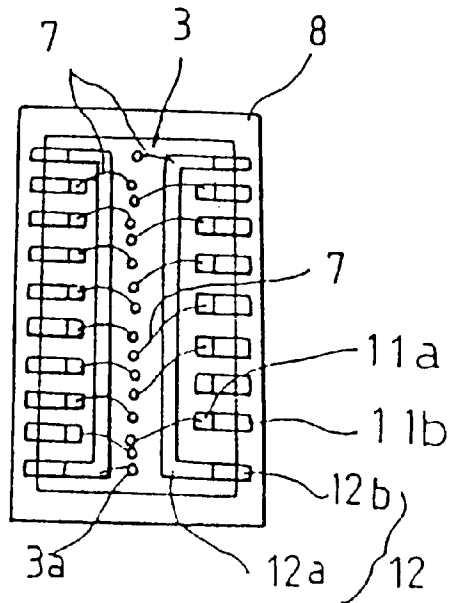


FIG. 6A

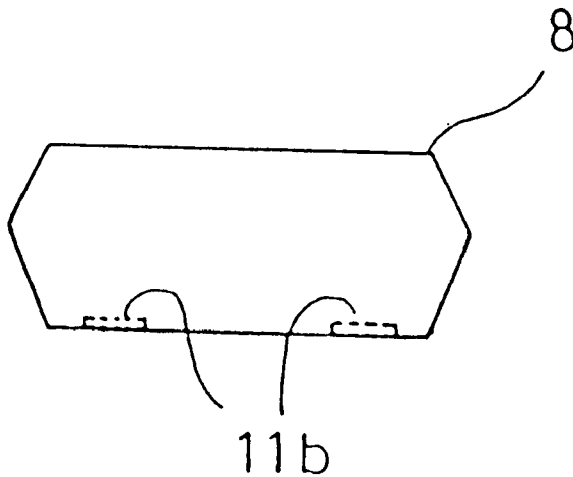


FIG. 6B

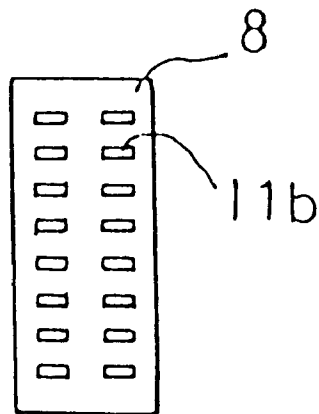
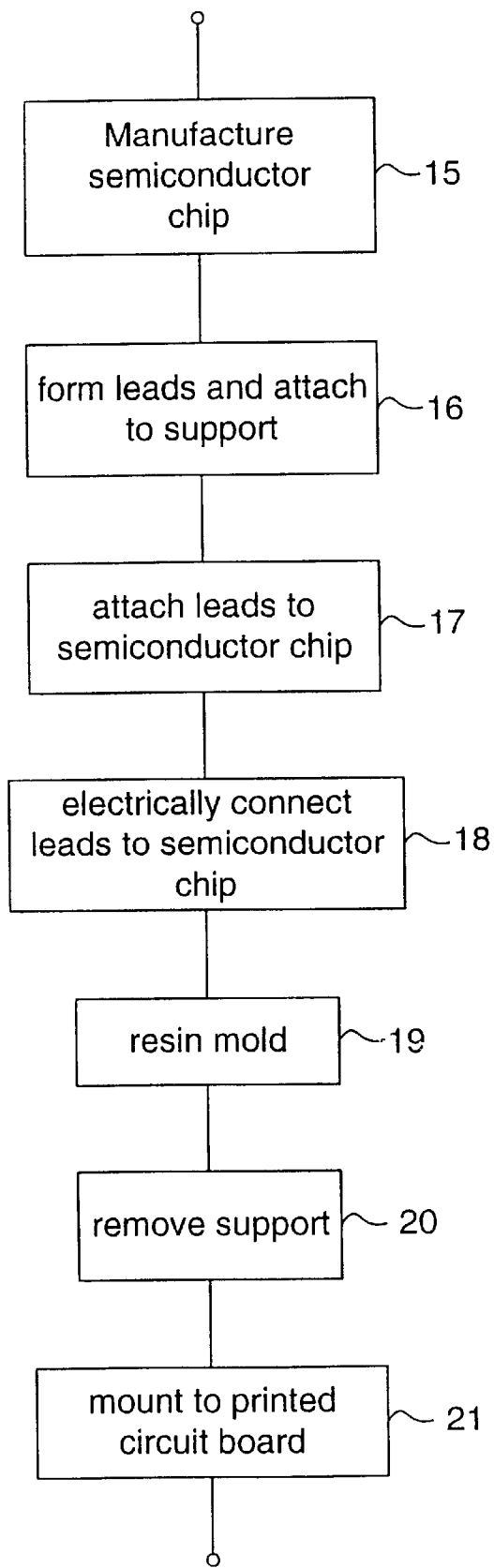


Fig. 7
(NEW)



**SEMICONDUCTOR PACKAGE FOR A
SEMICONDUCTOR CHIP HAVING
CENTRALLY LOCATED BOTTOM BOND
PADS**

Matter enclosed in heavy brackets [] appears in the original patent but forms no part of this reissue specification; matter printed in italics indicates the additions made by reissue.

This is a Divisional Reissue Application of application Ser. No. 08/748,460 filed Nov. 8, 1996 (now matured into U.S. Pat. No. Re. 36,097), which is a Reissue Application of U.S. Pat. No. 5,363,279 issued on Nov. 8, 1994.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a semiconductor package, and more particularly to a semiconductor package suitable for packaging a center pad layout-shaped memory chip wherein paddles of a lead frame are removed and outer leads of a lead frame are not protruded from the package but only exposed to a lower surface of molding resin of a semiconductor package.

2. Description of the Prior Art

Generally, semiconductor packages may be mainly classified into a semiconductor of SOP (small outline package) type and a semiconductor of SOJ (small outline J-lead) type.

In this case, the semiconductor packages are manufactured in accordance to following procedures. A semiconductor chip is attached on paddles of a lead frame and then wire bonding is carried out between inner leads of the lead frame and pads on the semiconductor chip. The wire bonded semiconductor and lead frame are molded by molding resin. Thereafter, the resulting product is subjected to deflash, trimming and forming procedures so that outer leads of the lead frame are protruded from the molded resin and then bent into predetermined shape respectively.

Referring to FIGS. 2 and 3, there are shown a front section and a bottom of a semiconductor package of LOC (lead on chip) type. In the semiconductor package shown in FIGS. 2 and 3, a semiconductor chip 3 is formed with a plurality of bond pads 3a at central portion thereof. Inner leads 4a of a lead frame 4 without paddles are attached on a surface of the semiconductor chip 3 at both sides of the bond pads 3a by means of insulation tapes 6. The inner leads 4a are electrically connected to the bond pads 3a of the semiconductor chip 3 by means of metal wires 7, respectively. Also, power supplying pads of the bond pads 3a are electrically connected to bus bars 5 by metal wires 7, respectively. Thereafter, the resulting semiconductor chip 3 and the inner leads 4a of the lead frame 4 are molded by molding resin 1.

The above-mentioned prior semiconductor packages are manufactured in such a manner that a semiconductor chip aggregate is subjected to a sawing step for dividing the semiconductor chip aggregate into separate semiconductor chips 3 and the semiconductor chip 3 is subjected to a die bonding step for attaching the separated semiconductor chip 3 to a lead frame 4, a wire bonding step for electrically connecting bond pads 3a of the semiconductor chip 3 to inner leads 4a of the lead frame 4 respectively, a molding step for enveloping the wire bonded semiconductor chip 3 and lead frame 4, a deflashing step, a solder plating step, a trimming step for cutting dampers of the lead frame 4, a forming step for bending outer leads into a certain shape, and a marking step.

The semiconductor package prepared as described above have outer leads protruded from the mold resin. The outer

leads are formed into a certain shape and then mounted on a printed circuit board.

However, the prior semiconductor packages have various disadvantages as follows. The prior semiconductor packages occupy large space due to the outer leads protruded from mold resins when the semiconductor packages are mounted on printed circuit boards.

Since the semiconductor packages have outer mechanical shock when their forming procedure, fine gaps may occur in contact areas between outer leads protruded from package bodies and mold resins, thereby causing humidity resistant property to be deteriorated due to the gaps.

Also, since the semiconductor packages require a trimming step and a forming step after a molding procedure, manufacturing process of the packages becomes complicated so that their manufacturing cost and poor products occurring rate are increased.

In addition, in case of the LOC type of semiconductor packages using lead frames without paddles, electrical property is decreased because of their long length between inner leads and outer leads.

Furthermore, so-called "good rate" which is a rate of good products in products identified as poor packages is increased because of poor lead contacts in testing of finished products.

SUMMARY OF THE INVENTION

Therefore, the present invention is made in view of the above-described prior art problems and an object of the invention is to provide a semiconductor package which is designed to occupy small space required to be mounted on a printed circuit board and to reduce manufacturing cost by omitting manufacturing procedures next to a molding procedure.

Another object of the invention is to provide a semiconductor package which has improved lead conductance and thus electrical property by reducing length between its inner leads and outer leads.

In accordance with the present invention, these object can be accomplished by providing a semiconductor package comprising: a semiconductor chip which is formed with a plurality of bond pads at a central portion of its bottom surface; a lead frame including leads connected to bond pads for input/output of the bond pads respectively and bus bars connected to power supplying pads of the bond pads; insulation adhesives for attaching inner leads of the leads and inner leads of the bus bars to a bottom surface of the semiconductor chip formed with the bond pads; metal wires for electrically connecting the inner leads of the leads and the inner leads of the bus bars to the bond pads respectively; and a molding compound enveloping the semiconductor chip assembly with outer leads of the lead frame exposed to outside.

Since the leads of the invention are shortened in length between their inner leads wire-bonded to the bond pads of the semiconductor chip and their outer leads exposed to outside, it is possible to improve lead conductance in a LOC type of semiconductor package and to radiate easily heat occurring in operation of the chip due to their short leads. Particularly, the semiconductor package is appropriate to package a semiconductor chip of 16-mega-bit DRAM or greater which is formed with bond pads at its central portion.

The leads are bent into a certain shape respectively at their inner leads and the outer leads and then the outer leads are attached to polyimide based adhesive tapes. The inner leads of the leads are attached to a bottom surface of the semi-

conductor chip via insulating films or insulating paste applied to the bottom surface. The attached lead frame and the semiconductor chip are molded such that the outer leads are not protruded from the molded resin but exposed to outside.

In accordance to the invention as described above, paddles are omitted and the outer leads are not protruded from the package but exposed to outside so that the exposed outer leads can be connected to a connection pattern of a printed circuit board. Since the semiconductor package has not protruded outer leads, space occupied by the package is reduced when the package is mounted on a printed circuit board. Also, it is possible to abbreviate trimming and forming procedures next to a molding procedure in its manufacturing process.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other objects and aspects of the invention will become apparent from the following description of an embodiment with reference to the accompanying drawings in which:

FIG. 1A is a schematic view of a prior SOP type of semiconductor package;

FIG. 1B is a schematic view of a prior SOJ type of semiconductor package;

FIG. 2 is a vertical sectional view of a prior LOC type of semiconductor package;

FIG. 3 is a bottom plan view of the semiconductor package shown in FIG. 2, showing its inner construction;

FIG. 4 is a vertical sectional view of a semiconductor package according to the present invention;

FIG. 5 is a bottom plan view of the semiconductor package shown in FIG. 4, showing its inner construction;

FIG. 6A is a front elevational view of a semiconductor package according to the invention; [and]

FIG. 6B is a bottom plan view of the semiconductor package shown in FIG. 6A[.]; and

FIG. 7 illustrates a manufacturing process in accordance with the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention will now be described by referring to FIGS. 4 to 6 in the accompanying drawings. FIG. 4 shows a vertical section of a semiconductor package according to the present invention and FIG. 5 shows an inner construction of the semiconductor package shown in FIG. 4.

As shown in the drawings, the semiconductor package of the present invention comprises a semiconductor chip 3 which is formed with a plurality of bond pads 3a at a central portion of its bottom surface, a lead frame 10 including leads 11 connected to bond pads for input/output of the bond pads 3a respectively and bus bars 12 connected to power supplying pads of the bond pads 3a, insulation adhesives 6 for attaching inner leads 11 of the leads 11 and inner leads 12a of the bus bars 12 to a bottom surface of the semiconductor chip 3 formed with the bond pads 3a, metal wires 7 for electrically connecting the inner leads 11a of the leads 11 and the inner leads 12a of the bus bars 12 to the bond pads 3a respectively, and a molding compound 8 enveloping the semiconductor chip assembly with outer leads 11b and 12b of the lead frame 10 exposed to outside.

In this description, the substantially identical or similar elements of the semiconductor package of the invention to

those of the prior art illustrated in FIGS. 1 to 3 are designated by the similar reference characters.

The plurality of inner leads 11a, 12a and outer leads 11b, 12b of the leads 11 and the bus bars 12 are bent into a predetermined shape respectively and arranged in a row. Then, the outer leads 11b, 12b are attached to adhesive tapes (not shown) at their outer surfaces so that the leads 11 and the bus bars 12 are integrally held. The adhesive tapes, which may serve as a support during a molding procedure, are removed after [a] the molding procedure.

The lead frame 10 is attached to the semiconductor package 3 in such a manner that insulating adhesives 6 such as insulating films and insulating paste are applied to the bottom surface of the semiconductor chip 3 formed with the bond pads 3a and then the inner leads 11a, 12a of the leads 11 and the bus bars 12 are attached to the insulating adhesives 6.

Also, the leads 11 and the bus bars 12 of the semiconductor package of the present invention are shorter than those of a prior LOC type of semiconductor package in lengths between its inner leads 11a, 12a and its outer leads 11b, 12b so that lead conductance is increased when a memory chip of 16-mega-bit DRAM or greater is packaged. In addition, heat occurring in operation of chip can be easily discharged from the short leads.

FIG. 6A shows a front side of the semiconductor package of the invention and FIG. 6B shows a bottom surface of semiconductor package of the invention. As shown in FIG. 6A, the outer leads 11b and 12b of the leads 11 and the bus bars 12 are not protruded from the semiconductor package but are flush with the bottom surface of the semiconductor package.

That is, the outer leads 11b and 12b of the leads 11 and the bus bars 12 are arranged in a row at the bottom surface of the package and faces to outside to be contacted with elements of a printed circuit board, as shown in FIG. 6B. As shown in FIGS. 4 and 6B, the leads may be elongated and contoured and extend away from the bottom surface, and the exposed portion of the leads may occupy less than a majority portion of the bottom surface.

A manufacturing process of the semiconductor package as constructed above will be described in detail hereinafter.

First, a semiconductor chip 3 which has been cut separately is applied with insulating adhesive 6 such insulating film and insulating paste at its bottom surface formed with bond pads 3a. Inner leads 11a and 12a of leads 11 and bus bars 12 are attached to the bottom surface of the chip via the insulating adhesive 6 applied to the bottom surface.

Thereafter, the lead frame 10 attached to the semiconductor chip 3 is die-attached in a wire bonder (a wire bonding apparatus) and subjected to a wire bonding procedure for electrically connecting the inner leads 11a, 12a of the leads 11 and the bus bars 12 to the bond pads 3a by metal wires 7 such as gold and aluminum wires.

Subsequently, the resulting semiconductor chip assembly is subjected to a known transfer molding procedure to be enveloped. Then, as adhesive tapes attached to a bottom surface of the molded resin are removed, the outer leads 11b and 12b of the leads 11 and the bus bars 12 are exposed to outside. Thereafter, as the bottom surface of the molded package and the exposed outer leads are simply removed by a deflash procedure, the manufacturing process of the semiconductor package is completed.

The semiconductor package of the invention as prepared above is mounted on a printed circuit board such that the

exposed outer leads 11b and 12b are connected to a pattern of printed circuit board by a soldering.

FIG. 7 illustrates a manufacturing process such as described herein. At step 15, the semiconductor chip is manufactured, as described earlier. At step 16, leads 11 are formed and attached to the support, which may be an adhesive tape as described earlier. At step 17, inner leads 11a and 12a are attached to semiconductor chip 3 with insulating adhesive 6. At step 18, inner leads 11a and 12a are wire bonded to bond pads 3a. At step 19, the resulting semiconductor chip assembly is subjected to a transfer molding procedure. At step 20, the adhesive tapes serving as the support during the molding procedure are removed. At step 21, the semiconductor package of the present invention is mounted on a printed circuit board.

As apparent from the above description, the present invention can leave out procedures next to a molding step. That is, since a prior semiconductor package has outer leads protruded therefrom, a manufacturing process of a prior semiconductor package requires a forming procedure for bending the protruded outer leads and a trimming procedure for cutting dampers of leads. However, since leads according to the invention are attached to adhesive tapes to form an integral lead frame and outer leads of leads are exposed to outside, a manufacturing process of the invention does not require trimming and forming procedures.

Therefore, the present invention has advantages in that since the number of manufacturing steps is significantly reduced, occurrence of poor products and manufacturing cost are reduced.

Also, since the semiconductor package of the invention has not outer leads protruded therefrom, space occupied by the semiconductor package is reduced thereby allowing the packages to be densely mounted when the packages are mounted on a printed circuit board.

In addition, since the semiconductor package of the invention has leads shortened as possible as, it is possible to improve its electrical property and to radiate heat easily as compared with prior art.

While prior semiconductor package may have gaps between outer leads and a molded resin due to outer shock applied to the outer leads during trimming and forming procedures, the semiconductor package of the invention has outer leads exposed to out side and does not require trimming and forming procedures so that the outer leads are not shocked. Therefore, the semiconductor package of the invention can prevent gaps from occurring in the contact area and thus improve humidity resistance. Also, since the semiconductor package is tested in state of tip, the test can be precisely carried out without a particular testing socket. That is, "Good rate" can be reduced.

Changes in construction will occur to those skilled in the art and various apparently different modifications and embodiments may be made without departing from the scope of the invention. The matter set forth in the foregoing description and accompanying drawings is offered by way of illustration only. It is therefore intended that the foregoing description be regarded as illustrative rather than limiting.

What is claimed is:

[1. A semiconductor package comprising:

a semiconductor chip with a plurality of bond pads including at least one power supplying bond pad at a central portion of a bottom surface of said semiconductor chip;

a plurality of leads connected to bond pads for input/output of said bond pads, respectively, each of said leads defining an inner lead and an outer lead;

at least one bus bar connected to said at least one power supplying bond pad, said at least one bus bar defining an inner lead and an outer lead;

insulation adhesives for attaching said inner leads of each of the leads and said at least one bus bar to said bottom surface of the semiconductor chip;

metal wires for electrically connecting the inner leads of the leads and the at least one bus bar to the bond pads, respectively; and

a molding compound enveloping the semiconductor chip, and the inner leads of the leads and the bus bar with bottom surfaces of said outer leads of the leads and the bus bar exposed to outside on the bottom surface of said molding compound.]

[2. A semiconductor package according to claim 1, wherein said adhesive tapes are polyimide based tapes.]

[3. A semiconductor package according to claim 1, wherein said adhesive is an insulating film.]

[4. A semiconductor package according to claim 1, wherein said adhesive is insulating paste.]

[5. A semiconductor package according to claim 1, wherein said metal wires are gold wires.]

[6. A semiconductor package according to claim 1, wherein said metal wires are aluminum wires.]

7. A method of packaging a semiconductor device, comprising the steps of:

forming a plurality of contoured leads attached to a support;

attaching the plurality of contoured leads to the semiconductor chip with an insulating adhesive, wherein the contoured leads each have at least a first portion and a second portion, wherein the chip is attached at a first portion of the contoured leads, wherein the contoured leads extend away from a point where a bottom surface of the semiconductor device will be formed to provide for electrical connection of the contoured leads to the semiconductor chip;

electrically connecting the contoured leads to the semiconductor chip;

molding the semiconductor chip and the plurality of contoured leads with a resin, wherein the support is attached to the second portion of the contoured leads during the molding, wherein the semiconductor chip is completely enveloped by the resin, wherein the second portion of the contoured leads attached to the support during the molding are not covered by the resin; and removing the support from the second portion of the contoured leads, wherein the second portion of the contoured leads is exposed to provide electrical connection points, wherein the second portion of the contoured leads is flush with the bottom surface of the semiconductor device.

8. The method of claim 7, wherein the support comprises an adhesive tape.

9. The method of claim 7, further comprising the step of connecting the exposed second portion of the contoured leads to a printed circuit board.

10. The method of claim 7, wherein the contoured leads are elongated and contoured to extend away from the bottom surface of the semiconductor device.

11. The method of claim 7, wherein the contoured leads are contoured away from the bottom surface of the semiconductor device to provide a portion for wire bonding of the contoured leads to the semiconductor chip.

12. The method of claim 7, wherein the exposed second portions of the contoured leads comprises less than a majority portion of the area of the bottom surface.

13. The method of claim 7, wherein the semiconductor chip has a length, wherein the contoured leads extend along the length of the semiconductor chip.

14. The method of claim 13, wherein the contoured leads do not extend beyond the length of the semiconductor chip.

15. The method of claim 14, wherein the semiconductor device comprises a memory device.

16. The method of claim 13, wherein the semiconductor device comprises a memory device.

17. The method of claim 7, wherein the semiconductor chip has a major surface on which are formed circuit elements, wherein the contoured leads are attached to the major surface by the insulating adhesive.

18. The method of claim 17, wherein the contoured leads are attached at a central portion of the major surface.

19. The method of claim 17, wherein the insulating adhesive comprises an insulating film.

20. The method of claim 17, wherein the insulating adhesive comprises an insulating paste.

21. The method of claim 7, wherein at least one of the contoured leads comprises a power supply bus bar.

22. The method of claim 21, wherein the power supply bus bar is attached to a central portion of the semiconductor chip.

23. The method of claim 7, wherein the contoured leads are electrically connected to the semiconductor chip with bonding wires.

24. The method of claim 7, wherein the exposed second portions of the contoured leads are positioned on the bottom surface of the semiconductor package, wherein the exposed second portion of the contoured leads do not extend beyond the bottom surface of the semiconductor package.

25. A method of packaging a semiconductor device, comprising the steps of:

manufacturing a semiconductor chip;

forming a plurality of leads, wherein the leads each have at least a first portion and a second portion, and attaching the leads to a support, wherein the support is attached to the leads at the second portion;

attaching the plurality of leads to the semiconductor chip with an insulating adhesive, wherein the chip is attached at the first portion of the leads;

electrically connecting the leads to the semiconductor chip;

molding the semiconductor chip and the plurality of leads with a resin, wherein the support is attached to the second portion of the leads during the molding, wherein the second portion of the leads are not covered by the resin; and

removing the support from the second portion of the leads, wherein the second portion of the leads is exposed to provide electrical connection points,

wherein the semiconductor chip has a length, wherein the leads extend along the length of the semiconductor chip, and

wherein the leads do not extend beyond the length of the semiconductor chip.

26. The method of claim 25, further comprising the step of connecting the exposed second portion of the leads to a printed circuit board.

27. The method of claim 25, wherein the exposed second portions of the leads are positioned on a bottom surface of the semiconductor device.

28. The method of claim 27, wherein the leads are contoured to extend away from the bottom surface of the semiconductor device.

29. The method of claim 27, wherein the leads are elongated and contoured to extend away from the bottom surface of the semiconductor device.

30. The method of claim 27, wherein the leads are flush with the bottom surface of the semiconductor device.

31. The method of claim 27, wherein the leads are contoured away from the bottom surface of the semiconductor device to provide a portion for wire bonding of the leads to the semiconductor chip.

32. The method of claim 25, wherein the semiconductor device comprises a memory device.

33. The method of claim 25, wherein the leads are electrically connected to the semiconductor chip with bonding wires.

34. The method of claim 25, wherein the exposed second portions of the leads are positioned on a bottom surface of the semiconductor package, wherein the exposed second portions of the leads do not extend beyond the bottom surface of the semiconductor package.

35. A method of packaging a semiconductor device, comprising the steps of:

manufacturing a semiconductor chip;

forming a plurality of leads, wherein the leads each have at least a first portion and a second portion, and attaching the leads to a support, wherein the support is attached to the leads at the second portion;

attaching the plurality of leads to the semiconductor chip with an insulating adhesive, wherein the chip is attached at the first portion of the leads;

electrically connecting the leads to the semiconductor chip;

molding the semiconductor chip and the plurality of leads with a resin, wherein the support is attached to the second portion of the leads during the molding, wherein the second portion of the leads are not covered by the resin; and

removing the support from the second portion of the leads, wherein the second portion of the leads is exposed to provide electrical connection points,

wherein the support comprises an adhesive tape.

36. A method of packaging a semiconductor device, comprising the steps of:

manufacturing a semiconductor chip;

forming a plurality of leads, wherein the leads each have at least a first portion and a second portion, and attaching the leads to a support, wherein the support is attached to the leads at the second portion;

attaching the plurality of leads to the semiconductor chip with an insulating adhesive, wherein the chip is attached to the first portion of the leads;

electrically connecting the leads to the semiconductor chip;

molding the semiconductor chip and the plurality of lead with a resin, wherein the support is attached to the second portion of the leads during the molding, wherein the second portion of the leads are not covered by the resin; and

removing the support from the second portion of the leads, wherein the second portion of the leads is exposed to provide electrical connection points;

wherein the exposed second portions of the leads are positioned on a bottom surface of the semiconductor device, and

wherein the exposed second portions of the leads comprise less than a majority portion of the area of the bottom surface.

37. A method of packaging a semiconductor device, comprising the steps of:
 manufacturing a semiconductor chip;
 forming a plurality of leads, wherein the leads each have at least a first portion and a second portion, and attaching the leads to a support, wherein the support is attached to the leads at the second portion;
 attaching the plurality of leads to the semiconductor chip with an insulating adhesive, wherein the chip is attached at the first portion of the leads;
 electrically connecting the leads to the semiconductor chip;
 molding the semiconductor chip and the plurality of leads with a resin, wherein the support is attached to the second portion of the leads during the molding, wherein the second portion of the leads are not covered by the resin; and
 removing the support from the second portion of the leads, wherein the second portion of the leads is exposed to provide electrical connection points,
 wherein the semiconductor chip has a length, wherein the leads extend along the length of the semiconductor chip, and wherein the leads do not extend beyond the length of the semiconductor chip, and
 wherein the semiconductor device comprises a memory device.

38. A method of packaging a semiconductor device, comprising the steps of:
 manufacturing a semiconductor chip;
 forming a plurality of leads, wherein the leads each have at least a first portion and a second portion, and attaching the leads to a support, wherein the support is attached to the leads at the second portion;
 attaching the plurality of leads to the semiconductor chip with an insulating adhesive, wherein the chip is attached at the first portion of the leads;
 electrically connecting the leads to the semiconductor chip;
 molding the semiconductor chip and the plurality of leads with a resin, wherein the support is attached to the second portion of the leads during the molding, wherein the second portion of the leads are not covered by the resin; and
 removing the support from the second portion of the leads, wherein the second portion of the leads is exposed to provide electrical connection points,
 wherein the semiconductor chip has a major surface on which are formed circuit elements, wherein the leads are attached to the major surface by the insulating adhesive.

39. A method of packaging a semiconductor device, comprising the steps of:
 manufacturing a semiconductor chip;
 forming a plurality of leads, wherein the leads each have at least a first portion and a second portion, and attaching the leads to a support, wherein the support is attached to the leads at the second portion;
 attaching the plurality of leads to the semiconductor chip with an insulating adhesive, wherein the chip is attached at the first portion of the leads;
 electrically connecting the leads to the semiconductor chip;
 molding the semiconductor chip and the plurality of leads with a resin, wherein the support is attached to the

second portion of the leads during the molding, wherein the second portion of the leads are not covered by the resin; and
 removing the support from the second portion of the leads, wherein the second portion of the leads is exposed to provide electrical connection points,
 wherein the semiconductor chip has a major surface on which are formed circuit elements, wherein the leads are attached to the major surface by the insulating adhesive, and
 wherein the leads are attached at a central portion of the major surface.

40. A method of packaging a semiconductor device, comprising the steps of:
 manufacturing a semiconductor chip;
 forming a plurality of leads, wherein the leads each have at least a first portion and a second portion, and attaching the leads to a support, wherein the support is attached to the leads at the second portion;
 attaching the plurality of leads to the semiconductor chip with an insulating adhesive, wherein the chip is attached at the first portion of the leads;
 electrically connecting the leads to the semiconductor chip;
 molding the semiconductor chip and the plurality of leads with a resin, wherein the support is attached to the second portion of the leads during the molding, wherein the second portion of the leads are not covered by the resin; and
 removing the support from the second portion of the leads, wherein the second portion of the leads is exposed to provide electrical connection points,
 wherein the semiconductor chip has a major surface on which are formed circuit elements, wherein the leads are attached to the major surface by the insulating adhesive, and
 wherein the insulating adhesive comprises an insulating film.

41. A method of packaging a semiconductor device, comprising the steps of:
 manufacturing a semiconductor chip;
 forming a plurality of leads, wherein the leads each have at least a first portion and a second portion, and attaching the leads to a support, wherein the support is attached to the leads at the second portion;
 attaching the plurality of leads to the semiconductor chip with an insulating adhesive, wherein the chip is attached at the first portion of the leads;
 electrically connecting the leads to the semiconductor chip;
 molding the semiconductor chip and the plurality of lead with a resin, wherein the support is attached to the second portion of the leads during the molding, wherein the second portion of the leads are not covered by the resin; and
 removing the support from the second portion of the leads, wherein the second portion of the leads is exposed to provide electrical connection points,
 wherein the semiconductor chip has a major surface on which are formed circuit elements, wherein the leads are attached to the major surface by the insulating adhesive, and
 wherein the insulating adhesive comprises an insulating paste.

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42. A method of packaging a semiconductor device, comprising the steps of:

manufacturing a semiconductor chip;

forming a plurality of leads, wherein the leads each have at least a first portion and a second portion, and attached the leads to a support, wherein the support is attaching to the leads at the second portion;

attaching the plurality of leads to the semiconductor chip with an insulating adhesive, wherein the chip is attached at the first portion of the leads;

electrically connecting the leads to the semiconductor chip;

molding the semiconductor chip and the plurality of leads with a resin, wherein the support is attached to the second portion of the leads during the molding, wherein the second portion of the leads are not covered by the resin; and

removing the support from the second portion of the leads, wherein the second portion of the leads is exposed to provide electrical connection points, wherein at least one of the leads comprises a power supply bus bar.

43. A method of packaging a semiconductor device, comprising the steps of:

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manufacturing a semiconductor chip;

forming a plurality of leads, wherein the leads each have at least a first portion and a second portion, and attaching the leads to a support, wherein the support is attached to the leads at the second portion;

attaching the plurality of leads to the semiconductor chip with an insulating adhesive, wherein the chip is attached at the first portion of the leads;

electrically connecting the leads to the semiconductor chip;

molding the semiconductor chip and the plurality of leads with a resin, wherein the support is attached to the second portion of the leads during the molding, wherein the second portion of the leads are not covered by the resin; and

removing the support from the second portion of the leads, wherein the second portion of the leads is exposed to provide electrical connection points, wherein at least one of the leads comprises a power supply bus bar; and

wherein the power supply bus bar is attached to a central portion of the semiconductor chip.

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