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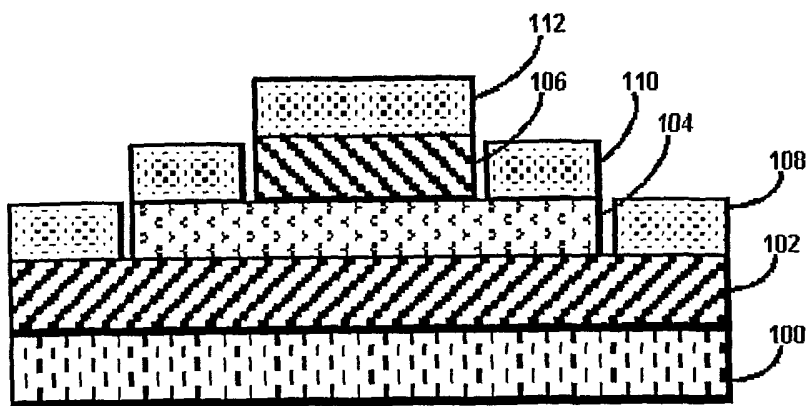
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(54) Title: TRANSISTOR WITH INTENTIONALLY TENSILE MISMATCHED BASE LAYER



(57) **Abstract:** A transistor having a substrate formed of indium phosphide (InP), and having emitter, base and collector layers formed over the substrate such that the base layer is disposed between the emitter and collector layers. The collector layer formed from InGaAs, and the collector layer being doped n-type. The emitter layer formed from InP, and the emitter layer being doped n-type. The base layer formed of indium gallium arsenide (InGaAs), the base layer being tensile mismatched, and doped p-type. A lattice mismatch between the substrate and the base material is greater than 0.2%. In an x-ray rocking curve of the heterojunction bipolar transistor, a peak corresponding to the base layer is separated from a peak corresponding to the substrate layer by at least 250 arcseconds. In one embodiment this results from the percentage of indium in the base layer is less than 51.5%, that is the lattice constant of the base layer is substantially smaller than a lattice constant of the substrate throughout an entire base region.



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TRANSISTOR WITH INTENTIONALLY TENSILE MISMATCHED BASE LAYER

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CROSS REFERENCE TO RELATED APPLICATION

This application is based on, and claims the benefit of, co-pending U.S. Application
10 Serial No. 09/883,582, filed on June 18, 2001, entitled "Transistor with Intentionally Tensile
Mismatched Base Layer," and incorporated herein by reference.

FIELD OF THE INVENTION

The present invention relates in general to high-speed electronic transistor devices, and
more specifically to InP/InGaAs Heterojunction Bipolar Transistors (HBT).

DESCRIPTION OF THE RELATED ART

15 The emitter injection efficiency of a bipolar transistor is limited by the fact that carriers
can flow from the base into the emitter region, over the emitter junction barrier, when the
junction is under forward bias. Such transistors use a lightly doped material for the base region
and a heavily doped material for the emitter. The requirement of a lightly doped material for the
20 base region results in undesirably high base resistances and a thick base region. It is known that
for high frequency applications it is desirable to have a thin, heavily doped base and a lightly
doped emitter. One solution is the heterojunction bipolar transistor. In these transistors the
emitter injection efficiency can be increased without strict requirements on doping. Materials
commonly used in heterojunction bipolar transistors include the aluminum gallium arsenide /
25 gallium arsenide (AlGaAs/GaAs) system because of the wide range of lattice matched
compositions. It is also known to use a system where indium gallium arsenide phosphide
(InGaAsP) is grown on indium phosphide (InP).

Lattice matching is well known in the art and refers to matching of the lattice structure and lattice constant for two materials, for example gallium arsenide and aluminum arsenide. Special consideration must be taken when depositing a material that has a lattice constant that is significantly different than the material on which it is being deposited. In the prior art, it is known that a thin layer is in compression or tension along the surface plane as its lattice constant adapts to the seed crystal. When this layer is grown very thick however, the layer eventually cannot maintain the compression or tension strain and it will relieve the strain by relaxing. It relaxes to its natural lattice constant. This is the difference between a relaxed layer and a strained layer. The thickness at which a layer begins to relax is referred to as the critical thickness and it depends on the difference in the lattice parameter of the two materials. For indium gallium arsenide on indium phosphide there is only one composition of indium gallium arsenide that is exactly lattice matched. Since it is very difficult to get the exact match during crystal growth, it is considered in the prior art that if the perpendicular mismatch is less than 0.2%, then the layers are considered to be lattice matched.

In the prior art gallium arsenide grown on aluminum arsenide provided a large change in the band gap between the materials with little change in the lattice constant. Because they have similar lattice constants, they are thus easily grown. The system allows for band gap engineering without a designer being constrained by excessive strain or lattice relaxation since the mismatch was just less than 0.2%.

These materials such as described above allow for band gap engineering, which results in various types of desirable devices. In prior art typical heterojunction bipolar transistors are nominally lattice matched to the substrate lattice constant to avoid defects, stress and relaxation of the base material. These effects are harmful to the performance of heterojunction bipolar transistors and limit band gap engineering. Band gap engineering is used to design devices for different optical effects and electronic effects. The heterojunction bipolar transistor may be formed using MOVCD. MOVCD stands for Metal Organic Chemical Vapor Deposition, a materials science technology used for growing compound semiconductor-based epitaxial wafers and devices. MOVCD technology is also known as OMVPE (Organo-Metal Vapor Phase Epitaxy) and MOVPE (Metal Organic Vapor Phase Epitaxy). Various epitaxial growth techniques are known in the prior art and include LPE (Liquid Phase Epitaxy) VPE (Vapor Phase Epitaxy) and MBE (Molecular Beam Epitaxy). MOVCD is a dominant growth

technique behind the major devices and a popular choice of manufacturers involved in high volume production of epitaxial wafers and devices.

It is a drawback of the prior art that the lattice mismatch is to be kept less than 0.2% and thus there is a need in the prior art for a system for band gap engineering, which provides for devices having greater than 0.2% lattice mismatch.

SUMMARY OF THE INVENTION

In general terms the present invention is a heterojunction bipolar transistor (HBT) having a substrate formed of indium phosphide (InP) and having emitter, base and collector layers formed over the substrate such that the base layer is disposed between the emitter and collector layers. In one embodiment, the collector layer is formed from InGaAs, and the collector layer being doped n-type. The emitter is layer formed from InP, and the emitter layer being doped n-type. The base layer is formed of InGaAs, the base layer being intentionally mismatched, and doped p-type. A lattice mismatch between the substrate and the base material is greater than 0.2%. In an x-ray rocking curve of the heterojunction bipolar transistor, a peak corresponding to the base layer being separated from a peak corresponding to the substrate layer by at least 250 arcseconds. In one embodiment this results from a percentage of indium in the base layer being less than 51.5%, that is a lattice constant of the base layer is substantially smaller than a lattice constant of the substrate throughout an entire base region of the base layer. More specifically, the base layer is intentionally lattice mismatched so that the lattice constant of the base is substantially smaller than that of the substrate material. From an x-ray rocking curve of an InP/InGaAs heterojunction bipolar transistor with an intentionally mismatched base layer, the base layer peak displays a splitting of 1,248 arcseconds from the substrate peak. Assuming the layer is fully strained, this splitting corresponds to a perpendicular lattice mismatch of 9,695 ppm (0.9695%), a perpendicular lattice constant of 5.8110 angstroms and a composition of $\text{In}_{0.461}\text{Ga}_{0.539}\text{As}$. The lattice constant of the InP substrate is 5.8688 ang. This composition results in base layer having a larger band gap than a base layer composed of the lattice matched composition ($\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$). The larger band gap will decrease the size of heterojunction discontinuity, ΔE_g , of the emitter-base junction and introduce a heterojunction at the base-collector junction. These changes impact device operation.

BRIEF DESCRIPTION OF THE DRAWINGS

The features of the present invention which are believed to be novel, are set forth with particularity in the appended claims. The invention, together with further objects and advantages, may best be understood by reference to the following description taken in conjunction with the accompanying drawings, in the several Figures of which like reference numerals identify like elements, and in which:

Figure 1 is a cross sectional view of a heterojunction bipolar transistor according to the present invention.

Figure 2 is an energy band diagram for a prior art heterojunction bipolar transistor.

Figure 3 is an energy band diagram for a heterojunction bipolar transistor according to the present invention.

Figure 4 is an X-ray rocking curve of the figure 3 heterojunction bipolar transistor of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Figure 1 is a cross-sectional view of a heterojunction bipolar transistor constructed according to the present invention. As depicted in figure 1 a substrate 100 (such as formed of InP) has a collector 102 on a first surface thereof. On the collector 102 is a base 104, and on the base 104 is an emitter 106. Each of the collector 102, the base 104 and the emitter 106 has respective metallic contacts 108, 110 and 112. Although the collector layer 102 is shown in figure 1 as being disposed between the base layer 104 and the substrate 100, it is within the scope of the present invention to reverse the positions of the collector 102 and the emitter 106. The heterojunction bipolar transistor depicted in figure 1 may be fabricated using conventional technology as is known in the art.

The substrate 100, the collector layer 102, the base layer 104 and the emitter layer 106 have the following thicknesses in one embodiment of the present invention:

Substrate layer 100 is in the range of 200 nm to 1000 nm;

Collector layer 102 is in the range of 100 nm to 50000 nm;

Base layer 104 is in the range of 10 nm to 200 nm; and

Emitter layer 106 is in the range of 20 nm to 200 nm.

In an embodiment of the present invention, a percentage of indium in the base layer is less than 51.5%.

Figure 2 depicts a typical prior art heterojunction bipolar transistor in terms of an energy band diagram. The energy band diagram is for a standard InP/InGaAs heterojunction bipolar transistor. For an InP emitter layer the ΔE_c is around 240 mV and the ΔE_v is around 330 mV. For an InAlAs emitter layer the ΔE_c is around 460 mV and the ΔE_v is around 200 mV. The ΔE_c is the conductive band continuity, and the ΔE_v is the valance band conductivity, and ΔE_c and ΔE_v are referenced to the equilibrium fermi level E_f .

Figure 3 is an energy band diagram of an intentionally lattice mismatched base heterojunction bipolar transistor according to the present invention. The band gap of the base layer decreases while the ΔE_c at the emitter base junction gets larger compared with the standard lattice matched structure of figure 2. A type II interface can form at the base-collector junction as the base composition approaches $\text{In}_{0.3}\text{Ga}_{0.7}\text{As}$. The size of the heterojunction discontinuities as the emitter-base and collector-base junctions depends on the exact composition of the base layer.

The novelty of the use of highly mismatched material as the base layer of an HBT is due to the underlying assumption that strain, strain relaxation and defects would result in degraded device performance such as current gain due to enhanced intrinsic base recombination current. However, the current gain does not show signs of degradation when the base layer is significantly mismatched from the rest of the device layers. This allows more flexibility in designing the bandgap of the base layer as depicted in Figures 2 and 3.

Figure 4 is an X-ray rocking curve of the InP/InGaAs heterojunction bipolar transistor. The base layer displays a splitting of 1,248 arcseconds from substrate peak. The measurement was taken of the (004) symmetric reflection using the double crystal x-ray diffraction technique and the $\text{Cu K}\alpha$ x-ray emission. The splitting corresponds to a perpendicular lattice mismatch of 9,695 ppm (perpendicular lattice constant of 5.8119 ang. The lattice constant of the InP substrate is 5.8688 ang. The rest of the layers (collector and emitter) are lattice matched to the substrate and cannot be easily differentiated from the substrate in this measurement.

An important feature of the present invention is that band gap is modifiable with regards to the base material and the emitter-base and base-collector junction characteristics. Tensile mismatched base material has important advantages in this device. A smaller conduction band discontinuity at the emitter base junction will decrease the offset voltage of the device, which is important for high efficiency devices. The residual strain in the base can cause the light and heavy hole bands in the valence band to split, improving charge carrier characteristics. The discontinuity at the collector-base junction serves as a "launching pad" for electrons as they enter the collector, resulting in shorter collector transit time. lifetime. Ultimately, the ability to use highly mismatched compositions in the base gives the designer greater flexibility in engineering the physical properties and characteristics of the heterojunction bipolar transistor.

The invention is not limited to the particular details of the apparatus depicted and other modifications and applications are contemplated. Certain other changes may be made in the above described apparatus without departing from the true spirit and scope of the invention herein involved. Also encompassed by the present invention are InAlAs/InGaAs heterojunction bipolar transistors in which the InP emitter layer is replaced with InAlAs or InAlGaAs. Double heterojunction devices in which the InGaAs collector material is completely or partially replaced with a wider bandgap material like InP, InGaAsP, InAlAs or InAlGaAs are also contemplated. Different base materials such as GaAsSb are also contemplated by the present invention. It is intended, therefore, that the subject matter in the above depiction shall be interpreted as illustrative and not in a limiting sense.

CLAIMS

I Claim:

1. A transistor comprising:

- 5 a substrate formed of indium phosphide (InP);
- emitter, base and collector layers formed over the substrate such that the base layer is disposed between the emitter and collector layers;
- the collector layer formed from InGaAs, and the collector layer being doped n-type;
- the emitter layer formed from InP, and the emitter layer being doped n-type;
- 10 the base layer formed of indium gallium arsenide (InGaAs), the base layer being tensile mismatched, and the base layer being doped p-type; and
- a lattice mismatch between the substrate and the base material being greater than 0.2%.
- 15 2. The transistor according to Claim 1, wherein the transistor is a heterojunction bipolar transistor (HBT).
3. The transistor according to Claim 2, wherein the HBT is npn-type.
4. The transistor according to Claim 1, wherein the substrate is semi-insulating.
5. The transistor according to Claim 1, wherein the collector layer is disposed between the substrate and the base layer.
- 20 6. The transistor according to Claim 1, wherein the base layer is doped with carbon.
7. The transistor according to Claim 1, wherein in an x-ray rocking curve of the transistor, a peak corresponding to the base layer being separated from a peak corresponding to the substrate layer by at least 250 arcseconds.
8. The transistor according to Claim 1, wherein a percentage of indium in the base layer is less than 51.5%.
- 25

9. The transistor according to Claim 1, wherein a lattice constant of the base layer is substantially smaller than a lattice constant of the substrate throughout an entire base region of the base layer.

10. A transistor comprising:

5 a substrate formed of indium phosphide (InP);

emitter, base and collector layers formed over the substrate such that the base layer is disposed between the emitter and collector layers;

the collector layer formed from InGaAs, and the collector layer being doped n-type;

the emitter layer formed from InP, and the emitter layer being doped n-type;

10 the base layer formed of indium gallium arsenide (InGaAs), the base layer being tensile mismatched, and the base layer being doped p-type; and

in an x-ray rocking curve of the transistor, a peak corresponding to the base layer being separated from a peak corresponding to the substrate layer by at least 250 arcseconds.

15 11. The transistor according to Claim 10, wherein the transistor is a heterojunction bipolar transistor (HBT).

12. The transistor according to Claim 10, wherein the substrate is semi-insulating.

13. The transistor according to Claim 10, wherein the collector layer is disposed between the substrate and the base layer.

20 14. The transistor according to Claim 10, wherein the base layer is doped with carbon.

15. The transistor according to Claim 10, wherein a percentage of indium in the base layer is less than 51.5%.

25 16. The transistor according to Claim 10, wherein a lattice constant of the base layer is substantially smaller than a lattice constant of the substrate throughout an entire base region of the base layer.

17. A transistor comprising:

a substrate formed of indium phosphide (InP);

emitter, base and collector layers formed over the substrate such that the base layer is disposed between the emitter and collector layers;

5 the collector layer formed from InGaAs, and the collector layer being doped n-type;

the emitter layer formed from InP, and the emitter layer being doped n-type;

the base layer formed of indium gallium arsenide (InGaAs), the base layer being tensile mismatched, and the base layer being doped p-type; and

the percentage of indium in the base layer being less than 51.5%.

10 18. The transistor according to Claim 17, wherein the transistor is a heterojunction bipolar transistor (HBT).

19. The transistor according to Claim 17, wherein the substrate is semi-insulating.

20. The transistor according to Claim 17, wherein the collector layer is disposed between the substrate and the base layer.

15 21. The transistor according to Claim 17, wherein the base layer is doped with carbon.

22. The transistor according to Claim 17, wherein in an x-ray rocking curve of the transistor, a peak corresponding to the base layer being separated from a peak corresponding to the substrate layer by at least 250 arcseconds.

20 23. The transistor according to Claim 17, wherein a lattice constant of the base layer is substantially smaller than a lattice constant of the substrate throughout an entire base region of the base layer.

24. A transistor comprising:

a substrate formed of indium phosphide (InP);

25 emitter, base and collector layers formed over the substrate such that the base layer is disposed between the emitter and collector layers;

the collector layer formed from InGaAs, and the collector layer being doped n-type;

the emitter layer formed from InP, and the emitter layer being doped n-type;

the base layer formed of indium gallium arsenide (InGaAs), the base layer being tensile mismatched, and the base layer being doped p-type; and

5 a lattice constant of the base layer being substantially smaller than a lattice constant of the substrate throughout an entire base region of the base layer.

25. The transistor according to Claim 24, wherein the transistor is a heterojunction bipolar transistor (HBT).

26. The transistor according to Claim 24, wherein the substrate is semi-insulating.

10 27. The transistor according to Claim 24, wherein the collector layer is disposed between the substrate and the base layer.

28. The transistor according to Claim 24, wherein the base layer is doped with carbon.

15 29. The transistor according to Claim 24, wherein in an x-ray rocking curve of the transistor, a peak corresponding to the base layer being separated from a peak corresponding to the substrate layer by at least 250 arcseconds.

30. The transistor according to Claim 24, wherein a percentage of indium in the base layer is less than 51.5%.

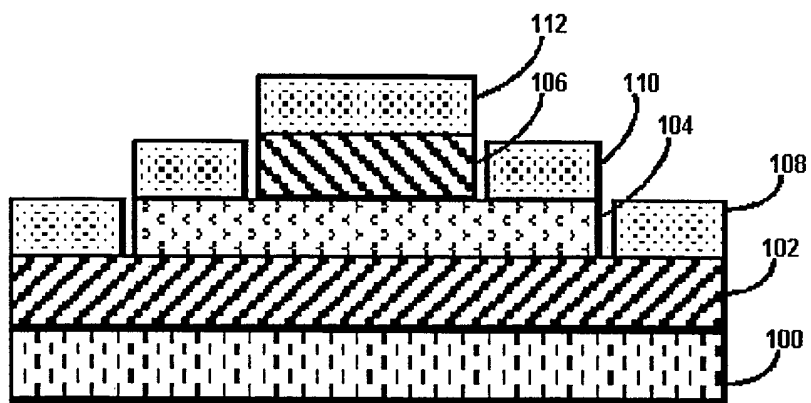


FIG. 1

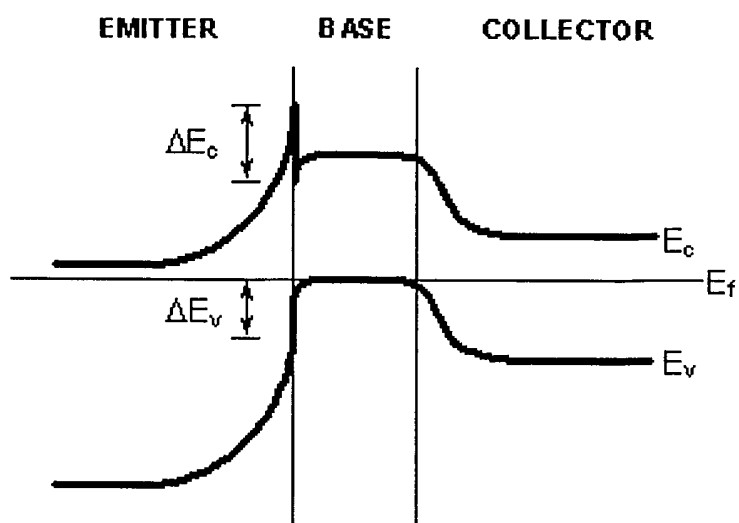


FIG. 2

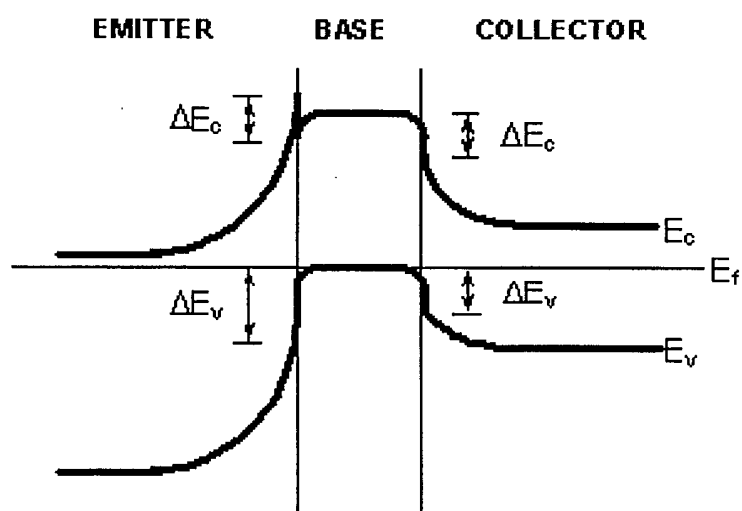


FIG. 3

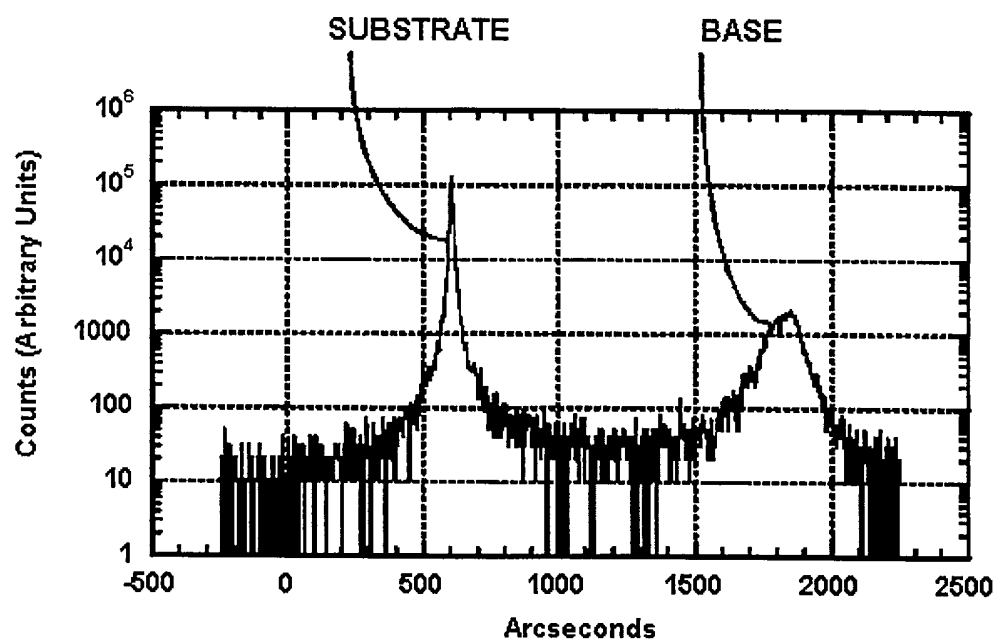


FIG. 4