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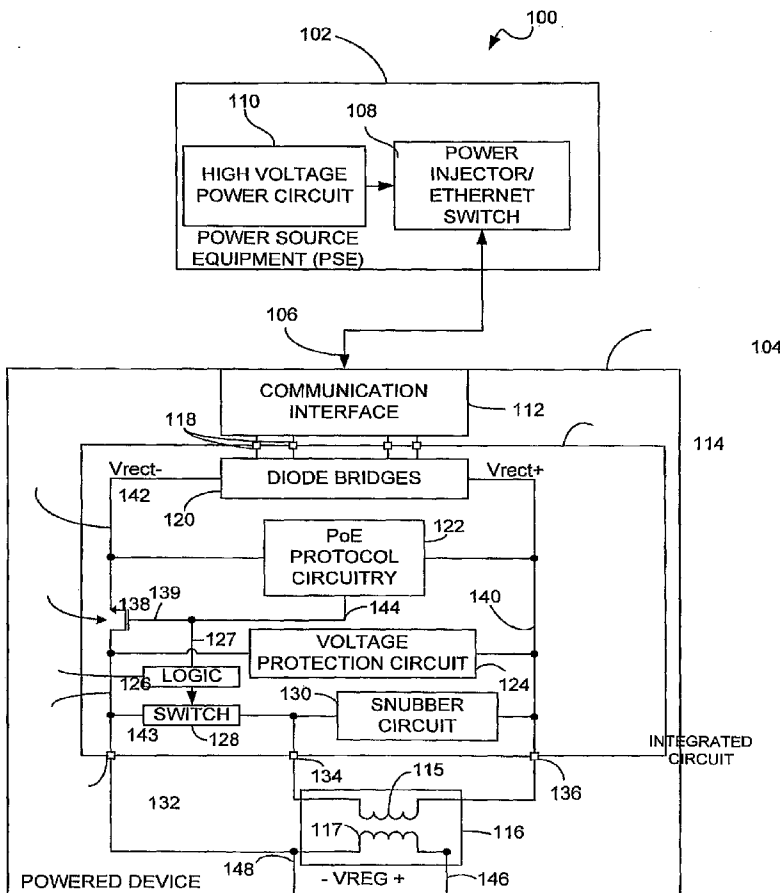
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(54) Title: SYSTEM AND METHOD FOR VOLTAGE PROTECTION IN A POWERED DEVICE

(57) Abstract: A powered device includes a voltage protection circuit, two outputs, a switch, and a snubber circuit. The two outputs of the integrated circuit may be coupled to an external transformer. The snubber circuit of the integrated circuit is responsive to the switch and is coupled with respect to the two outputs to direct energy from at least one of the two outputs to the voltage protection circuit.



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ABSTRACT OF THE DISCLOSURE

A powered device includes a voltage protection circuit, two outputs, a switch, and a snubber circuit. The two outputs of the integrated circuit may be coupled to an external transformer. The snubber circuit of the integrated circuit is responsive to the switch and is coupled with respect to the two
5 outputs to direct energy from at least one of the two outputs to the voltage protection circuit.

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SYSTEM AND METHOD FOR VOLTAGE PROTECTION IN A POWERED DEVICE**FIELD OF THE DISCLOSURE**

The present disclosure relates generally to systems and methods of protecting integrated circuit components against power events, such as inductive voltage and electrostatic discharge (ESD) events.

5 BACKGROUND

In general, power over Ethernet (PoE) refers to a technique that is outlined in the IEEE Std 802.3™-2005 clause 33 (the PoE standard) for delivering power via Ethernet cabling to a powered device, which is an electronic device adapted to derive power from the Ethernet cabling. PoE eliminates the need for a separate power source for powered devices. Powered devices may include voice over
10 Internet protocol (VoIP) telephones, wireless routers, security devices, field devices to monitor process control parameters, data processors, other devices, or any combination thereof.

In general, power sourcing equipment delivers power to one or more powered devices via a twisted pair network cable, such as an Ethernet cable. The PoE standard specifies that the power sourcing equipment should provide a power supply voltage having a range of 36 to 57 volts direct current (DC)
15 and having a current that is limited to less than 400mA. The use of extended cable lengths and transformers in some applications may induce transient voltage and current surges far in excess of 57 volts and 400mA.

Conventionally, to manage such transients and other power events, many powered devices include a high voltage transient suppressor, which may protect circuitry of the powered device from high
20 voltages by clamping the input voltage at or below a breakdown voltage threshold during a power surge event. A typical high voltage transient suppressor may be a high voltage zener diode, such as the SMAJ58A surface mount diode, which is commercially available from a wide variety of circuit component manufacturers. The high voltage zener diode is typically connected in parallel with a diode bridge between the positive and negative voltage supply terminals to clamp transient voltages in excess
25 of a threshold to protect associated circuitry. For example, a typical zener diode is a 58-volt zener diode, which is designed to breakdown and conduct current at voltages in excess of 58 volts.

The PoE standard specifies that powered devices are required to survive transient events up to a 1000 volt power surge and to a transient current of 5A. A transient surge with a duration of 300 nanoseconds to 50 microseconds dissipates considerably more energy than typical zener diodes are rated to
30 withstand. If the high voltage transient suppressor is a diode stack including a plurality of zener diodes arranged in series, the duration of the transient power surge may cause the zener diodes to undergo self-heating. Additionally, typical zener diodes exhibit significant voltage overshoot during high-current events. This overshoot may damage other circuit elements of the powered device.

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In an integrated circuit having a flyback switching regulator topology, an external transformer is coupled to the integrated circuit to provide a direct-current-to-direct-current (DC-to-DC) isolated power supply to attached circuitry. Typically, a primary winding of the transformer may be coupled to a transistor that is controlled by an output pin of the integrated circuit to activate the external
5 transformer. The transformer may produce an inductive voltage, sometimes referred to as an inductive voltage kick, when the transistor is shut off, for example. The inductive voltage kick is generated due to the change in current of the inductive winding of the transformer, since the inductive winding tends to oppose current change. The inductive winding of the transformer continues to drive current, even when the voltage supply to the inductive winding is removed. The inductive voltage kick may cause
10 the voltage level to exceed a voltage rating of the transistor.

Generally, an integrated circuit device may include components to prevent such an inductive voltage kick from exceeding a safe voltage level for the transistor. For example, a snubber circuit may be utilized to provide a level of voltage protection for the transistor. A typical snubber circuit is
15 implemented using external, discrete circuit components. However, if the snubber circuit is external to the integrated circuit device, the connection pins that couple the snubber circuit to the integrated circuit device may expose the integrated circuit device to electrostatic discharge (ESD) events during manufacture, assembly, and handling. Adding ESD protection components may add additional costs and complexity.

Therefore, there is a need for an integrated circuit device that has enhanced protection against power
20 events, such as ESD and inductive voltage events.

SUMMARY

In a particular illustrative embodiment, a powered device is provided that includes a voltage protection circuit, two pins, a switch, and a snubber circuit. The two pins include a first pin and a second pin that are responsive to an external transformer. The snubber circuit is part of an integrated circuit and is
25 responsive to the switch. The snubber circuit is coupled with respect to the two pins to direct energy from at least one of the two pins to the voltage protection circuit. In one embodiment, the energy results from an inductive voltage kick from the external transformer. In another embodiment, the energy results from an electrostatic discharge (ESD) event.

In another particular illustrative embodiment, the powered device includes first and second input pins
30 responsive to an external power source and first and second output pins responsive to an external transformer. The first output pin may be coupled to the first input pin. The powered device also includes a third output pin coupled to the second input pin, and a voltage protection circuit to limit an input voltage. When a voltage on the second output pin exceeds a threshold, energy applied to the second output pin is directed to the voltage protection circuit. When a voltage on the second output pin
35 is at or below the threshold, energy applied to the second output pin may be directed to the third output pin.

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In yet another particular illustrative embodiment, a method is provided that includes detecting a power event at a snubber circuit of an integrated circuit. The snubber circuit may be coupled to a voltage protection circuit and may be responsive to an external transformer that is selectively connected to a negative supply terminal of the integrated circuit via a switch. The method also includes directing energy resulting from the power event to the voltage protection circuit via the snubber circuit when a voltage level associated with the power event exceeds a threshold.

In still another particular embodiment, an integrated circuit includes a transistor, an interface, and a snubber circuit. The transistor includes a first terminal, a second terminal coupled to a first power supply terminal, and a control terminal. The interface is coupled to the first terminal and is responsive to an external transformer to selectively activate the external transformer. The snubber circuit is responsive to the interface to direct an inductive voltage that exceeds a threshold to a voltage protection circuit to protect the transistor.

In another particular illustrative embodiment, a powered device includes a first supply terminal, a second supply terminal, and at least one input pin coupled to the first supply terminal. The powered device further includes an external capacitor having a first terminal coupled to the first supply terminal, a switch coupled to the second supply terminal and coupled to a second terminal of the external capacitor, and power surge detection logic coupled to the switch. The external capacitor is charged in response to a detected power surge that exceeds a threshold.

In yet another particular illustrative embodiment, a method is provided that includes detecting a power surge event at a first power supply terminal of an integrated circuit. The method further includes activating a surge protection circuit to shunt the power supply terminal to a second power supply terminal of the integrated circuit while concurrently activating a switch within the integrated circuit in response to detecting the power surge event to enable an external capacitor to receive energy associated with the power surge event.

In still another particular illustrative embodiment, a powered device includes at least one input responsive to an external power supply and a diode bridge responsive to the at least one input to provide a rectified power supply to a pair of supply terminals, including a first supply terminal and a second supply terminal. The powered device further includes a detector responsive to the first supply terminal and the second supply terminal to detect a surge event in excess of a threshold. The powered device includes an external capacitor including a first terminal coupled to the first supply terminal and including a second terminal, and a switch to selectively couple the second terminal of the external capacitor to the second supply terminal. Additionally, the powered device includes logic to selectively activate the switch in response to detection of the surge event to deliver energy resulting from the surge event to the external capacitor.

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BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a general diagram of a particular illustrative embodiment of a Power over Ethernet (PoE) system;

5 FIG. 2 is a block diagram illustrating a particular embodiment of an integrated circuit coupled to an external direct current to direct current (DC-to-DC) converter, which may be utilized in a powered device, such as that shown in FIG. 1;

FIG. 3 is schematic circuit diagram of an illustrative portion of a particular embodiment of a system that includes protection for inductive voltage kicks and for ESD events;

10 FIG. 4 is a flow diagram of a particular illustrative embodiment of a method of protecting a switching transistor against over voltage conditions.

FIG. 5 is a general diagram of an embodiment of a Power over Ethernet enabled system with enhanced surge protection;

FIG. 6 is a partial block and partial circuit diagram illustrating a particular embodiment of a powered device integrated circuit with enhanced surge protection;

15 FIG. 7 is a partial block and partial circuit diagram illustrating a particular embodiment of a powered device integrated circuit, such as that shown in FIG. 5, with enhanced surge protection;

FIG. 8 is a block diagram illustrating a particular embodiment of a system, such as the systems shown in FIG. 5 or 6, to provide enhanced surge protection; and

20 FIG. 9 is a flow diagram of a particular embodiment of a method of providing enhanced surge protection.

The use of the same reference symbols in different drawings indicates similar or identical items.

DETAILED DESCRIPTION OF THE DRAWINGS

FIG. 1 is a general diagram of a particular illustrative embodiment of a power over Ethernet system 100. The system 100 includes power sourcing equipment (PSE) 102 coupled to a powered device 104 via an Ethernet connection 106. The Ethernet connection 106 may be a twisted pair cable, such as a CAT5 twisted pair cable, a coaxial cable, and the like. The PSE 102 includes a high-voltage power circuit 110 and a power injector/Ethernet switch 108. The power injector/Ethernet switch 108 receives a power supply from the high-voltage power circuit 110 and injects the power supply to selected Ethernet ports to provide power to the powered device 104 via the Ethernet cable 106. Generally, the PSE 102 provides both power and data over the same cable 106.

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The powered device 104 includes a communication interface 112, an integrated circuit 114, and a DC-to-DC converter 116. The integrated circuit 114 includes pins 118, diode bridges 120, Power over Ethernet (PoE) protocol circuitry 122, a voltage protection circuit 124, logic 126, a switch 128, and a snubber circuit 130. The integrated circuit 114 also includes output pins 132, 134, and 136. The
5 integrated circuit 114 may also include a transistor 138 and voltage supply terminals 140, 142, and 143. The DC-to-DC converter 116 may include a primary winding 115, and a secondary winding 117. The primary winding 115 is coupled to the output pin 136 and to the output pin 134. Current flow through the primary winding 115 creates a magnetic flux in a core of the transformer 116, which induces a voltage in the secondary winding 117 based on a mutual inductance between the windings 115 and 117.
10 The secondary winding 117 includes a first terminal 146 and a second terminal 148 to provide a regulated voltage (V_{reg}) to power an associated load. The second terminal 148 is coupled to the output pin 132.

The communication interface 112 is coupled to the Ethernet cable 106 to receive power and data from the PSE 102. The diode bridges 120 are coupled to the communication interface 112 via input pins
15 118. The diode bridges 120 are connected to voltage supply terminals 140 and 142 to deliver a rectified power supply to associated circuit elements. The diode bridges 120 may be responsive to the communication interface 112 to receive a power supply input from the PSE 102 and to provide a rectified power supply to the voltage supply terminals 140 and 142.

The power over Ethernet (PoE) protocol circuitry 122 is coupled between the voltage supply terminals
20 140 and 142 and provides PoE protocol functions, including controlling the powered device 104 to respond to the PSE 102 during a PoE detection process, for example. The voltage protection circuit 124, such as a surge protector, is coupled between the power supply terminals 140 and 142 to detect a power surge event and to shunt a voltage between the power supply terminals 140 and 142 when the voltage exceeds a threshold. The snubber circuit 130 is coupled to the power supply terminal 140 and
25 to output pin 134. The switch 128 is coupled to output pin 134 and to the power supply terminal 143.

The transistor 138 may include a control terminal 139 coupled to the power over Ethernet protocol circuitry 122 via line 144, a first terminal coupled to the voltage supply terminal 142, and a second terminal coupled to the voltage supply terminal 143. The switch 128 may be connected between the snubber circuit 130 and the voltage supply terminal 143. The switch 128 is also coupled to logic 126 to
30 receive a control signal. The logic 126 may be coupled to the PoE protocol circuitry 122, such as by line 127, to receive a control signal related to a connection status of the powered device 100. For example, the logic 126 may selectively activate the switch 128 when at least two inputs pins 118 of the integrated circuit 114 are coupled to an external power source, such as the PSE 102. In one particular embodiment, such as that shown in FIG. 2 below, the logic 126 may be included in the snubber circuit
35 130.

In general, the powered device 104 utilizes a flyback switching regulator topology, where the switch 128 may be used to activate the primary winding 115 of the DC-to-DC converter 116 to induce a voltage in the secondary winding 117. The switch 128 may include a transistor having a first terminal

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coupled to the primary winding 115 of the DC-to-DC converter 116 via the pin 134, a control terminal responsive to the logic 126, and a second terminal coupled to the voltage supply terminal 143. The switch 128 may selectively couple the pin 134 to the voltage supply terminal 143 to activate, for example, the primary winding 115 of the DC-to-DC converter 116.

- 5 In operation, during an overshoot condition, when the switch 128 is turned off, an inductive voltage kick may develop at the output pin 134 due to a leakage inductance from the primary winding 115 of the DC-to-DC converter 116. The snubber circuit 130 may direct energy resulting from a power event, such as the inductive voltage kick or an electrostatic discharge at the output pin 134, to the voltage protection circuit 124 via the voltage supply terminal 140. The voltage protection circuit 124 may be
10 an over-voltage protection circuit to shunt excess voltage between the voltage supply terminals 140 and 143 when the voltage differential between the voltage supply terminals 140 and 143 exceeds a threshold voltage.

In general, the snubber circuit 130 impedes current flow when a voltage level across the snubber circuit 130 is less than a threshold and directs energy to the voltage protection circuit 124 when the voltage
15 level across the snubber circuit 130 exceeds the threshold. The snubber circuit 130 directs energy resulting from inductive voltage kicks and ESD events from the external pins 134 and 136 to the voltage protection circuit 124, after an inductive voltage kick of the external DC-to-DC converter 116 (such as a transformer) or after an electrostatic discharge (ESD) event. By directing energy resulting from both inductive voltage kicks and ESD events, the snubber circuit 130 enables utilization of a
20 single voltage protection circuit 124 to protect the integrated circuit 114 from multiple types of power events, thereby lowering the overall cost of providing power surge protection.

In general, the snubber circuit 130 may be designed to selectively block current flow during normal operation (during a first mode of operation) and to direct current flow when the voltage across the snubber circuit 130 exceeds a threshold (during a second mode of operation). In one particular
25 embodiment, the snubber circuit 130 is designed to divert or direct energy away from the switch 128 such that a sum of an input voltage supply (across voltage supply terminals 140 and 142 during normal operation) and the voltage across the snubber circuit 130 (between the voltage supply terminal 140 and the output pin 134) is less than a safe operating voltage rating of the switch 128.

In one particular illustrative embodiment, the snubber circuit 130 prevents a voltage across the switch
30 128 (for example, measured between the output pins 134 and 132) from exceeding a voltage rating of the switch 128. Generally, the voltage rating of the switch 128 may be defined by a manufacturer of the switch 128 based on a voltage level at which the switch 128 may fail.

In still another particular embodiment, energy at the output pin 134 is received after an inductive kick of the DC-to-DC converter 116 (from the primary winding 115 of the transformer). In another
35 particular embodiment, energy at the output pin 134 is received after an electrostatic discharge (ESD) event.

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FIG. 2 illustrates a particular embodiment of a powered device 200, such as that shown in FIG. 1. The powered device 200 includes a communication interface 201, an integrated circuit 202 and a DC-to-DC converter 204. The integrated circuit 202 includes diode bridges 206, over-voltage protection 208, a detection and classification circuit 210, a hot swap switch and current limit circuit 212, a hot swap control and common bias circuit 214, switch control and snubber circuit 216, and a switching field effect transistor 218. Additionally, the integrated circuit 202 includes multiple pins. Input pins 220, 222, 224, and 226 are adapted to connect to a communication interface, such as communication interface 112 in FIG. 1. The integrated circuit 202 also includes internal power supply terminals 140, 142 and 143.

In a Power over Ethernet (PoE) environment, input pins 220 and 222 may be coupled to spare wire pairs of an Ethernet cable via the communication interface 201 to receive power from power sourcing equipment (PSE) coupled to the other end of the cable. Input pins 224 and 226 may be coupled to center taps of transformer windings 232 of the communication interface 201 to connect to twisted wire pairs of an Ethernet cable, such as the cable 106 in FIG. 1, that carry both power and data. Output pins 228 and 230 are coupled to the diode bridges 206 to provide a positive rectified voltage supply and a negative rectified voltage supply, respectively. The detection and classification circuit 210 may draw an appropriate detection current for the powered device 200 during a detection phase of operation and an appropriate current for classification of the powered device 200 during a classification phase. The hot swap control and common bias circuit 214 may provide a power loss indicator to associated circuitry, when a connection to the PSE is lost.

The hot swap switch and current limit circuit 212 may provide a hot swap output indicator, such as when the powered device 200 is connected to or disconnected from an Ethernet cable via the communication interface 201, for example. The pin 240 may be coupled to the switch control and snubber circuit 216 and to the external DC-to-DC converter 204. The pin 242 may be coupled to the switching field effect transistor (FET) 218 to provide a voltage supply output to a secondary winding of the DC-to-DC converter 204. The pin 246 is coupled to the switch control and snubber circuit 216, to a primary winding of the DC-to-DC converter 204, and to the switching FET 218 via line 248.

In operation, when the switching FET 218 is deactivated, an inductive voltage kick may be applied to the pin 246 by the DC-to-DC converter 204 due to inductive current leakage of the primary winding of the DC-to-DC converter 204. The switch control and snubber circuit 216 directs energy resulting from the inductive voltage kick from pin 246 to the over voltage protection circuit 208 via the voltage supply terminal 140. Additionally, during non-operating conditions, such as during transport or during manufacture, if an electrostatic discharge (ESD) event is received at the pin 246, the switch control and snubber circuit 216 directs ESD energy resulting from the ESD event away from the switching field effect transistor 218 to the over-voltage protection circuit 208 via the voltage supply terminal 140.

In general, the switch control and snubber circuit 216 serves a dual purpose as both an inductive voltage kick (inductive voltage flyback) protector and an ESD protector. By directing energy resulting from an inductive voltage or an ESD event away from the switching field effect transistor 218, the

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switch control and snubber circuit 216 allows a single bulk over voltage protection circuit, such as the over voltage protection circuit 208, to be utilized to protect against over voltage events, against ESD events, and against inductive voltage events. By using a single protection circuit 208, costs associated with the integrated circuit 202 of the powered device 200 may be reduced, while still providing voltage protection.

FIG. 3 is schematic circuit diagram of an illustrative portion of a particular embodiment of a system 300 that includes protection for inductive voltage kicks and for ESD events. The system 300 includes an integrated circuit portion 302, which includes a voltage supply terminal 310, a voltage supply terminal 312, a voltage protection circuit 314, a snubber circuit 316, a transistor 318, and logic 320.

The snubber circuit 316 includes a diode 322 and a breakdown diode 324. The integrated circuit portion 302 also includes pins 306, 308, and 332, which may be coupled to external circuitry 304, such as circuitry that may be used to implement the DC-to-DC converter 204 of FIG. 2. The voltage supply terminal 310 is connected to the pin 306. The voltage supply terminal 312 is connected to the pin 332. The voltage protection circuit 314 is coupled between the voltage supply terminals 310 and 312. The snubber circuit 316 is coupled between the voltage supply terminal 310 and the pin 308. The transistor 318 includes a first terminal coupled to the pin 308, a control terminal coupled to the logic 320, and a second terminal coupled to the voltage supply terminal 312.

The external circuitry 304 includes a primary winding 326 coupled to pin 306 and to pin 308. The external circuitry 304 also includes a secondary winding 330 coupled to the voltage supply pin 332.

The secondary winding 330 is also coupled to an anode terminal of a diode 334. The cathode terminal of the diode 334 provides a voltage supply output on a positive supply terminal 335. The output pin 332 provides a voltage supply output on a negative supply terminal 333. A resistor 336 includes a first terminal coupled to positive supply terminal 335 and a second terminal coupled to a cathode of a diode 338, which includes an anode coupled to the negative supply terminal 333. A load 340 may be connected across the positive and negative supply terminals 335 and 333 to receive a DC voltage supply.

The voltage protection circuit 314 may include a zener breakdown diode or a diode stack including multiple diodes arranged in series, such that the cathode terminal is coupled to the voltage supply terminal 310 and the anode terminal is coupled to the voltage supply terminal 312. The snubber circuit 316, in a particular embodiment, may include a diode 322 and a breakdown diode 324. The diode 322 may include an anode terminal coupled to pin 308 and a cathode terminal. The breakdown diode 324 may include an anode terminal coupled to the voltage supply terminal 310 and a cathode terminal coupled to the cathode terminal of the diode 322. The breakdown diode 324 may include a zener diode, multiple zener diodes arranged in series, or another device adapted to switch on when a voltage across the device exceeds a threshold. The arrangement of the diode 322 and the breakdown diode 324 may be referred to as an anti-series arrangement. During normal operation, the diode 322 prevents or impedes current flow through the snubber circuit 316 from the voltage supply terminal 310 to the pin 308. In response to an ESD event or an inductive voltage kick from the external transformer 304, the

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breakdown diode 324 breaks down, allowing current to flow from the pin 308 to the voltage supply terminal 310.

During operation, the switch 318 couples the primary winding 326 of the external DC-to-DC converter 304 between the voltage supply terminals 310 and 312. When the logic 320 deactivates the transistor 318, the primary winding 326 may produce an inductive voltage kick received at the pin 308 due to leakage current within the primary winding 326, increasing a voltage level at pin 308. It should be understood that many low power devices operate using a negative power supply voltage, where the voltage supply terminal 310 may be at a voltage level that is approximately zero and where the voltage supply terminal 312 may be at a voltage level that is negative, for example.

When a voltage differential between the voltage supply terminal 310 and the pin 308 exceeds a threshold defined by the breakdown voltage of the diode 324, the snubber circuit 316 conducts current from the pin 308 to the voltage supply terminal 310. As the voltage level of the voltage supply terminal 310 increases, and when the differential voltage between the voltage supply terminals 310 and 312 exceeds a threshold voltage defined by the voltage protection circuit 314, the voltage protection circuit 314 breaks down to shunt the voltage between the positive and voltage supply terminals 310 and 312. Thus, the snubber circuit 316 may direct excess power or energy from the pin 308 to the voltage protection circuit 314. The snubber circuit 316 also operates to direct energy resulting from electrostatic discharge events from the pin 308 to the voltage protection circuit 314 during manufacture. Thus, the snubber circuit 316 directs energy away from the transistor 318 to the voltage protection circuit 314 when the voltage at pin 308 exceeds a threshold voltage level, to prevent the voltage at pin 308 from damaging the transistor 318 by exceeding its voltage rating.

In one particular embodiment, the zener diode 324 is a diode circuit including three diodes arranged in series, where each diode in the series has a breakdown characteristic of approximately 6.2 volts, which establishes a threshold breakdown voltage of approximately 18.6 volts. During normal operation, the diode 322 prevents current flow through the snubber circuit 316. During an overshoot condition, such as during an ESD event or when a flyback inductance voltage is received at pin 308, the snubber circuit 316 conducts current through diode 322 and the zener diode circuit 324 breaks down to conduct current to the voltage supply terminal 310. The snubber circuit 316 prevents the total voltage across the transistor 318 from exceeding a sum of the input voltage (between the voltage supply terminals 310 and 312) and a snubber voltage (across the snubber circuit 316, taken between the voltage supply terminal 310 and the pin 308).

In one particular illustrative embodiment, the integrated circuit 302 may include a transistor 318 that is operable as a switch. The transistor 318 includes a first terminal coupled to the pin 308, a second terminal coupled to a voltage supply terminal 312, and a control terminal coupled to the logic 320. The pin 308 is responsive to the external transformer 304 to selectively activate the external transformer 304. The snubber circuit 316 is responsive to the pin 308 to direct an inductive voltage that exceeds a threshold to a voltage protection circuit 314 to protect the transistor 318. In one particular embodiment, the snubber circuit 316 may be responsive to the pin 308 to direct an electrostatic

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discharge (ESD) event from the pin 308 to the voltage protection circuit 314 when the integrated circuit 302 is inactive.

In general, it should be understood that any of the pins 306, 308 and 332 may be exposed to an ESD event. If the ESD event is applied to either of the pins 306 or 332, the ESD event may be controlled by the voltage protection circuit 314, which shunts the surge between the voltage supply terminals 310 and 312. However, if the ESD event is applied to the pin 308, as shown, the snubber circuit 316 directs the energy away from the transistor 318 to the voltage protection circuit 314 via the voltage supply terminal 310. If the power event is an inductive voltage kick from the primary winding 326 of the transformer 304, the snubber circuit 316 directs the energy away from the transistor 318 via the same path. Thus, the snubber circuit 316 provides a dual use, which allows a single voltage protection circuit 314 to provide protection for both ESD and inductive voltage kick events.

When a voltage differential between the pin 306 and the pin 332 is approximately zero, the integrated circuit 302 may be below a lower threshold (such as a power on threshold). During this mode of operation, energy applied to the pin 308 may be directed away from the transistor 318 and to the voltage protection circuit 314, if the energy exceeds a threshold of the snubber circuit 316. During normal operations, such as when a voltage differential between the pins 306 and 332 is at a voltage level that is between the lower threshold and an input threshold (where the input threshold is defined by the voltage protection circuit 314), energy applied to the pin 308 may be directed to the pin 332 via the transistor 318.

In general, the integrated circuit 302 may be designed to include a voltage protection circuit that defines a first breakdown voltage and a snubber circuit 316 that defines a second breakdown voltage such that a sum of the first and second breakdown voltages is less than a voltage rating of the transistor 318. The manufacturer of the transistor 318 may define its voltage rating.

FIG. 4 is a flow diagram of a particular illustrative embodiment of a method of protecting a switching transistor against destructive overvoltage. A power event is received at a pin that is responsive to a snubber circuit, where the power event is either an electrostatic discharge (ESD) event or an inductive voltage kick event (block 400). An energy level at the pin is detected to determine if the detected energy level exceeds a threshold (block 402). If the energy level does not exceed the threshold at block 404, then the power event is monitored at the pin (block 406) and block 402 is repeated. If the energy level exceeds the threshold at block 404, the energy resulting from the power event is directed away from the transistor via the snubber circuit and to a voltage protection circuit (block 408). In a particular embodiment, the threshold is associated with a safe power level of the transistor, such as a safe voltage rating for the transistor.

In one particular illustrative embodiment, the power event may include an electrostatic discharge (ESD) event. In another particular illustrative embodiment, the power event may include an inductive voltage kick. In one embodiment, a voltage may be detected that is in excess of a breakdown voltage level of a breakdown diode circuit of the snubber circuit. Current may be conducted via the snubber

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circuit away from the switch and to the voltage protection circuit in response to detection of the power event. In yet another embodiment, the safe power level of the switch includes a voltage rating determined by a manufacturer of the switch.

In general, it should be understood that a power event may include an electrostatic discharge event, an inductive voltage kick from an external transformer, other similar events, or any combination thereof. Additionally, it should be understood that the snubber circuit, such as the snubber circuit 316 in FIG. 3, may be designed to include a zener breakdown diode with a breakdown voltage level, such that the sum of the input voltage and the voltage across the snubber does not exceed a voltage rating of the transistor.

In one particular embodiment, a powered device detects a power event by detecting a voltage in excess of a breakdown voltage level of the breakdown diode circuit and conducting current across the snubber circuit from the switch to the voltage protection circuit in response to detection of the power event.

It should be understood that the external power source may be power sourcing equipment of a power over Ethernet (PoE) system. Alternatively, the external power source may be a battery or other external power supply. By integrating the snubber circuit with the integrated circuitry, the snubber circuit may be utilized to provide protection to the switching transistor, to protect the switching transistor from ESD events and from flyback inductive voltage kick from, for example, an external transformer. Thus, the snubber circuit provides dual protection for the transistor without requiring additional dedicated ESD protection circuitry.

In addition to electrostatic discharge (ESD) events, Power over Ethernet systems may be exposed to power surges and other types of power events, which may have different electrical characteristics from an ESD event. For example, a power surge may have a lower peak voltage and a longer duration relative to an ESD event. In general, it may be desirable to utilize a different technique to manage excess current and voltages that are unrelated to ESD events. For example, a powered device, such the powered device 504 illustrated in FIG. 5, may include power surge protection circuitry and associated logic to safely divert excess power so that circuitry is not damaged by a power surge.

Referring to FIG. 5, a power over Ethernet system 500 is shown. The power over Ethernet system 500 includes power sourcing equipment (PSE) 502 and a powered device 504 coupled via a network connection 506, such as a twisted pair Ethernet cable, to the PSE 502. The PSE 502 includes a power injector/Ethernet switch 508 and a high voltage power circuit 510. The PSE 502 provides power and data communications over the network connection 506 to the powered device 504.

The powered device 504 includes a connection interface 512 coupled to the network connection 506 and includes an integrated circuit 514, and an input filter, such as the external capacitor 526. The integrated circuit 514 includes diode bridges 516, Power over Ethernet (PoE) protocol circuitry 522, a surge protector 524, and a DC-to-DC converter 528. In general, the integrated circuit 514 is formed from various functional elements and appropriate circuitry. The diode bridges 516 are coupled to the

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connection interface 512 via pins 513 to receive a power supply from the PSE 502 via the network connection 506. At least one input pin 513 is responsive to an external power supply, such as power provided via the network connection 506 from the PSE 502. The diode bridge 516 has an input that receives the power supply input from at least one input pin 513 of the connection interface 512. The diode bridge 516 is configured to couple the power supply input from the at least one input pin 513 to a first voltage supply terminal 518 and to a second voltage supply terminal 520 to provide a rectified power supply to the first and second supply terminals 518 and 520, which carry voltages identified as V_{RECT+} and V_{RECT-} .

In general, the positive voltage supply terminal 518 is coupled to the external capacitor 526 via a pin 542, and the negative voltage supply terminal 520 is coupled to the capacitor 526 via a switch 530 (such as a field effect transistor) and via a pin 544. The PoE protocol circuitry 522, the surge protector 524, and the DC-to-DC converter 528 are coupled between the positive and negative voltage supply terminals 518 and 520. The PoE protocol circuitry 522 includes a control output 536, which is coupled to a control terminal 538 of the switch 530 via logic, such as an analog OR gate 540. The surge protector 524 includes a control output 542 that is coupled to the control terminal 538 of the switch 530 via the analog OR gate 540. One or both of the control outputs 536 and 542 may activate the switch 530 to connect the external capacitor 526 between the voltage supply terminals 518 and 520. The switch 530 selectively couples the second supply terminal 520 to a terminal of the external capacitor 526 via the pin 544.

The power over Ethernet (PoE) protocol circuitry 522 is responsive to the voltage supply terminals 518 and 520. The PoE protocol circuitry 522 is used to perform and to control PoE protocol detection and PoE protocol operations with respect to the powered device 504. For example, the PoE protocol circuitry 522 may provide appropriate current or voltage signals to respond appropriately to the PSE 502 during power detection and classification operations. Additionally, the PoE protocol circuitry 522 may activate the switch 530 when the powered device 504 is connected to the network cable 506 and may deactivate the switch 530 when the network cable 506 is disconnected, for example.

The surge protection logic 524 is configured to provide a current flow path between the first supply terminal 518 and the second supply terminal 520 in response to detecting that a power surge exceeds a given voltage threshold. Thus, the surge protector 524 protects other elements within the integrated circuit 514 from power surges. An example of a power surge is a voltage spike received from the network cable 506 or a power surge that results from an electrostatic discharge (ESD) event at a pin, such as the pins 513 of the integrated circuit 514. In general, a power surge or power surge event may include an over-voltage condition caused by ESD, by electrical fast transients (EFT), by lightning, by cable discharge events, or by another source. In general, a power surge event may include an electrostatic discharge (ESD) event, a lightning-induced transient voltage surge, and a floating cable discharge, or other similarly occurring or characteristic event.

In operation, the PoE protocol circuitry 522 provides a control output 536 to the control terminal 538 of the switch 530 via the analog OR gate 540 to complete a circuit across the DC-to-DC converter 528

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and across the external capacitor 526. When the switch 530 is deactivated, the negative voltage supply on the voltage supply terminal 520 is not provided to the pin 544.

When a power surge is detected that exceeds the threshold of the surge protector 524, the surge protector 524 provides a current path to shunt power between the voltage supply terminals 518 and 520. Additionally, regardless of whether the switch 530 is active, the surge protector 524 can generate a control output 542 to the analog OR gate 540 to activate the switch 530 in response to detection of the power surge. If the switch 530 is already active, the control output 542 ensures that switch 530 remains active and that the voltage supply terminal 520 remains coupled to the pin 544. Thus, the surge protector 524, upon detection of a power surge that exceeds the threshold, can selectively activate the switch 530 to couple the second terminal of the external capacitor 526 to the second voltage supply terminal 520 via the pin 544, allowing current to flow into the external capacitor 526. The external capacitor 526 stores the extra energy resulting from the power surge instead of permitting the extra energy from being dispersed or discharged within elements of the integrated circuit 514.

In a particular embodiment, the PoE protocol circuitry 522 includes logic to activate and selectively deactivate the switch 530 during operation in response to connection and disconnection respectively of a network cable 506 to at least one input pin, such as input pin 513 via the connection interface 512. In a particular embodiment, the switch 530 includes a field effect transistor and may be part of a hot swap switch.

Also, as shown in FIG. 5, the external capacitor 526 may be configured as an input filter in parallel with the DC-to-DC converter 528. The external capacitor 526 provides a dual function of providing an input filter to the DC-to-DC converter 528 while also being available for storage of extra energy due to a power surge event detected by the surge protector 524.

Referring to FIG. 6, another illustrative embodiment of a powered device 600 is shown. The powered device 600 includes an integrated circuit 616 having a plurality of inputs 618 and having a first power supply output 630 and a second power supply output 632. The first power supply output 630 and the second power supply output 632 may be coupled to an external capacitor 620. The integrated circuit 616 also includes one or more diode bridges 602, a voltage protection circuit 604, a hot swap switch and current limit circuit 606, a detection and classification circuit 608, a hot swap control and common bias circuit 610, a switch control circuit 612, and a switching field effect transistor 614. The switch control circuit 612, the hot swap control and common bias circuit 610, and the detection and classification circuit 608 are each coupled to a first power supply output 622 provided by the diode bridges 602. The hot swap switching current limit circuit 606 is coupled to a second power supply output 624 of the diode bridges 602.

In general, the diode bridges 602 are responsive to input pins 618 to receive a power supply from an external power source, such as the power sourcing equipment 502 in FIG. 5. The diode bridges 602 produce a rectified voltage on first and second power supply outputs 622 and 624. The voltage protection circuit 604 is coupled to the first and the second power supply outputs 622 and 624. The hot

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swap switch and current limit circuit 606 is coupled to the power supply output 624 and provides a switched output to power supply output 625, which is coupled to pin 632. The switching field effect transistor 614 is coupled to the power supply output 625.

5 The hot swap control and common bias circuit 610 is adapted to generate an output 640 to the hot swap switch and current limit circuit 606 via an analog OR gate 642 to selectively couple the second power supply output 624 to the power supply output 625 and to pin 632 during operation. The voltage protection circuit 604 provides a control output 644 to the hot swap switch and current limit circuit 606 via the analog OR gate 642 to selectively couple the second power supply output 624 to the power supply output 625. The voltage protection circuit 604 may selectively couple the second power supply output 624 to the power supply output 625 and to the pin 632 in response to detection of a power surge event.

The powered device 600 includes a DC-to-DC converter 640 that is external to the integrated circuit 616. The DC-to-DC converter 640 includes a first terminal 652 coupled to the first power supply output 630, a second terminal coupled to a pin 656, and a third terminal 654 coupled to the second power supply output 632. In general, the DC-to-DC converter 640 may be implemented as a transformer having a primary winding coupled between the first output 630 and the pin 656 and a secondary winding that is inductively coupled to the primary winding. The secondary winding may have a first terminal 658 and a second terminal 660 to provide a regulated supply voltage (V_{reg}) to associated load circuitry (not shown). The second terminal 660 may be coupled by line 654 to the second power supply output 632. In this embodiment, the external capacitor 620 serves both as a filter capacitor to the DC-to-DC converter 640 and as a supplemental surge protector to store energy from a surge event.

During operation, the hot swap switch and current limit circuit 606 is selectively activated in response to a control signal from the voltage protection circuit 604 to couple a terminal of the external capacitor 620 to the second voltage supply terminal 624 via the pin 632. The voltage protection circuit 604 detects an over-voltage condition, for example, due to a particular type of power surge event. The voltage protection circuit 604 may shunt excess energy between the power supply outputs 622 and 624 and may provide a control signal to the hot swap switch and current limit circuit 606. Once the hot swap switch and current limit circuit 606 is activated, the output 632 is coupled to the power supply output 624 providing a current path such that the external capacitor 620 can receive charge from excess energy due to the voltage protection condition and the associated power surge event.

Referring to FIG. 7, another illustrative embodiment of a powered device 700 is shown. The powered device 700 includes an integrated circuit 702 that is coupled to an external capacitor 704 via power supply pins 706 and 708. The integrated circuit 702 includes input pins 710, a communication interface and diode bridges 712, a PoE protocol circuit 714, a diode circuit 715, a diode 722, a resistor 724, transistors 726, 728, and 730, logic 732, a field effect transistor 734, a DC-to-DC converter 736, and load circuitry 738. The diode circuit 715 includes a plurality of diodes 716, 718, and 720, which may be zener diodes. In general, the diode circuit 715 operates as a detector to detect a surge event in

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excess of a threshold. The diodes 716, 718 and 720 are arranged in series such that the breakdown voltages for each diode aggregates to define a total breakdown voltage of the diode circuit 715. In one particular embodiment, the total breakdown voltage of the diode circuit 715 defines a threshold above which a surge event may be detected.

5 The communication interface and diode bridges 712 are coupled to the input pins 710 to receive a power supply and data from a network cable, such as an Ethernet cable. The communication interface and diode bridges 712 operate to rectify the received power supply and to provide a rectified power supply via voltage supply terminals 740 and 742. The communication interface and diode bridges 712 may also include one or more transformers with center taps (not shown) to which the diode bridges 10 may be coupled. The PoE control circuit 714 is coupled between the voltage supply terminals 740 and 742.

The diode circuit 715 may be designed to include additional diodes as indicated by the dotted line 721. Generally, the diodes 716, 718 and 720 are arranged to form a diode stack such that the diode circuit 715 has a cathode terminal 719 coupled to the voltage supply terminal 740 at a node 717 and having an 15 anode terminal 723. The diode 722 includes a cathode terminal 725 coupled to the voltage supply terminal 742 and an anode terminal 727 coupled to the anode terminal 723 of the diode circuit 715. The transistor 726 includes a first (collector) terminal 729, a control (base) terminal 731 that is coupled to the anode terminals 727 and 723 of the diodes 722 and 720, and a second (emitter) terminal 733 that is coupled to the voltage supply terminal 742. The transistor 728 includes a first (collector) terminal 20 737 that is coupled to the first terminal 729 of the transistor 726. The transistors 728 and 730 share a second (emitter) terminal 735 coupled to the diode circuit 715 and a control (base) terminal 739 that is coupled to the second terminal 737. The transistor 730 includes a first (collector) terminal 741 that is coupled to the logic 732. The transistors 728 and 730 operate as a current mirror to activate a switch, such as the field effect transistor 734, via the logic 732 when the power surge exceeds the threshold. 25 The transistor 734 includes a first (source) terminal 747 coupled to the voltage supply terminal 742, a control (gate) terminal 745 coupled to the output of the logic 732, and a second (drain) terminal 743 coupled to the pin 708. The DC-to-DC converter 736 is coupled between the voltage supply terminal 740 and the pin 708. The DC-to-DC converter 736 is adapted to produce a regulated supply voltage to regulated voltage terminals 750 and 752 and to the load 738 that is coupled between the regulated 30 voltage terminals 750 and 752.

In one particular embodiment, the field effect transistor 734 also serves as a hot swap switch to turn off a power supply to the DC-to-DC converter 736 and to its associated load circuitry 738.

In general, the integrated circuit 702 of the powered device 700 includes inputs 710 that are responsive to an external power supply, such as the PSE 502 in FIG. 5. The communication interface and diode 35 bridges 712 are responsive to the inputs 710 to provide a rectified power supply to a pair of supply terminals, the first supply terminal 740 and the second supply terminal 742. The diode circuit 715, in conjunction with the logic 732, operates as a detector that is responsive to the first supply terminal 740 and to the second supply terminal 742 to detect a power surge event in excess of a threshold, which

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may be defined by a breakdown voltage of the diode circuit 715. The external capacitor 704 includes a first terminal 705 coupled to the first supply terminal 740 via pin 706 and includes a second terminal 707 that is coupled to the second supply terminal 742 via pin 708 and via drain terminal 743 of the field effect transistor 734. The field effect transistor 734 operates as a switch to selectively couple the second terminal 707 of the external capacitor 704 to the second supply terminal 742. The logic 732 selectively activates the field effect transistor 734 in response to detection of the surge event to deliver energy resulting from the surge event to the external capacitor 704.

In operation, a voltage surge received at the inputs 710 to the integrated circuit 702 is rectified by the communication interface and diode bridges 712. The resulting rectified power supply is applied to the voltage supply terminals 740 and 742. When a power surge voltage at the voltage supply terminals 740 and 742 exceeds the aggregate breakdown voltage of the diode circuit 715, including the illustrated diodes 716, 718 and 720, current flows across the diodes 716, 718 and 720 to the control terminal of the transistor 726. The current activates the transistor 726, which draws current from the transistor 728, producing a mirrored current in the first terminal 741 of the transistor 730, thereby activating the field effect transistor 734 via the logic 732.

The field effect transistor 734 may be utilized as a hot-swap switch controlled by the PoE protocol circuit 714 through the logic 732. During the surge event, the transistor 734 may be activated by either the PoE protocol circuit 714 or the diode circuit 715 to deliver surge energy to the external capacitor 704 that also serves as an input capacitor for the DC-to-DC converter 736.

Upon termination of the power surge event, the external capacitor 704 may discharge through the DC-to-DC converter 736 and through associated load circuitry 738 or other load circuitry coupled to the regulated voltage terminals 750 and 752. For example, once the power surge event terminates, the current flowing into the external capacitor 704 stops, and the switch 734 may be deactivated. In this instance, the external capacitor 704 may have a stored voltage, which may be discharged and which the DC-to-DC converter 736 may regulate and provide to the regulated voltage terminals 750 and 752 and any load circuitry coupled to the regulated voltage terminals 750 and 752.

In one particular embodiment, negative feedback from the source terminal 747 is fed back to the diode circuit 715 to deliver additional voltage to the control terminal 731 of the transistor 726, which transfers the feedback to the gate terminal 745 of the field effect transistor 734 via the current mirror (transistors 728 and 730) and via the logic 732. In particular, the negative feedback from the source terminal 747 of the field effect transistor 734 is fed back through the resistor 724 to the breakdown diode 720 and via the transistors 726, 728 and 730 to the logic 732 to the control terminal 745 of the field effect transistor 734 via the logic 732, thereby causing the field effect transistor 734 to conduct sufficient current to keep the voltage supply terminals 740 and 742 clamped at a voltage level that is approximately equal to the breakdown voltage of the diode circuit 715. This clamping action serves to reduce the likelihood of voltage overshoot which may be seen in typical zener-based transient voltage suppressors. A significant portion of the power surge energy may be delivered to the external capacitor

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704. The remaining portion of the power surge energy may be absorbed by the diode bridges of the communication interface 712 and by the diode circuit 715.

It should be understood that the field effect transistor 734 may be activated either by the PoE protocol circuit 714 or by the surge detector (e.g. diode circuit 715, transistors 726, 728 and 730, and logic 732).

5 Thus, the field effect transistor 734 may serve a dual role as both a hot-swap switch and as a power surge switch to connect the voltage supply terminals 740 and 742 to the DC-to-DC converter 736 and to the external capacitor 704. The external capacitor 704 is arranged in parallel to the DC-to-DC converter 736, allowing the capacitor 704 to provide a dual function as both an input filter to the DC-to-DC converter 736 and as a power storage device to absorb energy resulting from a power surge
10 event. By steering current through the field effect transistor 734 and into the capacitor 704, the capacitor 704 may thus be used to serve a dual purpose: to filter the input voltage to the DC-to-DC converter 736 and to absorb some of the excess energy resulting from a transient power event.

In general, the external capacitor 704 has a size that is relatively large to comply with the PoE standard and to operate in conjunction with the field effect transistor 734. In one particular embodiment, the
15 external capacitor 704 has a capacitance of approximately 22 uF. In response to a current surge of 5 Amperes for approximately 50 microseconds, the external capacitor 704 can absorb current until a change in a capacitive voltage (ΔV_{C1}) of approximately 11.4 volts is reached, according to the following equation:

$$\Delta V_{C1} = \frac{5 \text{ Amps}}{22 \mu\text{F}} * 50 \mu\text{S} = 11.4 \text{ volts} \quad (\text{Equation 1})$$

20 The external capacitor 704 may absorb the 11.4 volts, which represents the power spike (a change in voltage) due to the power surge.

In another particular illustrative embodiment, the capacitor is 10uF, and the voltage protection circuit (i.e. the diode stack) 715 is designed to clamp the input voltage on the voltage supply terminals 740 and 742 to approximately 65 volts. In this instance, the external capacitor 704 may absorb a current of
25 up to 13A given a 50uS transient, where $I = C \frac{dV}{dt}$. The external capacitor 704 may absorb current as follows:

$$I = 10 \mu\text{F} * \frac{65\text{v}}{50 \mu\text{S}} = 13 \text{ A}. \quad (\text{Equation 2})$$

By activating the field effect transistor 734 to connect the voltage supply terminal 742 to the external capacitor 704 via the pin 708, energy resulting from the power surge is directed to and absorbed by the
30 external capacitor 704. Thus, the powered device 700 may withstand a much higher transient current than the source limited 5A current specified by the PoE standard. Moreover, since a typical transient

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power surge begins decaying immediately after reaching a peak current, the time to charge the external capacitor 704 may increase, since the current provided to the external capacitor 704 is decreasing while the external capacitor 704 is charging. Since the external capacitor 704 takes additional time to charge as the power surge induced current decreases, the external capacitor 704 allows the powered device 700 to withstand a relatively high transient current that might otherwise overheat and damage the diode circuit 715.

Additionally, the external capacitor 704 and the field effect transistor 734 make it possible to reduce the size of the voltage protection diode circuit 715, since the breakdown diodes 716, 718, and 720 no longer need to dissipate as much of the energy from the transient power surge event. If the voltage protection circuit 715 is utilized to generate a turn-on signal for the field effect transistor 734 (the hot swap switch), the voltage protection circuit 715 need only consume sufficient energy to hold the field effect transistor 734 in an on-state to consume the remaining energy of the transient. Since the integrated circuit 702 includes the PoE protocol circuitry 714, which controls the field effect transistor 734, the same control signal that enables the field effect transistor 734 may disable the field effect transistor 734 to prevent unnecessary operation during an ESD-type or other type of fault condition.

Referring to FIG. 8, a block diagram of another illustrative embodiment of a particular powered device 800 is shown. The powered device 800 includes an integrated circuit 802 including a first output 820 and a second output 822 that are coupled respectively to terminals of an external capacitor 810. The integrated circuit 802 includes power surge protection logic 806 and a switch 804. The switch 804 is controlled by a control signal 812 provided by the output of the power surge protection logic 806. The power surge protection logic 806 is coupled to a first power supply terminal 830 and to a second power supply terminal 832.

During operation, a power surge event is detected at the first power supply 830 by the power surge protection logic 806 within the integrated circuit 802. The power surge protection logic 806 then provides a shunting effect with respect to the first power supply terminal to the second power supply terminal 832 and provides an activation signal over control terminal 812 to the switch 804. In addition, the switch 804 is activated in response to detection of the power surge event to connect the second power supply terminal 832 to the pin 822, which enables the external capacitor 810 to receive energy associated with the power surge event. Thus, energy that exceeds a voltage threshold level that is detected by the power surge protection logic 806 may be provided safely to and shared by the external capacitor 810 and may avoid negative thermal and other power surge dissipation effects, such as a snap back voltage within the integrated circuit 802. The external capacitor 810 thereby provides an energy relief mechanism to assist with energy dispersion and storage of energy related to the power surge event.

In a particular embodiment, the switch 804 may be activated in a gradual manner and may react to feedback provided by the level of surge of the power surge event to provide a gradual turn on. With the gradual turn on, the switch 804 provides a gradually lower resistance level until the switch 804 is fully enabled. In this manner, the power surge protection logic 806 may provide a gradual and

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controlled turn on command to the switch 804 that thereby provides increased and controlled routing of excess energy to the external capacitor 810 as needed. In one particular embodiment, the switch 804 may include a voltage controlled field effect transistor that includes a gate terminal that is coupled to the power surge protection logic 806. The power surge protection logic 806 may control the voltage applied to the gate terminal of the transistor to throttle current flow through the capacitor 810.

In general, the term power surge or power surge event includes, but is not limited to, an over-voltage condition caused by ESD, by electrical fast transients (EFT), by lightning, by cable discharge events, or by another source. An over-voltage condition includes, but is not limited to, a voltage level that exceeds a threshold. In general, a power surge event may be caused by an inductive kick back from a DC-to-DC converter, for example, when a cable carrying DC current is disconnected from the powered device. If a powered device, for example, is drawing 700mA of current and the Ethernet cable is disconnected, an inductive kick may be created. The length of the Ethernet cable determines the inductance, so a long Ethernet cable may produce a larger inductive kick. In one embodiment, the inductive voltage kick may create an electrical arc, which can damage the RJ-45 Ethernet connection interface and create large differential voltage signals.

Additionally, when an Ethernet cable is unplugged, one pin may physically disconnect from the powered device before the other pins. This asynchronous disconnection may be a result of construction variation within a connector. If one pin disconnects, an imbalance may be created in the current that should be flowing in a common mode via transformer windings of a connection interface. This imbalance may appear as a large differential signal.

Moreover, cable discharge events may cause a power surge. Cable discharge events may be caused by charge storage on a cable from being dragged on the floor or for contacting high-voltage sources. Ethernet cables, such as CAT-5e and CAT-6, are designed to have very low leakage, so such cables may hold a charge for a period of time. When the cable is plugged in, the stored charge may discharge into the powered device. If, due to construction variations, one pin establishes a connection first, a large transient may be created.

By utilizing an external capacitor and a switch to couple the external capacitor to the power supply terminals, power surge events (regardless of their source) may be contained, controlled, and dissipated by shunting voltage between the power supply terminals and by storing excess energy in the external capacitor, as described above with respect to FIGS. 5-8.

Referring to FIG. 9, a method of operating a powered device such as those shown with reference to FIGS. 5-8 is shown. The method includes detecting a power surge event, such as an electrostatic discharge (ESD) event at a first power supply terminal of an integrated circuit, at 900. The method further includes activating a surge protection circuit to shunt the power supply terminal to a second power supply terminal of an integrated circuit while concurrently activating a switch within the integrated circuit to enable an external capacitor to receive energy associated with the power surge event in response to detecting such power surge event, as shown at 902. The method also includes

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transferring current from a terminal of the switch to the power surge protection circuit, as shown at 904, and increasing a level of the current through the switch, as shown at 906. In addition, a portion of the energy from the surge protection circuit may be fed back to provide a further adjustment in controlled management of the switch and the resulting energy provided to charge the external capacitor.

Although the present specification describes components and functions that may be implemented in particular embodiments with reference to particular standards and protocols, the invention is not limited to such standards and protocols. For example, the IEEE STD 802.3TM standard for PoE represents an example of the state of the art. Such standards are periodically superseded by newer equivalents specifying substantially similar functions and specifying additional requirements. Accordingly, replacement standards and protocols having the same or similar functions as those disclosed herein are considered equivalents thereof.

In general, though the embodiments described above have focused largely on PoE implementations, it should be understood that the surge protection systems and methods, such as that described above with respect to FIGS. 5-9, may be utilized in other applications where it is desirable to protect load circuitry from power surge events. Moreover, the above-described embodiments may be employed with other types of powered networks, where the power supply voltage cabling also carries data. For example, the power supply and data may be received from a bus including power and data. Alternatively, the power supply may be derived from electrical power lines that also carry data transmissions. In general, a powered device may be adapted to derive power and to receive data from the same wire, wire pair, or alternative communication link, regardless of the network type.

Additionally, it should be understood that the snubber circuit 130 of FIG. 1 and the techniques for handling an electrostatic discharge event may be utilized in cooperation with power surge detection logic (such as the surge protector 524) and the switch 530 illustrated in FIG. 5 to provide ESD protection and surge protection for a single circuit or for a circuit device. Additionally, in a particular illustrative example, the switch control circuit 612 and the switching field effect transistor 614 illustrated in FIG. 6 may be used in cooperation with the snubber circuit 130 of FIG. 1. Additionally, the various illustrated embodiments and the associated discussion are intended for illustrative purposes only. Other combinations of the various embodiments described above with respect to FIGS. 1-9 will be understood by a worker skilled in the art.

The illustrations of the embodiments described herein are intended to provide a general understanding of the structure of the various embodiments. The illustrations are not intended to serve as a complete description of all of the elements and features of apparatus and systems that utilize the structures or methods described herein. Many other embodiments may be apparent to those of skill in the art upon reviewing the disclosure. Other embodiments may be utilized and derived from the disclosure, such that structural and logical substitutions and changes may be made without departing from the scope of the disclosure. Additionally, the illustrations are merely representational and may not be drawn to scale. Certain proportions within the illustrations may be exaggerated, while other proportions may be

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reduced. Accordingly, the disclosure and the figures are to be regarded as illustrative rather than restrictive.

Although specific embodiments have been illustrated and described herein, it should be appreciated that any subsequent arrangement designed to achieve the same or similar purpose may be substituted
5 for the specific embodiments shown. This disclosure is intended to cover any and all subsequent adaptations or variations of various embodiments. Combinations of the above embodiments, and other embodiments not specifically described herein, will be apparent to those of skill in the art upon reviewing the description.

The above-disclosed subject matter is to be considered illustrative, and not restrictive, and the
10 appended claims are intended to cover all such modifications, enhancements, and other embodiments, which fall within the true spirit and scope of the present invention. Thus, to the maximum extent allowed by law, the scope of the present invention is to be determined by the broadest permissible interpretation of the following claims and their equivalents, and shall not be restricted or limited by the foregoing detailed description.

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WHAT IS CLAIMED IS:

1. A powered device comprising:
a voltage protection circuit of an integrated circuit;
two pins of the integrated circuit coupleable to an external transformer;
a switch of the integrated circuit; and
5 a snubber circuit of the integrated circuit responsive to the switch, the snubber circuit responsive to the two pins to direct energy resulting from a power event away from the switch to the voltage protection circuit.

2. The powered device of claim 1, wherein the snubber circuit comprises:
a diode including an anode terminal coupled to the switch and including a cathode terminal;
10 and
a diode breakdown circuit including a cathode terminal coupled to the cathode terminal of the diode and including an anode terminal coupled to the voltage protection circuit.

3. The powered device of claim 1, wherein the snubber circuit is to prevent a voltage across the switch from exceeding a threshold voltage.

- 15 4. The powered device of claim 1, further comprising:
at least two inputs of an integrated circuit responsive to an external power source, the at least two inputs including a first input and a second input; and
a diode bridge responsive to the at least two inputs to provide a rectified power supply to a first power supply terminal and a second power supply terminal;
20 wherein the external power source comprises power sourcing equipment.

5. The powered device of claim 4, wherein the voltage protection circuit is coupled between the first and second power supply terminals.

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- 5 6. The powered device of claim 4, wherein the switch comprises a transistor having a first terminal coupled to a terminal of an external transformer, a control terminal responsive to Power over Ethernet (PoE) protocol logic, and a second terminal coupled to the negative supply terminal, the switch to selectively couple the first and second terminals to activate the external transformer.
7. The powered device of claim 1, wherein the snubber circuit impedes current flow when the voltage across the snubber circuit is less than a threshold, and wherein the snubber circuit directs energy to the voltage protection circuit when the voltage across the snubber circuit exceeds the threshold.
- 10 8. The powered device of claim 1, wherein the energy is received after an inductive kick of the external transformer at the at least one of the two inputs.
9. The powered device of claim 1, wherein the energy is received after an electrostatic discharge (ESD) event.
- 15 10. The powered device of claim 1, further comprising:
logic to selectively activate the switch when at least two inputs including a first input and a second input of the integrated circuit are coupled to the external power source.
- 20 11. A method comprising:
detecting a power event at a snubber circuit of an integrated circuit, the snubber circuit responsive to an external transformer connected to a negative supply terminal of the integrated circuit;
directing energy resulting from the power event to a voltage protection circuit via the snubber circuit when a voltage level of the power event exceeds a threshold, the threshold less than a safe power level of a switch within the integrated circuit.
- 25 12. The method of claim 11, wherein the power event comprises an electrostatic discharge (ESD) event.
13. The method of claim 11, wherein the power event comprises an inductive voltage kick.
14. The method of claim 11, wherein detecting the power event comprises:
detecting a voltage in excess of a breakdown voltage level of a breakdown diode circuit of the snubber circuit.

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15. The method of claim 11, wherein the voltage protection circuit is part of the integrated circuit.

16. The method of claim 11, wherein the safe power level of the switch comprises a voltage rating determined by a manufacturer of the switch.

5 17. The method of claim 11, further comprising:
detecting a power supply from an external power source; and
selectively activating the switch responsive to detection of the power supply to deliver power to an external transformer.

10 18. An integrated circuit comprising:
a transistor including a first terminal, a second terminal coupled to a first power supply terminal, and a control terminal;
a pin coupled to the first terminal of the transistor and responsive to an external transformer;
and
a snubber circuit responsive to the pin to direct an inductive voltage that exceeds a threshold
15 to a voltage protection circuit to protect the transistor.

19. The integrated circuit of claim 18, wherein the snubber circuit is responsive to the pin to direct energy resulting from an electrostatic discharge (ESD) event from the pin to the voltage protection circuit.

20 20. The integrated circuit of claim 18, further comprising a Power over Ethernet (PoE) protocol circuit to provide PoE protocol functions including PoE detection.

21. The integrated circuit of claim 18, further comprising:
a diode bridge responsive to a communication interface to receive a power supply input from power sourcing equipment and to provide a rectified power supply to a pair of power supply terminals, the pair of power supply terminals including the first power supply terminal.

25 22. The integrated circuit of claim 21, wherein the voltage protection circuit is coupled between the pair of power supply terminals.

30 23. The integrated circuit of claim 18, wherein the snubber circuit comprises:
a first diode circuit including an anode terminal coupled to a second power supply terminal of the pair of power supply terminals and including a cathode terminal; and
a second diode circuit including an anode terminal coupled to the interface and a cathode terminal coupled to the cathode terminal of the first diode circuit:

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wherein the first diode circuit blocks current flow when a voltage level across the snubber circuit is less than the threshold.

24. The integrated circuit of claim 18, wherein the threshold is defined by a breakdown voltage of a diode circuit.

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25. A powered device comprising:
first and second input pins responsive to an external power source;
first and second output pins responsive to an external transformer, the first output pin coupled
to the first input pin;
5 a third output pin coupled to the second input pin; and
a voltage protection circuit to limit an input voltage to a level that is less than an input
threshold;
wherein, when a voltage on the first and second input pins is below a lower threshold or above
the input threshold, power applied to the second output pin is directed to the voltage protection
10 circuit;
wherein, when a voltage on the first and second input pins is at a voltage level that between
the lower threshold and the input threshold, power applied to the second output pin is directed
to the third output pin.
26. The powered device of claim 25, wherein the first and second input pins, the first and
15 second output pins, the third output pin, and the logic are fabricated on an integrated circuit.
27. The powered device of claim 25, further comprising:
a snubber circuit coupled to the first output pin and to the second output pin; and
a switch coupled to the second output pin and to the third output pin, the switch to selectively
connect the external transformer to the second output pin.
- 20 28. The powered device of claim 27, wherein the snubber circuit and the voltage protection
circuit limit the first voltage to a level that is less than a voltage rating of the switch.

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29. A powered device comprising:
a first supply terminal and a second supply terminal;
at least one input pin coupled to the first supply terminal;
an external capacitor having a first terminal coupled to the first supply terminal;
5 a switch coupled to the second supply terminal and coupled to a second terminal of the
external capacitor; and
power surge detection logic coupled to the switch;
wherein the external capacitor is charged in response to a detected power surge that exceeds a
threshold voltage.
- 10 30. The powered device of claim 29, wherein the power surge detection logic is to activate a
current flow path between the first supply terminal and the second supply terminal in response
to detecting that the power surge exceeds the threshold voltage.
31. The powered device of claim 29, wherein the at least one input pin is responsive to an
external power supply, the powered device further comprising:
15 a diode bridge having an input to receive a power supply input from the at least one input pin,
the diode bridge to couple the power supply input to the first supply terminal and to the
second supply terminal to provide a rectified power supply to the first and second supply
terminals.
32. The powered device of claim 29, further comprising:
20 logic to selectively activate and deactivate the switch during operation in response to
connection and disconnection, respectively, of a network cable to the at least one input pin.
33. The powered device of claim 29, wherein the first supply terminal, the second supply
terminal, the at least one input pin, the switch, and the power surge detection logic are
fabricated on an integrated circuit.
- 25 34. The powered device of claim 29, wherein the power surge results from an electrical event
selected from a group consisting of an electrostatic discharge (ESD) event, a lightning-
induced transient voltage surge, and a floating cable discharge.
35. The powered device of claim 29, wherein the power surge detection logic comprises:
30 a diode circuit comprising a plurality of diodes arranged in series, wherein a sum of
breakdown voltages of the plurality of diodes defines the threshold voltage;
an n-type transistor including a collector terminal, a control terminal coupled to the diode
circuit, and an emitter terminal coupled to the second supply terminal;

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a current mirror having a first terminal coupled to the diode circuit and a second terminal coupled to the collector terminal of the n-type transistor, the current mirror to mirror current to activate the switch when the power surge exceeds the threshold.

5 36. The powered device of claim 35, wherein the switch comprises a field effect transistor including a source coupled to the second terminal of the external capacitor, a gate coupled to the current mirror, and a drain terminal coupled to the second supply terminal.

37. The powered device of claim 36, wherein negative feedback from the source terminal is fed back to the diode circuit to deliver additional voltage to the gate of the field effect transistor.

10 38. The powered device of claim 29, wherein the switch comprises a hot swap switch.

39. The powered device of claim 29, wherein the external capacitor comprises an input capacitor of a DC-to-DC converter.

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40. A method comprising:
detecting a power surge event at a first power supply terminal of an integrated circuit;
activating a surge protection circuit to shunt the power supply terminal to a second power
supply terminal of the integrated circuit while concurrently activating a switch within the
integrated circuit in response to detecting the power surge event to enable an external
capacitor to receive energy associated with the power surge event.
- 5
41. The method of claim 40, further comprising:
feeding back a portion of the energy to the surge protection circuit.
42. The method of claim 40, wherein the switch comprises a voltage controlled field effect
transistor and wherein a gate terminal of the voltage controlled field effect transistor is
coupled to the surge protection circuit, wherein the method further comprises:
transferring a current from a source terminal of the voltage controlled field effect transistor to
the surge protection circuit; and
increasing a level of the current through the voltage controlled field effect transistor by
providing the transferred current to the gate terminal.
- 10
- 15
43. The method of claim 40, wherein the power surge event comprises an electrical event
selected from a group consisting of an electrostatic discharge (ESD) event, a lightning-
induced transient voltage surge, and a floating cable discharge.
44. The method of claim 40, wherein the switch comprises a hot swap switch to selectively
couple a DC-to-DC converter to a communication interface.
- 20

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45. A powered device comprising:
at least one input responsive to an external power supply;
a diode bridge responsive to the at least one input to provide a rectified power supply to a pair
of supply terminals comprising a first supply terminal and a second supply terminal;
5 a detector responsive to the first supply terminal and the second supply terminal to detect a
surge event in excess of a threshold;
an external capacitor including a first terminal coupled to the first supply terminal and
including a second terminal;
a switch to selectively couple the second terminal of the external capacitor to the second
10 supply terminal; and
logic to selectively activate the switch in response to detection of the surge event to deliver
energy resulting from the surge event to the external capacitor.
46. The powered device of claim 45, wherein the detector comprises a diode stack comprising
a plurality of diodes arranged in series.
- 15 47. The powered device of claim 45, wherein the at least one input, the diode bridge, the
detector, the switch and the logic are fabricated on an integrated circuit.
48. The powered device of claim 45, wherein the external capacitor discharges through load
circuitry upon termination of the surge event.

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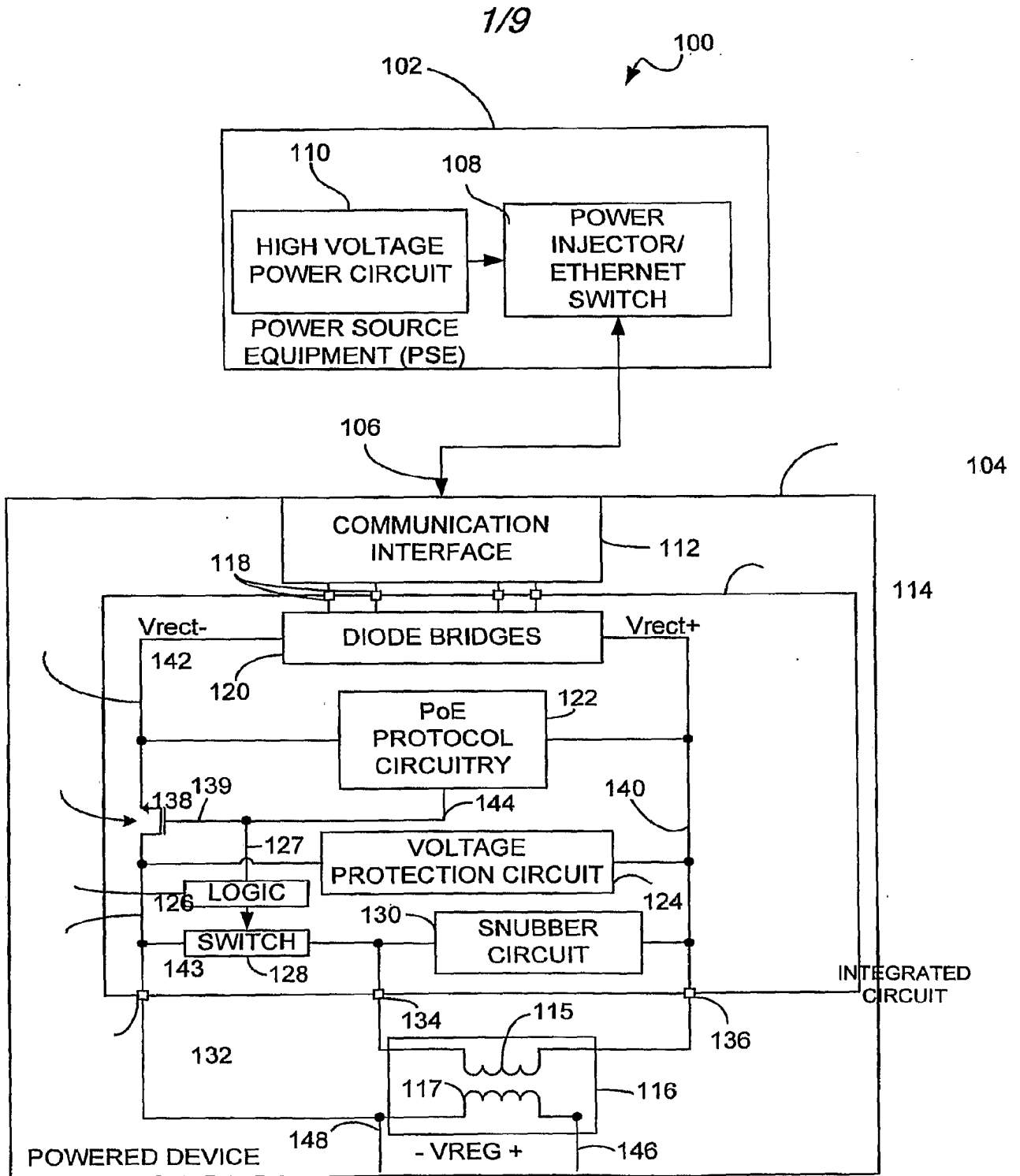


FIG. 1

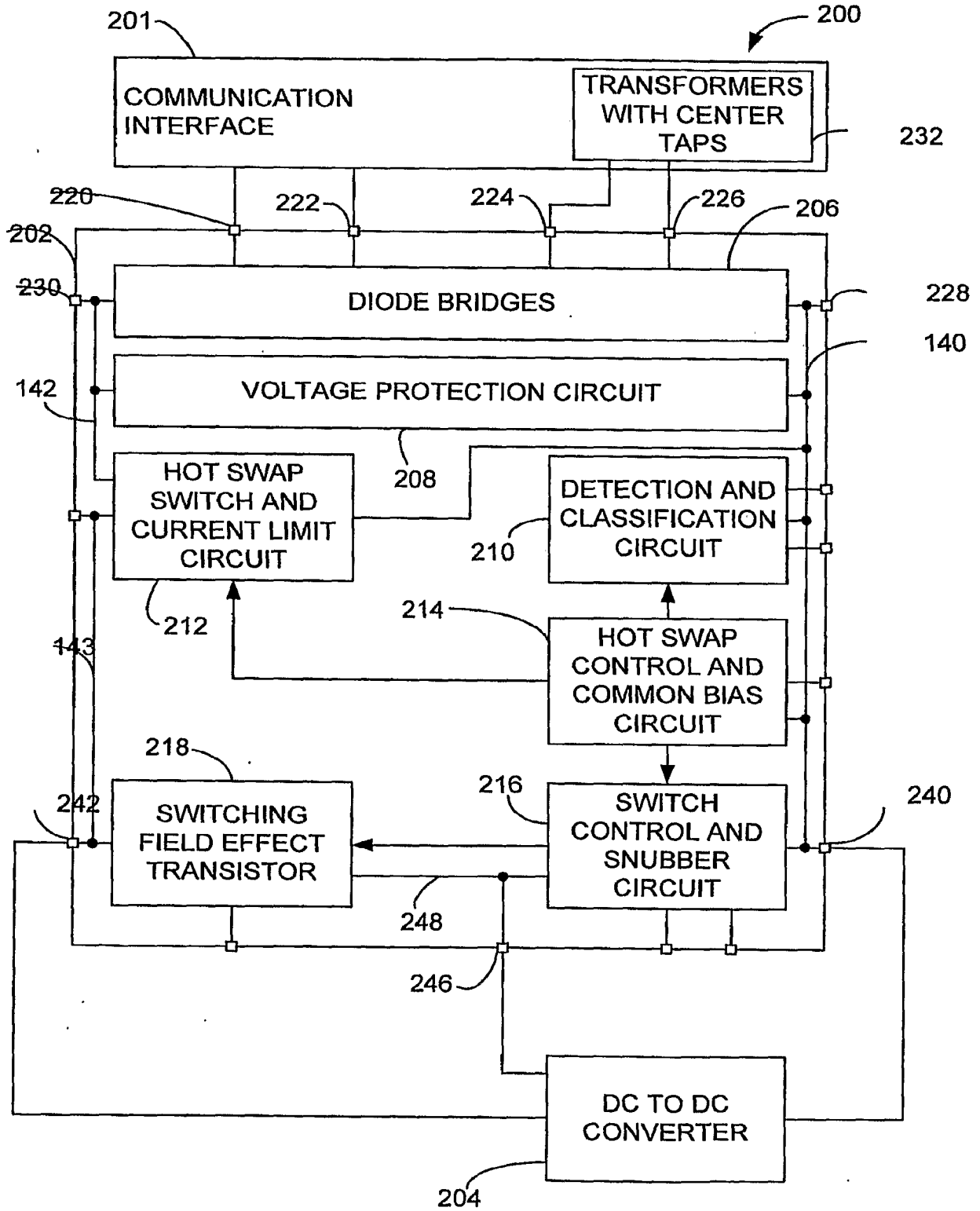


FIG. 2

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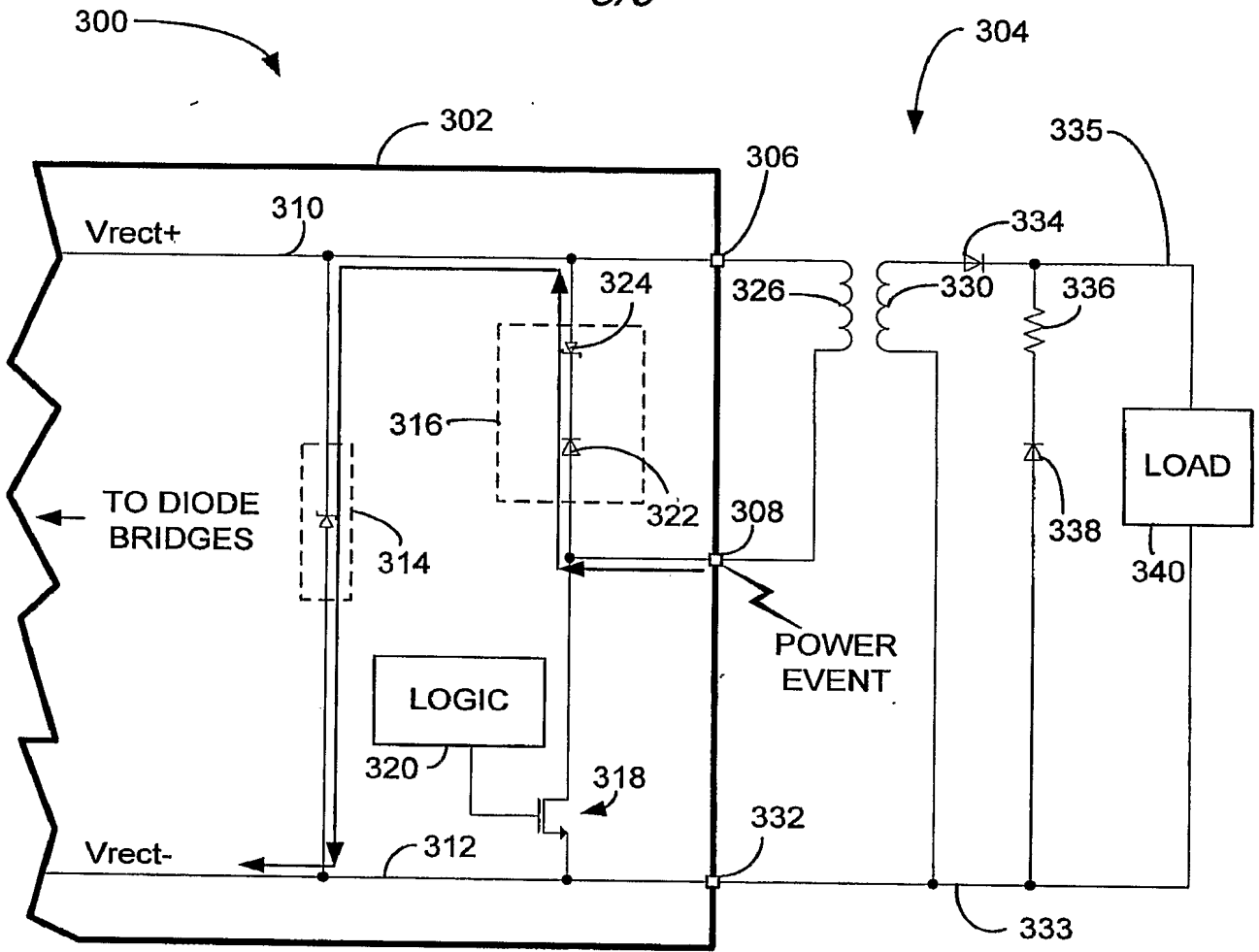


FIG. 3

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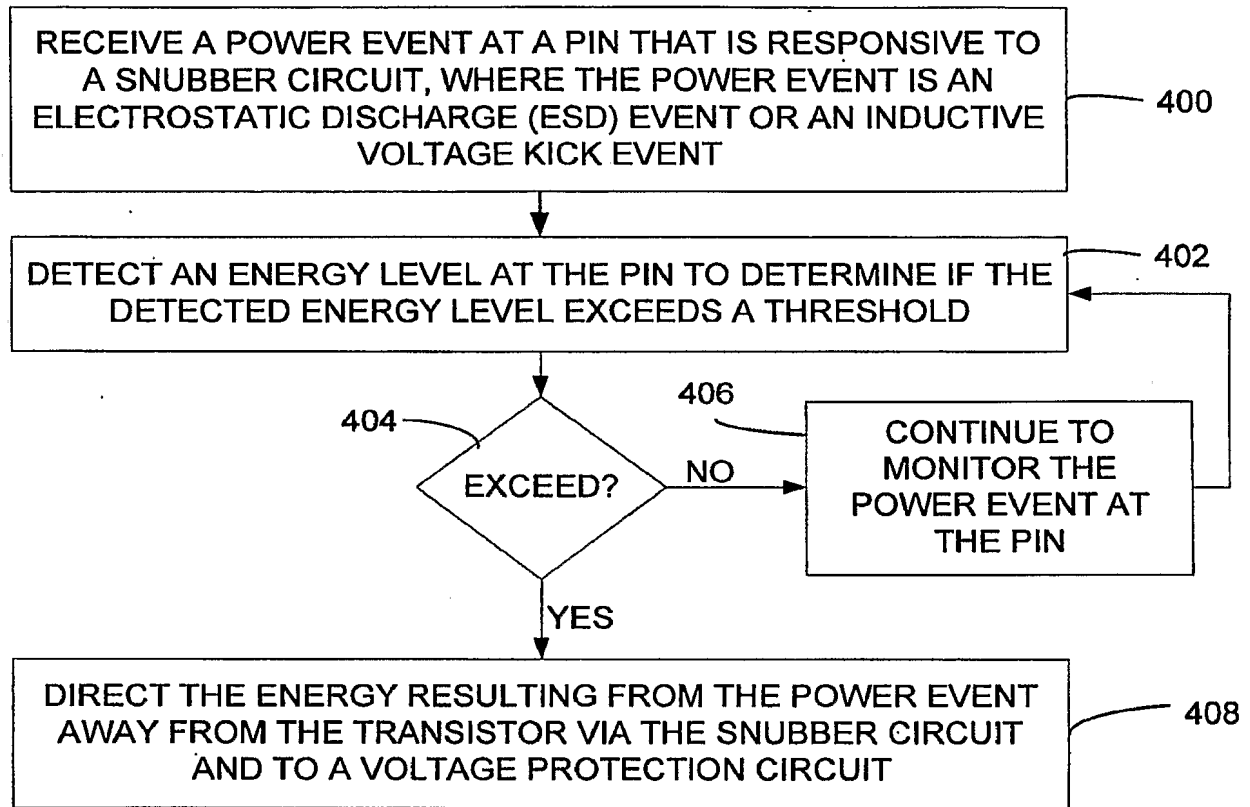


FIG. 4

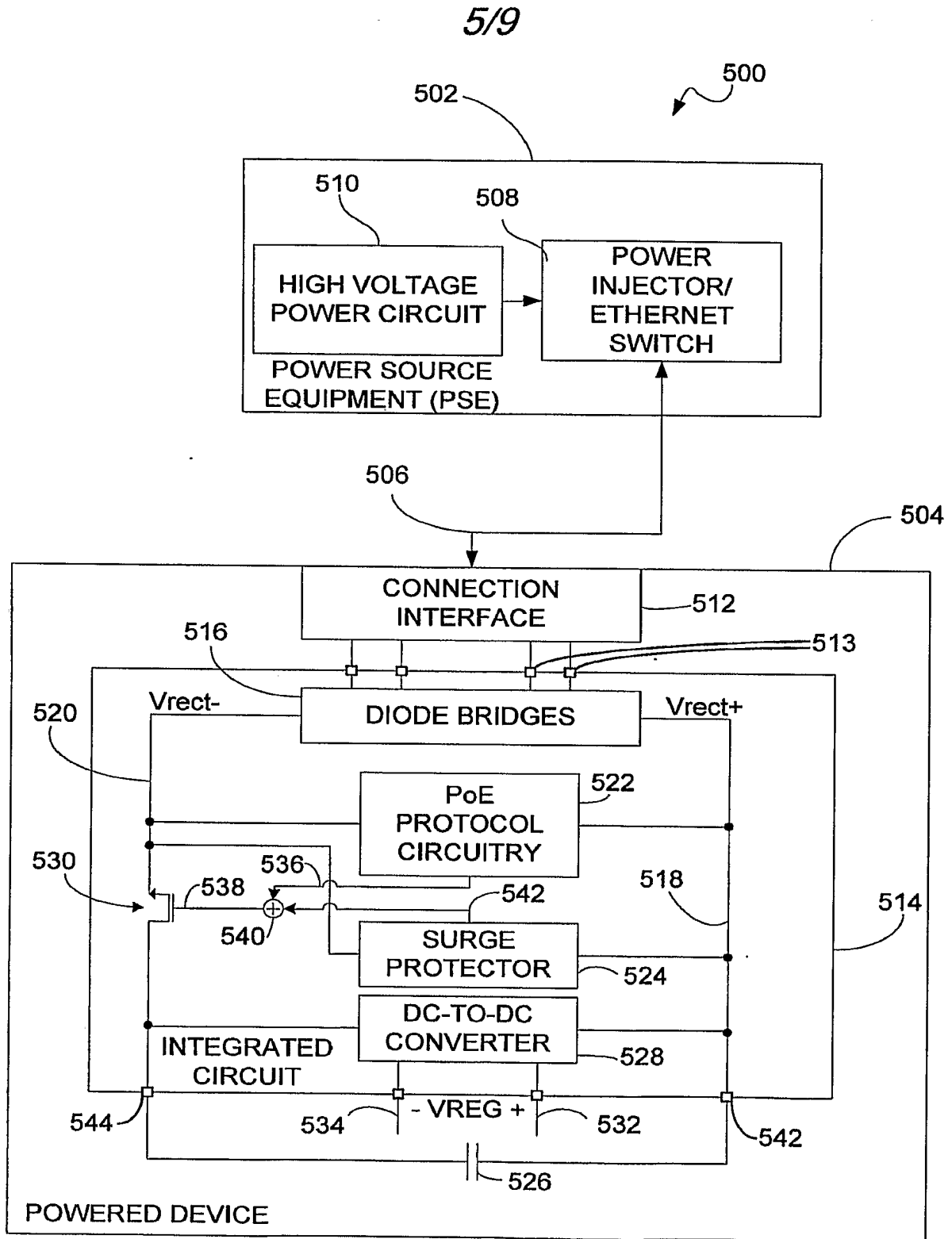


FIG. 5

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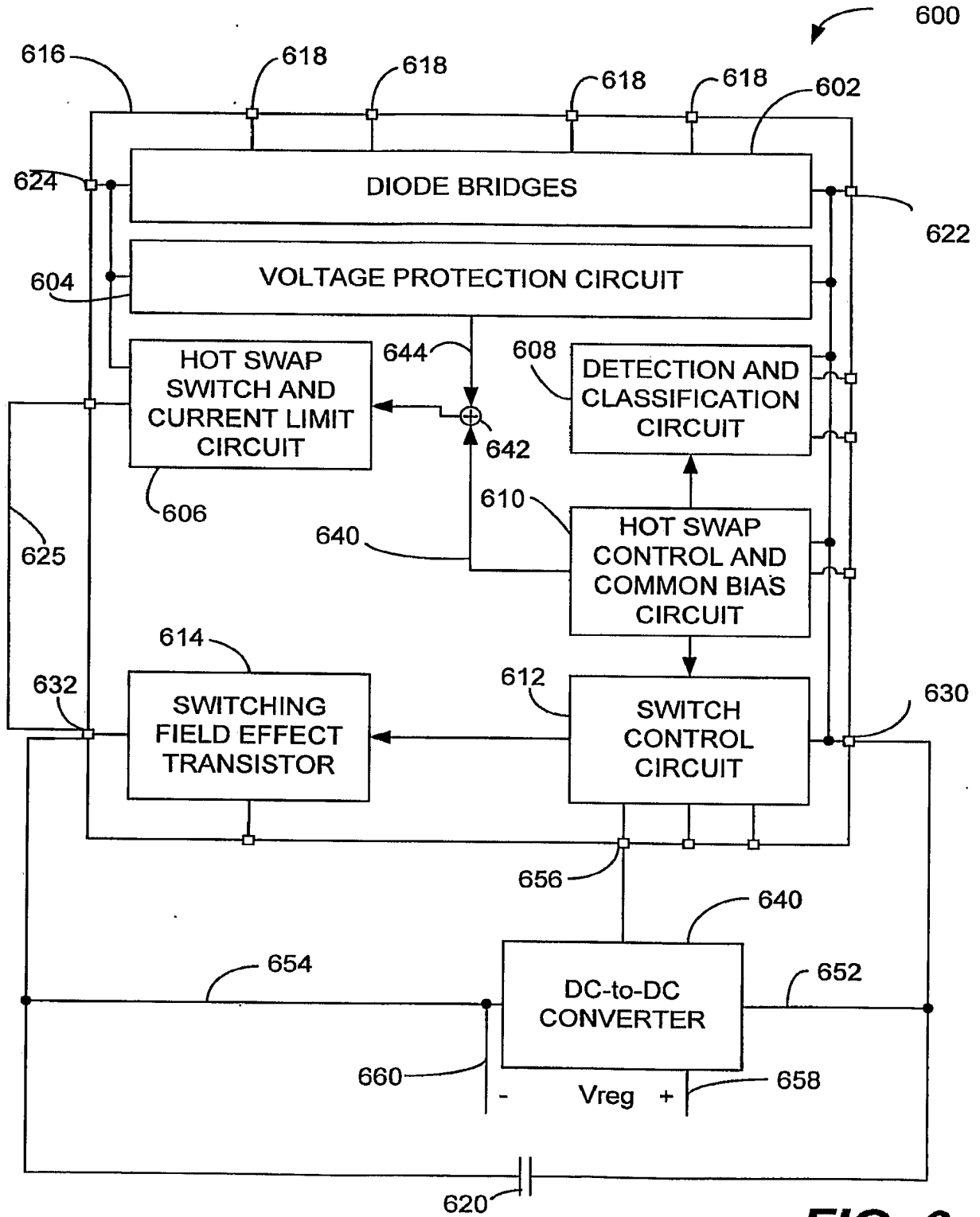


FIG. 6

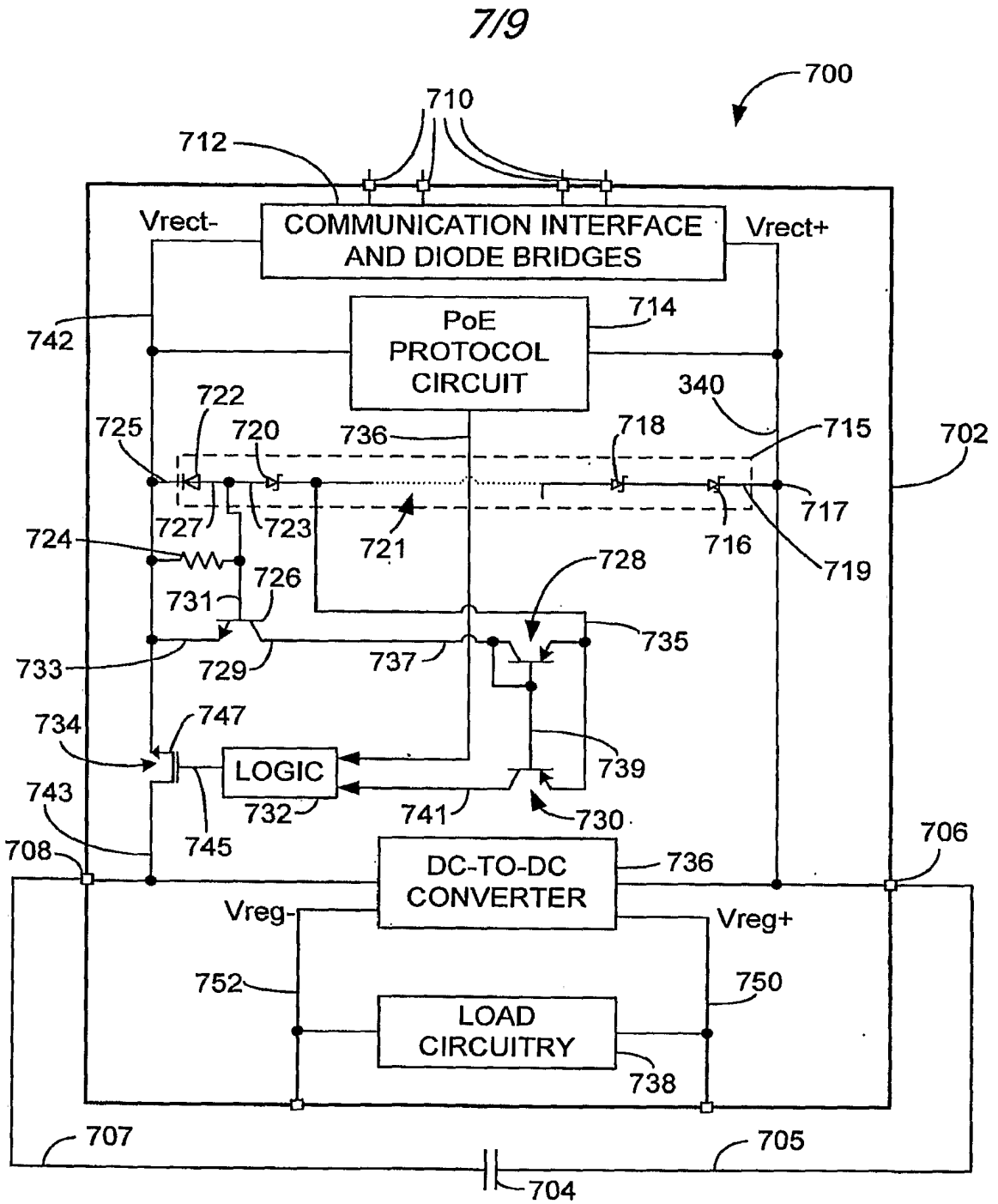


FIG. 7

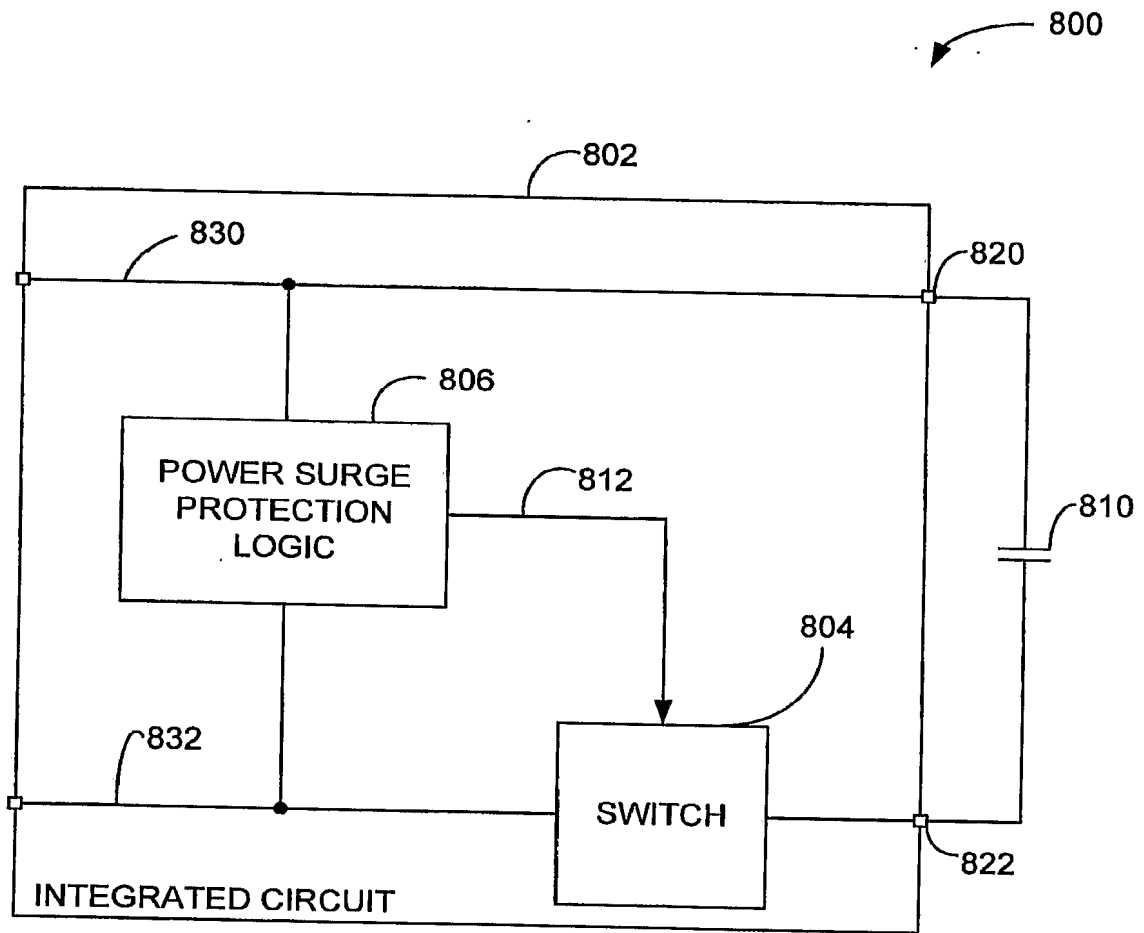
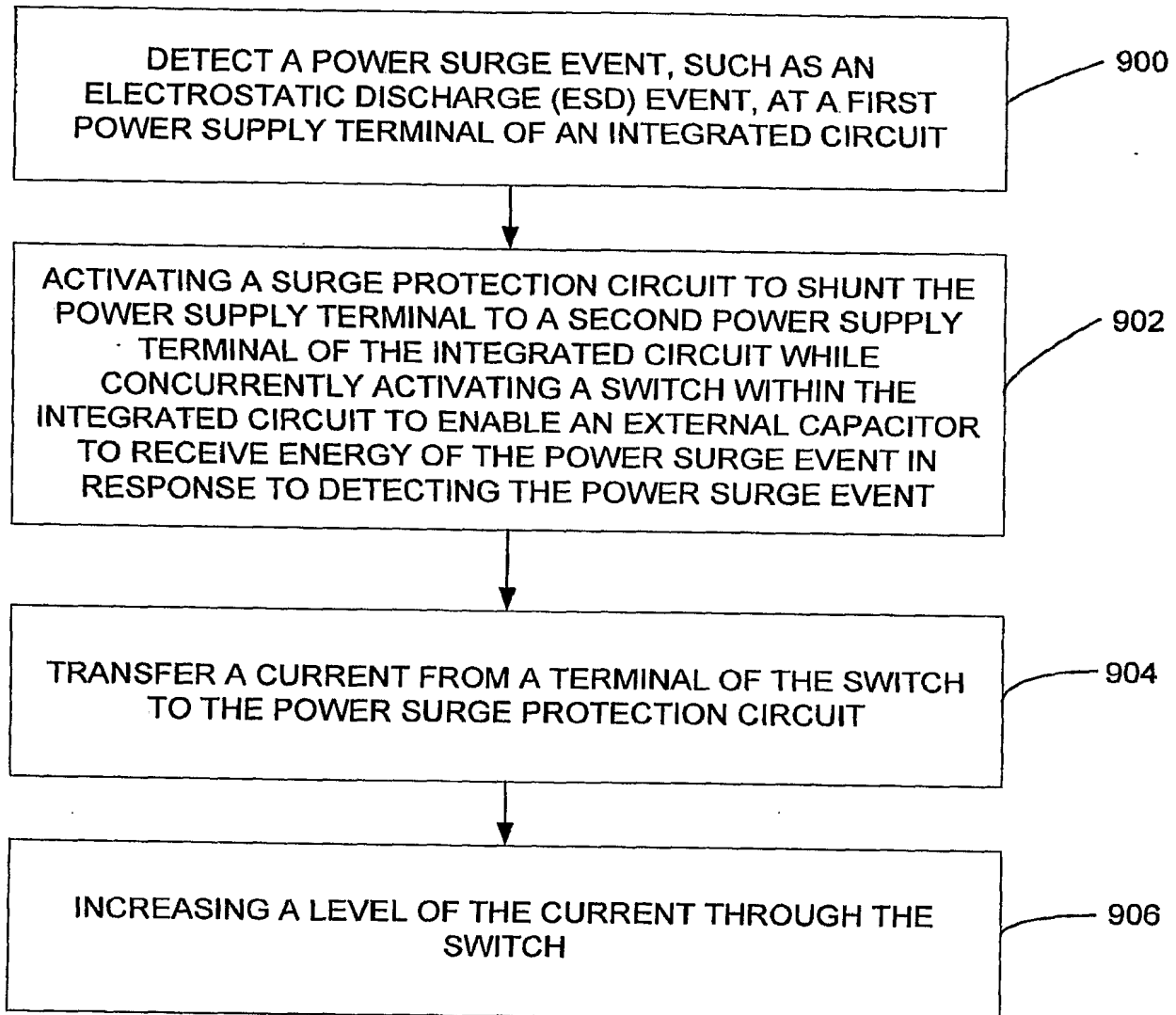


FIG. 8

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**FIG. 9**