

Oct. 9, 1962

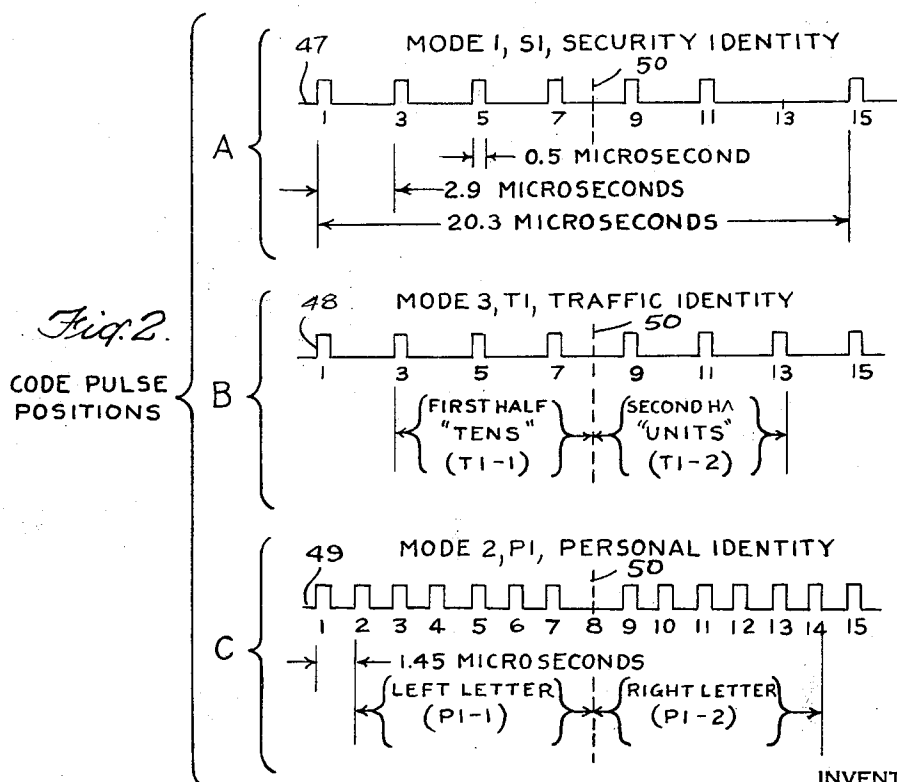
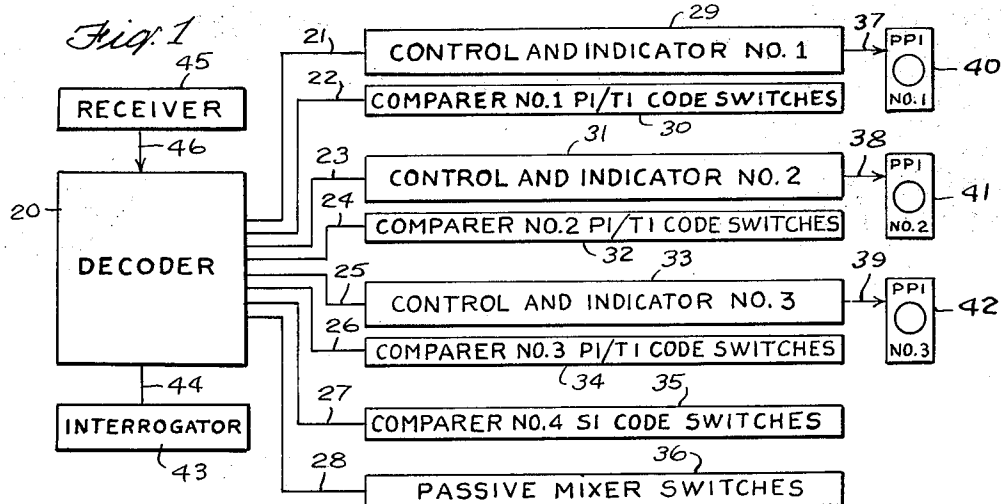
A. R. GARFINKEL ET AL

3,058,104

DECODER-INDICATOR

Filed Nov. 2, 1959

21 Sheets-Sheet 1



INVENTORS
ALAN R. GARFINKEL
NATHANIEL L. SIMS
BIAGIO A. SPINELLI

BY *Borst and Borst* ATTORNEYS

Oct. 9, 1962

A. R. GARFINKEL ETAL

3,058,104

DECODER-INDICATOR

Filed Nov. 2, 1959

78 79 BRACKET COINCIDENCE GATE

21 Sheets-Sheet 2

TO FIG. 17-1 664

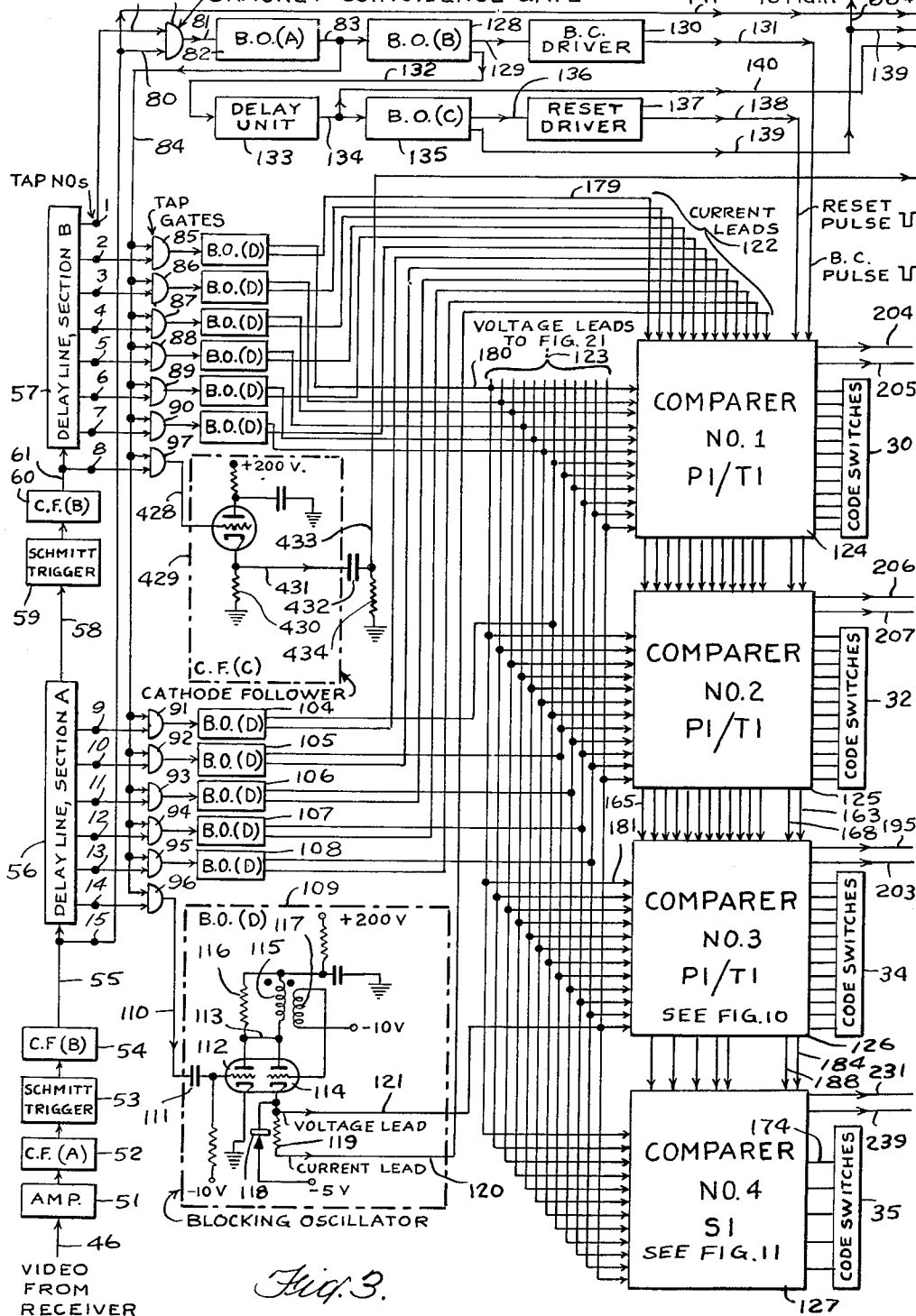
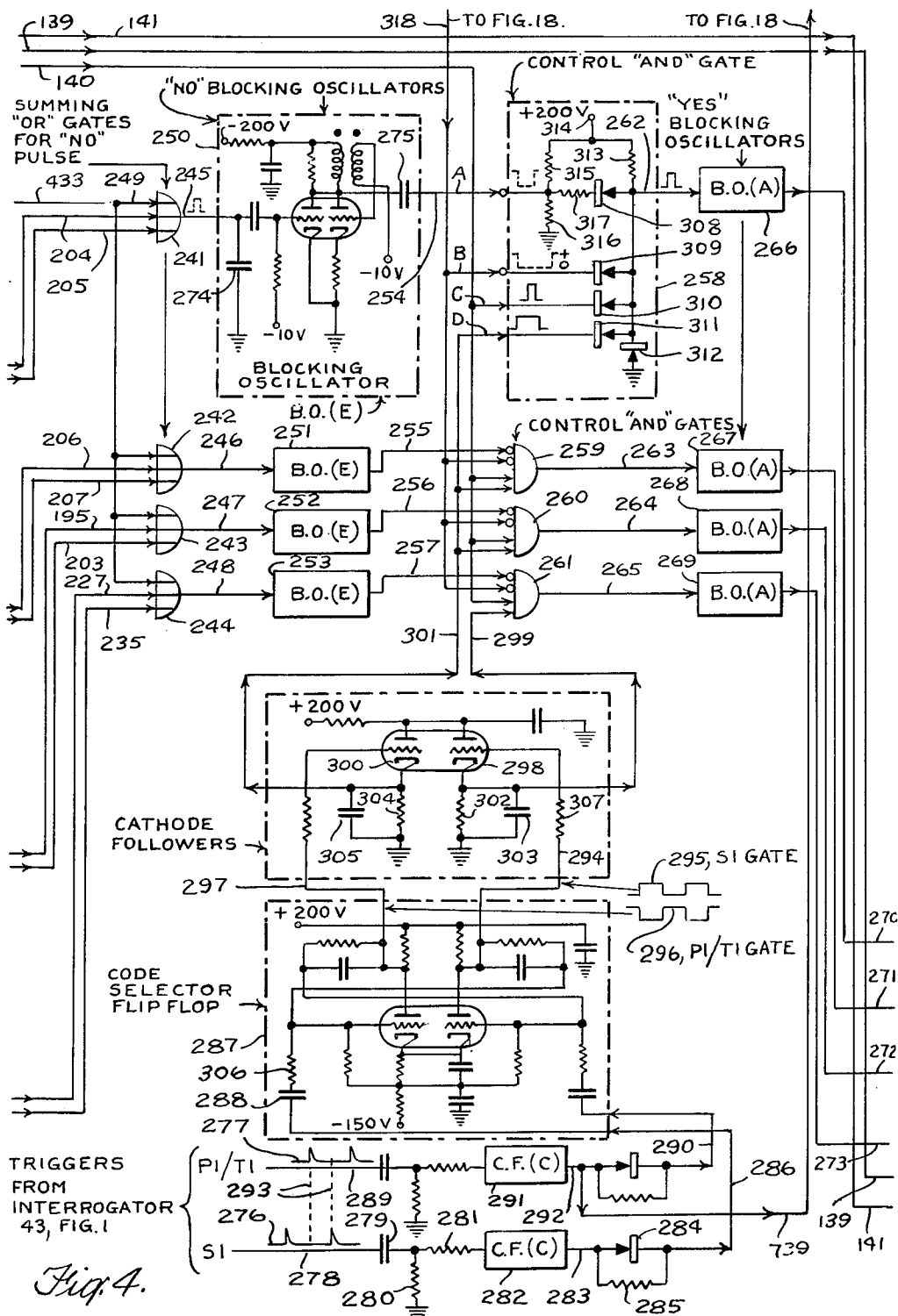


Fig. 3.

3,058,104

21 Sheets-Sheet 3



Oct. 9, 1962

A. R. GARFINKEL ETAL

3,058,104

DECODER-INDICATOR

Filed Nov. 2, 1959

21 Sheets-Sheet 4

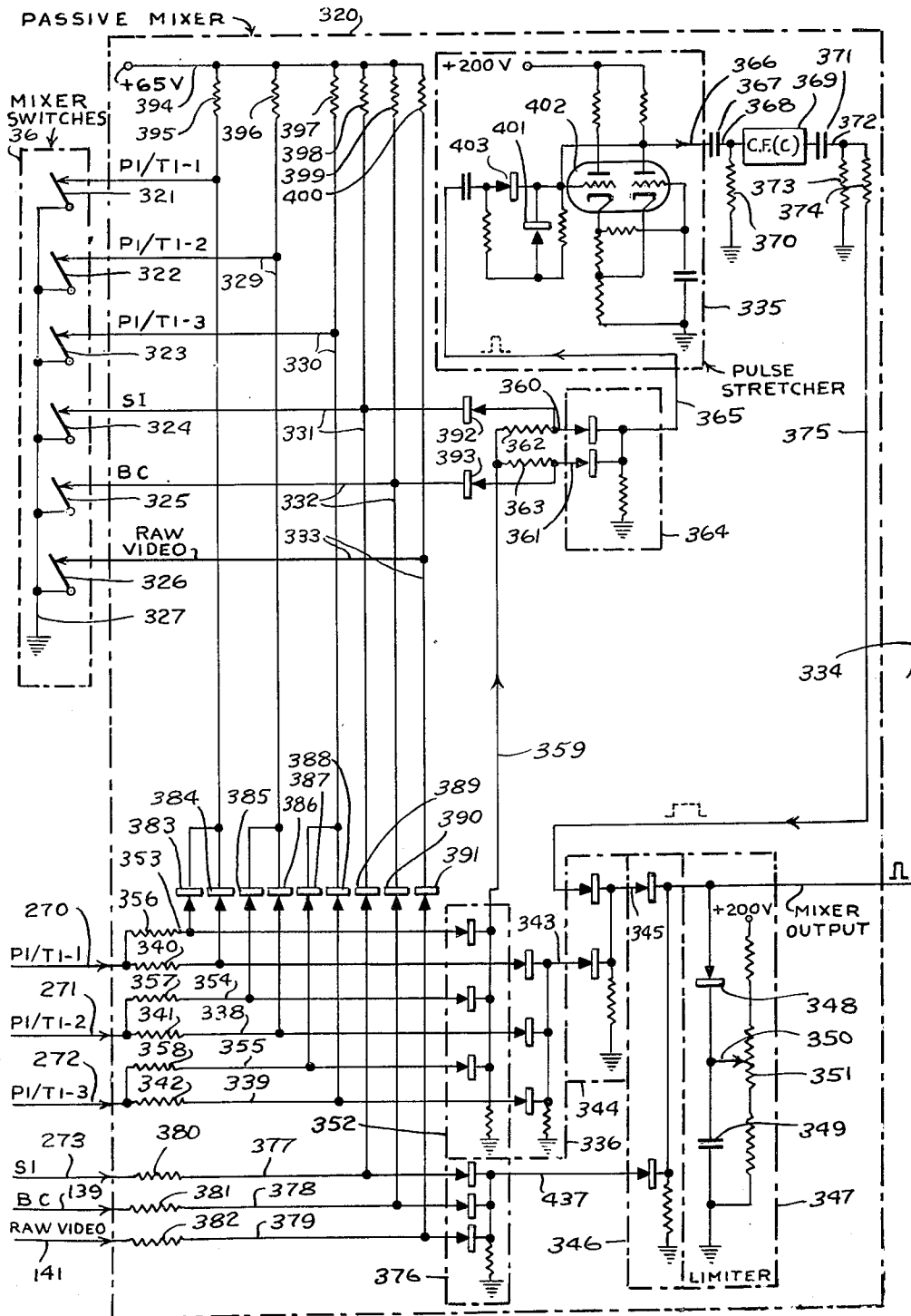


Fig. 5.

Oct. 9, 1962

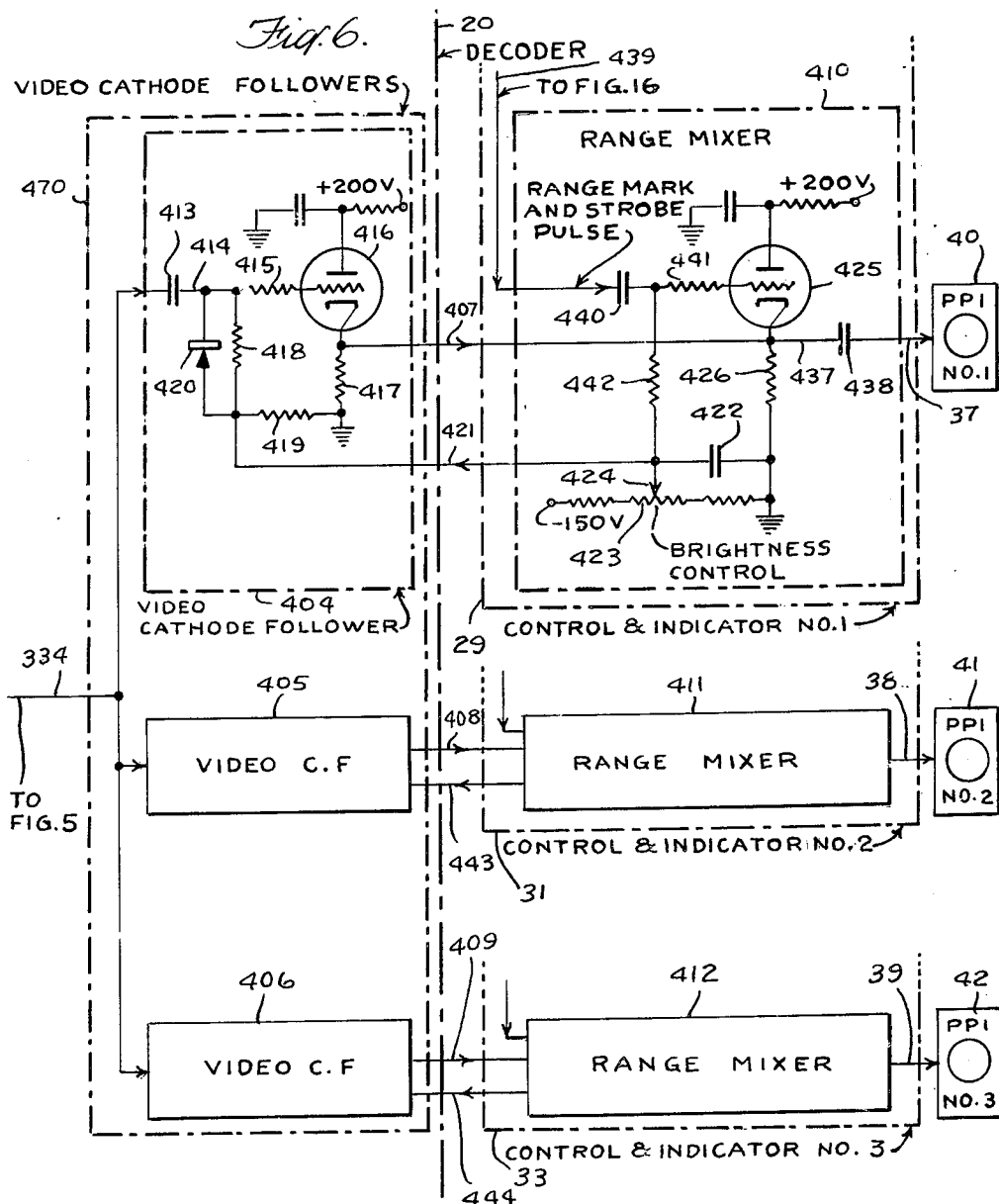
A. R. GARFINKEL ETAL

3,058,104

DECODER-INDICATOR

Filed Nov. 2, 1959

21 Sheets-Sheet 5



PASSIVE DECODING AND INDICATING SYSTEM.

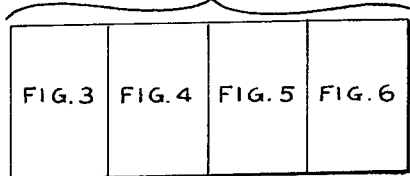


Fig. 7

INVENTORS
ALAN R. GARFINKEL
NATHANIEL L. SIMS
BIAGIO A. SPINELLI

BY *Borst and Borst*
ATTORNEYS

Oct. 9, 1962

A. R. GARFINKEL ET AL

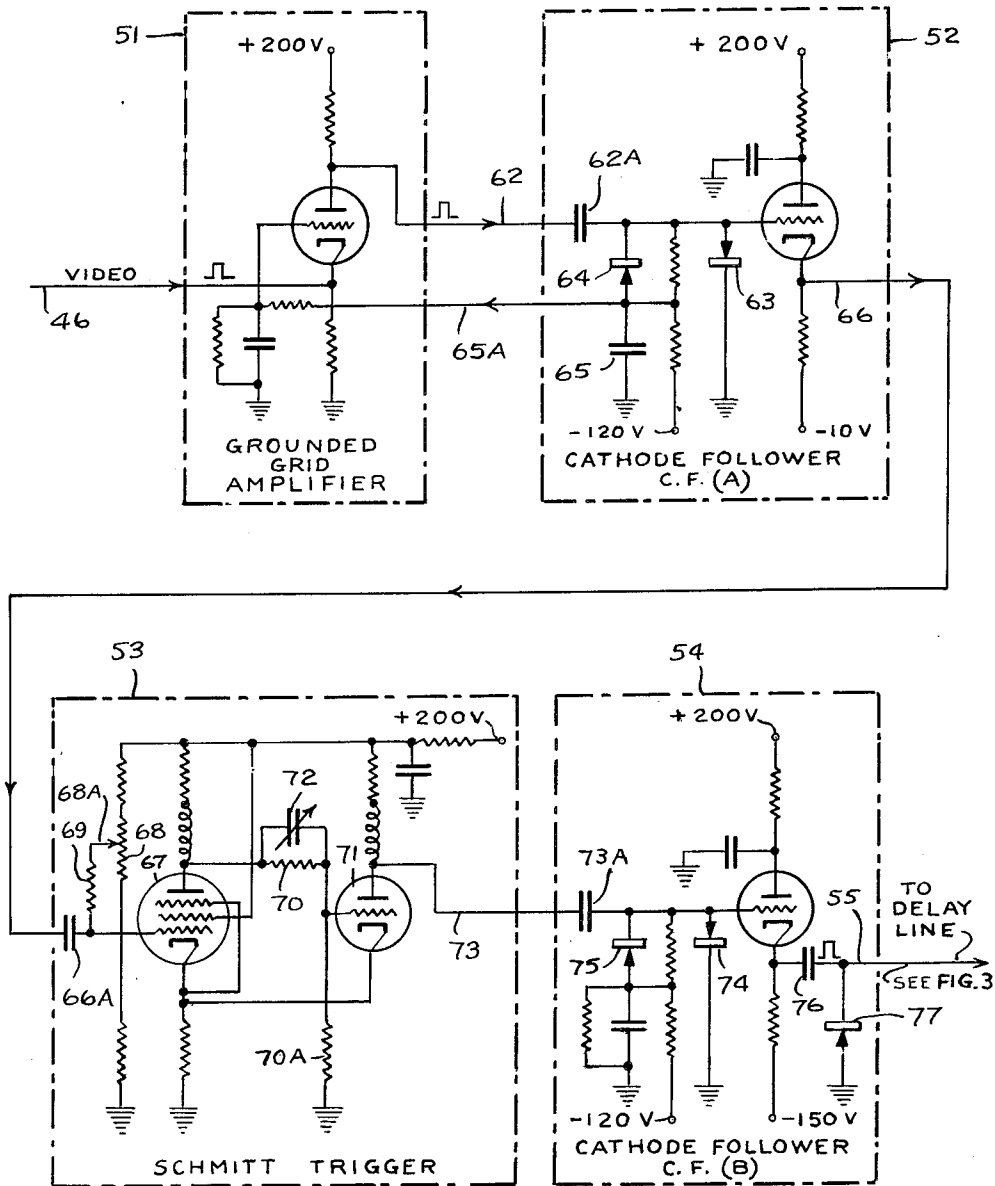
3,058,104

DECODER-INDICATOR

Filed Nov. 2, 1959

21 Sheets-Sheet 6

Fig. 8.



INVENTORS
ALAN R. GARFINKEL
NATHANIEL L. SIMS
BIAGIO A. SPINELLI
BY *Borset and Borset*
ATTORNEYS

Oct. 9, 1962

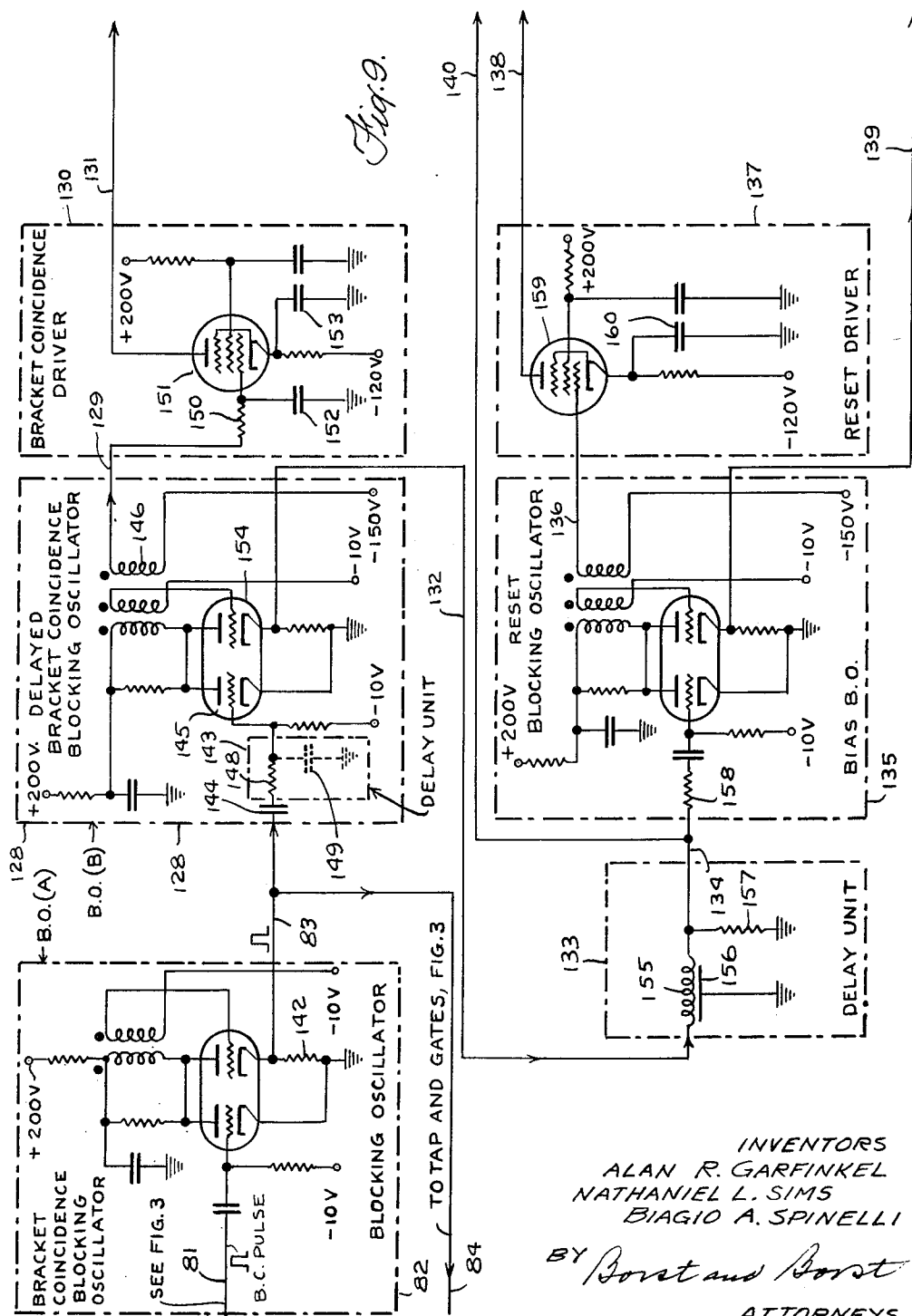
A. R. GARFINKEL ETAL

3,058,104

DECODER-INDICATOR

Filed Nov. 2, 1959

21 Sheets-Sheet 7



Oct. 9, 1962

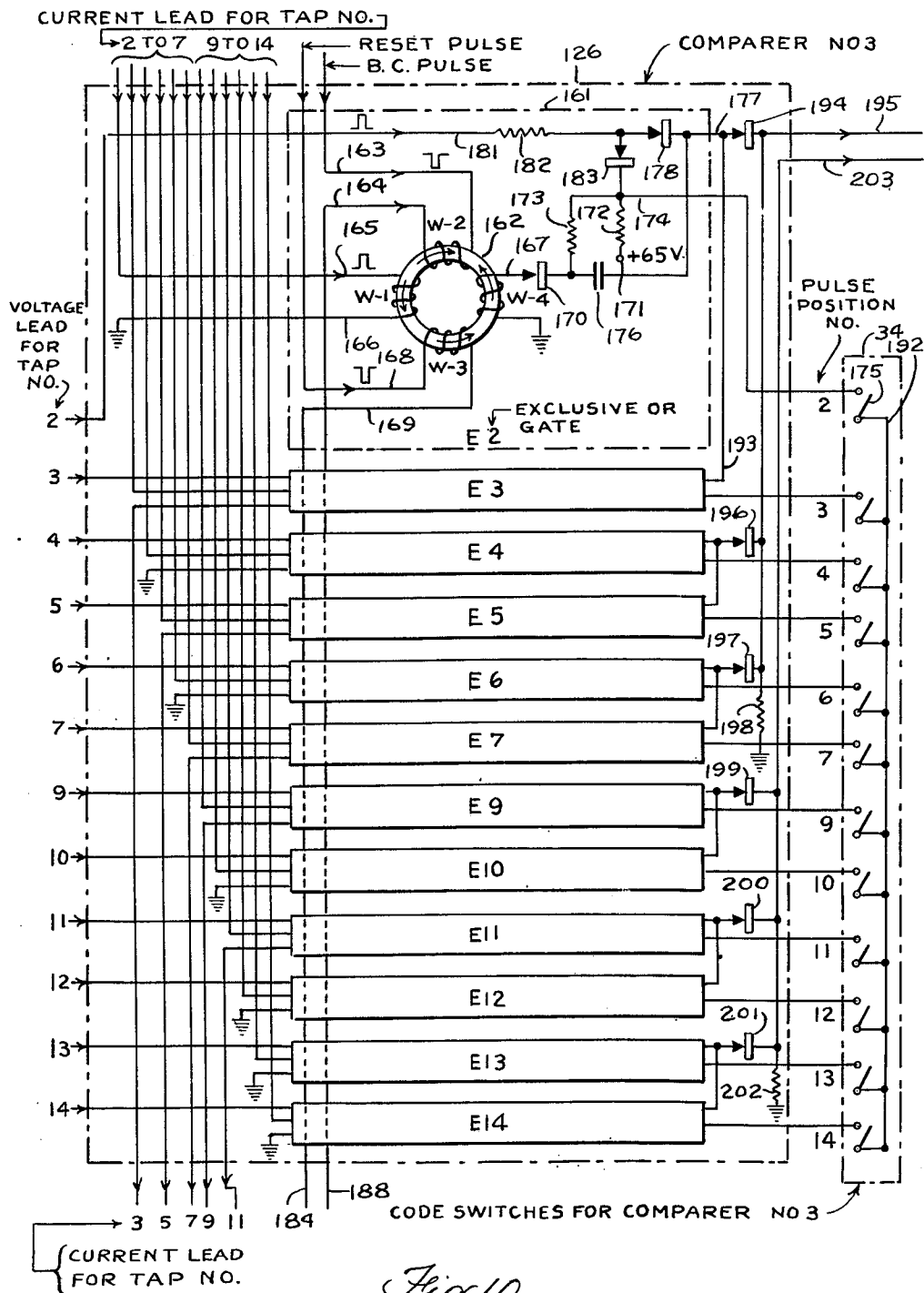
A. R. GARFINKEL ET AL

3,058,104

DECODER-INDICATOR

Filed Nov. 2, 1959

21 Sheets-Sheet 8



Oct. 9, 1962

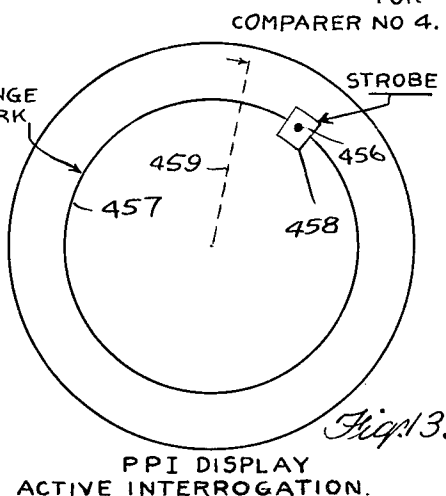
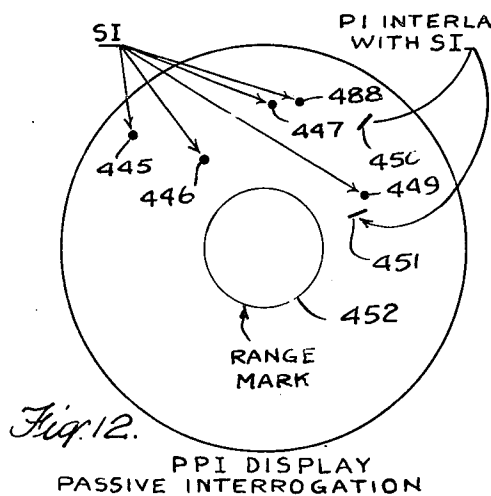
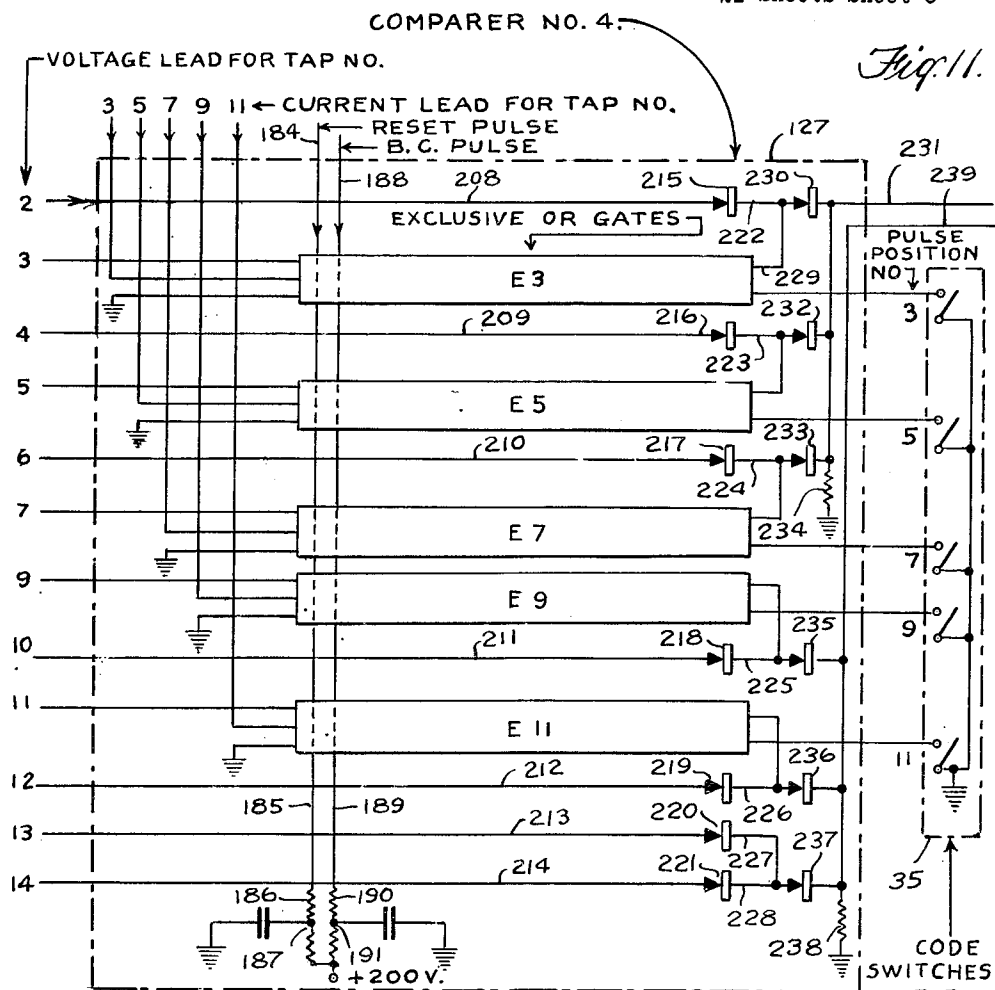
A. R. GARFINKEL ETAL

3,058,104

DECODER-INDICATOR

Filed Nov. 2, 1959

21 Sheets-Sheet 9



Oct. 9, 1962

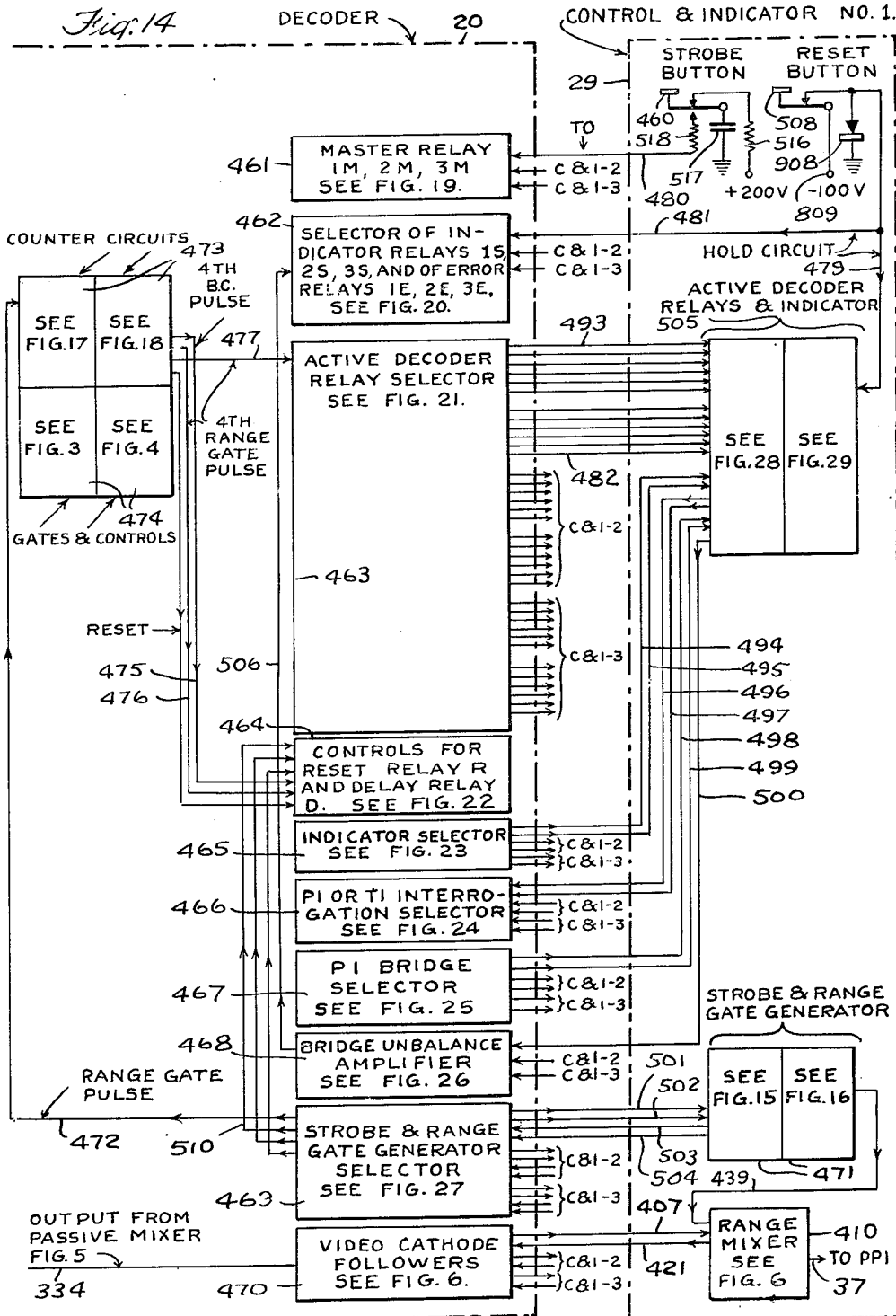
A. R. GARFINKEL ETAL

3,058,104

DECODER-INDICATOR

Filed Nov. 2, 1959

21 Sheets-Sheet 10



Oct. 9, 1962

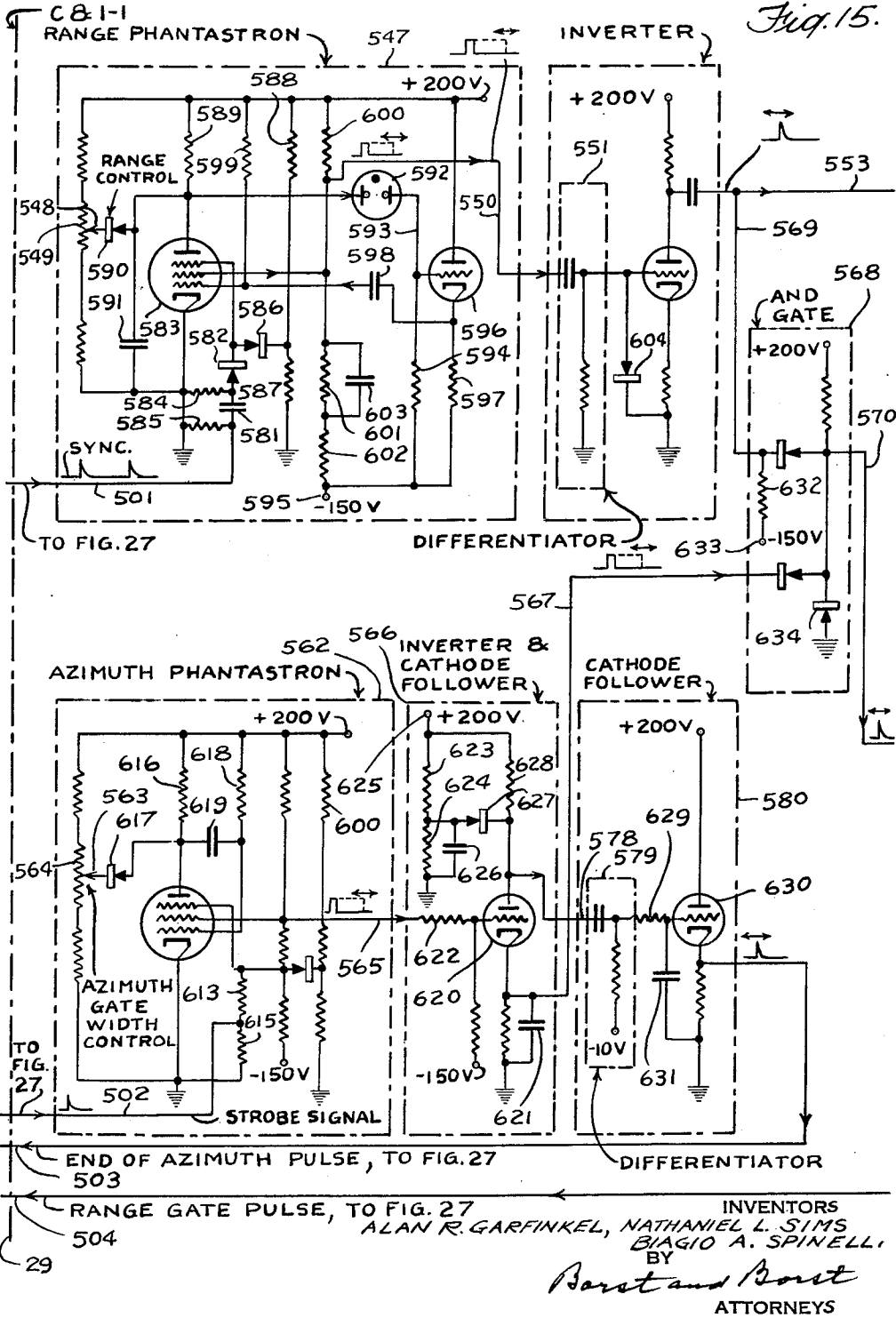
A. R. GARFINKEL ET AL

3,058,104

DECODER-INDICATOR

Filed Nov. 2, 1959

21 Sheets-Sheet 11



Oct. 9, 1962

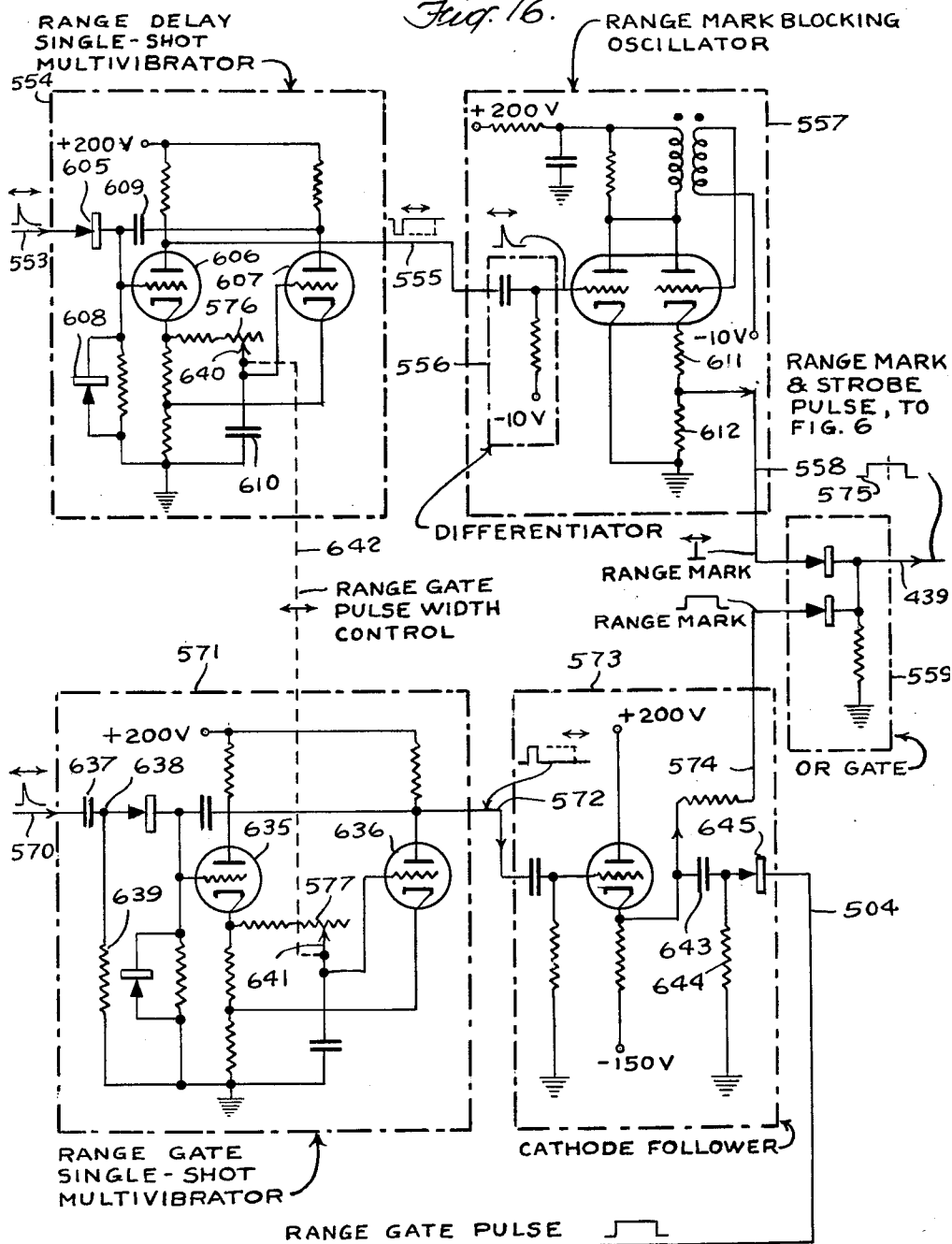
A. R. GARFINKEL ETAL

3,058,104

DECODER-INDICATOR

Filed Nov. 2, 1959

21 Sheets-Sheet 12



INVENTORS
ALAN R. GARFINKEL, NATHANIEL L. SIMS
BY
BIAGIO A. SPINELLI

Borst and Borst
ATTORNEYS

Oct. 9, 1962

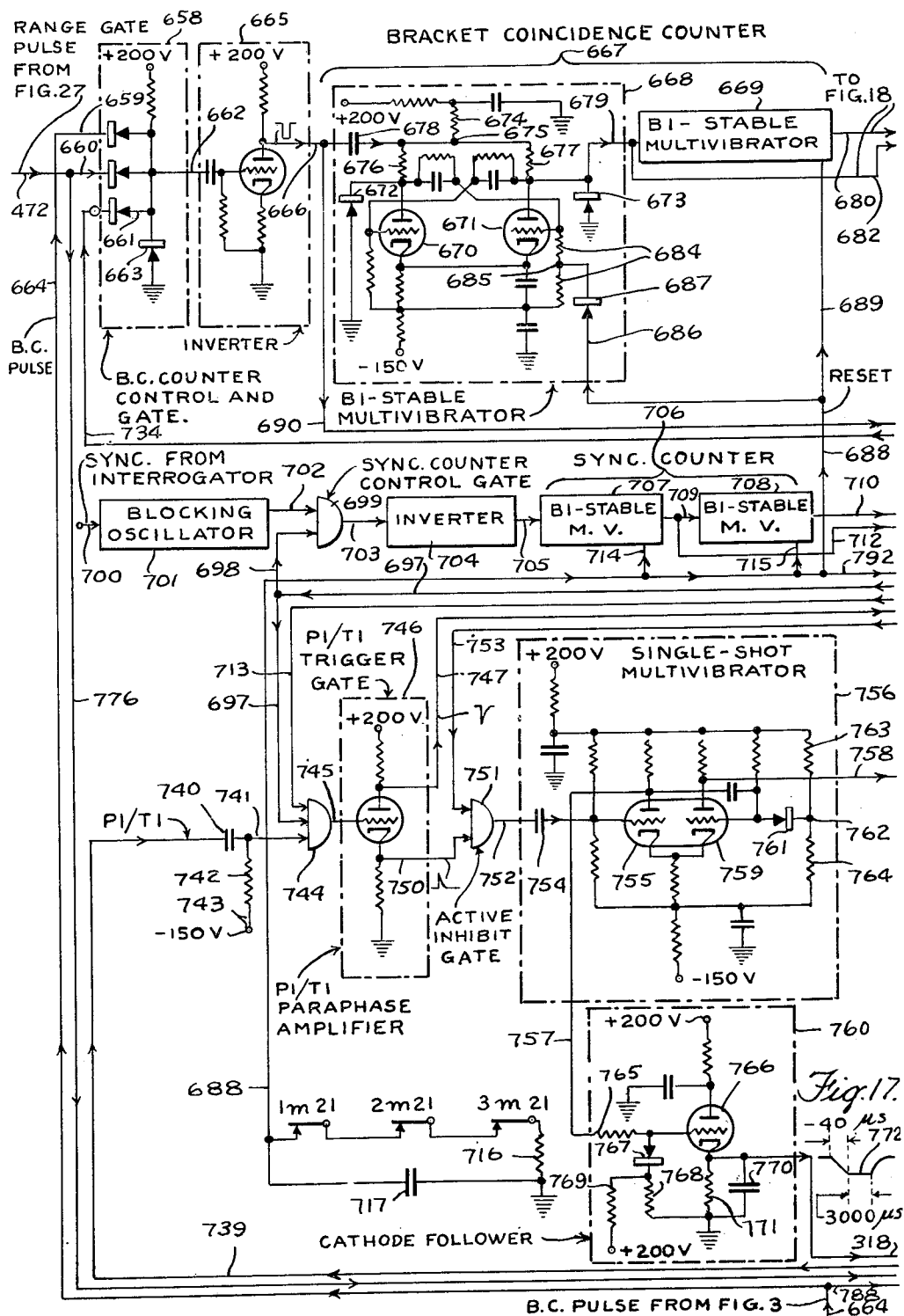
A. R. GARFINKEL ETAL

3,058,104

DECODER-INDICATOR

Filed Nov. 2, 1959

21 Sheets-Sheet 13



Oct. 9, 1962

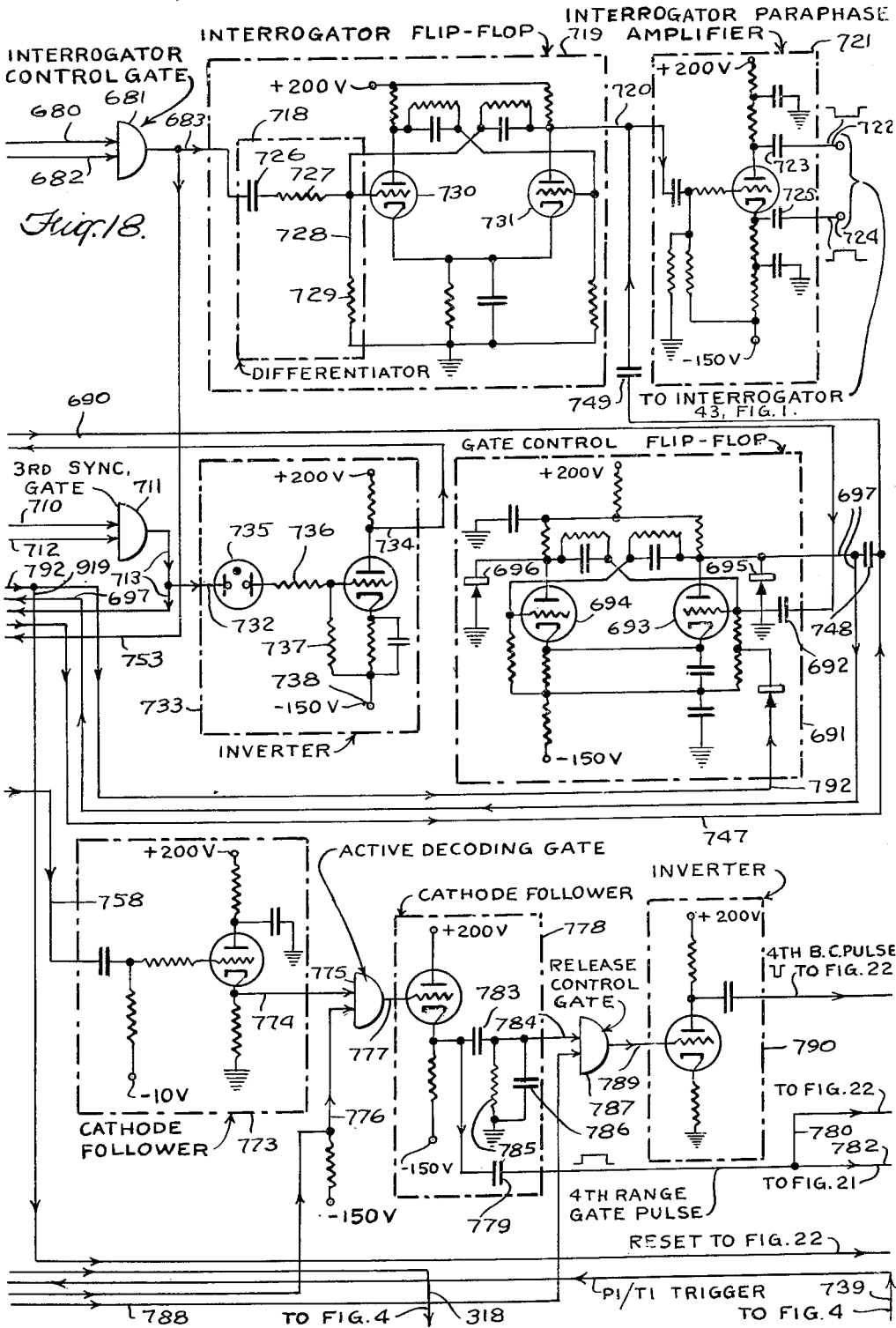
A. R. GARFINKEL ETAL

3,058,104

DECODER-INDICATOR

Filed Nov. 2, 1959

21 Sheets-Sheet 14



Oct. 9, 1962

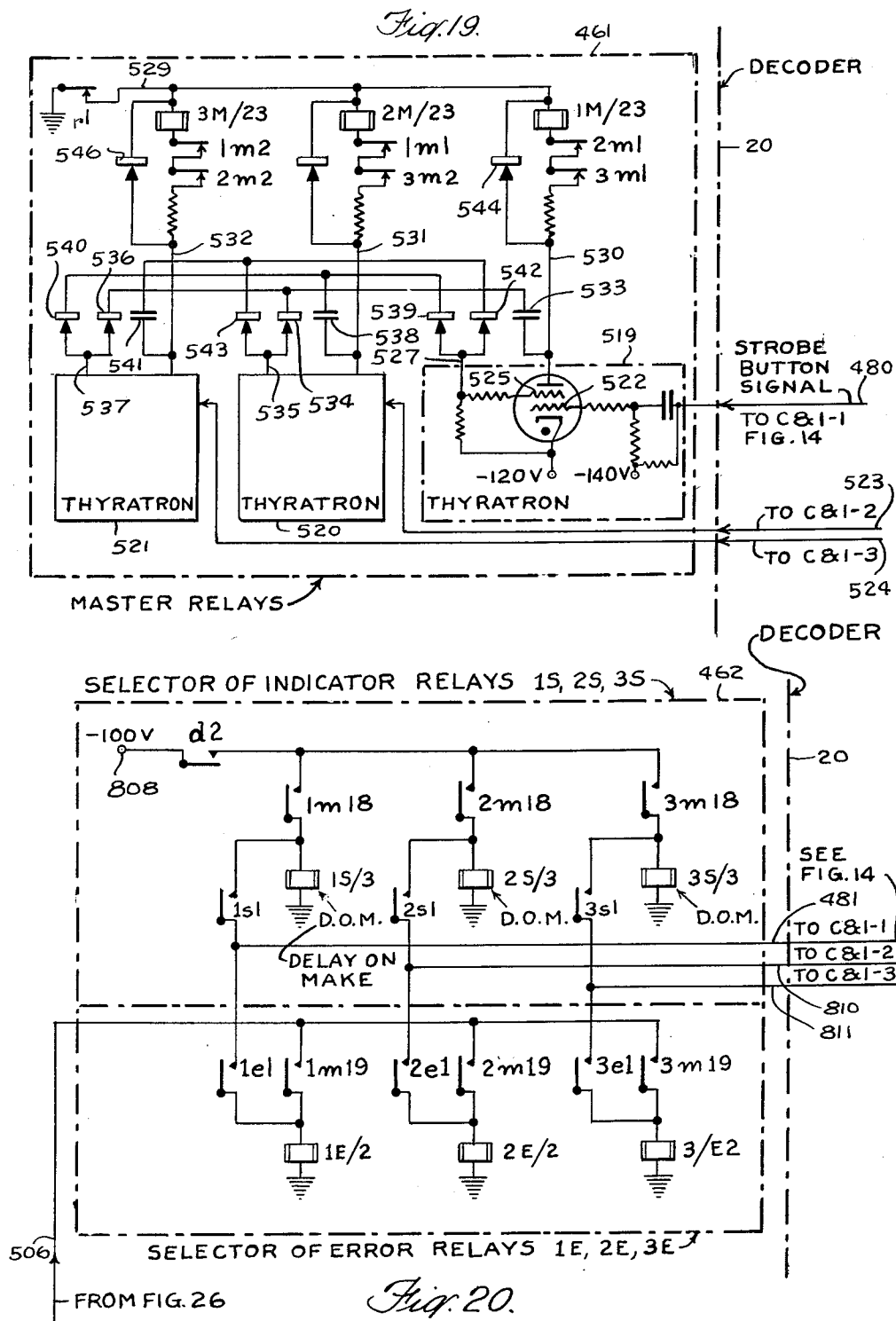
A. R. GARFINKEL ETAL

3,058,104

DECODER-INDICATOR

Filed Nov. 2, 1959

21 Sheets-Sheet 15



Oct. 9, 1962

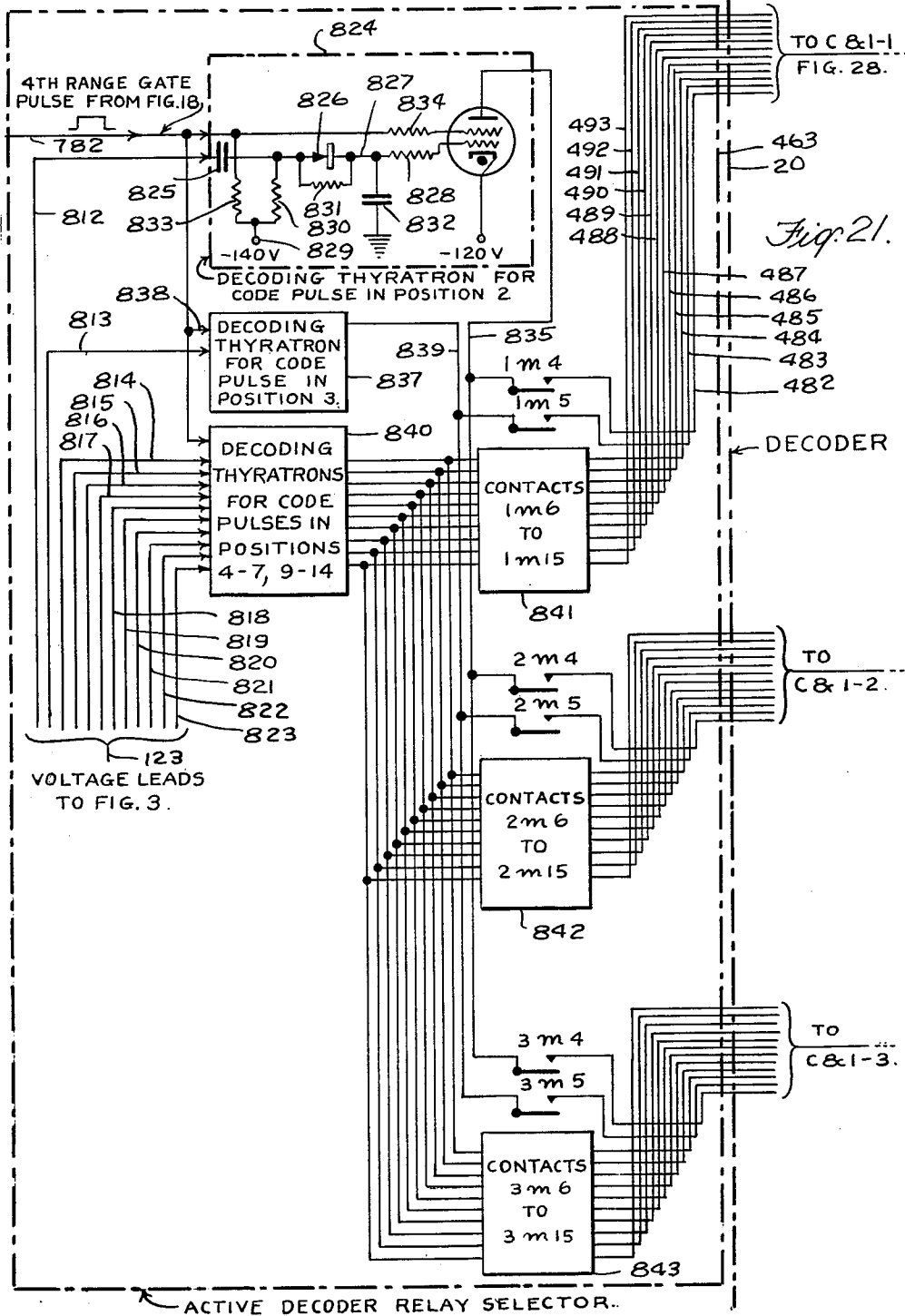
A. R. GARFINKEL ETAL

3,058,104

DECODER-INDICATOR

Filed Nov. 2, 1959

21 Sheets-Sheet 16



Oct. 9, 1962

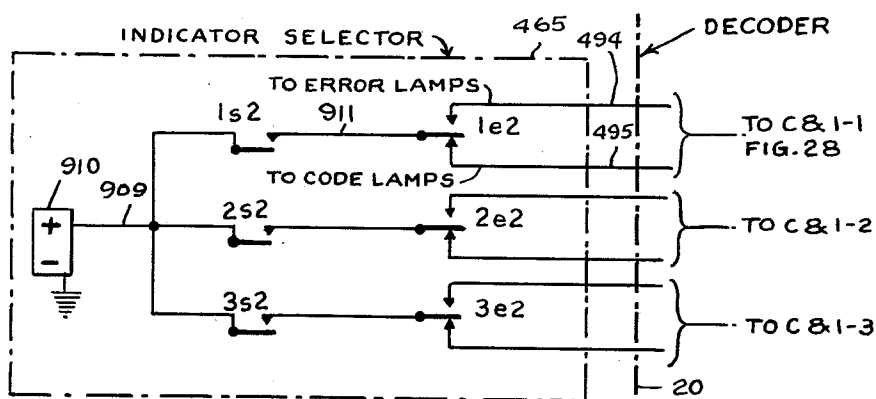
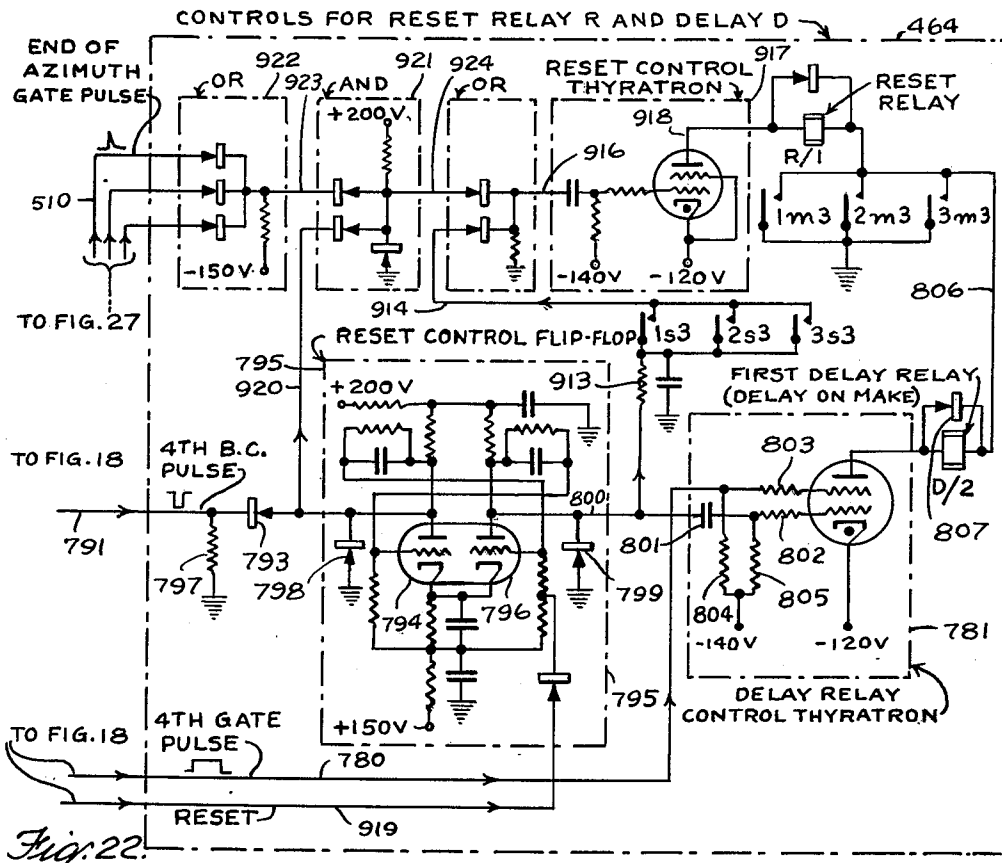
A. R. GARFINKEL ETAL

3,058,104

DECODER-INDICATOR

Filed Nov. 2, 1959

21 Sheets-Sheet 17



INVENTORS
ALAN R. GARFINKEL
NATHANIEL L. SIMS
BIAGIO A. SPINELLI

BY *Boerst and Boerst*
ATTORNEYS

Oct. 9, 1962

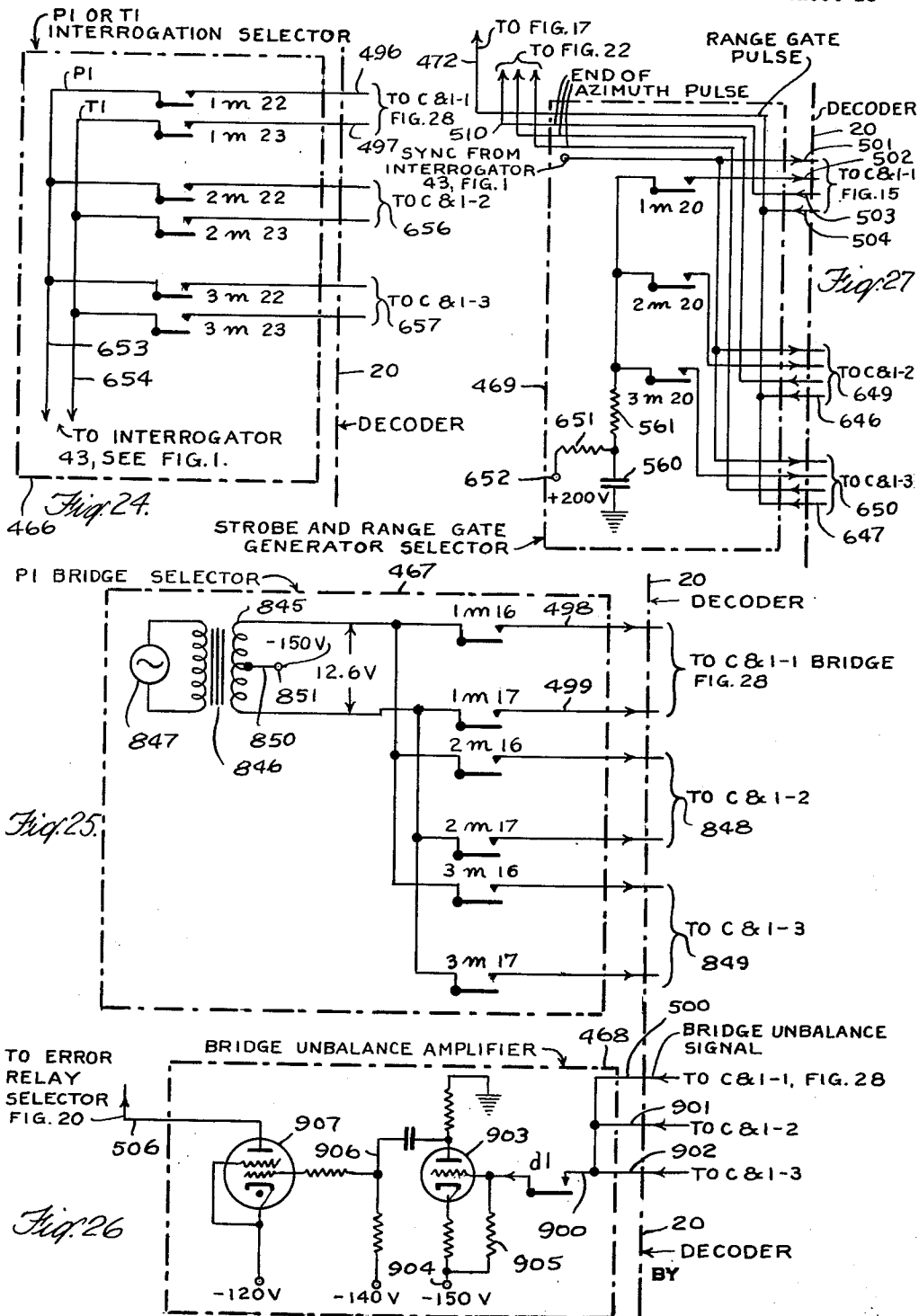
A. R. GARFINKEL ETAL

3,058,104

DECODER-INDICATOR

Filed Nov. 2, 1959

21 Sheets-Sheet 18



Oct. 9, 1962

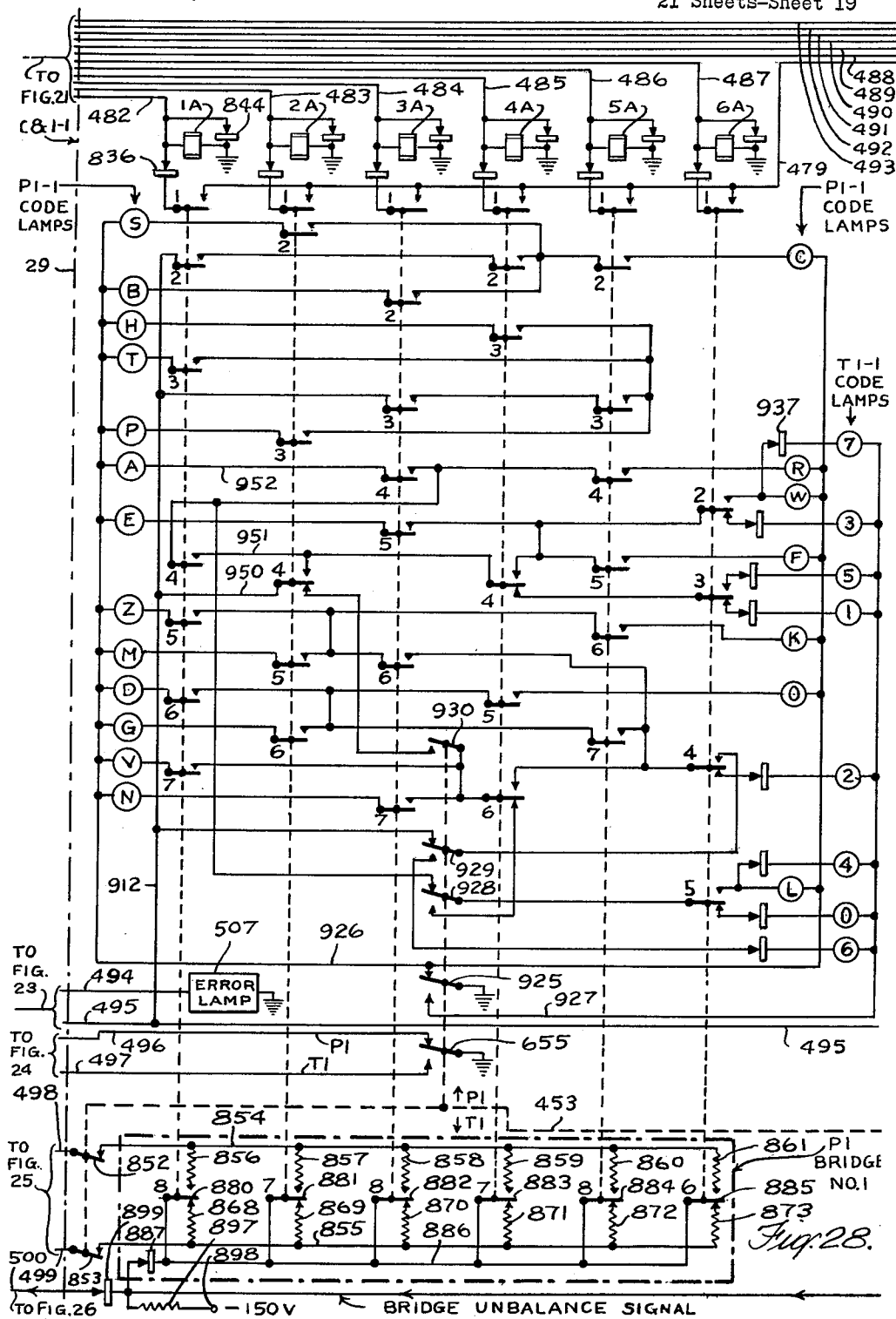
A. R. GARFINKEL ET AL

3,058,104

DECODER-INDICATOR

Filed Nov. 2, 1959

21 Sheets-Sheet 19



Oct. 9, 1962

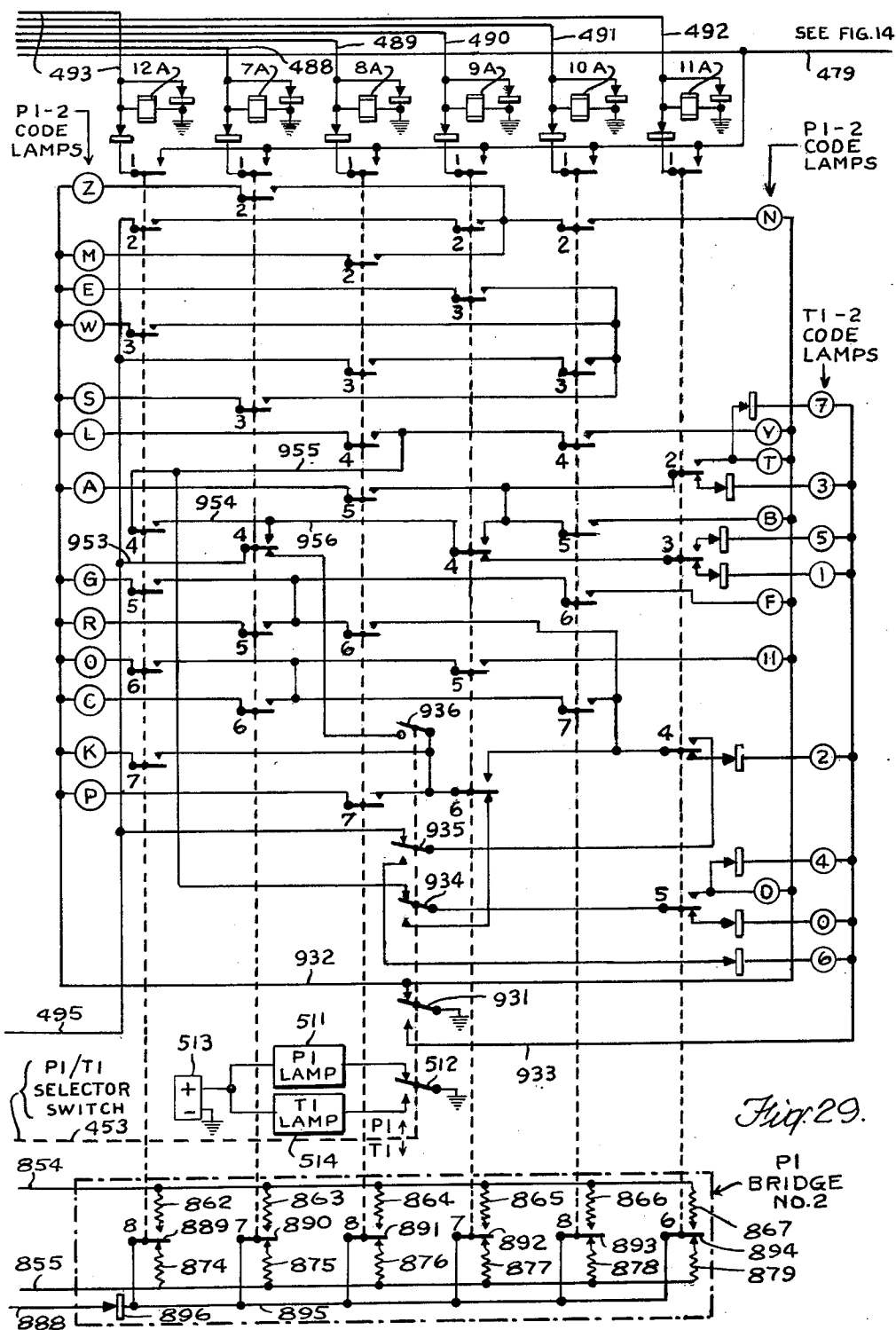
A. R. GARFINKEL ETAL

3,058,104

DECODER-INDICATOR

Filed Nov. 2, 1959

21 Sheets-Sheet 20



Oct. 9, 1962

A. R. GARFINKEL ETAL

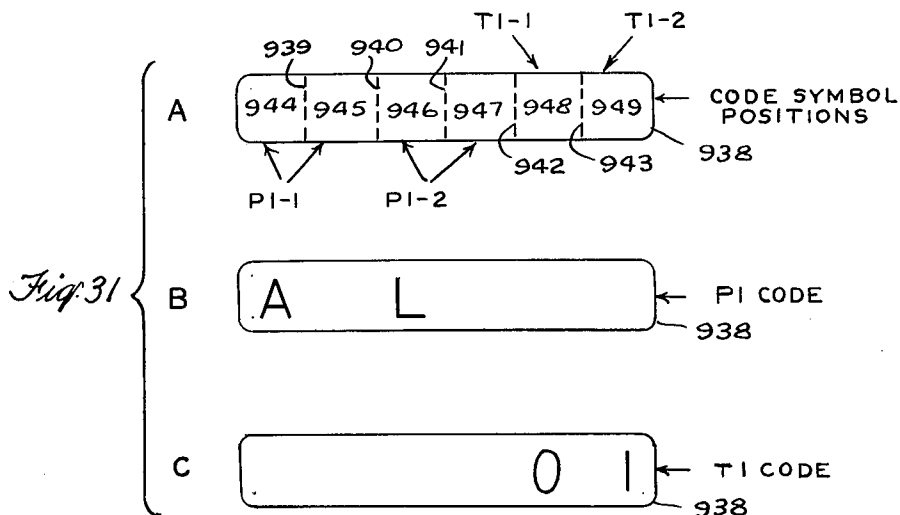
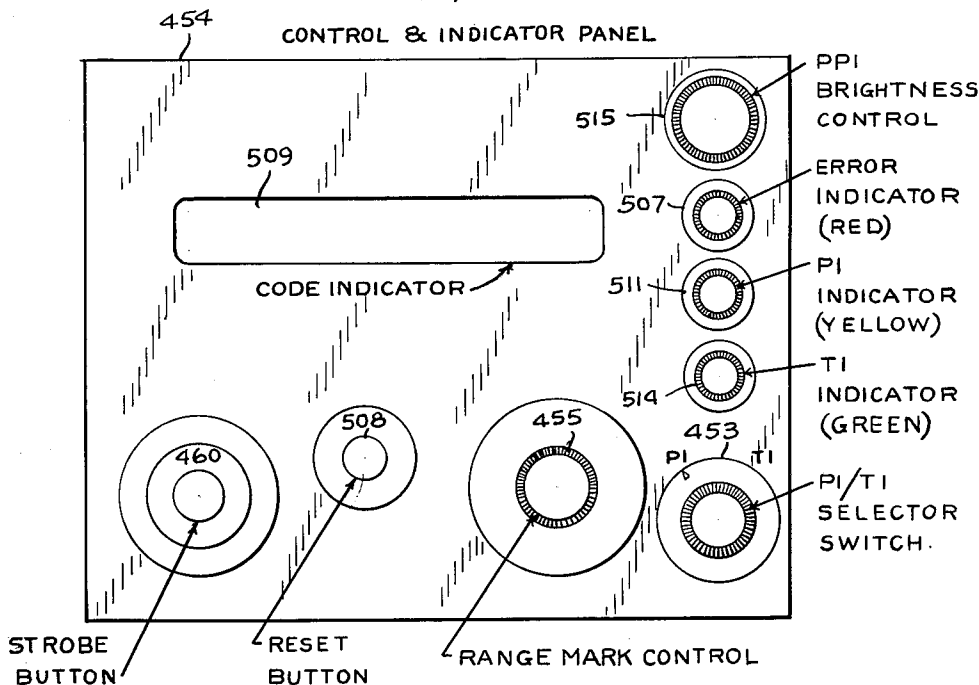
3,058,104

DECODER-INDICATOR

Filed Nov. 2, 1959

21 Sheets-Sheet 21

Fig. 30.



INVENTORS
ALAN R. GARFINKEL
NATHANIEL L. SIMS
BIAGIO A. SPINELLI

BY *Borst and Borst*
ATTORNEYS

1

3,058,104

DECODER-INDICATOR

Alan R. Garfinkel, Forest Hills, and Nathaniel L. Sims and Biagio A. Spinelli, Brooklyn, N.Y., assignors to Sperry Rand Corporation, Ford Instrument Company Division, Wilmington, Del., a corporation of Delaware
Filed Nov. 2, 1959, Ser. No. 851,215
28 Claims. (Cl. 343-6.5)

This invention relates to systems for the selective identification of an aircraft or other object by an interrogating signal station, and more particularly relates to means in a radar interrogating station for decoding reply pulses received from an interrogated aircraft, for utilizing the decoded pulses to indicate the identity and location of the aircraft, and for coordinating certain interrogating operations with the decoding operations.

Reference is made to volume 1 of the Radiation Laboratory Series, published by McGraw-Hill Book Company, New York, for certain of the general features of radar type interrogating systems and to the other volumes of the Series for certain related details of such systems.

Heretofore, decoding and indicating equipment for the purpose of accomplishing some of the objectives of the present invention, has been subject to various difficulties, including being undesirably limited in the ability to verify the identity of an interrogated aircraft, undesirably complicated, undesirably hampered by mechanical relays and slow in operation, subject to unreliable and erratic performance, and undesirably inconvenient and costly to construct, operate, and maintain.

An object of the present invention is to overcome one or more of the difficulties referred to, and to improve the construction, operation, convenience, and economy of such systems.

Another object is to improve the processing of a coded train of signal pulses received from an aircraft or other object in response to an interrogation and to verify the identification code of the object and indicate the position of the object on a PPI display.

Another object is to initiate an interrogation of the identity of a particular aircraft or other object represented by a blip in any selected position in a PPI display, and automatically to indicate the identification code of the object in response to the reply.

Another object is to provide an improved indication of whether an aircraft is a friend or a foe.

Another object is to provide an improved decoder and indicator which utilizes only electronic components and does not require any mechanically moving relays, or the like, and which is capable of rapidly indicating and following the changing position of an aircraft having a selected identification code, while being able to suppress the indication of aircraft not having the selected identification code.

Another object is to indicate in a PPI display the position of an aircraft having an identification code in one mode, interlaced with the indication of an identification code in another mode.

Another object is to produce a distinctive PPI blip to represent the position of an aircraft having a single identification code selected by the PPI operator and to produce a PPI blip, distinguished in appearance from the first mentioned blip, to represent the position of an aircraft having more than one identification code selected by the operator, where each of the selected codes is in a respectively different mode.

Another object is to provide efficient means for comparing the positions of pulses in a received coded train of pulses with the pulse positions in a verification code set up by the operator before making the interrogation.

Another object is automatically to test the pulse posi-

2

tions in a coded train of reply pulses, for conformity with the pulse positions in a verification code selected by the interrogation operator, to produce an indication, if the pulses pass the test, and to prevent the indication of conformity, if they fail the test.

Another object is automatically to subject each coded train of reply pulses to two successive tests of the correctness of the presence or absence of a pulse in certain of the pulse positions in the train, the pulse positions tested in one of the tests being different from those in the other, and indicating whether the train passes the tests.

Another object is automatically to indicate at high speed, the identification code, if any, assigned to an aircraft or other object represented by a blip within a PPI strobe set up by the operator the strobe having a position in the PPI display selectable by the operator, and automatically preventing the operation of the code indicating equipment in response to any object represented by a PPI blip outside the strobe area.

Another object is to simplify the construction and reduce the cost of a decoding and indicating system in a radar interrogating station having several PPI operator positions, each having a different PPI display unit, by centralizing certain parts of the system to avoid duplication of parts for each operator, so that any one of the operators initiating an interrogation, causes the centralized parts of the system automatically to select the proper connections with his individual control equipment, while excluding interference with his interrogation cycle by any of the other operators, the centralized parts being so constructed and arranged as to quickly and automatically release the system for the use of the other operators as soon as his interrogating cycle is completed.

Another object is to subject a series of coded interrogation replies to a sequence test before permitting such a coded reply to be fully decoded, and to reject the decoding of such a reply, if the series of replies fails to meet the sequence test.

In accordance with the present invention, either of two forms of operation may be employed, one passive and the other active.

The passive operation automatically indicates by a blip in a PPI display at the interrogating station, the position of a friendly aircraft that has the same identification code as a verification code set up by switches by the PPI operator, before the interrogation. One or more aircraft having the same code as the switch code may be indicated in the same PPI display.

The active operation indicates by a symbol display the identification code of a particular aircraft in response to the operator's selection of the PPI blip representing the aircraft which he wishes to interrogate.

The passive operation is so named, because after a code has once been set up by the operator to verify a reply code, and the interrogation proceeds, the same interrogating operation continues automatically to be repeated to produce new indications as the positions of the replying aircraft change, without requiring any further action by the PPI operator.

The active operation is distinguished from the passive in that the operator must act by at least operating a switch each time he interrogates. The active operation has an important time saving advantage over the passive operation when time may be vital, because it makes possible a substantially instantaneous indication of the individual identification code of a friendly aircraft without requiring the operator to set up one or more trial codes, as in the passive operation, before finding the one which verifies the code of the aircraft.

In the form of the invention described herein for the purpose of illustration, three different code systems may

be employed, thus making possible three different modes of identification, Mode 1 being for Security Identity, abbreviated SI; Mode 2 for personal identity, PI; and Mode 3 for Traffic Identity, TI. The passive operation may identify a code in any one of the three modes. The active operation may identify a code in only the PI and TI modes.

In either passive or active operation, a coded train of code bits represented by pulses and absence of pulses, is received from an aircraft in response to an interrogation as to its identity, and is applied to a tapped delay line to change the train from a succession of bits, to a simultaneous group of bits derived from the taps. If the pulses in the train are of proper duration and spacing, and the train passes a test for proper length, the pulses at the first and last taps combine as bracket pulses to produce a bracket coincidence pulse which enables a separate tap gate for each of the intervening bit positions, each tap gate being in a separate channel for decoding or otherwise checking the bit therein.

In a passive interrogation, certain of the reply code bits received from the interrogated aircraft, are then automatically checked in a comparer for conformity with a verification code previously set up by a group of code switches. If the received code agrees with the verification code and there are no inhibitions for other reasons, a delayed bracket coincidence pulse fires a "Yes" blocking oscillator, which in turn may transmit a pulse to a PPI display, to indicate the position of the aircraft and to indicate that the identification code of the aircraft is the same as the verification code set up in the switches. If the codes disagree, or if a pulse should be present on the mid-tap of the delay line, a "No" blocking oscillator is fired and produces an inhibiting pulse which prevents the firing of the "Yes" blocking oscillator. Only aircraft whose identity is verified by a valid reply code can therefore produce a PPI display.

An active interrogation may be made by any one of several PPI operators. Since an active interrogation may be made in either the PI or the TI mode, the operator's first step is to check the PI/TI mode selecting switch on his control and indicator panel to see that it is in position to select the desired mode. The second step is to make a range selection of the PPI blip representing the aircraft to be actively interrogated, by adjusting the range mark control on the operator's control and indicator panel so that the PPI range mark circle is in line with the blip. The third step is to make an azimuth selection of the blip by watching the radar sweep line on the PPI and pressing the strobe button on the control and indicator panel just before the sweep line comes to the blip. The active operation cycle then becomes entirely automatic.

The other PPI operators are excluded from control of the active circuits by their strobe buttons until the cycle of the first started active operation is completed. Since the whole cycle of an active operation is completed in about two tenths of a second, the other operators have access to the active circuits with no substantial delay.

The pressing of the strobe button causes the operator's strobe and range gate generator to generate a series of range gate and strobe pulses. The strobe pulses immediately produce a square area of intensified light, called a strobe, surrounding the selected blip. The strobe informs the operator that he has seized active control and has not been prevented by an earlier started uncompleted interrogation of another operator. The strobe also shows the operator the area from which a reply will be accepted in response to the active interrogation, because the active decoding circuits are so gated that they will accept pulses during only those portions of the PPI scan included within the strobe. No aircraft outside the area represented by the strobe, can therefore produce an active code indication.

The range gate pulses control certain gatings of bracket coincidence and other pulses in the decoder for deter-

mining the time of transmission of the active interrogation to the aircraft in relation to the operation of the active decoding equipment. The transmission of the active interrogation to the aircraft is initiated in response to the electronic count of three regularly timed successive bracket coincidence pulses derived from successive reply trains received from the aircraft in response to corresponding passive interrogations following actuation of the strobe button. These bracket coincidence pulses must be in regular sequence in order to be counted and in order to initiate an active interrogation.

When the active interrogation takes place, and the reply train in response thereto is received by the decoder and properly meets the tests for such a reply, the active circuits in the decoder transmit signals to the operator's control and indicator unit to energize the proper active decoding relays therein. The decoding relays translate the received reply into the corresponding PI or TI identification code of the aircraft. This code is then displayed as symbols by a code indicator on the control and indicator panel.

When an active interrogation is made in the PI mode, a special bridge circuit checks the structure of each half of the reply train located on each side of and apart from the mid-tap bit and between the bracket pulses, to see that the number of pulses in each half equals the number of pulses omitted from that half, and in case of any unbalance in either half, the circuit finds the reply code to be invalid and no code is indicated, but an error signal lamp is lighted.

The active circuits, except for those of the decoding relays and the code and error indicators, are automatically restored to normal within about two tenths of a second after the strobe button is depressed by the first operator, and thus become available to the other operators. The active decoding relays and the code or error indicator of the interrogating operator, remain operated to provide adequate time for observing them. Each operator has a reset button for restoring to normal his active decoding relays, and his active code or error indicator circuits.

These and other objects and features of the invention will be more readily apparent from the following detailed description, the appended claims, and the accompanying drawings, in which:

FIG. 1 is a block diagram showing a decoder, associated switches, and three control and indicator units, in relation to a receiver, an interrogator, and three PPI display units, to illustrate one example of how the present invention may be employed;

FIG. 2 is a diagram showing at A, B and C, the pulse positions in a coded reply train in three different modes, SI, PI and TI, respectively;

FIG. 3 is a schematic diagram showing input and code checking circuits in the decoder employed in part for passive operation and in part for active operation;

FIG. 4 is a schematic diagram of the gating and control circuits in the decoder for processing signals derived from FIG. 3 during passive operation;

FIG. 5 is a schematic diagram showing the passive mixer circuits in the decoder for selecting pulses derived from the circuits of FIG. 4, which are to be fed to display circuits;

FIG. 6 is a schematic diagram showing the circuits fed by pulses from the circuits of FIGS. 5 and 16, for producing PPI displays during passive and active operations;

FIG. 7 is a block diagram showing how FIGS 3 to 6, may be fitted together to provide the complete schematic circuits of the passive decoding and indicating system;

FIG. 8 is a schematic diagram of the circuits in FIG. 3 for transmitting video signal pulses from the receiver to Section A of the delay line;

FIG. 9 is a schematic diagram of the circuits in FIG. 3 for transmitting signal pulses from the bracket coincidence gate through the B.C. driver and the reset driver;

FIGS. 10 and 11 are schematic diagrams of the circuits within comparers No. 3 and No. 4, respectively, in FIG. 3;

FIGS. 12 and 13 are diagrams showing PPI displays obtained while making passive and active interrogations, respectively;

FIG. 14 is a block diagram showing the relation of circuits within the decoder to circuits within the control and indicator units, particularly in connection with active operation;

FIGS. 15 and 16, which may be fitted together as shown in FIG. 14, are schematic circuit diagrams of the strobe and range gate pulse generator utilized during active operation;

FIGS. 17 and 18, which may be fitted together as shown in FIG. 14, are schematic diagrams of the bracket coincidence pulse counter circuits and related circuits utilized during active operation;

FIG. 19 is a schematic diagram of the active circuits within the decoder for operating the master relays;

FIG. 20 is a schematic diagram of selector circuits in the decoder for selecting the indicator relay and error relay corresponding to the control and indicator unit within which an active interrogation originates;

FIG. 21 is a schematic diagram of selector circuits in the decoder for selecting the group of active decoder relays in the control and indicator unit within which an active interrogation originates;

FIG. 22 is a schematic diagram of control circuits in the decoder for controlling the operation of the reset relay and the first delay relay during active interrogation;

FIG. 23 is a schematic diagram showing selector circuits in the decoder for selecting the code or error indicator circuits in the control and indicator unit within which an active interrogation originates;

FIG. 24 is a schematic diagram showing selector circuits in the decoder for selecting interrogator control circuits of the control and indicator unit originating an interrogation, and for transmitting to the interrogator unit from the selected circuits a signal instructing the interrogator unit whether an active interrogation is to be made in the PI or the TI mode;

FIG. 25 is a schematic diagram showing selector circuits in the decoder for selecting the PI code checking bridge in the control and indicator unit within which an active interrogation originates, and for energizing the selected bridge;

FIG. 26 is a schematic diagram of the circuits in the decoder for amplifying the PI bridge unbalance signal from the control and indicator unit originating an active interrogation in the PI mode;

FIG. 27 is a schematic diagram showing selector circuits for selecting the strobe and range gate generator in the control and indicator unit within which an active interrogation originates;

FIGS. 28 and 29, which may be fitted together as shown in FIG. 14, are schematic diagrams of the circuits of the active decoder relays, the code and error indicators for displaying the results of an active decoding operation, and the hand switch for selecting an active interrogation in the PI or the TI mode;

FIG. 30 is a front elevation of a control and indicator unit, showing the hand controls thereon and the code and error indicators;

FIG. 31 is a diagram showing at A, code symbol positions in the code indicator of FIG. 30, and at B and C, respectively, examples of PI and TI code indications.

Referring now to the drawings, FIG. 1 shows a decoder unit 20, having the connections 21 to 28, extending therefrom, respectively to the Control and Indicator No. 1 unit 29, the PI/TI Code Switches unit 30 for Comparer

No. 1, the Control and Indicator No. 2 unit 31, the PI/TI Code Switches unit 32 for Comparer No. 2, the Control and Indicator No. 3 unit 33, the PI/TI Code Switches unit 34 for Comparer No. 3, the SI Code Switches unit 35 for Comparer No. 4, and the passive Mixer Switches unit 36. For brevity, the Control and Indicator unit will be referred to as C&I, for example, C&I-1 for the C&I No. 1 unit 29. Each of the connections 21 to 28 consists of a plurality of separately insulated conductors, as will be explained hereinafter.

The video output conductors 37, 38 and 39 of C&I units 29, 31 and 33 connect with the radar PPI No. 1 display unit 40, PPI No. 2 unit 41, and PPI No. 3 unit 42, respectively. The C&I-1 unit 29 and the switch unit 30 are preferably located close to the PPI No. 1 unit 40, as indicated in FIG. 1, for convenience of adjustment and manipulation by the operator, while observing the No. 1 PPI 40. The units 31, 32 and 41 are likewise in convenient proximity to each other for the observer at the No. 2 PPI 41; and the units 33, 34 and 42 form a similar group for the observer at No. 3 PPI 42. Switch units 35 and 36 are preferably positioned for operation by any one of the operators.

The Interrogator unit 43, FIG. 1, is connected to the decoder 20 by a plurality of insulated conductors, referred to hereinafter, represented by the line 44, and contains equipment of any known suitable design, not shown herein, for programming interrogations and for controlling the transmission of radar interrogations to an aircraft to be identified, the interrogating pulses being radiated by any known suitable radar interrogating antenna, not shown, having the usual rotational equipment for azimuth scanning of the area to be interrogated.

The receiver 45 demodulates the radio waves, automatically returned by the aircraft in reply to an interrogation, into trains of pulses, transmitted over the conductor 46 to the decoder 20. The circuit of the receiver may be of any suitable conventional radar receiver design, not shown, and may derive its input signals in well known manner from the interrogating antenna, referred to above, or from a separate antenna of any suitable well known form, not shown, moving synchronously with the radiating antenna according to well known radar system principles.

Each of the connecting lines 21, 23 and 25, FIG. 1, represents, in addition to certain power conductors, not shown, a number of separately insulated conductors, shown in FIG. 14, for connecting the decoder 20 to the respective C&I unit. Each of the connecting lines 22, 24 and 26, FIG. 1, represents twelve insulated conductors, connecting the respective code switches unit with the comparer in the decoder 20, having the number indicated, as shown in FIG. 3. The connecting line 27, FIG. 1, represents five separately insulated conductors, connecting the code switches unit 35 with the Comparer No. 4 in the decoder 20, as shown in FIG. 3. The connecting line 28, FIG. 1, represents six insulated conductors, as shown in FIG. 5, extending from the Passive Mixer to the Mixer Switches. The connecting line 44, FIG. 1, represents a number of separately insulated conductors, such as those for supplying from the interrogator 43, FIG. 1, the PI/TI and SI triggers, indicated in FIG. 4; the sync, as indicated in FIG. 27; and the conductors for transmitting to the interrogator the PI or the TI signal, as indicated in FIG. 24.

FIG. 2, at A, B and C, shows the 15-bit pulse trains 47, 48 and 49, respectively, in Mode 1, SI, Security Identity; Mode 3, TI, Traffic Identity; and Mode 2, PI, Personal Identity, any one of these trains being an example of a coded reply automatically transmitted from an aircraft in response to an interrogation for identification in

the corresponding mode, the train being in the form in which it reaches the decoder 20 after demodulation by the receiver 45.

The pulse trains 47, 48 and 49, show by the presence of a pulse, each position that may contain a valid identification pulse in the mode designated. The trains are drawn to the same scale and have the same length of 20.3 microseconds between the leading edges of the first pulse 1 and the last pulse 15, termed the "bracket" pulses, which must always be present to identify a reply to an interrogation in Modes 1, 2 or 3.

The position 8, designated by the dotted line 50 at the mid-position of each of the trains 47, 48 and 49, is never occupied by a valid identification pulse, and no valid identification pulse is used in the pulse position 13 in Mode 1, SI, train 47.

Each pulse in each of the trains 47, 48 and 49 has a nominal length of 0.5 microsecond, as indicated at pulse 5 in train 47. In train 49, the PI mode, the leading edges of adjacent pulses in the positions 1 to 7, and 9 to 15, are spaced 1.45 microseconds, as indicated at pulses 1 and 2; and in train 47, the SI mode, the spacing of the leading edges of adjacent pulses in pulse positions 1, 3, 5, 7, 9 and 11, is 2.9 microseconds, as indicated at pulse positions 1 and 3, which is just twice that in train 49, the PI mode; and in train 48, the TI mode, the spacing of the leading edges of adjacent pulses in the positions 1, 3, 5, 7, 9, 11, 13 and 15, is also 2.9 microseconds.

In Mode 1, SI, train 47, the five pulse positions, 3, 5, 7, 9 and 11, are subject to binary code changes in value, that is, any one of these positions may have the value "1," represented by the presence of a pulse, or the value "0," represented by the absence of a pulse, thus making possible the thirty-two SI code combinations, listed in Table No. 1.

TABLE NO. 1.—SI CODES, MODE 1

Tens	Units	Pulse Positions				
		3	5	7	9	11
0	0	0	0	0	0	0
0	1	0	0	0	1	0
0	2	0	0	0	0	1
0	3	0	0	0	1	1
1	0	1	0	0	0	0
1	1	1	0	0	1	0
1	2	1	0	0	0	1
1	3	1	0	0	1	1
2	0	0	1	0	0	0
2	1	0	1	0	1	0
2	2	0	1	0	0	1
2	3	0	1	0	1	1
3	0	1	1	0	0	0
3	1	1	1	0	1	0
3	2	1	1	0	0	1
3	3	1	1	0	1	1

TABLE NO. 1—Continued

Tens	Units	Pulse Positions				
		3	5	7	9	11
4	0	0	0	1	0	0
4	1	0	0	1	1	0
4	2	0	0	1	0	1
4	3	0	0	1	1	1
5	0	1	0	1	0	0
5	1	1	0	1	1	0
5	2	1	0	1	0	1
5	3	1	0	1	1	1
6	0	0	1	1	0	0
6	1	0	1	1	1	0
6	2	0	1	1	0	1
6	3	0	1	1	1	1
7	0	1	1	1	0	0
7	1	1	1	1	1	0
7	2	1	1	1	0	1
7	3	1	1	1	1	1

In Mode 3, TI, train 48, the six pulse positions, 3, 5, 7, 9, 11 and 13, are subject to binary code changes in value, the six being equally divided into two groups of three, 3, 5, 7, referred to as TI-1, and 9, 11, 13, referred to as TI-2, with one group in each half of the train. Each group of three positions makes possible eight different SI code combinations, as listed in Table 2, thus providing a total of sixty-four SI codes. The relay items in the parentheses in Table 2, relates only to the active operation.

TABLE NO. 2.—TI CODES, MODE 3

Tens	TI-1 Pulse Positions			Units	TI-2 Pulse Positions		
	3	5	7		9	11	13
(Relays)-----	(2A)	(4A)	(6A)	(Relays)-----	(7A)	(9A)	(11A)
0	0	0	0	0	0	0	0
1	1	0	0	1	1	0	0
2	0	1	0	2	0	1	0
3	1	1	0	3	1	1	0
4	0	0	1	4	0	0	1
5	1	0	1	5	1	0	1
6	0	1	1	6	0	1	1
7	1	1	1	7	1	1	1

In Mode 2, PI, train 49, the twelve pulse positions, 2 to 7, and 9 to 14, are subject to binary code changes in value, the twelve being equally divided into two groups of six, 2 to 7, referred to as PI-1, and 9 to 14, referred to as PI-2, with one group in each half of the train. Each group of six positions always has three pulses present and three absent, thus making possible twenty different PI code combinations, as listed in Table 3, thus providing at total of four hundred PI codes. The relay items in parentheses in Table 3, relate only to the active operation.

TABLE NO. 3.—PI CODES, MODE 2

Left Letters	PI-1 Pulse Positions						Right Letters	PI-2 Pulse Positions					
	2	3	4	5	6	7		9	10	11	12	13	14
Relays-----	(1A)	(2A)	(3A)	(4A)	(5A)	(6A)	Relays-----	(7A)	(8A)	(9A)	(10A)	(11A)	(12A)
A	1	1	1	0	0	0	A	1	1	1	0	0	0
B	1	0	1	1	1	0	B	1	0	1	1	1	0
C	1	0	0	1	1	0	C	1	0	0	1	1	0
D	1	0	0	0	1	1	D	1	0	0	0	1	1
E	0	1	1	1	0	0	E	0	1	1	1	0	0
F	0	1	0	1	1	0	F	0	1	0	1	1	0
G	0	1	0	0	1	1	G	0	1	0	0	1	1
H	0	0	1	1	1	0	H	0	0	1	1	1	0
I	0	0	1	0	1	1	I	0	0	1	0	1	1
K	1	1	0	0	0	1	K	1	1	0	0	0	1
L	0	1	1	0	0	1	L	1	1	0	0	0	1
M	0	0	1	1	0	1	M	0	1	1	0	0	1
N	0	0	1	1	0	1	N	0	0	1	1	0	1
O	0	0	0	1	1	1	O	0	0	0	1	1	1
P	0	1	1	0	1	0	P	0	1	1	0	1	0
R	1	1	0	0	1	0	R	1	1	0	0	1	0
S	1	1	0	1	0	0	S	1	1	0	1	0	0
T	1	0	1	0	1	0	T	1	0	1	0	1	0
V	1	0	0	1	0	1	V	1	0	0	1	0	1
W	0	1	0	1	0	1	W	0	1	0	1	0	1
Z	1	0	1	0	0	1	Z	1	0	1	0	0	1

The passive operating system is used to identify and locate the position of an aircraft whose code is previously known. During the passive operation, the operator manually sets the switches in his code switch unit 35, FIG. 1, to a desired SI code; or sets the switches in his code switch unit 30, 32 or 34 to a desired PI or TI code; or sets the switches in more than one or in all of the code switch units 30, 32, 34, 35 to desired codes.

When the aircraft whose code corresponds to the desired code is interrogated by the interrogating station, its security identification code is verified to confirm its status as a "friend" and its position is indicated by a PPI display during an SI interrogation; its personal identification code is verified and its position is indicated by a PPI display during a PI interrogation; and its traffic identity code is verified and its position is indicated by a PPI display during a TI interrogation. Three different standard passive interrogation procedures may be employed to identify and locate the position of an aircraft, these being the SI interrogation alone, or interlaced SI and PI interrogations, or interlaced SI and TI interrogations. As long as the code switches set up by the operator remain unchanged, the aircraft is identified and its position is indicated during each successive scan of the PPI unit.

The interrogator unit 43, FIG. 1, previously set into operation, automatically programs a continuous series of passive interrogations, and transmits to the decoder 20, gating triggers corresponding to the modes of interrogation. These triggers consist of either a single series of SI trigger pulses, or two series of trigger pulses interlaced with respect to time, and consisting of a series of SI trigger pulses and a series of PI or TI trigger pulses timed to occur approximately halfway between the timings of the SI trigger pulses. The triggers are initiated when the circuits of the interrogator are turned on, at which time the SI mode alone, or the SI mode interlaced with the PI mode, or the SI mode interlaced with the TI mode, may be selected for interrogation. The triggers in any one series are used to gate a "Yes" pulse to produce a PPI blip to indicate verification of the identification code and the position of the interrogated aircraft, when the reply being decoded meets all the automatic checks on its validity.

When the aircraft, whose code corresponds to the switch code set up by the operator, receives the request to identify itself in the mode being interrogated by the operator, the aircraft automatically replies by transmitting its identification code in that mode. The decoder 20 then automatically processes the reply code by checking for the presence of bracket pulses, and comparing the reply code with the code switch settings to verify the reply code and thus verify the identification code of the aircraft. When the codes agree, and there is no other inhibition, the "Yes" pulse produced in response to the reply, in turn produces a PPI blip which indicates the position of the aircraft and the fact that it has been identified.

The passive decoding and code checking circuits are located within the decoder 20, FIG. 1, except for the circuits of the code switching units 30, 32, 34 and 35, and are shown schematically or by block diagrams, in FIGS. 3, 4, 5 and 6, fitted together as shown in FIG. 7. The train of video pulses representing the incoming reply code received from an interrogated aircraft, is subjected by these circuits to several checks and the circuits then signify whether the reply code agrees with the verification code set up by the code switches. The result of a successful comparison is used to mark the target on the PPI display.

In the decoder 20, FIG. 1, a delay line having 15 taps, numbered 1 to 15, corresponding to the 15-bit pulse train 49, in FIG. 2, makes it possible to derive at the taps, simultaneous pulses from the incoming train of sequential pulses. A bracket coincidence checking "AND" gate is

arranged to trigger a bracket coincidence blocking oscillator in response to the bracket pulses at the No. 1 and No. 15 taps of the delay line. Each of the thirteen taps Nos. 2 to 14, between the No. 1 and No. 15 taps, connects with a separate tap "AND" gate, the No. 8 tap gate being reserved for checking the validity of a reply code, and the remaining twelve tap gates providing channels for the pulses to be decoded, or otherwise checked.

The outputs of the twelve tap gates are fed to the inputs of tap blocking oscillators the outputs of which are fed to three comparers for PI and TI codes, and one comparer for SI codes.

Each of the comparers has its own group of code switches 30, 32, 34, 35, respectively, for use by an operator to set up a code to verify the reply code from an interrogated aircraft. Each PI/TI comparer has a separate "EXCLUSIVE OR" gate for each of its twelve decoding channels, while the SI comparer has a separate "EXCLUSIVE OR" gate for each of its five decoding channels and a separate ordinary "OR" gate path for each of its seven remaining channels used for checking the code structure of SI reply trains. Each "EXCLUSIVE OR" gate circuit is of the type described in A. R. Garfinkel et al. Patent No. 2,868,999, and has three input circuits driven, respectively, by the bit in the decoding channel containing that gate, by a delayed "Bracket Coincidence" pulse, and by a reset pulse. Hereinafter throughout the specification the abbreviation "B.C." will be used in place of "Bracket Coincidence." The output circuit of the "EXCLUSIVE OR" gate produces a "No" pulse when the reply bit in that decoding channel disagrees with the code switch setting for that channel. The "No" pulse is fed through a summing "OR" gate to a "No" blocking oscillator for that comparer.

Four control "AND" gates are provided, one for each of the three PI/TI comparers, and one for the single SI comparer, the output of each control "AND" gate being fed to a separate "Yes" blocking oscillator. When there is a PI or a TI interrogation, the PI/TI control "AND" gates are periodically enabled by the PI/TI trigger voltage from the interrogator 43, FIG. 1, and the SI control "AND" gate is periodically enabled by the SI trigger voltage from the interrogator 43, between the enabled periods of the PI/TI control "AND" gates.

If the code bits gated into the PI/TI comparer, during a passive interrogation, agree with the code set up by the code switches for that comparer, and the control "AND" gate for that comparer is enabled by the PI/TI trigger gate voltage without there being any inhibition pulse applied thereto, a delayed B.C. pulse is passed by the control "AND" gate to the "Yes" blocking oscillator, causing it to fire and transmit a "Yes" pulse to the passive mixer in the decoder. The passive mixer switches 36, FIG. 1, select by the appropriate switches, the "Yes" pulse or other pulses which the operator wishes to have displayed by his PPI. The passive mixer contains pulse stretching circuits for stretching the 1 microsecond pulse of the "Yes" PI/TI signals into 15 microsecond pulses to permit easy distinguishing of the PI/TI pulses from the other pulses selectable for PPI display. The selected pulses are transmitted to each of the control indicators 29, 31 and 33, FIG. 1, and from there to the connected PPI units 40, 41 and 42 to produce the desired displays.

If any one of the PI/TI code bits in the reply received from the aircraft does not agree with the code set up by the code switches for a given PI/TI comparer, a "No" output pulse is generated by the "EXCLUSIVE OR" gate in the decoding channel for that bit in the comparer and fires the "No" PI/TI blocking oscillator. The pulse from the "No" blocking oscillator is used to inhibit the control "AND" gate for that comparer, so that gate cannot pass the delayed B.C. pulse and therefore cannot supply a pulse to fire the "Yes" PI/TI blocking oscillator. As a result, the passive mixer receives no video pulse from the control "AND" gate for that comparer to show

varification of that PI/TI reply code, or to show identification of the aircraft by way of that comparer.

Each of the five decoding channels for pulse positions 3, 5, 7, 9, and 11, in the SI comparer contains an "EXCLUSIVE OR" gate, and any "EXCLUSIVE OR" gate in which a reply code bit does not agree with the code switch set up for that pulse position, produces a "No" pulse at the SI comparer output. The "No" pulse fires the "No" blocking oscillator and the resulting "No" output pulse inhibits the control "AND" gate for the SI comparer, so that the gate cannot pass the delayed B.C. pulse to fire the "Yes" blocking oscillator. Verification of the reply code and identification of the aircraft is thus prevented when the reply code disagrees with the verification code set up in the code switches 35.

When the reply bit in each of the five SI decoding channels agrees with the code switch position for that channel, none of these decoding channels produces a "No" pulse. It is necessary, however, for the reply code to meet other tests of validity before a "Yes" SI pulse can be produced to identify and locate the aircraft on the PPI. Each of the seven checking channels for pulse positions 2, 4, 6, 10, 12, 13, and 14, in the SI comparer, as distinguished from the five decoding channels, tests the passive SI reply train of pulses for validity to see that it has no pulse in the pulse position corresponding to that checking channel when the delayed B.C. pulse is applied to the control "AND" gate to fire the "Yes" blocking oscillator. If a pulse is erroneously present in any one of the seven checking channels, it passes directly through the ordinary "OR" gate leg for that channel in the SI comparer, and thus appears in the SI comparer output as a "No" pulse which inhibits the control "AND" gate for the SI comparer, thus preventing the firing of the "Yes" blocking oscillator for the SI comparer. The passive mixer consequently cannot receive any SI video pulse to pass on to the PPI to show verification of the reply code, or to show identification of the aircraft, when there is a pulse in any one of the seven SI checking channels 2, 4, 6, 10, 12, 13, and 14, respectively.

Tap No. 8, corresponding to the pulse position 8 at the dotted line 50, FIG. 2, in each of the modes SI, PI, and TI, has no valid pulse when the bracket coincidence pulse is produced and enables the No. 8 tap "AND" gate. If a pulse should erroneously appear at the No. 8 tap at the time referred to, the No. 8 tap "AND" gate transmits an output pulse which serves as a "No" pulse feeding through each of the summing "OR" gates to the "No" blocking oscillators, causing them to fire and to feed a "No" pulse to an inhibiting leg on each of the control "AND" gates, thereby preventing any of these gates from passing a delayed B.C. pulse, and thus preventing the production of a "Yes" pulse by the "Yes" blocking oscillator for any of the comparers. The No. 8 pulse, when present in a reply train, thus prevents the erroneous indication by a PPI blip of recognition of the interrogated aircraft in any of the modes SI, PI, or TI.

Passive System, Detailed Description

The input conductor 46, FIG. 3, applies positive video pulses in trains similar to those shown in FIG. 2, from the receiver 45, FIG. 1, to the input of the constant amplitude grounded grid amplifier 51, FIG. 3, whose output is coupled to the input of the cathode follower 52, having the circuit identified as C.F.(A), referred to hereinafter. The output of cathode follower 52 is coupled to the input of the Schmitt trigger 53, serving as a regenerative amplifier to reshape the input wave into an output wave of square form. The output of the Schmitt trigger 53 is coupled to the input of the cathode follower 54, having the circuit C.F.(B). The schematic circuits of the grounded grid amplifier 51, the C.F.(A) cathode follower 52, the Schmitt trigger 53, and the C.F.(B) cathode follower 54, are shown in FIG. 8, and described hereinafter.

The output conductor 55 of the cathode follower 54 connects with the input of the delay line 56, 57 may be of the lumped parameter type, such as that described in the Radiation Laboratory Series, volume 9, chapter 22, page 730, and is provided with a total delay of 20.3 microseconds, which is equal to the time interval between the leading edges of the No. 1 and No. 15 pulses in a reply train, as shown in FIG. 2, and has fifteen taps, numbered 1 to 15, having 1.45 microsecond spacing between adjacent taps, thus corresponding to the pulse position spacings in the reply trains. The delay line therefore is adapted to convert a train of 15 signal bits in sequence, into a group of 15 simultaneous bits appearing individually at the respective taps numbered 1 to 15. Each delay line section 56 and 57 is terminated with its characteristic impedance, not shown.

The output conductor 58 of the delay line section 56 is coupled to the input of the Schmitt trigger 59, whose output is coupled to the input of the cathode follower 60, having the C.F.(B) circuit. The output conductor 61 of the cathode follower 60 connects with the input of the delay line section 57. The Schmitt trigger 59 and cathode follower 60 have circuits similar to those of the Schmitt trigger 53 and the cathode follower 54, respectively, and operate similarly thereto. They compensate for the reduced pulse amplitude and smearing caused by the attenuation and limited band width of delay line section 56, and apply pulses of the desired form and amplitude to the delay line section 57.

FIG. 8 shows the schematic circuits of the electronic stages 51, 52, 53, 54 for feeding video pulses to the delay line section 56, FIG. 3. The video pulses are applied by the input conductor 46 to the cathode of the constant amplitude grounded grid triode amplifier 51 whose circuit is designed to terminate the input line conductor 46 properly, and to supply constant amplitude pulses at its anode output conductor 62, which is coupled through the capacitor 62A to the grid of the triode cathode follower 52, having the circuit C.F.(A).

The cathode of the crystal diode rectifier 64 is connected to the grid of the cathode follower 52, and back-biased by the negative bias on the grid. The diode 63 clamps to ground any positive grid potentials exceeding the back-bias potential. The cathode of the crystal diode rectifier 64 is connected to the grid of the cathode follower 52 and clamps negative pulses to ground through the capacitor 65. The ungrounded terminal of the capacitor 65, is maintained at a negative potential by the grid bias circuit of the cathode follower 52 and has the conductor 65A connected thereto to supply a negative bias to the grid of the grounded grid amplifier 51 to control the amplitude of output pulses on conductor 62.

The cathode of cathode follower 52 couples through output conductor 66 and the capacitor 66A to the control grid of the pentode 67 in the Schmitt trigger 53 of well-known form which functions as a regenerative amplifier to produce square output pulses in response to input pulses. The grounded grid amplifier 51 is adjusted to limit the amplitude of pulses applied to the input of the Schmitt trigger 53 to a maximum of about 12 volts in response to signal pulses above two volts in amplitude applied to the input of the grounded grid amplifier 51. The Schmitt trigger 53 triggers in one direction when the input potential is raised to a critical value and triggers in the reverse direction when the input is reduced to another level. The Schmitt circuit is designed so that the two critical voltage levels of signal input do not exactly coincide, that is, a certain amount of hysteresis is designed into the circuit in order to prevent the circuit from oscillating. The hysteresis provided in the circuit is of the order of two volts and is not critical. The transition level is so adjusted by the potentiometer 68, having the slide 68A connected through the resistor 69 to the control grid of the pentode 67, as to provide an optimum pulse width for the delay line section 56, FIG. 3.

The anode of the pentode 67 couples through the resistor 70 of the voltage divider resistors 70, 70A with the control grid of the triode 71. In order to obtain an extremely rapid rise time in the output signal at the anode of triode 71, it is necessary to compensate for the stray capacitance across the voltage divider 70, 70A, this being done by the adjustable trimmer capacitor 72 shunted across resistor 70. The output conductor 73 of the Schmitt trigger 53 couples the anode of triode 71 through the capacitor 73A to the control grid of the triode cathode follower 54, having the circuit C.F.(B). The crystal diode rectifier 74 and 75 are connected similarly to diodes 63 and 64, respectively, in cathode follower 52, and function similarly thereto. The output conductor 55, coupled by the capacitor 76 to the cathode follower 54, has the cathode of the crystal diode 77 connected thereto for clamping conductor 55 to ground. The conductor 55 couples with the input of delay line section 56, FIG. 3.

The input leg 78 of the bracket coincidence "AND" gate 79, FIG. 3, is connected to the tap No. 1 on the delay line section 57 for receiving therefrom the bracket pulse in position number 1, FIG. 2C, and the input leg 80 of bracket coincidence gate 79 is connected to tap No. 15 of delay line section 56 for receiving therefrom the bracket pulse number 15. When a reply train of pulses from an interrogated aircraft is properly bracketed by containing the bracket pulses 1 and 15, FIG. 2C, these pulses simultaneously appear on the input legs 78, 80 of "AND" gate 79. Their coincidence causes "AND" gate 79 to transmit a bracket coincidence, or B.C. pulse over output lead 81 to the input of the bracket coincidence blocking oscillator 82, having the circuit B.O.(A), which fires and regenerates the B.C. pulse and feeds it over output lead 83, 84, to the upper input leg of each of the thirteen tap "AND" gates 85 to 97.

The lower input leg of each of the thirteen tap gates 85 to 97, connects with a different one of the thirteen taps numbered 2 to 14 on the delay line 56, 57. The lower input legs of tap gates 85 to 90 connect with taps 2 to 7, respectively, those of tap gates 91 to 96 connect with taps 9 to 14, respectively, and the lower input leg of tap gate 97 connects with tap 8. Taps 2 to 7 and 9 to 14 are in decoding channels, while tap 8 is in a channel for checking SI, PI, or TI reply codes for a false signal.

The B.C. pulse on lead 84 enables the upper leg of each of the tap "AND" gates 85 to 97, and a reply code pulse on the lower leg of any of these gates simultaneously with the B.C. pulse on the upper leg, produces a corresponding pulse in the output of the tap "AND" gate in that channel. The code pulses from tap "AND" gates 85 to 96 are fed, respectively, to the inputs of the tap blocking oscillators 98 to 109, each having the same circuit B.O.(D) of the form shown in box 109, for regenerating the code pulse which is applied to the input lead 110 and fed through the capacitor 111 to the grid of the input triode 112, having a grounded cathode, and an anode connection 113 with the anode of the output triode 114. The anode circuit inductor 115, shunted by the resistor 116, couples inductively with the secondary inductor 117 in circuit with the grid of triode 114. The back-biased crystal diode rectifier 118 has its cathode connected to the cathode of triode 114 to clamp the triode cathode to ground in response to negative potentials exceeding the back-bias, thereby preventing noise pulses from causing an undesired firing of the blocking oscillator.

The cathode of triode 114 connects through the cathode resistor 119 to the output current lead 120 for the regenerated code pulse produced when the blocking oscillator 109 is fired in response to a code pulse appearing at tap 14, representing pulse position 14, FIG. 2C, when the B.C. pulse is on lead 84. The output voltage lead 121 connects with the cathode of triode 114 for the regenerated code pulse representing pulse position 14. The lower of the two output leads shown at the right

edge of each of the tap blocking oscillator boxes 98 to 109, represents a current lead similar to the lead 120 in box 109, and the upper of the two output leads represents a voltage lead similar to the lead 121 in box 109.

The twelve output current leads in the bracket 122 and representing pulse positions 2 to 7 and 9 to 14, extend from the blocking oscillators 98 to 109, and to the three PI/TI comparers 124, 125, 126 in series, while five of these leads representing pulse positions 3, 5, 7, 9, 11, extend through comparer 126 to the SI comparer 127 in series therewith. The twelve output voltage leads in the bracket 123, extending from the blocking oscillators 98 to 109, provide parallel connected input leads to the comparers 124, 125, 126, 127.

The tap "AND" gate 97 when enabled by a B.C. pulse on lead 84 and a pulse is on tap 8, feeds an output pulse to the lead 423 and the grid of the triode cathode follower 429, of well-known form, having the circuit C.F.(C). The triode cathode connects through the resistor 430 to ground and through the output lead 431 and the capacitor 432 to the lead 433 having a connection to ground through the resistor 434.

The regenerated B.C. pulse on lead 83 is fed to the input of the delayed bracket coincidence blocking oscillator 128, having the circuit B.O.(B). The output lead 129 of blocking oscillator 128 is coupled to the input of the bracket coincidence driver 130, having the output lead 131 which feeds a B.C. pulse to each of the comparers 124 to 127 in series.

The blocking oscillator 128 has a second output lead 132 coupled to the input of the delay unit 133 which has an output lead 134 coupled to the input of the reset blocking oscillator 135, having the circuit B.O.(C), and having an output lead 136 coupled to the input of the reset driver 137 whose output lead 138 feeds a reset pulse to each of the comparers 124 to 127 in series. The blocking oscillator 135 has a second output lead 139 to supply a delayed B.C. pulse to the passive mixer in FIG. 5, and to the circuits of FIGS. 17 and 18. The delayed B.C. pulse on lead 134 is fed over lead 140 to FIG. 4. Lead 141 from tap 15 supplies raw video pulses to the passive mixer in FIG. 5.

FIG. 9 shows the schematic circuits of blocking oscillators 82, 128, and 135, delay unit 133, B.C. driver 130, and reset driver 137, FIG. 3. The B.O.(A) circuit of the bracket coincidence blocking oscillator 82, FIG. 9, is of well-known form, being similar to the B.O.(D). Circuit of the blocking oscillator 109, FIG. 3, except that the connection of the clamping diode 118 in the blocking oscillator 109, is not provided in the blocking oscillator 82, and the cathode resistor 142 in blocking oscillator 82, connects directly to ground.

The B.O.(B) circuit of the delayed B.C. blocking oscillator 128, FIG. 9, is similar to that of blocking oscillator 82, except that a delay unit 143 is inserted between the grid coupling capacitor 144 and the grid of the input triode 145, and except that an extra secondary inductor 146, is inductively coupled to the primary inductor 147 and feeds a 1 microsecond B.C. pulse to the output lead 129. The delay unit 143 consists of a resistor 148 for introducing a delay of about 0.1 microsecond in the time of firing of the blocking oscillator 128 in response to a B.C. pulse from the blocking oscillator 82. The resistor 148 in combination with the stray capacitance of the circuit, represented by the dotted-line capacitor 149, slightly integrates the B.C. pulse and causes the rise time of the leading edge of the pulse to increase.

The B.C. pulse on lead 129, FIG. 9, is fed through the resistor 150 to the control grid of the pentode 151 in the B.C. driver 130, the anode of the pentode 151 being connected directly to the driver output lead 131. The small grounded capacitor 152 is connected to the control grid, and the small grounded capacitor 153 is connected to the cathode of the pentode 151 to suppress noise pulses. The resistor 150 cooperates with the capacitor 152 as an

integrator to provide a fine adjustment of the time delay of the B.C. pulse.

The output lead 132 from the cathode of the output triode 154 feeds a delayed B.C. pulse to the delay unit 133, which introduces a delay of 0.4 microsecond in the time of firing of the blocking oscillator 135. The delay unit 133 is constructed as a delay line, and includes an inductor 155 in series with the input lead 132, the inductor 155 having distributed capacitance with the grounded conductor 156, and the delay line having a terminating resistor path 157 to ground.

The B.O.(C) circuit of the reset blocking oscillator 135 is similar to that of blocking oscillator 128, except that the delay unit circuit 143 is omitted, and except that the resistor 158 is provided in series with the lead 134 as a buffer. The blocking oscillator 135 fires in response to the delayed B.C. pulse fed through the delay unit 133 from the blocking oscillator 128, and generates a 1 microsecond reset pulse which is fed to the control grid of the pentode 159 in the reset driver 137. The anode of the pentode 159 is connected directly to the driver output lead 138. The small grounded capacitor 160 is connected to the cathode of the pentode 159 to suppress noise pulses.

Passive Comparers

Each of the three PI/TI comparers 124, 125, 126, tests the twelve decoding channels 2 to 7 and 9 to 14 for the presence or absence of a tap pulse therein whenever a B.C. pulse is produced by pulses at taps 1 and 15, and the SI comparer 127 similarly tests the five decoding channels 3, 5, 7, 9 and 11 for the presence or absence of a tap pulse. The test in any given comparer consists of comparing the code bits present in the decoding channels with the code bits set up by the code switches for that comparer.

A closed switch in any one of the groups of code switches 30, 32, 34, 35, FIG. 3, represents a code bit having a binary value of 1. An open switch represents a code bit having a binary value of 0. Similarly, the presence of a pulse in any bit in a reply code from an interrogated aircraft is represented by 1, and the absence of a pulse is represented by 0. It is thus possible to set up any one of PI/TI codes in Tables No. 2 or 3 by the switches in any one of the code switch groups 30, 32, or 34, FIG. 3, or to set up any one of the 31 codes in Table No. 1 by the switches in the code switch group 35.

The comparison of the code bits in a reply code from an interrogated aircraft with the code bits set up in any given group of code switches 30, 32, 34, or 35, is accomplished by a separate "EXCLUSIVE OR" gate in each of the decoding channels of the comparer associated with that group of code switches.

FIG. 10 shows the schematic circuits of the PI/TI comparer 126, and the "EXCLUSIVE OR" gate 161 of the type employed in the present invention and described in A. R. Garfinkel et al. Patent No. 2,868,999. The "EXCLUSIVE OR" gate differs from an ordinary "OR" gate in that it transmits an output signal pulse only if one input leg or the other of its two input legs, but not both, has the code bit 1 applied thereto. When the code bit 1 appears on both input legs simultaneously, or does not appear on either input leg, the gate does not generate an output pulse. By applying a reply code bit from a decoding channel to one input leg, and applying a code bit representing the position of the code switch for that channel to the other input leg, the "EXCLUSIVE OR" gate produces no output when the reply code bit, whether 1 or 0, agrees with the code switch bit. When the reply code bit disagrees with the code switch bit, however, the "EXCLUSIVE OR" gate produces an output pulse which is used to prevent verification of the reply code and recognition of the aircraft. A single invalid bit in a reply code thus prevents false identification of an aircraft.

The "EXCLUSIVE OR" gate 161, labelled E2, is in the decoding channel 2 for the reply code bit on tap 2

of the delay line 56, 57, FIG. 3, this bit being in the pulse position 2, FIG. 2C. The saturable toroidal inductor core 162 in the "EXCLUSIVE OR" gate 161, has the three input magnetizing coils consisting of the tap or channel pulse coil W-1 which, if acting alone, would create the "0" state in the core 162, the B.C. or clock pulse coil W-2 which acting alone would create the number 1 state in the core 162, and the reset coil W-3, designed to return the core 162 to its normal "0" state to complete the operational cycle of the core. A fourth coil W-4 serves as an output coil.

The B.C. pulse lead 163 feeds a 1 microsecond negative pulse from the B.C. driver 130, FIG. 3 through the coil W-2 to the lead 164. We may assume this B.C. pulse produces a flux in the core 162 in the direction shown by the arrow at the coil W-2. When a tap pulse is present in the pulse position 2, the current lead 165 for tap No. 2 feeds a 1 microsecond positive pulse through the coil W-1 and lead 166 to ground, producing a flux in the core 162 in the direction shown by the arrow which is opposite to that produced by the B.C. pulse in coil W-2, thereby cancelling the effect of the B.C. pulse when coils W-1 and W-2 are pulsed simultaneously. Under these conditions, no substantial pulse is produced in the output coil W-4.

The B.C. pulse is always present whenever a reply code is to be examined, but the tap pulse to be applied to the coil W-1, may or may not be present. When the tap pulse is not present, the B.C. pulse on coil W-2 changes the magnetic state of the core 162 from its normal or 0 state to the number 1 state which is the reverse of that in the 0 state, thereby producing a positive voltage pulse at the upper ungrounded end 167 of the output coil W-4.

If both the B.C. and the tap pulse were applied to their respective coils W-2 and W-1 at the same nominal time, but the circuit, through a small maladjustment, caused the B.C. pulse to be applied to coil W-2 slightly before the tap pulse reached coil W-1, the flux in core 162 would be momentarily reversed and produce an unwanted output pulse. In order to avoid this undesired effect, the B.C. pulse is delayed 0.1 microsecond after the tap pulse, by the delay unit 143, FIG. 9, as already described. Since the tap pulse does not reverse the flux in core 162 from the 0 state, but cancels the flux from the B.C. pulse, the output coil W-4 cannot produce an output pulse.

The reset pulse, consists of a negative pulse fed from the reset driver 137, FIG. 3, over lead 138 in series with the lead 168, FIG. 10, through reset coil W-3 and lead 169, and produces a flux in the direction shown by the arrow at coil W-3, which is in the same direction as that produced by the tap pulse in coil W-1, and opposite to that produced by the B.C. pulse in coil W-2. The reset pulse is timed to start 0.5 microsecond after the tap pulse and the undelayed B.C. pulse on lead 83, FIG. 9. The 0.5 microsecond delay is produced by the sum of the 0.1 microsecond delay in the delay unit 143, and the 0.4 microsecond delay in the delay unit 133. The reset pulse cancels the effect of the B.C. pulse on coil W-2 during the 0.1 microsecond that the B.C. pulse continues after the end of the tap pulse, and thus prevents the end portion of the B.C. pulse from changing the core from the 0 to the 1 state and thereby producing a false output pulse.

When no tap pulse is present on coil W-1 while the B.C. pulse is on coil W-2, the core is changed by the B.C. pulse from the 0 to the 1 state, and is then reset to the 0 state by the reset pulse. As previously described, the effect of the B.C. pulse on coil W-2 when no tap pulse is present on coil W-1, is to produce a pulse in the output coil W-4. The path for this output pulse may be traced from the grounded end of coil W-4, through coil W-4 and lead 167, in a forward direction through the crystal diode rectifier 170 when the diode is not back-biased by a positive voltage applied to the cathode thereof by way of the lead 171 in series with

the resistors 172 and 173 in series. The back-bias voltage is adjusted to exceed the output voltage induced in the coil W-4. When the reset pulse changes the core 162 from the 1 state to the 0 state, a negative pulse is generated in the output coil W-4, but since this pulse is negative and inverse to the diode 170, it cannot pass therethrough.

If we assume that the conductor 174 has a ground potential applied thereto by closure of the code switch 175 for pulse position 2, the positive back-bias voltage on lead 171 is completely absorbed in resistor 172, thus removing the back-bias from diode 170. The pulse induced in coil W-4 is then free to pass through diode 170 and the capacitor 176 in series to the "EXCLUSIVE OR" gate output lead 177. The crystal diode rectifier 178 with its cathode connected to lead 177 is poled inversely to the pulse on lead 177 and acts as an open circuit.

The current lead 165, FIG. 10, derives the tap 2 current pulse it applies to coil W-1 over the current lead 179, FIG. 3, from the tap blocking oscillator 98, which at the same time is feeding a voltage pulse over the voltage lead 180, FIG. 3, to the voltage lead 181, FIG. 10. The current lead 165 and the corresponding voltage lead 181 for tap 2 constitute in effect two branch input paths which act together as the tap input leg of the "EXCLUSIVE OR" gate 161 for reply code bits in channel 2. The other input leg of exclusive "OR" gate 161 has the conductor 174 as an input path and will be referred to as the switch input leg, since it is responsive to the code switch 175. Since each of the two input legs may have either of two binary bits applied thereto, there are four possible combinations of input bits. Each of the following four numbered paragraphs describes the operation of the exclusive "OR" gate 161 with a different one of these bit combinations.

(1) When the code switch 175 is closed and the tap 2 reply code bit is a pulse, the switch input leg of the "EXCLUSIVE OR" gate examines this combination by comparing the switch bit with the tap bit, finds that the bits agree, and therefore produces no output pulse on lead 177. This result is produced as follows. The tap 2 pulse produces a positive voltage pulse on the voltage lead 181 which feeds the pulse through the resistor 182 and in a forward direction through the crystal diode rectifier 183 to the lead 174 which is grounded by the closed code switch 175. The voltage pulse thus appears across a voltage divider formed by resistor 182 in series with the low forward resistance of diode 183. Since resistor 182 has a much greater resistance than the forward resistance of the diode 183, the tap pulse voltage on lead 181 is dropped across the resistor 182, and the very small voltage produced across diode 183 is insufficient to feed any appreciable pulse through the diode 178 in a forward direction to the output lead 177. Furthermore, the output coil W-4 produces no pulse in response to the simultaneous application of the tap 2 current pulse on coil W-1 and the B.C. pulse on coil W-2, as previously explained. No pulse is therefore fed to the output lead 177. This operation thus fulfills the logical requirement that the "EXCLUSIVE OR" gate 161 shall produce no output pulse when the code switch bit is 1, and the corresponding reply code bit is 1.

(2) When the code switch 175 is closed, but the tap 2 reply code pulse is absent, the switch input leg of the "EXCLUSIVE OR" gate 161 has the signal bit 1, and the tap input leg has the signal bit 0. Since the bits disagree, an output pulse is produced on the output lead 177 in the following manner. The B.C. pulse on tap pulse coil W-2 produces a pulse in the output coil W-4 due to the absence of a tap pulse on coil W-1 to cancel the effect of the B.C. pulse. Since switch 175 eliminates the back-bias on diode 170, the pulse is fed from coil W-4 through diode 170 and capacitor 176 to output 177. This operation fulfills the logical requirement that the "EXCLUSIVE OR" gate shall produce an output pulse when

the code switch bit is 1 and the corresponding reply code bit is 0.

(3) When the code switch 175 is open, and the tap 2 reply code pulse is absent, the switch input leg of the "EXCLUSIVE OR" gate 161 has the signal bit 0, and the tap input leg has the signal bit 0. Since the bits agree, no output pulse is produced on lead 177 for the following reasons. The B.C. pulse on coil W-2 produces a pulse in the output coil W-4, but this pulse cannot pass the back-biased diode 170 to reach the lead 177. Since there is no tap 2 pulse, there is no pulse on voltage lead 181 to be fed to the output lead 177. This operation thus satisfies the logical requirement that the "EXCLUSIVE OR" gate shall produce no output pulse when the code switch bit is 0, and the corresponding reply code bit is 0.

(4) When the code switch 175 is open, and the tap 2 reply code bit is a pulse, the switch input leg of the "EXCLUSIVE OR" gate 161 has the signal bit 0, and the tap input leg has the signal bit 1. Since the bits disagree, an output pulse is produced on the output lead 177, as follows. The tap pulse on the coil W-1 cancels the effect of the B.C. pulse on the coil W-2 and prevents the production of a pulse in the output coil W-4 to be fed to lead 177. The open code switch 175 allows the full back-bias voltage of lead 171 to be applied to diode 183. The tap pulse voltage on voltage lead 181 appears across a voltage divider formed by resistor 182 in series with the very much higher resistance of the back-biased diode 183. Consequently, most of the tap pulse voltage is fed through resistor 182 and the low forward resistance of diode 178, to the output lead 177. The operation thus conforms to the logical requirement that the "EXCLUSIVE OR" gate 161 shall produce an output pulse when the code switch bit is 0, and the corresponding reply code bit is 1.

The "EXCLUSIVE OR" gates E3 to E7, and E9 to E14, FIG. 10, and those in the group E3, E5, E7, E9, and E11, FIG. 11, have the same circuit as and operate in the same manner as that described for the gate E2, FIG. 10. The number in each "EXCLUSIVE OR" gate label, such as E2, is the number of the decoding channel in which the gate is located, as well as the pulse position number for the code bits applied to that gate. The connections to each of these "EXCLUSIVE OR" gates are similarly drawn. Consequently at the top and at the bottom edge of each gate, the left lead for the reset pulse, provides connections placing the reset coil W-3 in gate E2, FIG. 10, in series with the reset coils W-3, not shown, in the other of these gates. The reset pulse lead 184 from gate E14, FIG. 10, provides the series connection between the "EXCLUSIVE OR" gates in FIG. 10 and those shown in FIG. 11. The reset pulse lead 185 from the gate E11, FIG. 11, connects through the resistor 186 to the positive terminal 187 for the source supplying anode current to the reset driver 137, FIG. 9. At the top and the bottom edge of each "EXCLUSIVE OR" gate, the right lead, for the B.C. pulse, provides connections placing the B.C. coil W-2 in gate 161, FIG. 10, in series with the B.C. coils W-2, not shown, in the other "EXCLUSIVE OR" gates in FIGS. 10 and 11. The B.C. pulse lead 188 from gate E14, FIG. 10, connects the "EXCLUSIVE OR" gates in FIG. 10 in series with those in FIG. 11. The B.C. pulse lead 189 from gate E11, FIG. 11, connects through the resistor 190 to the positive terminal 191 for the source supplying anode current to the B.C. driver 130, FIG. 9.

The circuits of the PI/TI comparers 124 and 125, FIG. 3, except as to the minor points noted below, are the same as those of the PI/TI comparer 126, FIG. 10. Each of the three PI/TI comparers has twelve "EXCLUSIVE OR" gates E3 to E7, and E9 to E14, not shown in comparers 124 and 125, there being a separate "EXCLUSIVE OR" gate for each of the twelve decoding channels in each of the PI/TI comparers. It will be noted that the twelve current leads at bracket 122, FIG. 3 shown entering at the top edge of comparer 124 in line with series

extensions thereof connecting the bottom edge of comparer 124 with the top edge of comparer 125, and connecting the bottom edge of comparer 125 with top edge of comparer 126, do not all appear at the bottom edge of comparer 126, because only five current leads, for tap numbers 3, 5, 7, 9, and 11, are needed in the SI comparer 127 for the five "EXCLUSIVE OR" gates therein.

In FIG. 10, the upper lead, entering the left edge of each "EXCLUSIVE OR" gate, such as the lead 181 for gate 161, is a voltage lead for the tap number corresponding to that gate, and the lower two leads, such as the leads 165 and 166 for gate 161, are the leads for the tap coil W-1 for the same tap numbers. Since the tap coils representing any given tap numbers are all placed in series in the same current lead path for that tap number, and since there is one tap coil W-1 in each of the three PI/TI comparers 124, 125, and 126 to represent any given tap number, and there is also one tap coil W-1 in the SI comparer 127 to represent, respectively, the tap numbers 3, 5, 7, 9, and 11, it will be seen that there is a total of three tap coils W-1 in series for each of the tap numbers 2, 4, 6, 10, 12, 13, and 14, and that there is a total of four tap coils W-1 in series for each of the tap numbers 3, 5, 7, 9, and 11, the fourth tap coil for each of the last five tap numbers being located in comparer 127. The tap current lead path, after passing through the last tap coil W-1 in the series chain in the current lead for that tap number, is terminated in a ground connection, as shown by the grounded lead 166, FIG. 10, for the "EXCLUSIVE OR" gate E2, and similar grounds for the current leads from the "EXCLUSIVE OR" gates E4, E6, E10, E12, E13, and E14, FIG. 10, and the gates E3, E5, E7, E9, and E11, FIG. 11.

The PI/TI code switch group 34, FIG. 10, for the PI/TI comparer 126 contains the twelve single pole, separately operable, manual, code switches at the twelve pulse positions 2 to 7 and 9 to 14, respectively. One contact of each switch is connected to the grounded lead 192, and the other contact of the switch for any one of the pulse positions in the group 2 to 7 and 9 to 14, is connected to the switch input leg of the "EXCLUSIVE OR" gate of the corresponding number, thus the switch 175 for pulse position 2 connects to the switch input leg 174 of the "EXCLUSIVE OR" gate E2. The PI/TI code switches, not shown, in the code switch groups 30 and 32, FIG. 3, for the PI/TI comparers 124 and 125 are similar to and have similar connections to those in the code switch group 34, FIG. 10. The five SI code switches for pulse positions 3, 5, 7, 9, and 11, respectively, in the SI code switch group 35, FIG. 11, are similar to and have connections similar to those for the corresponding pulse positions 3, 5, 7, 9, and 11 respectively, in the code switch group 34, FIG. 10.

The outputs of the "EXCLUSIVE OR" gates in FIG. 10 are arranged in pairs, the output lead 193 of gate E3 being connected to the output lead 177 of gate E2 to feed an output pulse from either gate forwardly through the crystal diode rectifier 194 to the output lead 195 of the comparer 126. Similarly, the outputs of gates E4 and E5 are combined to feed a pulse forwardly through the crystal diode rectifier 196 to lead 195, and the outputs of gates E6 and E7 are combined to feed a pulse forwardly through the crystal diode rectifier 197 to lead 195, so that any one of the six gates E2 to E7, in a group representing a first half of the twelve tap numbers 2 to 7, and 9 to 14, can feed an output pulse to the comparer output lead 195. The diodes 194, 196, and 197, with their cathodes connected together and to ground through the load resistor 198, thus provide a three input leg "OR" gate having the output lead 195.

The outputs of the six "EXCLUSIVE OR" gates E9 to E14 in the group representing the second half of the comparer 126, are connected in pairs similarly to the first half, the crystal diode rectifiers 199, 200, 201, with their cathodes connected together and to ground through the

load resistor 202, providing a three input leg "OR" gate for feeding an output pulse from any of the gates E9 to E14 to the output lead 203 of the comparer 126.

The output connections for the PI/TI comparers 124 and 125 are similar to those described for PI/TI comparer 126, the comparer 124 having the output leads 204 and 205, and the comparer 125 having the output leads 206 and 207.

Since the SI codes employed in the present invention, as listed in Table No. 1, contain no pulse in any of the seven channels 2, 4, 6, 10, 12, 13, and 14, corresponding to tap numbers 2, 4, 6, 10, 12, 13, and 14, respectively, each of the voltage leads 208 to 214, respectively, representing these seven channels is employed as a reply code checking channel to test the code for the invalid presence of a pulse therein. Each of the code checking voltage leads 208 to 214, includes a crystal diode rectifier 215 to 221, respectively, for feeding a pulse in a forward direction to the output leads 222 to 228, respectively.

The outputs of the diodes 215 to 221, and the "EXCLUSIVE OR" gates E3, E5, E7, E9, and E11, FIG. 11, are arranged in pairs, as were the outputs of the "EXCLUSIVE OR" gates in FIG. 10, the output lead 229 for gate E3 being connected to the output lead 222 of diode 215, to feed a pulse from either lead forwardly through the crystal diode rectifier 230 to the output lead 231 of the comparer 127. Similarly, the outputs of diode 216 and gate E5 are combined at lead 223 to feed a pulse forwardly through the crystal diode rectifier 232 to lead 231, and the outputs of diode 217 and gate E7 are combined at lead 224 to feed a pulse forwardly through the crystal diode rectifier 233 to lead 231, so that any one of the six outputs thus combined, and representing a first half of the twelve tap numbers 2 to 7, and 9 to 14, can feed an output pulse to the comparer output lead 231. The diodes 230, 232, and 233 with their cathodes connected together and to ground through the load resistor 234, thus provide a three input leg "OR" gate having the output lead 231. Furthermore, each of the diodes 215, 216, and 217, may be regarded as providing an independent input leg of a three input leg "OR" gate for the code checking channels 2, 4, and 6, by virtue of their connections through the diodes 230, 232, and 233 to the output lead 231.

The outputs of the diodes 218 to 221 and the "EXCLUSIVE OR" gates E9 and E11, representing the second half of the twelve tap numbers 2 to 7, and 9 to 14, are connected in pairs similarly to the first half, the diode rectifiers 235, 236, and 237 with their cathodes connected together and to ground through the load resistor 238, providing a three input leg "OR" gate through which any one of the six outputs, thus combined, may feed a pulse to the comparer output lead 239. Each of the diodes 218 to 221 may be regarded as providing an independent input leg of a four input leg "OR" gate for the code checking channels 10, 12, 13, and 14, by virtue of their connections through the crystal diode rectifiers 235, 236, and 237, to the output lead 239.

From the foregoing description of the comparers 124 to 127, FIG. 3, it will be evident that a pulse reaching any one of the comparer output leads 204 to 207, 195, 203, 231, or 239, signifies that a reply train of pulses applied to the input lead 46, FIG. 3, has passed the test of containing properly positioned bracket pulses at tap numbers 1 and 15 on the delay line 56, 57, but has failed to pass the test of the comparer whose output contains the pulse. In each case, the presence of the comparer output pulse, indicates that a code bit on at least one of the twelve tap numbers 2 to 7, and 9 to 14, disagrees with the code set up by the code switches for that comparer.

In the case of the PI/TI comparers 124, 125, and 126, a comparer output pulse signifies disagreement of at least one code switch bit with the corresponding tap number bit. In the case of the SI comparer 127, a comparer output pulse signifies either disagreement of at least one

code switch bit with the corresponding tap number bit, or disagreement of at least one tap number bit with any valid SI code, because of the presence of an invalid pulse in one of the seven checking channels corresponding to tap numbers 2, 4, 6, 10, 12, 13, and 14. A comparer output pulse is always employed to inhibit an aircraft identification indication.

When a bracket coincidence (B.C.) pulse is present on lead 81, FIG. 3, and consequently on leads 139 and 140 extending to other figures, the absence of a pulse on the output leads of any one comparer, signifies that the code bits in the twelve channels corresponding to taps 2 to 7, and 9 to 14 agree with the code set up by the code switches for that comparer.

FIG. 4 shows circuits for the gating and control of signal pulses to be used for producing an indication that the reply code applied to any given one of the comparers 124 to 127 agrees with the verification code set up by the code switches for that comparer. The circuits are arranged to inhibit such indication producing pulses when the reply code disagrees with the switch code.

The four summing "OR" gates 241 to 244, FIG. 4, having the output leads 245 to 248, respectively, correspond to the four comparers 124 to 127, FIG. 3, respectively. Each of these summing "OR" gates has three input legs. The first input leg 249 of gate 241, FIG. 4, and the corresponding first input legs of gates 242, 243, and 244 are connected in parallel to the lead 433 for the delay line tap number 8 pulse fed through tap gate 97, FIG. 3, and cathode follower 429 to lead 433. The second and third input legs of each of the summing "OR" gates 241 to 244, respectively, are connected, respectively, to the two output leads of the comparer corresponding to that summing "OR" gate, as in the case of the second and third input legs of gate 241 which are connected, respectively, to the output leads 204 and 205 of the PI/TI comparer 124, FIG. 3. The output pulse from each of the summing "OR" gates 241 to 244 is employed as a "NO" pulse to inhibit the production of a "YES" pulse which in turn is employed to produce an indication signifying identification of an interrogated aircraft.

Each of the summing "OR" gate output leads 245 to 248, respectively, connects to the input of a separate one of the "NO" blocking oscillators 250 to 253, respectively, each having the circuit B.O.(E) for regenerating the "NO" pulse applied to its input and feeding the regenerated pulse to its output lead 254 to 257, respectively. Each of the "NO" blocking oscillator output leads 254 to 257, respectively, provides an inhibiting input leg connection of a separate one of the similar control "AND" gates 258 to 261, respectively. Each of these gates has four input legs, as shown by the input legs A, B, C, and D of gate 258, the first and second legs, A and B, being shown conventionally as inhibiting legs, and the third and fourth legs, C and D, being shown as enabling legs. Each of the control "AND" gate output leads 262 to 265 connects to the input of a separate one of the "YES" blocking oscillators 266 to 269, respectively, each having the circuit B.O.(A) similar to the B.O.(A) circuit 82, FIG. 9, and having the output leads 270 to 273, respectively, for feeding a "YES" pulse to the passive mixer, FIG. 5.

The B.O.(E) circuit of the "NO" blocking oscillator 250, FIG. 4, is similar to that of the B.O.(A) circuit 82, FIG. 9, except that in the blocking oscillator circuit 250, FIG. 4, a noise suppressing capacitor 274 connects the input lead 245 to ground, and except that the output lead 254 connects through the capacitor 275 to the anodes of the blocking oscillator triodes instead of being connected directly to the cathode of the output triode as in the blocking oscillator 82, FIG. 9. Since the output lead 254 connects with the anodes of the blocking oscillator 250, the output pulse is negative.

The SI trigger pulse train 276, FIG. 4, and a combined PI/TI trigger pulse train 277, derived from the interrogator 43, FIG. 1, are used to control the gating of

pulses by the control "AND" gates 258 to 261. These triggers, either SI alone, or interlaced SI and PI, or SI and TI, are initiated by the external interrogator circuits, now shown. The SI trigger pulses 276, and the PI/TI trigger pulses 277 recur at the radar pulse repetition frequency of 400 cycles per second. The SI trigger pulses 276 are shown by the dotted lines 293 to be timed about half way between the PI/TI trigger pulses 277.

The SI trigger 276 is applied to the lead 278 and fed through the capacitor 279, across the grounded resistor 280, and through the resistor 281 to the input of the cathode follower 282, having the circuit C.F.(C), shown in the cathode follower 429, FIG. 3, and having the output lead 283, FIG. 4, which feeds the SI trigger forwardly through the crystal diode rectifier 284, shunted by the resistor 285, to the lead 286 to the grid of the left triode of the two triode, code selector flip-flop 287 which is of conventional flip-flop design. The resistor 285 provides a high resistance leak path for discharging the capacitor 288 in the input of the flip-flop 287, while the diode 284 provides a low resistance forward path for the SI trigger, and a high resistance to suppress reactions of the flip-flop 287 in an inverse direction through the diode. The PI/TI trigger 277 is applied to the lead 289 and fed to the lead 290 to the grid of the right triode of the flip-flop 287, the cathode follower 291 with its output lead 292 and the other circuit elements between the leads 289 and 290, being similar to those described between leads 278 and 286.

The SI and PI/TI triggers 276 and 277, applied alternately to the two input leads 286 and 290 of the flip-flop 287 cause the flip-flop to assume first one and then the other of its two stable states, depending upon which trigger is last present. When the last trigger is an SI pulse on input lead 286, the left triode of the flip-flop 287 conducts, thereby causing the anode voltage of the left triode to drop, while the anode current of the right triode is cut off, thereby producing a high positive anode voltage. The resulting positive pulse 295 on the flip-flop output lead 294 is called the SI gate pulse. These conditions are reversed when the PI/TI trigger appears on the input lead 290, thereby removing the SI gate from the flip-flop output lead 294, and producing a high positive voltage pulse 296, called the PI/TI gate pulse on the left triode anode and the flip-flop output lead 297 connected thereto. The time relation of the SI gate 295 on lead 294 and the PI/TI gate pulse 296 on lead 297, is shown by their juxtaposed positions.

The SI gate is fed by the lead 294 to the grid of the triode cathode follower 298, having the output lead 299 connected to the cathode thereof, and to the fourth input leg of the SI control "AND" gate 261. The PI/TI gate is fed by the lead 297 to the grid of the triode cathode follower 300, having the output lead 301 connected to the cathode thereof and, in parallel to the fourth input leg of each of the PI/TI control "AND" gates 258, 259, and 260. In the triode cathode follower 298, the resistor 302, connecting the cathode to ground, is shunted by the by-pass capacitor 303, and in the triode cathode follower 300, the resistor 304, connecting the cathode to ground, is shunted by the by-pass capacitor 305. The purpose of the by-pass capacitors is to present a low impedance to the "AND" gate during the inhibition period.

The resistor 281 through which the SI trigger is fed to the grid of the cathode follower 282, the resistor 306 through which the SI trigger is fed to the left triode of flip-flop 287, the resistor 307 through which the SI gate is fed to the grid of cathode follower triode 298, and similar resistors through which the input pulse is fed to the grid of triode 300, and the grid of the right triode in flip-flop 287, and the grid of the triode in cathode follower 291, also serve as buffers.

The control "AND" gate 258, which is similar to the gates 259, 260, 261, has one of the four crystal diode

rectifiers 308, 309, 310, 311, respectively, in each of the input legs A, B, C, D, respectively, these diodes having their cathodes connected to the input end of their respective legs, and their anodes connected together to the output lead 262 of the gate. The rectifier 312 clamps negative pulses to ground from output lead 262.

In control "AND" gate 258, the resistor 313 feeds current from the positive voltage terminal 314 to the lead 262 and forwardly through diodes 310 and 311 in input legs C and D, when no signal is present on these legs. The voltage divider consisting of the resistor 315 connected to the input leg A and in series with the resistor 316 connecting to ground, applies a back-bias voltage through the resistor 317 to the diode 308, thereby preventing current fed from the terminal 314 and through resistor 313 from passing through diode 308 when no signal is present on the input leg A. A high positive voltage normally on the lead 318 from the active operation circuits of FIG. 18, when no inhibiting signal is present thereon, back-biases the diode 309 sufficiently to prevent the flow of current from the terminal 314 through resistor 313 and forwardly through diode 309. When no inhibiting signal is present on the inhibiting input legs A and B, the effect of legs A and B on the legs C and D is negligible, and the legs C and D are free to operate as though the inhibiting legs A and B were not present.

When there is a positive input pulse on leg C simultaneously with a positive input pulse on leg D of control "AND" gate 258, and no signal is present on either inhibitor leg A or B, ordinary well-known "AND" gate principles apply, and a positive "YES" PI/TI pulse is produced on the "AND" gate output lead 262 during the period of coincidence of the input pulses on legs C and D.

The "NO" PI/TI pulse from blocking oscillator 250, serves as an inhibiting pulse to be applied to the first input leg A of control "AND" gate 258, and is a negative pulse which overcomes the positive back-bias normally applied to the diode 308 by the voltage divider 315, 316, thus making possible the flow of current from terminal 314 and resistor 313 forwardly through diode 308 for the duration of the "NO" pulse, thereby holding lead 262 at near ground potential. If we now assume that an inhibiting pulse is present on leg A during coincidence of enabling pulses on legs C and D, these enabling pulses are inhibited from producing a "YES" PI/TI output pulse on lead 262, because lead 262 is held close to ground potential by the inhibiting pulse.

In a similar manner, the "NO" PI/TI pulse from blocking oscillator 251 is fed to the first input leg of gate 259 and inhibits the production of a "YES" PI/TI output pulse from the gate 259. The "NO" PI/TI pulse from blocking oscillator 252 similarly inhibits the production of a "YES" PI/TI output pulse from the gate 260, and the "NO" SI pulse from the blocking oscillator 253 similarly inhibits the production of a "YES" SI output pulse from the gate 261.

An active inhibit pulse is fed over the lead 318, in parallel to the second input leg of each of the control "AND" gates 258 to 261, during the period of active operation of the system, to interrupt during that period the production of a "YES" PI/TI pulse by any of gates 258, 259, or 260, or the production of a "YES" SI pulse by the gate 261. The active inhibit pulse is a negative pulse which removes the back-bias on diode 309 in gate 258, and on the corresponding diode, not shown, in gates 259, 260, and 261, thereby holding the output leads 262 to 265, respectively, close to ground potential, thus acting similarly to the inhibiting pulse on leg A, and preventing the production of a "YES" pulse on any of these output leads.

The third input leg of each of the four control "AND" gates 258 to 261, as shown by the leg C of gate 258, is connected to the single lead 140 for the delayed bracket

coincidence (B.C.) pulse derived from the delay unit 133, FIG. 3, so that this leg is enabled in each of the four gates whenever the delayed B.C. pulse is present on lead 140.

The fourth input leg of each of the control "AND" gates 258, 259, and 260 is connected to the single lead 301 over which the PI/TI gate pulse is fed, and is enabled whenever the PI/TI gate pulse appears on lead 301. The fourth input leg of control "AND" gate 261 is connected to the lead 299 over which the SI gate pulse is fed, and is enabled whenever the SI gate pulse appears on lead 299.

When the bracket coincidence (B.C.) pulse appears on the input leg C of the gate 258, during the period of the PI/TI gate pulse, and there is no inhibition on leg A or B, a "YES" PI/TI pulse, representing the No. 1 PI/TI comparer 124, FIG. 3, is produced on lead 262 and fed to "YES" blocking oscillator 266 which fires and regenerates the "YES" PI/TI pulse, and feeds it over lead 270 to the passive video mixer in FIG. 5. Gates 259 and 260, when not inhibited, operate similarly to gate 258, to feed "YES" PI/TI pulses representing No. 2 PI/TI comparer 125, and No. 3 PI/TI comparer 126, respectively, over leads 271 and 272, respectively, to the passive video mixer, FIG. 5.

When the B.C. pulse appears on the third input leg of control "AND" gate 261, during the period of the SI gate pulse, and there is no inhibition of the first or second input leg, a "YES" SI pulse, representing the No. 4 SI comparer 127, FIG. 3, is produced on lead 265, and is fed to "YES" blocking oscillator 269, which in turn feeds the regenerated "YES" SI pulse over lead 273 to the passive video mixer, FIG. 5.

When the SI trigger appears on lead 286, the flip-flop 287 transfers to its other stable state, thereby cutting off the anode current of cathode follower triode 300 and removing the back-biasing previously produced on diode 311 by the PI/TI gate pulse. Since diode 311 is grounded through cathode resistor 304 of triode 300, there is a small current flow through this circuit, traced from positive terminal 314, through resistor 313, diode 311, and resistor 304 to ground. If the cathode by-pass capacitor 305 were not present, the next bracket coincidence pulse would cause the leg D to generate a noise pulse of a magnitude sufficient to trigger the "YES" blocking oscillator 266, because of the voltage divider action of the resistors 313 and 304.

In order to overcome this difficulty, the cathode resistor 304 is partially by-passed with the small capacitor 305 in order to prevent the noise pulse from appearing on lead 262 at the output of the gate 258. The capacitor 305 charges slowly when the B.C. pulse appears and integrates the noise pulse. The capacitor 305 discharges through resistor 305 when the pulse terminates. The combined action of the capacitor 305 in the partially by-passed cathode follower 300 and the removal of the cathode gate voltage by the flip-flop, completely inhibits the gate 258 until the next PI/TI trigger appears. The by-pass capacitor 303 across the cathode resistor 302 of the cathode follower triode 298 functions similarly to the capacitor 305 across resistor 304 of triode 300.

From the foregoing description of FIG. 4, it will be seen that the logic of the circuits employed for the passive operation is completed by the action of either the "YES" or "NO" SI blocking oscillators, or the "YES" or "NO" PI/TI blocking oscillators. A "YES" SI or PI/TI output is possible, therefore, only under the following conditions tested by the passive decoding circuits: (1) a correctly bracketed reply train of pulses is received in response to an interrogation; (2) the interrogation is a conventional passive interrogation and not an active interrogation; (3) the reply code agrees identically with the code set up by the comparer code switches; (4) no pulse is present in pulse position 8; (5) no pulse is present in pulse position 2, 4, 6, 10, 12, 13 or 14 in the case of an

SI reply code; and (6) no pulse is present in pulse position 2, 4, 6, 10, 12, or 14 in the case of a TI reply code.

Passive Video Mixer

The passive video mixer 320, FIG. 5, is provided in the decoder 20, FIG. 1, to make possible the selection for PPI display of any one, or several, of six sets of signal pulses available in the decoder. The pulses from any one source are referred to as being in a set, because a succession of repeated "YES" pulses or other interrogation reply pulses, is received during passive operation, there being one reply code from each of the successive passive interrogations of a given aircraft. Included in the six sets referred to, are three sets of "YES" PI/TI pulses to indicate agreement, respectively, of the three switch codes of the three PI/TI comparers 124, 125, and 126, with the corresponding PI/TI reply codes received, respectively, from three passively interrogated aircraft. A fourth set is a set of "YES" SI pulses to indicate agreement of the comparer 127 SI switch code with the corresponding SI reply code received from one or more passively interrogated aircraft having the same identity, SI, code. A fifth set is a set of bracket coincidence, B.C., pulses, there showing that a properly bracketed reply code has been received, regardless of whether or not, a "YES" PI/TI or a "YES" SI pulse is produced. The sixth set is a set of raw video pulses showing the pulses appearing on the delay line tap No. 15, FIG. 3, before any decoding operation is performed thereon.

The three sets of "YES" PI/TI pulses, No. 1, No. 2, and No. 3, respectively, are fed from FIG. 4 to FIG. 5, over leads 270, 271, and 272, respectively. The set of "YES" SI code pulses is fed over lead 273. The set of B.C. pulses is fed over lead 139, which may be traced from reset blocking oscillator 135, FIG. 3, and through FIG. 4 to FIG. 5. The set of raw video pulses is fed over lead 141, which may be traced from delay line tap 15, FIG. 3, and through FIG. 4 to FIG. 5.

The group of six mixer switches 36, FIG. 5, is provided to select from the available sets of pulses, those to be used for producing PPI indications. Each switch in the group 36 is a single pole, individually manually operable, normally closed switch, which is opened by the operator to select the set of pulses controlled thereby for display. One contact of each of the mixer switches 321 to 326, is permanently connected to grounded lead 327. The other contact of each switch 321 to 326, respectively, is connected to a separate one of the control lines 328 to 333, respectively, for selecting the desired input to the mixing circuits.

When all the control lines are grounded, all of the signal inputs are inhibited and none of the input signals are accepted through the mixing circuits. When one of the mixer switches is opened, the control line connected thereto is enabled and the associated signal input is gated through the mixer circuits. One or more signal inputs may be simultaneously selected by opening the appropriate mixer switches, and the resulting signals, fed to the mixer output lead 334, are then fed to the PPI units 40, 41, 42, FIG. 6, to produce passive interrogation indications therein. The passive mixer includes a single-shot pulse stretching multivibrator 335 for increasing the 1 microsecond "YES" PI/TI signals into 15 microsecond pulses, so that they may more easily be distinguished from other signals, and to indicate that they represent mixed or interlaced signals.

The signal "OR" gate 336 has the three input legs 337, 338, 339, respectively, connected through the resistors 340, 341, 342, respectively, to the PI/TI No. 1 lead 270, the PI/TI No. 2 lead 271, and the PI/TI No. 3 lead 272, respectively, and has the output lead 343, forming one of the two input legs of mixing "OR" gate 344, having the output lead 345, forming one of the two input legs of the output "OR" gate 346, having the output lead 334. The voltage limiter 347, of well-known design, clips the peaks

of positive output pulses on lead 334 to a uniform amplitude level by providing a low impedance path traced from lead 334 forwardly through the low resistance crystal diode rectifier 348 and the low impedance capacitor 349 to ground, for voltages on lead 334 exceeding the diode back-bias voltage. The back-bias voltage is applied across the capacitor 349, and may be adjusted to any desired value by the sliding contact 350 on the potentiometer 351.

The stretch mixing "OR" gate 352 has the three input legs 353, 354, 355, respectively, connecting through the resistors 356, 357, 358, respectively, to the leads 270, 271, 272, respectively, for "YES" PI/TI signals No. 1, No. 2, and No. 3, respectively, and has the output lead 359, connected to the two branch leads 360, 361, respectively, containing the resistors 362, 363, respectively. The leads 360 and 361 provide the two input legs of the stretch input "OR" gate 364, having the output lead 365, connected to the input of pulse stretcher 335, having the output lead 366, which couples through the capacitor 367 to the input lead 368 of cathode follower 369, having the circuit C.F.(C), as shown in cathode follower 429, FIG. 3. The lead 368 connects to ground through the grid leak resistor 370. The output of cathode follower 369 is coupled through the capacitor 371 to the output lead 372, having the connection through the resistor 373 to ground, and being connected through the resistor 374 to the lead 375 forming one of the two input legs of mixing "OR" gate 344.

The signal "OR" gate 376 has the three input legs 377, 378, 379, respectively, connected through the resistors 380, 381, 382, respectively, to the input leads 273, 139, 141, respectively, for the "YES" SI pulses, the B.C. pulses, and the raw video pulses, respectively. The output lead 437 of gate 376 forms one of the two input legs of the output "OR" gate 346.

The "YES" PI/TI No. 1 input leg 353, FIG. 5, of the "OR" gate 352 connects forwardly through the diode 383 with the PI/TI No. 1 control lead 328, and the corresponding input leg 337 of "OR" gate 336 connects forwardly through the diode 384 with lead 328. Similarly, the PI/TI No. 2 input leg 354 of "OR" gate 352 connects forwardly through the diode 385 to the PI/TI No. 2 control lead 329, and the corresponding input leg 338 of "OR" gate 336 connects forwardly through the diode 386 to lead 329, and the PI/TI No. 3 input leg 355 of "OR" gate 352 connects forwardly through the diode 387 with control lead 330, and the corresponding input leg 339 of "OR" gate 336 connects forwardly through the diode 388 with lead 330. Similarly, the SI lead 377, the B.C. lead 378, and the raw video lead 379, respectively, connect forwardly through the diodes 389, 390, 391, respectively, with the control leads 331, 332, 333, respectively. The input legs 360 and 361 of "OR" gate 364 connect forwardly through diodes 392 and 393, respectively, with control leads 331 and 332, respectively.

The diodes 383 to 393 are of the crystal rectifier type, having a very high resistance in an inverse direction and a low resistance in a forward unbiased direction. The lead 394 having a 65 volt positive back-biasing potential thereon, connects through the high resistance resistors 395 to 400, respectively, with the control leads 328 to 333, respectively.

When the mixer switches 36 are all closed, the control leads 328 to 333 are grounded, and the resistors 395 to 400 absorb the full back-bias voltage. Furthermore, when all the switches 36 are closed, all of the input legs of the "OR" gates 336, 352, 364, and 376, are grounded through the low forward resistance of the diodes 383 to 393, and each input leg is thus inhibited from passing any signal to the "OR" gate output. When any mixer switch, such as switch 323, is open, the ground is removed from the corresponding control lead 330, and the full back-bias voltage is applied to the diodes connected to that control lead. When switch 323 is open, diodes 387 and 388 become back-biased and act as high

impedance circuits to signals on PI/TI No. 3 lead 272, and thus do not divert the signals to ground as when switch 323 was closed, but permit the PI/TI No. 3 one microsecond pulses to pass through input leg 339 of gate 336, from which the signals are fed through gates 344, and 346 to the mixer output lead 334. The PI/TI No. 3 signals on the input leg 355 of gate 352 pass over lead 359 and through the parallel resistors 362 and 363 which are grounded by the switches 324 and 325, respectively, through the low forward resistances of the diodes 392 and 393, thus preventing these signals from reaching the pulse stretcher 335.

If either the "YES" SI switch 324, or the B.C. switch 325 is now opened, the ground previously applied by that switch to the input leg 360 or 361 of gate 354, is removed, and the signals pass over lead 365 to pulse stretcher 335 wherein the 1 microsecond pulse is lengthened to a 15 microsecond pulse which is fed through cathode follower 369, over lead 375, and to gate 344 where it is mixed with the one microsecond pulse applied thereto from gate 336, previously described, the overlapped unstretched and stretched pulses being fed through gate 346 to output lead 334.

It will be seen from the FIG. 5 circuits, as described, that neither a "YES" SI pulse, nor a B.C. pulse can be fed to the pulse stretcher 335, but that only the "YES" PI/TI pulse No. 1, No. 2, or No. 3 can be stretched in the passive mixer 320.

There are four main types of passive mixer outputs that are generally employed. These outputs are obtained by opening the appropriate switches, and consist of—(1) the "YES" SI code alone, as set up by the SI code switches 35, FIG. 3; (2) one or more of the three "YES" PI/TI codes as set up by the code switches 30, 32, or 34; (3) the B.C. pulse combined with one or more of the three stretched "YES" PI/TI codes; and (4) the "YES" SI code combined with one or more of the three stretched "YES" PI/TI codes.

In the pulse stretcher single-shot multivibrator 335, the crystal diode rectifier 401, having its anode grounded and its cathode connected to the grid of the input triode 402, clamps the grid to ground, and the crystal diode rectifier 403, having its cathode connected to the triode 402 grid, presents a low impedance to positive input pulses, and a high inverse impedance to negative potential noise disturbances on the grid, thereby preventing undesired noise reactions on circuits connected to the stretcher 335 input.

Passive System Indicators

The output lead 334, FIG. 5, for the passive video mixer 320 connects with the inputs of the similar video, cathode followers 404, 405, 406, FIG. 6, which are located inside the decoder 20, and have the output leads 407, 408, 409, respectively, connected to the similar range mixers 410, 411, 412, respectively, located respectively in the No. 1 control and indicator 29, the No. 2 control and indicator 31, and the No. 3 control and indicator 33. The output leads 37, 38, 39, of the range mixers 410, 411, 412, respectively, connect with the No. 1, No. 2, and No. 3 PPI display units 40, 41, 42, respectively, which constitute passive system indicators to show the results of the passive interrogating, decoding, and code checking operations, by indicating the position of an aircraft whose identification code has been found to be valid and in agreement with the switch code set up by the operator.

The video cathode followers 404, 405, 406, have the circuit shown for cathode follower 404, which has a capacitor 413 coupling the lead 334, to the lead 414 and through the resistor 415 to the grid of the triode 416. The resistor 417 connects the cathode of triode 416 to ground. The resistors 418 and 419, in series with resistor 415, connect the grid of triode 416 to ground. The crystal diode rectifier 420 having its cathode connected to lead 414, is back-biased over lead 421 by

the voltage across the low impedance capacitor 422, and clamps negative pulses, exceeding the back-biasing voltage, to ground through the capacitor 422.

The brightness control potentiometer 423, FIG. 6, by the sliding contact 424, adjusts the back-biasing voltage across capacitor 422 and the clamping level of diode 420, and also adjusts the negative bias potential applied to the grid of triode 416 to control the amplitude of pulses on output lead 407, and thus the brightness of the displays produced on the PPI unit 40 by pulses fed to the cathode follower 404. The video cathode follower 404 has its output lead 407, connected to the cathode of triode 425 in the cathode follower range mixer 410, having the cathode-to-ground resistor 426 and the output lead 437 coupled through the capacitor 438 to the lead 37 to the No. 1 PPI unit 40.

The cathode follower range mixer 410 has the input lead 439 for the range mark pulses and the strobe pulses supplied from the active interrogation circuits in FIG. 16, the range mark pulses being utilized only in preparation for or during active interrogation operations. Lead 439 is connected through the coupling capacitor 449 in series with the resistor 441, to the grid of triode 425. The potentiometer voltage across capacitor 422 is fed through resistors 442 and 441 in series to the grid of triode 425, so that the brightness control potentiometer 423 controls the negative potential bias on the grid of the range mixer triode 425 and on the grid of video cathode follower 404, and thereby controls—(1) the brightness of the passive interrogation PPI blips; (2) the brightness of the range mark circle used before an active interrogation is made to select the passive PPI blip representing the aircraft to be actively interrogated; and (3) the brightness of the strobe produced in the PPI display during active interrogation to distinctively label the selected blip on the PPI and to indicate that the operator initiating an active interrogation has seized control of the active interrogating circuits. A description of the active operating system follows that of the passive operating system herein. The range mark pulses, though present during passive operation of the system, are not utilized during passive operations, except when preparation is being made for an active interrogation.

A brightness control potentiometer, corresponding to potentiometer 423 in range mixer 410, is also provided (not shown) in each of the range mixers 411 and 412 and feeds a brightness control voltage over leads 443 and 444, respectively, to video cathode followers 405 and 406, respectively.

FIG. 12 shows an example of a PPI display produced during passive interrogating operations. The operator has set up an SI code, for Security Identity, by his code switches 35, FIGS. 3 and 11, knowing that this SI code has been assigned, by prearrangement, to all friendly aircraft. He also has selected a "YES" SI indication by opening the appropriate mixer switch 324, FIG. 5. If no other code were set up by the code switches 30, 32, or 34, FIG. 3, all of the blips 445 to 451 would be of one microsecond duration and would appear as similar dots, and we may assume that the operator first had followed this plan, and then wished to locate two aircraft expected to have individual Personal Identity, PI, identification codes. These PI codes were then set up in code switches 32 and 34, FIG. 3, and the appropriate mixer switches 322 and 323, FIG. 5, were opened to select the indications of the result of the comparisons, by comparers 125 and 126, of the received PI codes with the respective PI switch codes.

Since the mixer switch selection of both a "YES" SI and a "YES" PI indication causes the PI pulse to be stretched from its normal 1 microsecond length to a 15 microsecond length, the location of the two desired aircraft is distinctively indicated by the two lines or elongated blips 450 and 451 in the PPI display. By manipulating one of the mixer switches 322 or 323 the blip cor-

responding to that switch is shortened to a dot or changed back to a line on the next radar sweep and clearly identifies the particular PI code set up by the corresponding PI code switches for that aircraft. At each radar scan produced on the PPI the new positions of the PPI blips indicate the new locations of the moving aircraft being passively interrogated.

It will be understood from the foregoing description of the passive system that if we now assume the same conditions as shown in FIG. 12, and that SI mixer switch 324 is then changed from an open to a closed position, and B.C. switch 325 is then selectively opened, no new SI blips would appear on the next radar scan, although the PI line-blips 450 and 451 would reappear, because of the PI mixer switches 322 and 323 remaining selectively open, and the B.C. switch 325 being selectively open, and the fact that a combined selection of PI or TI, and of B.C., by the mixer switches 36, results in the PI or TI pulses being stretched.

The range mark circle 452, FIG. 12, is produced by the range mark pulses fed from FIG. 16, to lead 439, FIG. 6, and mixed on lead 437 with the pulses fed over lead 407 from the video cathode follower 404.

Active System, General Description

The active operating system is used when a PPI operator wants to know the PI code of a particular aircraft represented by a passive operation blip in his PPI display.

When an active interrogation is to be made, the PI/TI mode selecting switch 453, FIG. 30, on the operator's control and indicator panel 454 is first turned to the position for selecting the desired mode. Secondly, he adjusts the range mark control 455 on his control and indicator panel 454 to the range shown by the PPI blip, representing the aircraft to be interrogated, such as the blip 456, in the FIG. 13 PPI display, so that the range mark circle 457 in the PPI display is in line with the blip 456. Up to this time, the strobe 458 has not yet been produced. Thirdly, he completes the selection of the blip 456 of the aircraft to be interrogated, by making an azimuth selection of the blip by watching the radar sweep line, shown as the dotted line 459, FIG. 13, and depressing the strobe button 460, FIG. 30, just before the sweep line comes to the blip 456, FIG. 13. The active cycle of operations then becomes entirely automatic, and the strobe 458 is immediately produced as a square area of intensified light surrounding the selected blip 456 to serve as a signal, as referred to hereinafter.

FIG. 14 shows the active operation circuits in the decoder 20 in relation to those in the control and indicator No. 1 unit 29, and shows the connections therebetween. The circuits of the control and indicator No. 2 (C&I-2) unit 31, FIG. 1, and of the control and indicator No. 3, (C&I-3) unit 33, FIG. 1, are similar to those of the control and indicator No. 1 unit 29, FIG. 14. The connections from the decoder 20 to C&I-2 and to C&I-3, as indicated in FIG. 14, are similar to those from the decoder 20 to the control and indicator No. 1 unit 29. The description of the active operation will be directed mainly to the control and indicator No. 1 unit, referred to as C&I-1, and the related circuits in decoder 20, as illustrative of the other control and indicator circuits and their operation.

Master relay block 461, directly or indirectly controls contacts in the circuits in blocks 461 to 469, and 473, FIG. 14, and makes it possible for the main active interrogation circuits in the decoder 20 to serve as centralized circuits available to any one of the operators at the three controls and indicators 29, 31, 33, FIG. 1, so that duplication of the centralized circuits for each of the operators is avoided, and the total cost, weight, and complication of the equipment is greatly reduced. The schematic circuits in blocks 461 to 469, FIG. 14, are shown in FIGS. 19 to 27, respectively; those in blocks 410 and 470 are shown in FIG. 6; those in block 471, in FIGS. 15 and 16;

those in block 473, in FIGS. 17 and 18; those in block 474, in FIGS. 3 and 4; and those in block 505, in FIGS. 28 and 29.

It will be assumed that the operator at control and indicator No. 1 unit 29, FIGS. 1 and 14, without interference by the other operators, has completed the final necessary step for starting an active interrogation, by depressing the stroke button 460, FIGS. 30 and 14, as referred to above. Depression of stroke button 460 feeds a pulse over lead 430 and energizes master relay 1M and interlocking circuits in the master relay block 461, which exclude the other operators from exercising any interfering control over the main active interrogation circuits in decoder 20 for the full duration of the active interrogation cycle started by C&I-1 unit 29, which lasts for about 0.2 second.

Master relay 1M in block 461, FIG. 14, by its contacts in block 469, selects the strobe and range gate generator 471 in C&I-1 unit 29, and causes it to generate a series of range gate and strobe pulses. The strobe pulses are fed over lead 439, FIG. 14, to the range mixer 410, and over lead 37 to the PPI unit 40, FIG. 6, to produce the strobe 458, FIG. 13, around the passive blip 456, which was produced by a passive operation pulse on lead 334, FIG. 14, fed through the video cathode follower block 470, to lead 407, and through the range mixer 410 to the PPI unit 40, FIG. 6. The block 469 feeds a sync pulse over lead 501 and a strobe signal pulse over lead 502 to generator block 471, which in turn feeds a pulse representing the end of an azimuth pulse over lead 503, and a range gate pulse over lead 504 to block 469.

The strobe has several functions, one being to inform the operator that he has seized active control and has not been prevented from doing so, as he could have been, if he had pressed his strobe button during an active interrogation cycle previously started by another operator. The strobe also shows the operator the area from which a reply will be accepted in response to the active interrogation, because the active decoding circuits are so gated that they will accept pulses during only those parts of the PPI scan included within the strobe, thus preventing an active code indication by any aircraft outside the area represented by the strobe.

Block 466, FIGS. 14 and 24, contains a PI mode order lead 653, FIG. 24, and a TI mode order lead 654, extending to the interrogator 43, FIG. 1, for selective connection to that one of the control and indicator units No. 1, 2, or 3, originating an active interrogation, so that a mode signal may be fed therefrom to the interrogator to inform the interrogator whether to make the interrogation in the PI or the TI mode. The mode signal is applied to the PI mode lead 496 or the TI mode lead 497, FIG. 14, depending upon which of these modes has been selected by the mode selecting switch 453, FIG. 30, and in block 505, FIG. 14. When the master relay 1M pulls up in block 461, FIG. 14, its contacts, in block 466, connect the PI and TI order leads of the interrogator 43 with the PI lead 496 and the TI lead 497, respectively, from C&I-1 unit 29, thereby feeding the mode signal to the interrogator to prepare it for making the active interrogation in the desired mode. The active interrogation is not transmitted to the aircraft yet, but waits until a start signal, referred to hereinafter, is given to the interrogator.

A series of range gate pulses from the generator 471, FIG. 14, is fed through the block 469 and lead 472 to the countercircuits block 473. The gates and controls in block 474 supply bracket coincidence and PI/TI trigger pulses to the countercircuits 473. The range gate pulses control certain gatings of bracket coincidence and other pulses in the countercircuits 473 for checking the reply from an aircraft selected for active interrogation, and unless three successive replies, in regularly timed sequence and with correctly bracketed pulses, are received from that aircraft, following the pressing of the strobe

button 460, the start signal for initiating the active interrogation is inhibited by the circuits in block 473. These circuits not only determine inhibitions due to unacceptable aircraft replies, but determine the time of transmission of an active interrogation to the aircraft.

The active interrogation is transmitted in response to a start signal produced in block 473 by the electronic count of three bracket coincidence pulses, in regularly timed sequence, received from the aircraft to be actively interrogated, following the pressing of the strobe button 460, FIG. 14. These three pulses are a part of a series of pulses received in response to the series of passive interrogations started prior to depression of the strobe button and continued thereafter until the third bracket coincidence pulse initiates the active interrogation, thereby interrupting the passive interrogations and inhibiting the production of the passive "YES" pulses used for making PPI passive indications. When the active interrogation cycle is completed, the series of passive interrogations is automatically resumed and the active inhibition of the passive indications is withdrawn.

The first delay relay D in block 464, is a delay-on-make relay, and has its energizing circuit prepared by closure of contacts of master relay 1M, when pulled up. The fourth B.C. pulse on lead 475 shifts a flip-flop multivibrator in block 464, thereby producing a pulse in coincidence with the fourth range gate pulse on lead 476, from countercircuits 473, and causes delay relay D to energize, and after its scheduled delay, to close one of its contacts in the indicator relay selector block 462 to complete the energizing circuit for the indicator signal relay 1S, which is also a delay-on-make relay, the circuit of which was previously prepared by the pulling up of master relay 1M. Indicator signal relay 1S in block 462, has contacts in block 465 for feeding current over lead 494 to the code indicator lamps, or over lead 495 to the error indicator lamp in block 505.

If three B.C. pulses fail to appear in regular timed order after strobe button 460 is depressed, the countercircuits in block 473 are inhibited from counting a third B.C. pulse, thereby inhibiting the production of a fourth B.C. pulse on lead 475 and a fourth range gate pulse on lead 476, thereby preventing relay D in block 464 and relay 1S in block 462 from pulling up, and preventing the code indicator lamps or the error indicator lamp in block 505 from making a display.

The fourth range gate pulse, when not inhibited as just referred to, is fed over lead 477 to block 463 wherein an active decoding thyatron is provided for each of the twelve tap voltage leads from FIG. 3. The thyatron is fired when one of its two grids is fed by the fourth range gate pulse while the other of its grids is fed by a tap voltage pulse derived from one of the tap Nos. 2 to 7 and 9 to 14, FIG. 3. The anode of each of the twelve thyatrons connects separately through separate contacts, respectively, of pulled up master relay 1M, to leads 482 to 493, respectively, FIG. 14, and to twelve active decoder relays, respectively, in block 505. Each decoder relay is thus responsive to a voltage pulse from a different one of the twelve tap Nos. 2 to 7 and 9 to 14, FIG. 3. The reply code pulses on these taps, thus cause the decoder relays to set up a corresponding code, and the decoder relay contacts translate this code into a direct symbol indication of the aircraft's PI or TI code, this being displayed by the code indicator 509, FIG. 30.

The PI bridge selector block 457 contains contacts closed by the pulling up of relay 1M in block 461 to energize the PI code checking bridges in block 505 over leads 498 and 499. Each half of each PI code contains three "0" bits and three "1" bits. A bridge circuit is provided for each half of the twelve decoding relays. The bridge for each resulting group of six decoder relays is so arranged that the decoder relay contacts for that group produce a balanced bridge, so that no unbalance signal is produced, when any three of the relays in the

group are pulled up and the other three remain de-energized.

If the code which sets up either or both groups of six decoder relays proves to be invalid by having more or less than three pulses therein, an unbalance signal is produced and fed over lead 500 to the bridge unbalance amplifier block 468 which feeds an amplified signal over lead 506 to block 462, causing the error relay 1E to pull up and transfer the active indicator current in block 465 from the code lamps to the error lamp in block 505, thereby preventing the lighting of the code lamps, and lighting the error lamp 507, FIG. 30, to indicate an invalid reply code.

The active circuits, except for those of the decoder relays, and the code indicator and error indicator of the operator making the active interrogation, are automatically reset to normal by the pulling up of a reset relay R in block 454 in response to a predetermined delayed reset pulse in response to a fourth B.C. pulse, or, if a fourth B.C. pulse fails to appear, the reset relay R is pulled up in response to the end of the azimuth gate pulse fed from block 471 over lead 503, and through block 469 to lead 510 to block 464.

Indicator signal relay 1S and error relay 1E, after pulling up, are latched over the holding circuit lead 481, fed by current through back contacts of reset button 508. These back contacts also feed current over the holding circuit lead 479 for latching the decoder relays in block 505. These holding circuits maintain the code indicator or error indicator on display after the active interrogation cycle has been completed and the main active circuits have been automatically restored to normal, thereby providing time, which would otherwise be inadequate, for the operator to observe his indicators without delaying the access of the other operators to the active interrogating system. Reset button 508, when depressed, opens the holding circuit leads 479 and 481, so that relays 1S and 1E in block 462, the decoder relays in block 505, and the code and error indicator circuits are restored to normal.

Active System, Detailed Description

The operator at any one of the PPI units 40, 41, or 42, FIG. 1, may initiate an active interrogation of an aircraft, represented by a passive blip on his PPI unit, to obtain a direct indication of the PI or the TI code of the aircraft.

Each operator has hand controls for initiating an active interrogation, and has a code indicator for displaying to him the PI or TI code of the aircraft, and an error indicator to tell him if an invalid reply code is received. These hand controls and the indicators are located on the panel 454, FIG. 30 of his control and indicator unit 29, 31, or 33, FIG. 1.

The panel 454 has PI/TI selector switch 453, FIGS. 30, 28, and 29, for selecting an active interrogation in either the PI mode or the TI mode. When the switch 453, is in the PI position, the PI switch indicator lamp 511 lights over the upper contacts of the switch arm 512, FIG. 29, from the D.C. source 513, and in the TI position, the TI switch indicator lamp 514 lights over the lower contacts of switch arm 512. The range mark control 455, FIG. 30, adjusts a movable range mark circle on the PPI to the range of the blip representing the aircraft to be actively interrogated. The PPI brightness control 515 controls the slide 434, FIG. 6, of the potentiometer 423 to simultaneously adjust the brightness of the blip 456, FIG. 13, the range mark 457, and the strobe 458. The strobe button 460, FIG. 30, is pressed as the final step in initiating an active interrogation.

The code indicator 509, FIG. 30, produces a direct symbol indication of the PI or TI code of the actively interrogated aircraft. The error indicator 507 lights up, if the PI reply code from an actively interrogated air-

craft proves to be invalid by failing to meet the PI code requirements that each half of the reply code shall have three bits in the form of pulses and three bits in the form of absences of pulses. The reset button 508 is used after a display by code indicator 509 or error indicator 507, to restore to normal the decoder relays and the code and error indicator circuits of the operator who initiated the active interrogation.

When the operator decides to make an active interrogation, for example, of the aircraft represented by the blip 456, FIG. 13, the strobe 458 being not yet present as shown, he first sees that the PI/TI mode selector switch 453, FIG. 30, is turned to the PI or the TI mode in which he desires the aircraft code to be indicated. Secondly, he adjusts the range mark control 455 to bring the range mark circle, which may have been in the position 452, FIG. 12, to the range position 457, FIG. 13, in line with the blip 456, to correspond with the range of the blip. Thirdly, he watches the radar sweep line 459 of his PPI display and completes the selection of the blip 456 by timing the depression of his strobe button 460, FIGS. 30 and 14, to match the azimuth position of the sweep line to that of the blip, this being done by depressing the strobe button just before the sweep line reaches the blip.

Master Relays for Active System

Control of the active system of interrogation is accomplished by three master relays 1M, 2M, and 3M, FIG. 19, and the active circuits associated therewith, as indicated diagrammatically in FIG. 14. The master relays are located in the decoder 20. Master relay 1M is associated with control and indicator No. 1, 2M with C&I-2, and 3M with C&I-3. Each of the master relays 1M, 2M, and 3M, or a relay controlled thereby, has contacts in each of the blocks 461 to 469, and 473, FIG. 14, for controlling circuits in these blocks.

The PPI operator of a particular control and indicator unit gains control over the active system by depressing his strobe button 460, FIG. 14, when he initiates an active interrogation, thereby energizing his master relay and preventing the other two master relays from being later energized during the already started interrogating cycle. When one master relay is energized, the other two operators must wait until the prior interrogation has been completed before the next interrogation can be initiated. The time interval for an operator to stand by, while a prior interrogating cycle is being completed, is about 0.2 of a second. When an operator succeeds in energizing his master relay, he gains control over the active system long enough for the active interrogation to be transmitted to the aircraft being interrogated, and for the reply code to be received, decoded, and displayed. Interlocking circuits are provided in the decoder 20 to prevent interruption of one operator's interrogation cycle by another operator.

The normally closed contacts of strobe button 460, FIG. 14, provide a path through the resistor 516 for positively charging the ungrounded terminal of the capacitor 517. When strobe button 460 is depressed to initiate an active interrogation, the capacitor 517 discharges through the resistor 518, and feeds a positive pulse to the strobe button signal lead 480 to the master relay block 461, FIG. 19.

Each of the master relays 1M, 2M, and 3M, FIG. 19, has its energizing coil in series with an individual control thyatron 519, 520, and 521, respectively. The circuits within the thyatron blocks 519, 520, and 521 are identical. The lead 480 from C&I-1 unit 29, FIG. 14, feeds the strobe button signal to the control grid 522 of thyatron 519, and the leads 523 and 524 feed the strobe button signals from C&I-2 and C&I-3, respectively, to the control grid, not shown, of the thyatrons 520 and 521, respectively. The suppressor grid 525 of the thyatron 519 connects through the resistor 526 to the suppressor

grid lead 527, and in series with the resistor 528 to the thyatron cathode.

When no signal is present on the suppressor lead 527, the potential on suppressor grid 525 is such that a strobe button signal applied to the normally negative control grid 522, fires the thyatron 519. The resulting anode current passes from ground through normally closed relay contacts *r1* to lead 529, through relay coil 1M, normally closed contacts 2*m1* and 3*m1* in series, to the anode lead 530 of the thyatron, the cathode being supplied with a suitable negative potential to maintain the anode current after firing. Master relay 1M is thus energized and pulls up.

Master relays 2M and 3M are individually energized over their anode leads 531 and 532, respectively, by the firing of thyatrons 520 and 521, respectively, in a manner similar to the energization of relay 1M. When master relay 1M is first energized, its contacts 1*m1* in series with master relay 2M and its contacts 1*m2* in series with master relay 3M are opened, thus preventing the energization of relays 2M and 3M. Similarly, when master relay 2M is first energized, its contacts 2*m1* in series with master relay 1M and its contacts 2*m2* in series with master relay 3M are opened, thus preventing energization of relays 1M and 3M. Likewise, when master relay 3M is first energized, its contacts 3*m1* in series with master relay 1M and its contacts 3*m2* in series with master relay 2M are opened, thus preventing energization of relays 1M and 2M.

Since there is a time lag of from 20 to 30 milliseconds after energizing current is applied to a master relay before its armature is pulled up, special circuits are provided to overcome the effects of this time lag, by interlocking at a higher speed until the relay contact interlocks can become effective.

If thyatron 519 is the first to fire, a negative potential pulse is produced on its anode and fed through the capacitor 533 through the diode 534 to the suppressor grid lead 535 of thyatron 520, and from the capacitor 533 through diode 536 to the suppressor grid lead 537 of thyatron 521. Thyatrons 520 and 521 are thus prevented from firing in response to a strobe button signal when thyatron 519 has fired first.

Similarly, if thyatron 520 fires first, a negative pulse is produced on the anode lead 531 and is fed through the capacitor 538 through the diode 539 to the suppressor grid lead 527 of thyatron 519, and from the capacitor 538 through diode 540 to the suppressor grid lead 537 of thyatron 521. Thyatrons 519 and 521 are thus prevented from firing, if thyatron 520 has fired first.

If thyatron 521 fires first, a negative pulse on anode lead 532 is fed through the capacitor 541 through diode 542 to the suppressor grid lead 527 of thyatron 519, and from the capacitor 541 through diode 543 to the suppressor grid lead 535 of thyatron 520. Thyatrons 519 and 520 are thus prevented from firing, if thyatron 521 has fired first.

The thyatron interlocking circuits just described prevent the firing of more than one thyatron, even though the master relay of the first fired thyatron has not had time to open its contacts in the other master relay energizing circuits. The nonconducting thyatrons remain disabled about 30 milliseconds. During this interval the master relay in the anode circuit of the first thyatron, has time to pull up its armature and open the energizing circuits of the other master relays. The two sets of interlocking circuits, one fast and the other delayed, prevent any interference or interruption of the interrogating cycle after it has once been started by an operator.

The diodes 544, 545, and 546 provide a discharge path for the energy stored in master relays 1M, 2M, and 3M, respectively, when the anode current supply to any one of these relays is cut off, as by opening the release contacts

r1, referred to hereinafter. All of the diodes shown in FIG. 19 are of the crystal diode rectifier type.

Strobe and Range Gate Generator

FIGS. 15 and 16 show the strobe and range gate generator circuits located in the block 471, FIG. 14, in C&I-1 unit 29. A similar generator is provided in C&I-2 and C&I-3.

One of the important functions of the strobe and range gate generator 471 is to produce range gate pulses for selecting replies from a particular interrogated aircraft, for gating these replies to the active decoding circuits, and for intensifying the PPI tract to form a small square strobe image to display the area from which replies will be accepted during an active interrogation. The strobe and range gate generator 471 also generates the azimuth gate pulse for determining the azimuth period of time within which replies will be accepted during an active interrogation. The azimuth gate is also used to release the main active circuits, if four interrogation replies are not received in regular succession after depressing the strobe button. The generator 471 also generates the movable range mark for producing the range mark circle 452, FIG. 12, and 457, FIG. 13.

The range gate pulses and the azimuth gate pulse are generated only during active operation. Their production is started by depressing the strobe button 460, FIG. 14. The range mixer 410, FIGS. 6 and 14, may be regarded as being functionally a part of the strobe and range gate generator 471, in the sense that it serves as a cathode follower for supplying the range mark pulses alone during passive operation, and the range mark pulses in combination with the strobe pulses during active operation to the PPI unit 40, FIG. 6.

The range mark pulses generated by the strobe and range gate generator 471, FIG. 14, are timed by radar sync pulses fed over lead 501 from the strobe and range gate generator selector block 469 which receives the sync pulses, as indicated in FIG. 27, from the interrogator 43, FIG. 1. The sync pulses on lead 501 trigger the range phantastron 547 which is described in a patent application of Alan R. Garfinkel, Serial No. 797,386, now abandoned, entitled Fast Recovery, Wide Range Phantastron, for generating square pulses having a duration adjustable from approximately 40 to 2500 microseconds by the range control slider 548 called the range control, which selects a desired value of positive voltage from the potentiometer 549.

The positive pulse from range phantastron 547 is fed over lead 550 to the differentiator 551 in the input of the triode inverter 552. The trailing edge of the differentiated output pulse from phantastron 547, is inverted to a positive pulse by the inverter 552 and fed over lead 553, FIG. 15, to the input of the range delay, single-shot multivibrator 554, FIG. 16. The multivibrator 554 is thus triggered and generates a negative square gate voltage pulse starting at the trailing edge of the range phantastron gate pulse. The negative output pulse from the range delay multivibrator is fed over lead 555 to the differentiator 556 in the input of the range mark blocking oscillator 557. The narrow positive pulse produced by differentiating the trailing edge of the negative range delay multivibrator pulse, fires the blocking oscillator 557, thereby generating a 2 microsecond positive range mark pulse which is fed over lead 558 and through the conventional "OR" gate 559 to the output lead 439, and to the range mixer 410, FIG. 6, and the PPI unit 40. A range mark pulse is thus generated in response to each sync pulse, the timing of the range mark pulse being adjustable by the range control 548, FIG. 15.

When the strobe button 460, FIG. 14, is depressed to start and active interrogation, master relay 1M, FIG. 19, pulls up and closes its contacts 1m20, FIG. 27, thereby feeding a positive pulse from the charged capacitor 560 through the resistor 561, to lead 502, FIG. 15. The strobe

and range gate generator selector 469 thus selects for connection to the strobe signal capacitor 560, the strobe and range gate generator in the control and indicator which originated the interrogation. The strobe signal on lead 502 is fed to the input of the azimuth phantastron 562, of conventional design, thereby triggering the phantastron and generating a positive azimuth gate pulse having a duration adjustable from approximately 10 to 150 milliseconds by the azimuth gate width control slider 563, which selects a desired value of positive voltage from the potentiometer 564.

The positive output pulse from azimuth phantastron 562 is fed over lead 565 to the input of the inverter and cathode follower 566 having the cathode output lead 567 for the positive azimuth pulse which enables the lower leg of the two-input "AND" gate 568. The positive pulses on lead 553, produced by inverting the differentiated trailing edges of the range phantastron pulses, are fed over lead 569 to the upper leg of "AND" gate 568, and a number of these relatively short duration pulses are transmitted through the "AND" gate to the output lead 570 during the relatively much longer duration period within which the azimuth pulse enables the lower leg of the "AND" gate. The resulting short duration pulses on lead 570 are fed to the input of the range gate single-shot multivibrator 571, FIG. 16, which triggers in response to each input pulse on lead 570, and thus generates a train of positive square range gate pulses on the output lead 572 for the duration of the azimuth gate. The range gate pulses on lead 572 are fed through the cathode follower 573 to the output lead 504 which extends through FIG. 15 to the decoder 20, FIG. 14 where the range gate pulses are used to selectively gate the replies from the aircraft chosen for active interrogation. The azimuth gate pulse, by controlling the duration of the train of range gate pulses, determines the azimuth interval of time during which the active circuits will accept interrogation replies.

The range gate pulses are also fed over the output lead 574, FIG. 16, of cathode follower 573 to the lower input leg of the "OR" gate 559. The range mark pulse on the upper leg of "OR" gate 559 combines with the range gate pulse on the output lead 439 to form a strobe pulse, as indicated by the wave form 575, which is fed to the PPI unit 40, FIG. 6, as previously mentioned. The position of the range mark pulse at the center of the range gate pulse, is due to the fact that the range delay multivibrator 554 and the range gate multivibrator 571, FIG. 16, are provided with ganged adjustable resistors 576 and 577, respectively, for controlling pulse duration, in such relation that an adjustment of the duration of the range gate pulse produces twice as large an adjustment as that of the range delay pulse. When the strobe button 460 is depressed, both multivibrators trigger simultaneously. Because of the pulse duration adjustments by the resistors 576 and 577, the range mark is thus always at the center of the range gate pulse.

The inverter 566, FIG. 15, has the anode output lead 578 which feeds a negative azimuth gate pulse to the differentiator 579 in the input of the cathode follower 580. The differentiated trailing edge of the negative azimuth pulse, referred to as the end of azimuth pulse, is a positive pulse which is fed through the cathode follower 580 to the output lead 503, and from C&I unit 29 to the generator selector block 469, FIG. 27, and from there over lead 510 to the block 464, FIG. 22 to control the reset relay R to reset the main active circuits, if a fourth B.C. pulse is not received in regular sequence after the strobe button 460, FIG. 14, has been depressed.

The range phantastron 547, FIG. 15, is triggered by the sync pulses on lead 501 which are fed through the capacitor 581 and forwardly through the diode 582 to the suppressor grid of the pentode 583. The coupling resistors 584 and 585 connect the two terminals, respectively, of capacitor 581 to ground. The diode 586, con-

553, to the diode 605, FIG. 16, to prevent the response of multivibrator 554 to noise disturbances, the back-bias being small enough to enable the multivibrator to respond readily to the positive trigger pulses from inverter 552. The resistor 632 provides a path for current which inhibits the "AND" gate 568 when the upper leg is not enabled. The diode 634, connected inversely from lead 570 to ground, clamps negative pulses on lead 570 to ground.

The output pulses from "AND" gate 568, FIG. 15, are fed over lead 570 to trigger the range gate single-shot multivibrator 571, FIG. 16, which produces a delay of from approximately 25 to 150 microseconds in addition to the delay of the range phantastron 547, depending upon the adjustment of the variable resistor 577 connected from the cathode of triode 635 to the grid of triode 636. The circuit of multivibrators 636 and 554, FIG. 15, are similar, except for their different time delays; the fact that the output lead 555 of multivibrator 554 is connected to the anode of the first triode 606 in multivibrator 554 to produce a negative output pulse, whereas the output lead 572 of multivibrator 571 is connected to the anode of the second triode in multivibrator 571 to produce a positive pulse; the fact that the multivibrator block 571 contains the coupling capacitor 637 in series between leads 570 and 638, whereas the block 554 contains no corresponding capacitor; and the fact that lead 638 connects through the coupling resistor 639 to ground, whereas the block 554 includes no corresponding resistor.

The control element 640 for the resistor 576 in the range delay multivibrator 554 is ganged for unitary control, with the control 641 for the resistor 577, as shown by the dotted line 642. These circuits are designed so that the duration of the range gate pulse, 25 to 150 microseconds, is always twice the duration of the range delay pulse, 12.5 to 75 microseconds. Since both the range gate and the range delay pulses start together, the range delay pulse always ends at the center of the range gate pulse. The circuits in the range mark blocking oscillator 557 produce a range mark pulse corresponding in time to the trailing end of the range delay pulse, and consequently the range mark pulse is always timed at the center of the range gate pulse, as shown by the combined range gate pulse and range mark pulse 575 on lead 439.

The range gate pulse is fed to lead 504 through the coupling capacitor 643, to the coupling resistor 644 to ground, and forwardly through the isolating diode 645 which prevents reaction between the circuits feeding range gate pulses to lead 504, FIG. 16, in C&I-1, and the circuits feeding range gate pulses to corresponding leads 646 and 647, FIG. 27, respectively, in C&I-2 and C&I-3, respectively. Each of the range gate leads 646 and 647 contains an isolating diode, not shown, corresponding to the isolating diode 645 in range gate lead 504. The range gate leads 504, 646, and 647, are connected together and to lead 472 in FIG. 27.

The leads 501 to 504, FIG. 27, in bracket 648, connecting to the strobe and range gate generator 471, FIG. 14, in C&I-1, correspond to the similar leads in bracket 649, connecting to the strobe and range gate generator, not shown, in C&I-2, and correspond to the similar leads in bracket 650, connecting to the strobe and range gate generator, not shown, in C&I-3. The contacts 2m20, FIG. 27, of master relay 2M, FIG. 19, when closed by energization of the relay, select the strobe and range gate generator in C&I-2 connected to the leads in bracket 649; and the contacts 3m20, FIG. 27, of master relay 3M, FIG. 19, select the generator in C&I-3, similarly to the selection by contacts 1m20, FIG. 27, of generator 471 in C&I-1. The capacitor 560 is charged through resistor 651, connected to the positive voltage source terminal 652.

In FIG. 24, the PI or TI interrogation selector 466 selectively connects the PI mode order lead 653 and

the TI mode order lead 654, extending to the interrogator 43, FIG. 1, to the control and indicator, C&I-1, C&I-2, or C&I-3, which initiates an active interrogation. When C&I-1 unit 29, FIG. 14, seizes control of an active interrogation by depressing strobe button 460, relay 1M, FIG. 19, pulls up, closing its contacts 1m22 and 1m23, FIG. 24, in the block 466, FIGS. 14 and 24, and connects leads 653 and 654 to leads 496 and 497, respectively, which go to the upper and lower contacts, respectively, of arm 655, FIG. 28 of the PI/TI mode selection switch 453, also shown on the panel 454, FIG. 30. The arm 655, FIG. 28, connects ground to either the PI lead 496 or the TI lead 497, depending upon whether the interrogation is to be in the PI or the TI mode, and the resulting ground signal prepares the interrogator to make the active interrogation in the mode selected by switch 453, FIG. 28.

When the operator at C&I-2 starts an active interrogation, contact 2m22 and 2m23, FIG. 24, of master relay 2M, FIG. 19, close and selectively connect mode order leads 653 and 654, FIG. 24, to the leads in bracket 656 to C&I-2 which correspond to leads 496 and 497 to C&I-1. Similarly the operator at C&I-3 controls the closing of contacts 3m22 and 3m23 of master relay 3M, FIG. 19, for connecting mode order leads 653 and 654 to the leads in bracket 657 to C&I-3. The interlocking circuits of the master relays in FIG. 19 prevent more than one operator at a time from informing the interrogator of a desired active interrogation mode.

Active Counter Circuits

The active counters and their related circuits perform several functions, including controlling a test of the regularity of sequence of passive replies received from an aircraft after an operator depresses his strobe button, such as button 460, FIG. 14; inhibiting a requested active interrogation, if these replies fail to meet the sequence test; providing a signal to start the active interrogation, if the sequence test is met; inhibiting passive operation indicating circuits, if the sequence test is met; and controlling the gating of a reply code to the active decoder relays, if the sequence test is met.

The countercircuits in block 473, FIG. 14, include a counter of bracket coincidence (B.C.) pulses, and a counter of sync pulses. The schematic circuits of the counters and the related circuits in block 473 are shown in FIGS. 17 and 18. The B.C. counter control "AND" gate 658, of conventional form, has three input legs 659, 660, and 661. Legs 659 and 660 are enabling legs, and leg 661 is an inhibiting leg. The output lead 662 connects inversely through the diode 663 to ground to clamp negative pulses to ground. Delayed B.C. pulses from the blocking oscillator 135, FIG. 3, are fed over lead 139 to lead 664 to the leg 659, FIG. 17, of "AND" gate 658, thereby enabling that leg for the one microsecond duration of each B.C. pulse. Range gate pulses from FIG. 27, are fed over lead 472 to the leg 660 of gate 658, thereby enabling that leg for the 25 to 150 microsecond duration of each range gate pulse. Since each range gate pulse is timed to include the timing of one B.C. pulse, the B.C. pulses are fed to output lead 662, in the absence of an inhibiting signal on leg 661.

Lead 662 feeds the B.C. pulse through the conventional triode inverter 665 to the output lead 666, where the pulse is negative, and is fed to the input of the bracket coincidence counter 667, having the two identical binary counter stages 668 and 669 of conventional bistable multivibrator form, designed to be triggered by negative pulses. The multivibrator 668 has two triodes 670 and 671, the anodes of which are connected inversely through the diodes 672 and 673, respectively, to ground to clamp negative pulses to ground. Anode current is fed through resistor 674 in series with lead 675 and resistor 676 to the anode of triode 670, and through resistor 674 in series with lead 675 and resistor 677 to the anode of

nected forwardly from the suppressor grid of pentode 583, through the resistor 587 to ground, and back-biased by the positive voltage fed through resistor 588 to the cathode of diode 585, clamps to ground the peaks of positive pulses exceeding the back-bias voltage across resistor 587.

The anode of pentode 583 is supplied with a positive potential through the resistor 589, and is connected forwardly through the diode 590 to the range control 548. A small capacitor 591 connects the anode of pentode 583 to ground. The positive potential fed through resistor 589 to the anode 583 is also fed through the voltage divider consisting of the small neon lamp 592 in series with the lead 593 and the resistor 594 leading to the terminal 595, maintained at a negative potential. Lead 593 connects with the grid of the triode cathode follower 596, and feeds the proper polarizing potential thereto. The cathode of triode 596 connects through the resistor 597 to the negative terminal 595, and couples through the timing capacitor 598 to the control grid of pentode 583, the control grid being fed with a positive potential through the resistor 599. The screen grid of pentode 583 is used as an output electrode and feeds the square wave output pulse from the range phantastron 547 to output lead 550. A positive potential is fed through the voltage divider, consisting of the resistors 600, 601, and 602 in series, to the negative potential terminal 595, the resistor 601 being shunted by the small capacitor 603. The screen grid of pentode 583 is polarized by the potential between the resistors 600 and 601.

The anode voltage value from which the phantastron 547 commences its run-down, is linearly controlled by the range control 548, and the connection through diode 590 to the anode of pentode 583. The potential through which the anode can fall is adjusted by means of the control 548. Since the rate of fall in voltage is constant, the time of fall varies according to the starting anode voltage. The duration of the approximately square wave-form pulse produced on the screen grid is thus adjusted by the range control 548.

Since the recovery time of a phantastron of conventional form is inherently slow, the timing network is coupled to the cathode follower 596 whose circuit provides a low resistance path for the timing capacitor 598. The action of the cathode follower reduces the recovery interval by a factor of approximately three. The neon lamp 592 sustains a constant voltage drop and thus increases the sensitivity of response of the cathode follower 596 as compared with the usual form of reactive or ohmic resistance coupling, without producing overload when the signals are large, and has the further advantage of supplying the proper bias voltage to the grid of triode 596. Since the lamp 592 draws very little current, its service life is extremely long. The use of a neon lamp in the manner described is the subject of a patent application of A. R. Garfinkel, filed March 5, 1959, S.N. 797,386, now abandoned. The range phantastron pulse on the lead 550 is differentiated by the differentiator 551. The leading edge pulse of the differentiated range phantastron pulse is shunted to ground by the diode 604. The trailing edge pulse is fed from inverter 552 over lead 553, FIG. 15, and through the isolating diode 605, FIG. 16, to the grid of the input triode 606 of range delay single-shot multivibrator 554. The isolating diode 605 prevents the positive pulse developed at the anode of the triode 607 from feeding back over lead 553 to the inverter 552. The diode 608, connected in an inverse direction from the grid of triode 606 to ground discharges the coupling capacitor 609 at the end of the multivibrator cycle, thus preventing the charge on the capacitor from maintaining a large bias on the multivibrator. If the capacitor 609 were not discharged, the multivibrator could not be triggered by the available trigger amplitude.

The range delay multivibrator 554 provides a range delay of from approximately 12.5 to 75 microseconds in addition to the delay of the range phantastron 547,

depending upon the adjustment of the variable resistor 576 connected from the cathode of triode 606 to the grid of triode 607. The capacitor 610 connects the grid of triode 607 to ground. The negative output pulse is differentiated by the differentiator 556, thereby producing a positive pulse at the end of the range delay pulse. The resulting positive pulse triggers the range mark blocking oscillator 557 which produces a 2 microsecond range mark pulse whose time of production can be adjusted over the time interval during which interrogation replies may be received. The timing of the range mark pulse is thus controlled by the run-down interval of the range phantastron 547, FIG. 15, and is adjusted by the range control 548. The amplitude of the movable range mark is limited to the required value by the voltage divider consisting of the series resistors 611 and 612 in the cathode to ground circuit of the range mark blocking oscillator 557, FIG. 16.

The strobe signal on lead 502, FIG. 15, is fed through the resistor 613 to the suppressor grid of the pentode 614 in azimuth phantastron 562. The resistor 615 connects lead 502 to ground. The anode of pentode 614 is supplied with a positive potential through the resistor 616, and connects forwardly through the diode 617 with the azimuth gate width control 563. The control grid of pentode 614 is fed a positive polarizing potential through the resistor 618 and connects through the timing capacitor 619 to the anode of pentode 614.

The timing circuit of the azimuth phantastron 562, FIG. 15, produces only a single output pulse in response to a single depression of the strobe button 460, FIG. 14, and so is not required to have a rapid recovery as is the case with the range phantastron 547 which must produce a train of output pulses during the period of the single azimuth gate pulse. For this reason, the azimuth phantastron does not require the use of a cathode follower in its timing network to correspond with the cathode follower 596 in the range phantastron 547. The similarity of the circuits of the range and azimuth phantastrons, apart from the cathode follower 596 in the range phantastron, is believed to be apparent, and except as already noted, these circuits are similar in operation.

The output lead 567, FIG. 15, for the positive pulse from the cathode of the triode 620 in the inverter and cathode follower 566, by-passes to ground through the capacitor 621, having a capacitance of about .01 microfarad, its function being to inhibit the "AND" gate 568 when the azimuth pulse is not being applied to the grid of triode 620. The charge and discharge time of capacitor 621 is small compared to the duration of the azimuth gate pulse.

The differentiator 579 is designed to differentiate the negative azimuth gate pulse on lead 578 into relatively wide negative and positive pulses, the trailing positive pulse being fed through triode 629 to lead 503. The resistor 622 in series with the grid of triode 620 serves as an amplitude attenuator between the azimuth phantastron 562 and the circuit of the inverter and cathode follower 566. The series resistors 623 and 624 form a voltage divider between the positive anode voltage supply terminal 625 and ground. The capacitor 626 shunting the resistor 624 is charged by the voltage across the resistor and discharges forwardly through the diode 627 to the anode of triode 620 when the anode circuit through the triode 620 needs to draw more anode current than can be supplied through the resistor 628 between the anode supply terminal 625 and the anode.

The resistor 629, FIG. 15, in series with the grid of the triode 630 in cathode follower 580, and the small capacitor 631, connecting the grid of triode 630 to ground, is used to integrate the triggering spike which appears at the leading edge of the azimuth gate pulse.

Lead 569, FIG. 15, to the upper leg of "AND" gate 568, is connected through the resistor 632 to the current supply terminal 633, maintained at a constant negative potential which applies a back-bias over leads 569 and

triode 671. Multivibrator 668 is triggered by the negative B.C. pulse fed through the coupling capacitor 673 to the lead 675. The multivibrator output lead 679, connected directly to the anode of triode 671, feeds its output pulse to the input of multivibrator 669, having the output lead 680 to the upper input leg of the interrogator control "AND" gate 681, FIG. 18. The output lead 679 of multivibrator 668 connects through lead 682 to the lower input leg of "AND" gate 681, having the output lead 683. The described circuits of the two multivibrators 668 and 669 in combination with the "AND" gate 681, count successive B.C. pulses and produce a positive pulse on the lead 683 in response to the third B.C. pulse applied to the input lead 666 of counter 667.

The resistor 684 in the grid circuit of triode 671 has the tap 685 connected to the reset lead 686 for resetting the counter stage 668 to zero or normal, with triode 670 non-conducting and triode 671 conducting, when the main active circuits are restored to normal. The diode 687 in lead 686 connected forwardly toward the tap 685 to feed a positive resetting current to the grid of triode 671 from the reset lead 688 to which the current is fed over a path traced through the series of normally closed contacts 1m21, 2m21, and 3m21 of master relays 1M, 2M, and 3M, respectively, and through resistor 716 to ground. A capacitor 717 across the circuit including the contacts 1m21, 2m21, and 3m21, in series with resistor 716, reduces disturbances from operation of the contacts, FIG. 19. When one of the master relays pulls up in response to the initiation of an active interrogation, one of the sets of contact 1m21, 2m21, or 3m21, FIG. 17, opens and frees the multivibrator 668 from the locked condition produced by the resetting current fed over lead 688, so that the multivibrator is ready to count. When the master relay restores to normal, the resetting current is restored through contacts 1m21, 2m22, and 2m23, thus resetting and locking the multivibrator 668 in the reset condition. Multivibrator 669 has the reset lead 689, similar in function and operation to the reset lead 686 just described, being connected in parallel with reset lead 686 to the lead 688. The diode 687, and the corresponding diode, not shown, in the reset lead 689 and in other reset leads connected to lead 688, prevent undesired reactions between the circuits connected to these leads.

When the first B.C. pulse is fed through B.C. counter control "AND" gate 658, FIG. 17, the resulting negative pulse on the output lead 666 of inverter 665, is fed over lead 690 to the gate control flip-flop 691, FIG. 18, of conventional design, and through the capacitor 692, to the grid of triode 693 in the flip-flop, thereby changing triode 693 from its normally conducting condition to a nonconducting condition, and the other triode 694 in the flip-flop from a normally nonconducting to a conducting condition. The diodes 695 and 696, connected inversely from the anodes of triodes 693 and 694, respectively, to ground, clamp negative pulses on the anodes to ground. The change of triode 693 from a conducting to a nonconducting condition, produces a positive pulse on the output lead 697 of flip-flop 691, the pulse being fed over lead 697 to the branch lead 698 to the lower input leg of the sync counter control "AND" gate 699, thereby enabling the lower leg as long as the triode 693, FIG. 18, remains nonconducting.

Radar sync pulses from the interrogator 43, FIG. 1, are fed over the lead 700, FIG. 17, to the blocking oscillator 701 which regenerates the sync pulses and feeds them over the output lead 702 to the upper input leg of "AND" gate 699, thereby enabling the upper leg while the lower leg is enabled by flip-flop 691, FIG. 18. The resulting sync pulses on output lead 703, are fed through the inverter 704 to produce negative sync pulses on lead 705 which are fed to the input of the sync counter 706, having the first bistable multivibrator 707, and the second bistable multivibrator 708, the output lead 709 of multi-

vibrator 707 being connected to the input of multivibrator 708. The multivibrators 707 and 708 have the same circuit as, and operate similarly to, the bracket coincidence multivibrators 668 and 669.

The output lead 710 of multivibrator 708, FIG. 17, connects to the upper input leg of the third sync "AND" gate 711, FIG. 18. The output lead 709 of multivibrator 707, FIG. 17, connects to lead 712 to the lower input leg of "AND" gate 711, having the output lead 713. The described circuits of the two multivibrators 707 and 708, in combination with the "AND" gate 711, count successive radar sync pulses and produce a positive pulse on the lead 713 in response to the third radar sync pulse applied to the input lead 705 of counter 706.

The reset leads 714 for multivibrator 707, and 715 for multivibrator 708, are connected in parallel to the reset lead 688 for controlling the locked reset condition of the sync counter multivibrators 708 and 709, in a manner similar to that described for the reset leads 686 and 689 for the B.C. counter multivibrators 668 and 669.

The radar sync counter 706 is initially one count behind the bracket coincidence counter 667. Although the radar sync pulses continuously appear at the upper input leg of the sync counter control "AND" gate 699, they cannot pass through the "AND" gate 699 and be counted by the sync counter 706 until the lower input leg of the "AND" gate 699 is enabled, as referred to above, by the response of the gate control flip-flop 691 to the first B.C. pulse reaching the lead 666 at the input of B.C. counter 667.

When an operator starts an active interrogation, and his master relay 1M, 2M, or 3M, pulls up its armature, causing range gate pulses to be applied to leg 660 of "AND" gate 658, the first B.C. pulse passed by "AND" gate 658 is fed to lead 666 at the input of B.C. counter 667 which registers the count of "one." This same B.C. pulse is fed over lead 690 and triggers flip-flop 691 from its normal reset condition to its on or set condition. The resulting pulse, fed over lead 697 to lead 698, enables the lower leg of sync counter control "AND" gate 703 which now accepts the first radar sync pulse to appear simultaneously on the upper leg of "AND" gate 699. This first radar sync pulse is fed to sync counter 706 which now registers the count of "one."

The second B.C. pulse is next applied to B.C. counter 667 which registers the count of "two." The second B.C. pulse has no further effect on the gate flip-flop 691, which remains in its set condition produced by the first B.C. pulse. The second radar sync pulse is then fed by sync counter control "AND" gate 699 to sync counter 706 which registers the count of "two."

The third B.C. pulse is next applied to B.C. counter 667 and causes it to register the count of "three." The resulting positive pulse produced on lead 683, as referred to above, is fed to the differentiator 718 in the input of the interrogator flip-flop 719, thereby triggering the flip-flop from its reset to its on condition, and producing a positive pulse on its output lead 720. The pulse on lead 720 is fed to the grid of the triode paraphase amplifier 721 of conventional form, thereby producing a negative pulse, called the low gate pulse, on the output lead 722, coupled through the capacitor 723 from the anode of amplifier 721, and producing a positive pulse, called the high gate pulse, on the output lead 724, coupled through the capacitor 725 from the cathode of amplifier 721. The high gate and the low gate pulses are fed over the leads 722 and 724, respectively, to the interrogator 43, FIG. 1, and serve as signals to request the interrogator to start the active interrogation on the next radar transmission. The interrogator 43 was previously prepared by the operator's setting of the PI/TI mode selector switch 453, FIGS. 28, 29 and 30, to make the interrogation in the desired PI or TI mode.

The differentiator 718 in the interrogator flip-flop 719, includes the capacitor 726 in series with the resistor 727,

the lead 728, and the grounded resistor 729. The lead 728 feeds the differentiated leading edge of the input pulse to the grid of the first triode 730 in flip-flop 719. The anode of the second triode 731 in flip-flop 719 is connected to the flip-flop output lead 720.

Following the third B.C. pulse counted on B.C. counter 667, the third radar sync pulse appears on the lead 702, and passes through the sync counter control "AND" gate 699, the inverter 704, and to the sync counter 706, causing it to register the count of "three." The resulting positive pulse produced on the lead 713 in response to the third radar sync pulse, is fed to the input lead 732 of the triode inverter 733 which produces in response thereto, a negative pulse on the inverter output lead 734. The negative pulse serves as an inhibiting pulse which is fed over lead 734 to the inhibiting leg 661, FIG. 17, of B.C. counter control "AND" gate 658, thereby inhibiting the gate from passing any B.C. pulse after the third, and thus preventing B.C. counter 667 from counting more than the three pulses.

In the inverter 733, the input lead 732 connects through the small neon lamp 735 having a constant voltage drop in series with the resistor 736, to the grid of the triode inverter, and through the resistor 737 to the negative power source terminal 738. The use of neon lamp 735 is similar to that of the neon lamp 592, FIG. 15, in the grid circuit of the cathode follower 596.

After the first B.C. pulse is fed through the B.C. counter control "AND" gate 658 and renders the sync counter 706 responsive to sync pulses by the action of gate control flip-flop 691, the sync counter counts the first three sync pulses. The third sync pulse causes the B.C. counter control "AND" gate 658 to be inhibited and thus prevent any B.C. pulse thereafter to get through gate 658. Consequently, if one of two B.C. pulses fail to appear at the input of gate 658 in regular sequential timing after the first B.C. pulse passed gate 658, the inhibited gate then prevents a later B.C. pulse from being counted in place of the missing one or two B.C. pulses.

The described circuits thus perform a sequence test on the replies received in response to a regular series of interrogations. If three B.C. pulses are received in the same regular sequence as three successive transmitted radar interrogations, the sequence test is met. Any other sequence of received B.C. pulses, fails to meet the sequence test and leaves the B.C. counter with less than three counts registered therein. If the sequence test fails, there is no pulse on lead 683, FIG. 18, to trigger interrogator flip-flop 719, or to cause a start signal to be fed to the interrogator 43, FIG. 1, to initiate the radar transmission of the active interrogation. If the sequence test is met, the start signal is sent to the interrogator, and the active interrogation proceeds as described, and is timed in the interrogator to take place 23.3 microseconds after the third sync pulse.

The PI/TI trigger, which is fed to the lead 289, FIG. 4, from the interrogator 43, FIG. 1, after being fed through the cathode follower 291, FIG. 4, to the lead 292, is fed over the lead 739 and through FIG. 18 to FIG. 17, through the coupling capacitor 740 to the lead 741, connected through the resistor 742 to the negative power source terminal 743, and connected to the third input leg of the PI/TI trigger "AND" gate 744. The third input leg is thus enabled by the PI/TI trigger.

The first input leg of "AND" gate 744 connects with the lead 713 from the output of third sync "AND" gate 711, and is enabled by the pulse on lead 713 in response to the count of the third sync pulse by sync counter 706. The pulse on lead 713 continues until the sync counter 706 is reset. The second input lead of PI/TI trigger "AND" gate 744 is connected to the output lead 697 of gate control flip-flop 691, FIG. 18, and is enabled by the flip-flop 691 output pulse in response to the first B.C. pulse fed over lead 690. The pulse on lead 697 continues until flip-flop 691 is reset.

Consequently, after the count of the third sync pulse by sync counter 706, the next PI/TI trigger appearing on lead 741 is fed through "AND" gate 744 to the output lead 745 and to the grid of the PI/TI paraphase triode amplifier 746 of conventional form. The low gate output lead 747, connected to the anode of triode amplifier 746, feeds a negative PI/TI trigger pulse to FIG. 18, and through the coupling capacitor 748, to the anode of triode 693 in flip-flop 691, thereby resetting flip-flop 691 to its original condition.

The negative PI/TI trigger pulse on lead 747 is also fed through the coupling capacitor 749 to the lead 720, to the anode of triode 731 in interrogator flip-flop 719, thereby resetting flip-flop 719 to its reset condition, and terminating the low gate pulse on output lead 722 and the high gate pulse on output lead 724 of interrogator paraphase amplifier 721, thus ending the signal which requested the interrogator to make the active interrogation, as it has completed its function, and allowing the interrogator to return to normal passive operation.

The PI/TI trigger pulses on the lead 741 at the third input leg of PI/TI trigger "AND" gate 744, are timed to occur 3 microseconds behind the radar sync pulses until the third B.C. pulse is counted by B.C. counter 667 and the active interrogation is requested in response to the third B.C. pulse. The interrogator then changes the timing of the next PI/TI trigger, so that it occurs 23.3 microseconds after the third sync pulse counted by sync counter 706, instead of occurring 3 microseconds after the sync pulses, as the PI/TI trigger was previously timed. During the 23.3 microsecond interval between the third radar sync pulse and the PI/TI trigger, the request for active interrogation is received and programmed by the interrogator. The 23.3 microsecond delay of the PI/TI trigger behind the third sync pulse also makes available sufficient time for the radar sync counter to register its count of "three" on the output lead 713 of the third sync gate 711, and to enable the first input leg of PI/TI trigger "AND" gate 744 before the PI/TI trigger appears.

When the gate control flip-flop 691 is reset by the PI/TI trigger, the gate voltage is removed from output lead 697, lead 698, and sync counter control "AND" gate 699. This action inhibits "AND" gate 699 and stops the sync counter from counting after the third sync pulse. The B.C. counter 667, as previously mentioned, was inhibited from counting after the third B.C. pulse, by the pulse on lead 713, fed through inverter 733 to lead 734 and to the inhibiting leg 661 of B.C. counter control "AND" gate 658. Thus, both the B.C. counter 667 and radar sync counter 706 stop counting and mutually interlock, until they are reset at the end of the active operation cycle when the master relay 1M, 2M, or 3M, FIG. 19, of the operator initiating an active interrogation, is deenergized, and the contacts 1m21, 2m21, and 3m21, FIG. 17, of the master relays are closed. The counters then remain locked in the reset state by the closed master relay contacts until the next active interrogation. Flip-flop 691, FIG. 18, is also locked in a reset condition by these closed contacts and the connection of reset lead 792, FIG. 18, to the reset lead 688, FIG. 17.

The high gate output lead 750, FIG. 17, connected to the cathode of PI/TI paraphase triode amplifier 746, feeds a positive PI/TI trigger pulse through the lower leg of the active inhibit "AND" gate 751 to the output lead 752, the upper input leg of "AND" gate 751 being enabled by the positive pulse fed over lead 753 from the output lead 683 of interrogator control gate 681 in response to the third B.C. pulse counted on B.C. counter 667.

The positive pulse on the lead 752 is fed through the coupling capacitor 754 to the grid of the triode 755 in the single-shot multivibrator 756 of conventional form, designed to produce a negative output gate voltage pulse of about 3000 microsecond duration on the lead 757 connected to the anode of triode 755, and to produce a

positive pulse of the same duration on the lead 758 connected to the anode of the other triode 759 in multivibrator 756. The positive pulse on lead 757 is fed through the cathode follower 760 to the output lead 318 which feeds the 3000 microsecond negative pulse to FIG. 18 and to the inhibiting leg 309, FIG. 4, of control "AND" gate 258, and the corresponding inhibiting legs of control "AND" gates 259, 260, and 261, to inhibit the transmission of a "YES" pulse to the passive video mixer circuits of FIG. 5, and the PPI display units 40, 41, and 42, FIG. 6. Further video indications by the passive circuits are thus inhibited until the end of the 3000 microsecond pulse produced by single-shot multivibrator 756. Unless the B.C. sequence test, described above, is met, no pulse is produced on lead 753, FIG. 18, and no active inhibit pulse is produced to inhibit the passive operation indications.

The crystal diode rectifier 761, FIG. 17, connected forwardly from the grid of triode 759 in multivibrator 756, to the junction 762 of the voltage divider resistors 763 and 764, serves as a clamp to suppress undesired transient positive potentials at the grid.

In the cathode follower 760, FIG. 17, the input lead 757 feeds the negative pulse thereon through the resistor 765 to the grid of the triode 766. The crystal diode rectifier 767 is connected forwardly from the grid of triode 766, through the resistor 768 to ground. Positive current fed over lead 769 and through resistor 768 to ground, produces a voltage across resistor 768 which back-biases diode 767, which serves to clamp to ground pulses exceeding the back-bias voltage. The capacitor 770, shunting the cathode to ground resistor 771 of triode 766, causes the output pulse on lead 318 to have the approximate wave form 772, having a leading edge of about 40 microseconds duration within which the negative pulse builds up to its maximum amplitude having a duration of about 3000 microseconds.

The 3000 microsecond positive pulse from multivibrator 756, FIG. 17, is also fed over lead 758 to FIG. 18, to the input of the triode cathode follower 773, having the output lead 774, which feeds the pulse to the upper input leg of the active decoding "AND" gate 775, thereby enabling the upper leg for the 3000 microsecond duration of the pulse. Since the 3000 microsecond pulse does not appear on the upper leg of gate 775 until after the third B.C. pulse has been counted by counter 667, FIG. 17, the range gate pulses prior thereto from lead 472, FIG. 17, and fed over lead 776 to FIG. 18 and the lower leg of "AND" gate 775, cannot pass gate 775. Consequently, the first range gate pulse that can pass to the output lead 777 of the active decoding "AND" gate 775, is the fourth range gate pulse.

The fourth range gate pulse is fed over lead 777 to the grid of the triode cathode follower 778, and from the cathode thereof, through the coupling capacitor 779, to the output lead 780, to FIG. 22, and to the suppressor grid of the delay relay control thyatron 781. The lead 780, FIG. 18, also feeds the fourth range gate pulse over lead 782, to the active decoder relay selector 463, FIG. 21, which will be described hereinafter. The fourth range gate pulse is also fed from the cathode of triode cathode follower 778, through the coupling capacitor 783, to the output lead 784 which is connected to ground through the resistor 785, shunted by the noise suppressing capacitor 786.

The output lead 784, FIG. 18, of cathode follower 778, connects to the upper input leg of the release control "AND" gate 787. Positive B.C. pulses are fed from blocking oscillator 135, FIG. 3, to lead 139, to lead 664, to FIG. 17, to branch lead 788, to FIG. 18, and to the lower input leg of "AND" gate 787. Until the fourth range gate pulse appears on lead 784 and the upper leg of "AND" gate 787, no B.C. pulse can pass through the gate. Consequently, the first B.C. pulse that can pass gate 787 is the fourth B.C. pulse, which is coin-

cident with the fourth range gate pulse. The fourth B.C. pulse is thus fed to the output lead 789, and through the triode inverter 790, thereby producing a negative fourth B.C. pulse which is fed over output lead 791 to FIG. 22 and the block 464 for the controls for the reset relay R and delay relay D.

It will be seen from the above description that no fourth B.C. pulse can appear on lead 791, FIG. 18, and no range gate pulse can appear on leads 780, or 782, unless the upper leg of active inhibit "AND" gate 751, FIG. 17, is enabled by a pulse on lead 753 in response to the third B.C. pulse counted by B.C. counter 667, that is, unless the B.C. sequence test is passed.

When the sequence test has been met by the reception and counting of three successive B.C. pulses in regular order after the operator's master relay has pulled up, and the fourth B.C. pulse has appeared on lead 791, FIG. 22, the fourth B.C. pulse is fed from the cathode to the anode of the crystal diode rectifier 793, to the anode of the left triode 794 in the reset control flip-flop 795, having a conventional flip-flop circuit. The voltage on the anode of triode 794 is thus triggered from its normal positive value to a negative value, and the voltage on the anode of the right triode 796 in flip-flop 795 is changed from its normal negative value to a positive value. The lead 800 connected to the anode of triode 796 thus receives a positive pulse in response to the fourth B.C. pulse on lead 791, and feeds this pulse through the coupling capacitor 801 in series with the resistor 802 to the control grid of the delay relay control thyatron 781. The lead 791 is connected to ground through the resistor 797. The crystal diode rectifiers 798 and 799, respectively, connected inversely from the anodes of triodes 794 and 796 to ground, clamp negative pulses on the anodes to ground.

The fourth range gate pulse on lead 780, FIG. 22, is fed through the resistor 803 to the suppressor grid of thyatron 781. A negative polarizing potential is supplied through resistors 804 and 803 in series to the suppressor grid and through resistors 805 and 802 in series to the control grid of thyatron 781. Both grids of thyatron 781 must be made positive, in order to fire the thyatron. Since the fourth B.C. pulse on lead 791 trips flip-flop 795 and makes the suppressor grid of the thyatron positive, and the fourth range gate pulse on lead 780 simultaneously makes the control grid of the thyatron positive, the thyatron is fired. The resulting current is fed from the anode of thyatron 781, through the coil of the first delay relay D, over the lead 806, and the closed contacts 1m3, FIG. 22, of master relay 1M, FIG. 19, to ground, assuming that the operator of control and indicator No. 1 initiated the active interrogation.

First delay relay D is thus energized, but is a delay-on-make relay, so that it delays pulling up for about 40 milliseconds the closing of its normally open contacts in FIGS. 20 and 26. The delay is provided so that there is sufficient time for the decoding relays 1A to 12A, FIGS. 28 and 29, to pull up and latch in accordance with the reply code, and for various other operations, referred to hereinafter, to take place. Master relay contacts 2m3 or 3m3, are closed in place of contacts 1m3 to complete the energizing circuit of relay D, when master relay 2M, or 3M, respectively, is pulled up in place of master relay 1M, in response to the initiation of an active interrogation by the operator at C&I-2, or C&I-3, respectively. The crystal diode rectifier 807 in shunt to the coil of relay D, is poled to discharge the current therein when the relay is deenergized.

When contacts d2, FIG. 20, of relay D, FIG. 22, close, they close a path from the negative voltage source terminal 808, through closed contacts d2, closed contacts 1m18 of master relay 1M, FIG. 19, and the relay coil of the indicator relay 1S, FIG. 20, to ground. Each of the indicator relays 1S, 2S, and 3S, is a delay-on-make relay, designed to delay for about 35 milliseconds after

energization of the relay, the closing of its normally open contacts in FIGS. 20, 22, and 23.

Contacts 1s2, 2s2, and 3s2, FIG. 23, of the relays 1S, 2S, and 3S, respectively, FIG. 20, select for energization the indicator power supply circuit of the control and indicator originating an active interrogation. Contacts 1s1 close to latch relay 1S when its armature is pulled up, the latching circuit being traced from the negative voltage source terminal 809, FIG. 14, the normally closed contacts of reset button 508, holding circuit lead 481, FIG. 14 to FIG. 20, closed contacts 1s1, the coil of relay 1S, to ground. Relay 1S is held latched until reset button 508, FIG. 14, is depressed to open its energizing circuit. The energizing and latching circuits of indicator relays 2S and 3S are similar to and operate similarly to that of relay 1S. The holding circuits 810 and 811, respectively, for relays 2S and 3S, are controlled by the reset buttons, not shown, in C&I-2 and C&I-3, respectively.

Active Decoder Relays and Indicators

The twelve voltage leads 812 to 823 in bracket 123, FIG. 21, extend from bracket 123, FIG. 3, and carry reply code bits corresponding to those on tap Nos. 2 to 7, and 9 to 14, respectively, FIG. 3. When a reply code pulse in position 2, FIG. 2C, appears on lead 812, in response to a pulse on tap No. 2, FIG. 3, the pulse is fed to the decoding thyatron 824, through the coupling capacitor 825, forwardly through the crystal diode rectifier 826, to the lead 827, and through the resistor 828, to the control grid of the thyatron. A negative polarizing voltage is fed from the terminal 829, through the resistor 830, the resistor 831 shunting diode 826, and the resistor 828 to the control grid of the thyatron. The small capacitor 832, connecting the lead 827 to ground, in conjunction with low forward impedance diode 826, form an integrating circuit which facilitates the triggering of the thyatron. A negative polarizing voltage is fed from the terminal 829 through the resistors 833 and 834 in series to the suppressor grid of the thyatron 824.

In order to fire thyatron 824, it is necessary to make both its control grid and its suppressor grid positive simultaneously. The fourth range gate pulse on lead 782 makes the suppressor grid positive, and the reply code pulse on lead 812, in response to the active interrogation, makes the control grid simultaneously positive.

Decoding thyatron 824, FIG. 21, is thus fired and feeds its anode current over the output lead 835, through the contacts 1m4 of master relay 1M, FIG. 19, which were closed when strobe button 460 was depressed, and over relay lead 482 to FIG. 28, and through the coil of the active decoder relay 1A, to ground. The relay 1A is thus energized and latches up over a circuit traced from ground at the relay, through the relay coil, forwardly through the crystal diode rectifier 836, contacts 1 of relay 1A, to lead 479, FIG. 28, through FIG. 29, to FIG. 14, and through closed contacts of reset button 508, FIG. 14, to the negative source terminal 809. Decoding relay 1A, FIG. 28, is thus latched up until its latching circuit is opened by depressing reset button 508, FIG. 14.

The active decoder relay selector 463, FIG. 21, in decoder 20, contains a total of twelve thyatrons, identical to thyatron 824, and operating similarly thereto, the fourth range gate pulse being fed to the thyatrons by lead 782, and the reply code pulse for the control grid of each thyatron being supplied over a different one of the twelve voltage leads 812 to 823, respectively, in bracket 123, FIG. 21, so that each thyatron is fired by a reply code pulse in a different one of the twelve pulse positions 2 to 7, and 9 to 14, respectively, corresponding to a different one of the twelve tap Nos. 2 to 7, and 9 to 14, respectively, FIG. 3.

Each of the twelve thyatrons, when fired, energizes a separate one of the active decoder relays 1A to 12A,

FIGS. 28 and 29, through separate contacts 1m4 to 1m15, respectively, of master relay 1M, and over the corresponding one of the decoder relay leads 482 to 493, respectively, in series with that set of contacts. Thus, the thyatron 837, FIG. 21, is supplied with the fourth range gate pulse over lead 838 from lead 782, and the reply code pulse for code pulse position 3 is fed over voltage lead 813. Current from the fired thyatron 837 is fed over lead 839 and through contacts 1m5 to active decoder relay lead 483, to decoder relay 2A, FIG. 28.

In order to simplify the drawing of FIG. 21, the decoding thyatrons for code pulses in positions 4 to 7, and 9 to 14, are represented as being in block 840, and the contacts 1m6 to 1m15 of master relay 1M, are represented as being in block 841. Similarly, the contacts 2m6 to 2m15 of master relay 2M, and the contacts 3m6 to 3m15 of master relay 3M, are represented as being in blocks 842 and 843, respectively.

Master relay 1M, FIG. 19, through its contacts 1m4 to 1m15, FIG. 21, selects the twelve active decoding relays in C&I-1 which originated the active interrogation, for connection to the twelve decoding thyatrons centralized in the active decoder relay selector 463, FIG. 21. Similarly, master relay 2M, FIG. 19, through its contacts 2m4 to 2m15, FIG. 21, and master relay 3M, FIG. 19, through its contacts 3m4 to 3m15, FIG. 21, select the corresponding twelve active decoding relays, not shown, in C&I-2 and C&I-3, respectively, for connection with the centralized decoding thyatrons in FIG. 21. The interlocking circuits in FIG. 19, prevent the connection of more than one control and indicator to the decoding thyatrons in FIG. 21, the control and indicator originating the active interrogation, being the only one obtaining the connection.

Each of the active decoder relays 2A to 6A, FIG. 28, and 7A to 12A, FIG. 29, has an energizing and resetting circuit similar to that of active decoder relay 1A. A separate crystal diode rectifier, similar to the diode 836 for relay 1A, is provided between each of the decoder relays 1A to 12A, and its contacts 1 in the holding and resetting circuit thereof to prevent reactions between the relay circuits. The crystal diode rectifier 844, shunting the coil of decoding relay 1A, is poled to discharge current from the coil when the relay is deenergized. A similar diode is connected for a like purpose across the coil of each of the other decoding relays 2A to 12A.

After the delay relay D, FIG. 22, is energized, but before it has pulled up its armature to close its contacts, those active decoding relays in the group 1A to 12A which have been energized in response to reply code pulses fed to the corresponding decoding thyatrons in FIG. 21, have time to pull up their armatures and latch, but do not produce any corresponding code indication until certain other operations have taken place.

When master relay 1M, FIG. 19, pulls up in response to depression of the strobe button 460, FIG. 14, master relay contacts 1m16 and 1m17, FIG. 25, in the PI bridge selector 467, close to select the PI bridge leads 498 and 499 to C&I-1, which originated the active interrogation, for connection to the secondary coil 845 of the transformer 846, fed by the A.C. power source 847. Master relay 2M, by closure of its contacts 2m16 and 2m17, similarly selects the PI bridge leads in bracket 848 to C&I-2, when the C&I-2 operator originates the active interrogation. Master relay 3M, by closure of its contacts 3m16 and 3m17, selects the PI bridge leads in bracket 849 to C&I-3, when the C&I-3 operator originates the active interrogation. The secondary coil 845 is provided with a center tap 850, connected to the negative D.C. voltage terminal 851.

In FIG. 28, in C&I-1 unit 29, the arms 852 and 853 of PI/TI selector switch 453, when in the upper position for selecting the PI mode, connect the leads 498 and 499, respectively, to the leads 854 and 855, respectively. Lead 854 connects with the upper end of the six resistors 856

to 861 in PI bridge No. 1, FIG. 28, and with the upper end of the six resistors 862 to 867 in PI bridge No. 2, FIG. 29. Lead 855 connects with the lower end of the six resistors 868 to 873 in PI bridge No. 1, and with the lower end of the six resistors 874 to 879 in PI bridge No. 2. These twenty-four resistors have the same resistance value, for example, 3,000 ohms in a particular case.

The six contact arms 880 to 885 of decoding relays 1A to 6A are connected to the lead 886, and inversely through the crystal diode rectifier 887 to the bridge unbalance signal lead 888. The six contact arms 889 to 894 of decoding relays 7A to 12A are connected to the lead 895, and inversely through the crystal diode rectifier 896 to the bridge unbalance lead 888 which is common to the PI bridges No. 1 and No. 2. Lead 888 is connected through the resistor 897 to the terminal 898, having the same negative voltage as the terminal 851, FIG. 25. Lead 888 is connected inversely through the crystal diode rectifier 899 to the lead 500.

Either PI bridge No. 1, or PI bridge No. 2 is balanced, and no bridge unbalance signal is produced thereby, if any three relays in the group of six decoding relays having contacts in that bridge, are energized, and the other three relays in the group are deenergized. If more or less than three of the six decoding relays in the group are energized, the bridge is unbalanced and produces a bridge unbalance signal. Diode 887 rectifies any unbalance signal voltage from bridge No. 1, and diode 896 rectifies any unbalance signal voltage from bridge No. 2. The rectified voltage is a negative voltage which feeds through the diode 899 to lead 500.

PI bridge No. 1 thus examines the first half and PI bridge No. 2 the second half of a PI reply code from an actively interrogated aircraft, to determine whether the reply contains three pulses present in each half of the reply code train, as required by the PI codes shown in Table No. 3, herein. If the reply code is correctly formed, the bridge balances, and no bridge unbalance signal voltage appears on lead 500. If the reply code is incorrectly formed, the bridge is unbalanced, and produces a negative signal voltage on lead 500. When a TI interrogation is selected by PI/TI selector switch 453, the switch arms 852 and 853, disconnect the bridges from the bridge energizing leads 498 and 499, thereby deenergizing PI bridges No. 1 and No. 2.

Lead 500 feeds any bridge unbalance signal to the lead 900 in the bridge unbalance amplifier 468, FIG. 26, in the decoder 20. This amplifier serves as centralized equipment for the three control and indicators, the lead 500 from C&I-1, and the corresponding bridge unbalance signal leads 901 and 902 from C&I-2 and C&I-3, respectively, being connected to the common lead 900. The diode 899 in series with lead 500 in C&I-1, and a corresponding diode, not shown, in the leads 901 and 902 in C&I-2 and C&I-3, respectively, prevent undesired interaction between the PI bridge circuits of these different control and indicator units. The master relay interlocking circuits in FIG. 19, and the master relay contacts in FIG. 25, prevent the PI bridges in more than one control and indicator unit from being simultaneously energized by A.C. current from transformer 846, FIG. 25.

In the bridge unbalance amplifier 468, FIG. 26, the contacts *d1* remain open until the 40 millisecond delay cycle of relay D, FIG. 22, is completed. Since delay relay D and decoder relays 1A to 12A are energized at substantially the same time, the delay in closing contacts *d1*, provides sufficient time for the decoder relays to latch up and change the PI bridges No. 1 and No. 2 from their normally unbalanced condition, as shown in FIGS. 28 and 29, with their contact arms 880 to 885, and 889 to 894, closing their lower contacts, to a balanced and stabilized condition in accordance with a valid PI reply code. Since an energized decoder relay represents a "1," and a deenergized decoder relay represents a "0," any valid reply code in the PI mode will cause three of

the first group of six decoder relays 1A to 6A, FIG. 28, and three of the second group of six decoder relays 7A to 12A, FIG. 29, to be latched up, while three relays in each group will remain deenergized.

The grid of the triode amplifier 903 is normally polarized by a negative voltage on the terminal 904, fed through the resistor 905 to the grid, this voltage being equal to that at the terminal 851, FIG. 25, and 898, FIG. 28, in order to avoid undesired disturbing signals when contacts *d1*, FIG. 26, are closed at a time when the PI bridges are balanced.

The negative voltage bridge unbalance signal applied to the grid of triode 903, FIG. 26, produces a positive signal on the output lead 906 which feeds the positive signal to control grid of the thyatron 907, thereby firing the thyatron, and causing current to be fed over the thyatron anode lead 506 to FIG. 20. The signal on lead 506 is fed through master relay contacts *1m19* and the coil of the error relay 1E, to ground. Relay 1E is thus energized, and latches up over a circuit traced from ground, through relay 1E and latching contacts *1e1* to holding circuit lead 481, to control and indicator unit No. 1, FIG. 14, through the normally closed contacts of reset button 508 to the negative voltage source terminal 809.

The circuits for error relays 2E and 3E, for C&I-2 and C&I-3, respectively, are similar to, and operate similarly to those of error relay 1E for C&I-1. Error relays 1E, 2E, and 3E are reset by interrupting their latching circuits over leads 481, 810, and 811, respectively, by depressing the reset button 508, FIG. 14, in C&I-1, for resetting relay 1E, and by depressing similar reset buttons, not shown, in C&I-2 and C&I-3, for resetting relays 2E and 3E, respectively. The crystal diode rectifier 908, FIG. 14, connected forwardly to ground from holding circuit leads 479 and 481, provides a discharge path for current from the decoder, indicator, and error relay coils when the reset button interrupts the latching current to these coils.

The indicator selector 465, FIG. 23, in decoder 20, provides circuits for selectively connecting the positive lead 909 of the D.C. voltage source 910, to the code indicator lamps, or the error indicator lamp, in C&I-1, C&I-2, or C&I-3. The first delay relay D, FIG. 22 closes its contacts to complete the first delay cycle about 40 milliseconds after energization in response to the combined action of the fourth B.C. pulse and the fourth range gate pulse. Indicator signal relay 1S is energized in response to the pulling up of delay relay D, but delays the closing of its contacts, to complete the second delay cycle, about 35 milliseconds after relay 1S is energized. This delay provides time for error relay 1E to transfer its contacts *1e2* from the code lamp circuit 495 to the error lamp circuit lead 494 before either circuit is energized by closure of contacts *1s2*.

When a valid reply code has been received, and error relay 1E remains deenergized, while indicator relay 1S closes its contacts *1s2*, lead 909 feeds current through contacts *1s2* to the code and error lamp lead 911, through the normally closed contacts *1e2*, over lead 495 to the branch lead 912, FIG. 28, for supplying current over the contacts of decoder relays 1A to 6A, for the PI-1 code lamps and the TI-1 code lamps in FIG. 28, and over lead 495 to FIG. 29 for supplying current over the contacts of decoder relays 7A to 12A, for the PI-2 code lamps and the TI-2 code lamps in FIG. 29.

If error relay 1E is energized in response to an invalid reply code, the contacts *1e2* transfer code and error lamp lead 911 from code lamp lead 495 to error lamp 494 before contacts *1s2* close, thereby preparing a circuit over lead 494 for lighting the error lamp 507, FIG. 28, when contacts *1s2* close, and preventing the code lamps from lighting. The lighted error lamp 507, FIG. 28, is displayed on the C&I-1 panel 454, FIG. 30. Contacts *2e2* and *2s2*, FIG. 23, for controlling the energization of the

code or error lamps of C&I-2, and contacts 3e2 and 3s2 for controlling the code or error lamps of C&I-3, operate similarly to contacts 1e2 and 1s2 for C&I-1.

The main active operation circuits are reset to their original condition in either of two ways, depending upon whether the fourth bracket coincidence pulse is present or absent.

When the fourth B.C. pulse is present, it is fed over lead 791, FIG. 22, to the reset control flip-flop 795, which is thereby triggered and produces a positive voltage on lead 800. Delay relay D is energized as a result, and 40 milliseconds later, at its contacts d2, FIG. 20, closes the energizing circuit of indicator relay 1S. Contacts 1s3, FIG. 22, close 35 milliseconds after relay 1S is energized, and by this time the main active circuits have performed all their functions and are ready for release.

The positive voltage on lead 800 is now fed through the resistor 913 and contacts 1s3, to lead 914 and the lower input leg of the reset "OR" gate 915, to the output lead 916, and to the grid of the reset control thyratron 917 which fires, and feeds its anode current over lead 918 through the reset relay R, and contacts 1m3 of master relay 1M, FIG. 19, and to ground. Reset relay R is thus energized and opens its contacts r1, FIG. 19, thus restoring master relay 1M and the main active circuits controlled thereby to normal. Deenergization of master relay 1M, opens contacts 1m3, FIG. 22, causing the deenergization of reset relay R and the reclosing of contacts r1, FIG. 19, thus restoring to ground the coils of all the master relays 1M, 2M, and 3M. The restoration of master relay 1M to normal, closes its contacts 1m21, FIG. 17, and causes the reset control flip-flop 795, FIG. 22, to restore to a locked reset condition, similar to that of gate control flip-flop 691, FIG. 18, the reset circuit being traced from ground, through contacts 1m21, FIG. 17, over lead 688, to lead 792, to FIG. 18, to reset lead 919, to FIG. 22, and flip-flop 795. The main active operation circuits are thus reset in accordance with one of the two ways referred to, and made ready for the next active interrogation cycle.

When the fourth B.C. pulse fails to appear on lead 791, the reset control flip-flop 795 remains in its locked reset condition, in which the anode of triode 794 in the flip-flop feeds its positive voltage over lead 920, to the lower input leg of the reset control "AND" gate 921, thereby enabling the leg. The positive differentiated trailing edge of the azimuth gate, referred to as the end of the azimuth gate pulse, is fed from the strobe and range gate generator 471, FIG. 14, over lead 503, to lead 510, to FIG. 22, and the upper input leg of the triple input leg "OR" gate 922, and to the output lead 923, to the upper input leg of reset control "AND" gate 921. The upper input leg is thus enabled and passes the end of azimuth gate pulse to the output lead 924, to the upper input leg of reset "OR" gate 915, to lead 916, firing thyratron 917, and energizing reset relay R over contacts 1m3, thereby resetting the main active circuits in accordance with the other of the two resetting methods referred to, so that they are prepared for the next active interrogation cycle.

When master relay 2M, or 3M, is in control of the interrogation, contacts 2m3 and 2s3, FIG. 22, or contacts 3m3 and 3s3, respectively, function similarly to contacts 1m3 and 1s3, when master relay 1M is in control.

When the fourth B.C. pulse is present and triggers the flip-flop 795 from its reset condition, the positive gate voltage which had enabled the lower input leg of reset control "AND" gate 921, is removed from lead 920, thus disabling the "AND" gate 921 and preventing it from passing the end of azimuth gate pulse and resetting the active circuits prematurely before the correctly coded reply could be properly registered on the decoder relays 1A to 12A, FIGS. 28 and 29. The release control flip-flop 795 thus permits the active decoding cycle to be completed before releasing the active decoding equipment.

In FIG. 28, the switch arm 925 of PI/TI selector switch

453, when in the PI, or upper position, connects ground to the lead 926, to which is connected one terminal of each of the PI-1 code lamps, displaying the "Left Letters" listed in Table No. 3. The switch arm 925, when in the TI, or lower position, connects ground to the lead 927, to which is connected one terminal of each of the TI-1 code lamps, displaying the "Tens" digits listed in Table No. 2. The switch arms 928, 929, and 930, of PI/TI selector switch 453, FIG. 28, control certain of the code lamp circuits selected by decoder relays 1A to 6A.

In FIG. 29, the switch arm 931 of PI/TI selector switch 453, when in the PI, or upper position, connects ground to the lead 932, to which is connected one terminal of each of the PI-2 code lamps, displaying the "Right Letters" listed in Table No. 3. The switch arm 931, when in the TI, or lower position, connects ground to the lead 933, to which is connected one terminal of each of the TI-2 code lamps, displaying "Units" digits, listed in Table No. 2. The switch arms 934, 935, and 936, of PI/TI selector switch 453, FIG. 29, control certain of the code lamp circuits selected by decoder relays 7A to 12A.

Each of the eight TI-1 numbered code lamps in FIG. 28 and the eight TI-2 numbered code lamps in FIG. 29, is provided with a crystal diode rectifier in series therewith, such as the diode 937 in series with the TI-1 code lamp "7," FIG. 28. These diodes are poled to pass the lamp signal current, and serve to prevent undesired interaction between the individual code lamp circuits.

The active code indicator 509, FIG. 30, presents the elongated horizontal display area 938, FIG. 31A, subdivided, as shown by the dotted lines 939 to 943, into six rectangular display module areas 944 to 949. Six code symbol positions are thus provided, although only two symbols are displayed at a time, as shown, for example, in FIG. 31B and 31C. Ten of the twenty PI-1 code lamps produce code letter displays in the module area 944, and the other ten of the twenty PI-1 code lamps produce code letter displays in the module area 945.

Ten of the twenty PI-2 code lamps produce code letter displays in the module area 946, and the other ten PI-2 code lamps produce code letter displays in the module area 947. The eight TI-1 code lamps produce code number displays in the module area 948, and the eight TI-2 code lamps produce code number displays in the module area 949. The PI-1 and PI-2 symbols are displayed in response to a valid reply code received from an actively interrogated aircraft when the PI/TI selector switch 453, FIGS. 28 and 29, is set in the PI position, the TI-1 and TI-2 symbols being displayed in response to a valid reply code received from an actively interrogated aircraft when switch 453 is set in the TI position.

Any well-known type of symbol displaying module, having a display area corresponding to one of the module areas 944 to 949, FIG. 31A, and capable of displaying any one of ten symbols in a single display area, may be utilized for making the active operation code indications of the present invention. One such display module, not shown, which has been employed with one embodiment of the present invention, is manufactured by the Burroughs Corporation, Detroit, Michigan, and identified as C-5/2010. Another type of module that may be used for this purpose is disclosed in U.S. Patent No. 2,874,320 to H. J. Hampel, it being necessary in this case to reverse the code voltage polarity of the source 910, FIG. 23 of the present invention, and to reverse the polarity of the diodes in series with the TI-1 and TI-2 code lamps, FIGS. 28 and 29.

A PI decoding operation by the contacts of decoder relays 1A to 12A, FIGS. 28 and 29, will now be described. Table No. 3 lists in the column marked "Left Letters," twenty PI-1 letters opposite the corresponding binary code bits set up by decoder relays 1A to 6A, FIG. 28, which register pulses in pulse positions 2 to 7, respectively. A pulse registered by a decoder relay is represented by a "1," and a registered absence of a pulse is represented by a "0" in Table No. 3. The column

marked "Right Letters" includes a similar list of twenty PI-2 letters opposite the corresponding code bits set up by decoder relays 7A to 12A, FIG. 29, which register pulses in pulse positions 9 to 14, respectively.

If we assume that an active PI interrogation has been transmitted to an aircraft, and that the aircraft has the PI code "AL," the reply code from the aircraft contains a pulse in each of the pulse positions 1, 2, 3, 4, 9, 10, 14, and 15. The test for the presence of the bracket pulses 1 and 15 is met in the circuits of FIG. 3, as previously described. The pulses in positions 2, 3, 4, 9, 10, and 14 are passed on to cause the operation of decoder relays 1A, 2A, 3A, 7A, 8A, and 12A, if we assume that three previous B.C. pulses from that particular aircraft have passed the sequence test in FIGS. 17 and 18.

Since there are three pulses and three absences of pulses in each half of the reply code, the PI bridge test is passed, and the PI code lamp supply circuits in FIGS. 28 and 29 are energized over lead 495, from FIG. 23 to FIG. 28, and over lead 912. The decoder relays 1A, 2A, and 3A are now latched up and a circuit may be traced from lead 912, to lead 950, through normally open transfer contacts 4 of decoder relay 2A, to lead 951, through contacts 4 of decoder relay 1A, over lead 952, contacts 4 of decoder relay 3A, through PI-1 code lamp A, to lead 926, to switch arm 925, to ground, thus lighting lamp A. Another circuit may be traced from lead 495, FIG. 29, to lead 953, through normally open transfer contacts 4 of decoder relay 7A, to lead 954, through contacts 4 of decoder relay 12A, to lead 955, through contacts 4 of decoder relay 8A, through PI-2 code lamp L, to lead 932, to switch arm 931, to ground, thus lighting lamp L. The resulting PI code indication by the lamps A and L, is shown in FIG. 31B.

A TI decoding operation by the contacts of decoder relays 1A to 12A, will now be described. Table No. 2 lists in the column marked "Tens," eight TI-1 digits opposite the corresponding binary code bits set up by decoder relays 1A to 6A. The column marked "Units" lists eight TI-2 digits opposite the corresponding binary code bits set up by decoder relays 7A to 12A.

If we assume that an active TI interrogation has been transmitted to an aircraft, and that the aircraft has the TI code "01," the reply code from the aircraft contains a pulse in each of the pulse positions 1, 9, and 15. The reply code, by having the pulses 1 and 15, passes the B.C. test, and will be assumed to have been preceded by three B.C. pulses which passed the B.C. sequence test in FIGS. 17 and 18. Since the PI/TI selector switch 453, FIGS. 28 and 29, is in the down position, the contact arms 852 and 853 have opened the bridge energizing circuit, and thus inhibited the PI bridges Nos. 1 and 2, FIGS. 28 and 29. Error relay 1E is thus inhibited, and the error lamp 507, FIG. 28, cannot be lighted.

The TI code lamp supply circuits are energized over lead 495, FIG. 28. The decoder relay 7A, FIG. 29, representing pulse position 9, is the only one of the decoder relays 1A to 12A, that is energized in response to the assumed TI reply code. In FIG. 28, a circuit may be traced from lead 495, to lead 912, to lead 950, through normally closed transfer contacts 4 of decoder relay 2A, through the closed contacts of arm 930 of PI/TI switch 453, through normally closed transfer contacts 6 of decoder relay 4A, through the closed lower contacts of arm 928 and normally closed transfer contacts 5 of decoder relay 6A, through TI-1 code lamp "0," to lead 927, to arm 925, and ground. TI-1 lamp "0" is thus lighted.

Another circuit may be traced from lead 495, FIG. 28, to FIG. 29, to lead 953, through the normally open transfer contacts 4 of decoder relay 7A, over lead 956, through the normally closed contacts 3, of decoder relay 11A, through TI-2 code lamp "1," to lead 933, to arm 931, to ground. TI-2 lamp "1" is thus lighted. The resulting TI code indication "01" by the lamps "0" and "1," is shown in FIG. 31C.

The circuits for the other PI and TI code indications corresponding to the codes listed in Tables Nos. 2 and 3, may be traced in a manner similar to that described above.

The features of the invention disclosed herein may obviously be employed to identify and locate the position of an object other than an aircraft, by providing such an object with equipment similar to that provided on an aircraft which is to be interrogated in one or more of the SI, PI, or TI modes.

It is to be understood that other forms of radiant energy or wire communication circuits may be used between the interrogating station and the interrogated object, instead of the described radio transmission, where the nature of the object, or its position, or surroundings are adapted for such use.

While the invention has been described as applied to a radar interrogating station utilizing three control and indicator units, more or less than three such units may be provided in accordance with the principles of the present invention by increasing or decreasing the number of master relays, and other parts of the station to correspond with the number of control and indicator units. It will be seen that the number of PI/TI comparers, FIG. 3, and the associated passive video circuits may be increased above or decreased below the three that are shown.

It is to be understood that various modifications of the invention other than those described above may be effected by persons skilled in the art without departing from the invention set forth in the appended claims.

What is claimed is:

1. In a decoder and indicator for determining the identity of a radar interrogated aircraft in response to the aircraft reply which, when valid, consists of a binary coded pulse train having a predetermined number of code bits and a bracket pulse in the first and last bit positions in the train, first means to test the validity of the reply train, including means to produce a bracket coincidence pulse in response to the bracket pulses when present in the train, second means responsive to the bracket coincidence pulse to further test the validity of the reply train, and means to produce an indication of the identity of the interrogated aircraft in response to a reply train meeting the tests of the first and second means and to prevent the indication when the train fails to meet said tests.

2. A decoder and indicator according to claim 1, in which said second means includes means to test the sequence of the reply train as a late train behind an earlier reply train of pulses and to count said bracket coincidence pulse as representative of a valid late reply train when the late train appears in predetermined timed succession after the early train, means to prevent the operation of the counting means when the late train fails to appear in the predetermined timed sequence, and means responsive to the counting of the late train to control said indication producing means.

3. A decoder and indicator according to claim 1, in which said second means includes means to test the reply code bits between the bracket pulses in the reply train for conformity with a verification code set up prior to the radar interrogation of the aircraft and to prevent the indication of the aircraft identification when the reply code disagrees with the verification code.

4. A decoder and indicator according to claim 1, in which the reply train, when valid, is without a pulse in the mid-position in the train, and said second means includes means to test the reply train for the presence of a pulse in the mid-position in the train and to inhibit the production of the identity indication when said mid-position pulse is present.

5. A decoder and indicator according to claim 1, in which the reply train, when valid, contains in the part thereof between said bracket pulses, a total number of pulse code bits equal to the total number of pulse-free

code bits, and said second means includes means to test the reply train to determine whether said number of pulse bits equals said number of pulse-free bits and to prevent the product of the identity indication when said numbers are unequal.

6. A decoder and indicator according to claim 1, in which the reply train, when valid, is divisible into two halves, each of which contains a total number of pulse code bits equal to the total number of pulse-free code bits, and said second means includes means to test each half of the reply train to determine whether the number of pulse bits equals the number of pulse-free bits therein and to prevent the production of the identity indication when said numbers are unequal in either half of the reply train.

7. A decoder and indicator according to claim 6, in which said equality testing means includes a circuit balancing bridge for each half of the reply train, and means to produce a bridge unbalance signal to inhibit said indication producing means when the bridge for either half of the reply train is unbalanced.

8. A decoder and indicator for determining the identity of a radar interrogated aircraft in response to the aircraft reply which, when valid, consists of a binary coded train of pulses having a predetermined number of code bits with a bracket pulse in the first and last bit positions in the train, means, including a delay line having taps, to change the train of reply bits into a group of simultaneous bits, each tap of the delay line being receptive to a different one of the reply code bits, means responsive to said bracket pulses to produce a bracket coincidence pulse therefrom, a separate two-input-leg tap "AND" gate for each tap of the delay line between the end taps thereon, each tap gate having one input leg thereof enabled in response to a pulse on its corresponding delay line tap, the other input leg being enabled in response to said bracket coincidence pulse, means responsive to the outputs of the tap "AND" gates for testing the validity of the reply code, an indicator, and means to transmit an aircraft identification signal to the indicator when the reply code meets the validity test and to prevent the transmission of the signal when the reply code fails to meet the validity test.

9. In a decoder and indicator for determining the identity of a radar interrogated aircraft, a decoder unit including means to produce a first video pulse signifying identification of the aircraft in a first mode code in response to a valid pulse train, coded in the first mode, received as a reply from the interrogated aircraft, said decoder unit also including means to produce a second video pulse signifying identification of the aircraft in a different second mode code in response to a valid pulse train, coded in the second mode, received from the interrogated aircraft in interlaced relation to the pulse train in the first mode code, mixing means to select either said first or second video pulse, or both together, and means, including a PPI unit, to display a blip of predetermined character when either said first or second video pulse is selected by said mixing means, and to display a blip of different predetermined character when both of said pulses are selected by said mixing means.

10. A decoder and indicator according to claim 9, in which said mixing means stretches said second video pulse when said first and second video pulses are selected together by the mixing means.

11. In a radar interrogating station for determining the identity of an aircraft, means, including a PPI unit, to display a PPI blip indicating the range and azimuth of the aircraft in response to a reply to a radar interrogation thereof, means controlled by an operator at the radar station to select for active interrogation in a predetermined mode the aircraft represented by said blip, means responsive to said selecting means to produce a PPI strobe of light surrounding the blip to mark the blip of the aircraft selected for active interrogation and to display the

area to which a reply in response to that interrogation will be restricted, means responsive to said selecting means to initiate an active interrogation of the aircraft in said predetermined mode, means to decode the resulting reply train of pulses coded in said predetermined mode received from the aircraft, and means to produce a symbol indication of the code of said aircraft in said mode in response to the resulting decoded reply train.

12. A radar interrogating station according to claim 11, including means responsive to said selecting means to count a predetermined number of blip producing replies received in predetermined timed succession from the interrogated aircraft before said interrogation initiating means can operate, and means to prevent the initiation of the interrogation in said predetermined mode when said blip producing replies fail to appear in said predetermined timed succession.

13. A radar interrogating station according to claim 11, including means responsive to said decoding means to test the decoded reply train for the presence therein of a total number of code bits of one binary value which is equal to the total number of code bits of opposite binary value, and means responsive to said equality testing means, to prevent the production of said symbol indication when the decoded reply train fails to meet said equality test.

14. In a radar station for interrogating an aircraft, a decoder unit including means to test the validity of each of a series of coded pulse trains received from an aircraft as passive radar interrogation replies representing a predetermined code of the aircraft, means in said decoder unit to produce a signal to represent each passive reply train that is found valid by said test means, a separate PPI display unit for each of a plurality of operators, means, including a separate control unit for each operator, to transmit to the PPI unit of that operator each said passive reply signal from said signal producing means to indicate by the resulting passive interrogation reply blip displayed on the PPI unit that the predetermined code of the aircraft has been identified and to indicate the range and azimuth of the aircraft, operator controlled means in each control unit to select for active interrogation the aircraft represented by a passive blip at any desired location in the display of the PPI unit for that control unit, and to transmit to the decoder unit a signal to request an active interrogation of the selected aircraft, central means in the decoder unit to process coded pulse trains received from the selected aircraft in reply to interrogations, said central means having an output for an active interrogation reply processed thereby, separate master control means in the decoder unit for each control unit, said master control means for any given control unit being responsive to the active interrogation request signal from that control unit, to seize control of said central means for the duration of an active interrogation cycle when no other control unit is exercising such control and to prevent interference with the operation of said central means by any other control unit during the active interrogating cycle, means to initiate an active interrogation of said selected aircraft in response to said request signal, code indicating means in each control unit, and means in the decoder unit to selectively connect said active interrogation reply output of said central means to the code indicating means in the control unit originating an active interrogation to indicate the actively interrogated code of said selected aircraft.

15. A radar station according to claim 14, including means responsive to said operator controlled means in the control unit which selects an aircraft for active interrogation, to produce a strobe of light surrounding the PPI blip representing the selected aircraft, to indicate that the operator selecting the aircraft has seized control of said central means, and to indicate the area from which an interrogation reply will be accepted.

16. A radar station according to claim 14, in which

said central means includes means to test the sequence of a predetermined number of said passive interrogation reply trains of pulses before initiating said active interrogation, and to prevent the initiation of said active interrogation when the passive interrogation reply trains fail to appear in a predetermined timed sequence.

17. A radar station according to claim 14, in which said code indicating means in each control unit, includes means to test the validity of the code of the active interrogation reply of an aircraft selected for active interrogation by that control unit, and said central means in said decoder unit includes means to prevent said code indication when the said reply code fails to meet said validity test.

18. A radar station according to claim 14, in which said central means includes means to prevent the transmission to said PPI unit of said signal representing a passive reply train during a predetermined period in which said active interrogation initiating means responds to said request signal.

19. In a decoder and indicator for determining the identity and location of a radar interrogated aircraft in response to the aircraft reply which, when valid, consists of a binary coded pulse train having a predetermined number of code bits and a bracket pulse in the first and last bit positions in the train, means to produce a bracket coincidence pulse in response to the bracket pulses when present in the train, comparer means responsive to the bracket coincidence pulse to compare certain code bits positioned between the bracket pulses in the reply train with the code bits in a verification code set up by an operator before interrogation of the aircraft, a PPI unit to display a blip in a range and azimuth position corresponding to the timing of a pulse transmitted to the PPI unit, and means to transmit a blip producing pulse to the PPI unit in timed relation to the reply train when the reply code agrees with said verification code and to prevent the transmission of said pulse when said codes fail to agree.

20. A decoder and indicator according to claim 19, in which said comparer means includes a separate test means corresponding to each of a plurality of reply code bits being compared, each of said test means being responsive to its corresponding reply code bit to produce an output pulse when said reply code bit disagrees with its corresponding verification code bit and to produce no output pulse when said bits agree, and means to combine the outputs of all of said test means, to produce a single inhibit pulse in response to an output pulse from one or more of said test means, said means for transmitting a blip producing pulse to the PPI unit, including means responsive to said inhibit pulse to prevent the transmission of the blip producing pulse to the PPI unit.

21. A decoder and indicator according to claim 20, in which each of said separate test means is an exclusive "OR" gate circuit.

22. A decoder and indicator according to claim 20, including second test means having a different operating characteristic from that of said first named test means, to test for the presence of an invalid pulse in the pulse train in a bit position not tested by said first named test means, said second test means being responsive to said invalid pulse to provide a nonconformity signal, said output com-

binning means being responsive to said nonconformity signal to produce said inhibit pulse.

23. A decoder and indicator according to claim 22, in which said first named test means is an exclusive "OR" gate circuit, and said second test means is a circuit containing only a single diode rectifier.

24. In a comparer for testing the conformity of code bits received in a binary coded pulse train with code bits in corresponding positions in a verification code, means to set up the verification code, including a separately operable switch for each code bit to be tested in the train, to represent the binary values of that code bit by the open and closed condition respectively, of the switch, means to change the pulse train from a succession of code bits to a group of simultaneous code bits, separate test means for each received code bit to be tested, to compare said bit while in said group with the corresponding verification code bit and to produce a nonconformity signal when said code bits disagree, and output means to produce a single output pulse in response to said nonconformity signal from one or more of said separate test means.

25. A comparer according to claim 24, in which each of said separate test means is an exclusive "OR" gate circuit.

26. A comparer according to claim 24, including second test means having a different operating characteristic from that of said first named test means, to test for the presence of an invalid pulse in the pulse train in a bit position not tested by said first named test means, said second test means being responsive to said invalid pulse to produce a nonconformity signal, said output means being responsive to said nonconformity signal to produce said single output pulse.

27. A comparer according to claim 26, in which said first named test means is an exclusive "OR" gate circuit, and said second test means is a circuit containing only a single diode rectifier.

28. In a decoder and indicator for determining the identity of a radar interrogated aircraft, a decoder unit having means therein to process a coded reply from a selected interrogated aircraft, a separate control unit for each of a number of operators connected to said decoder unit, operator controlled means in each control unit to transmit a control signal to the decoder unit, separate master control means in the decoder unit corresponding to each control unit, any given master control means being actuated in response to said control signal from the corresponding control unit when that control unit is the first to transmit a control signal to the decoder unit, to selectively connect the output of said interrogation reply processing means exclusively to that control unit and to disable the other of said master control means during actuation of said given master control means, and means in each control unit, effective when the output of said reply processing means is selectively connected thereto, to produce a symbol indication of the code of the selected aircraft when a valid reply code is received therefrom by the decoder unit.

References Cited in the file of this patent

UNITED STATES PATENTS

2,706,810 Jacobsen ----- Apr. 19, 1955