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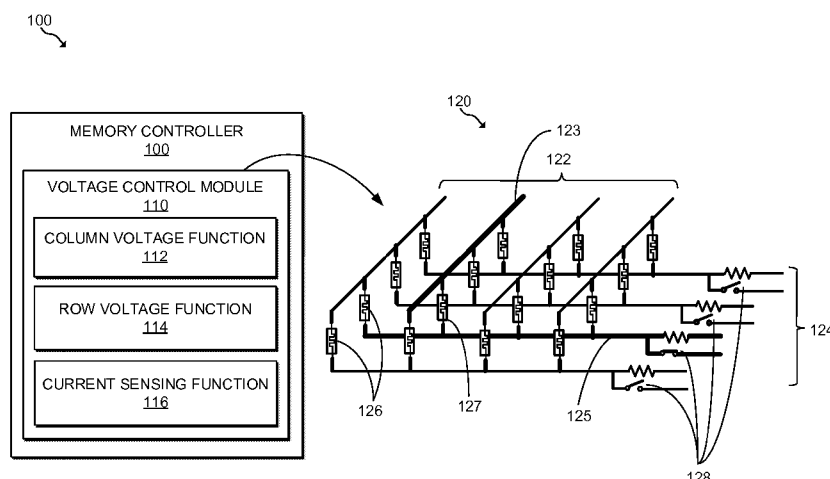
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(54) **Title:** MEMORY CONTROLLERS**FIG. 1**

(57) **Abstract:** A memory controller includes a voltage control module that operates to isolate a target memristor of a memory crossbar array. The voltage control module applies a column voltage to a column line coupled to the target memristor, applies a first row voltage to all row lines not coupled to the target memristor and a second row voltage to a row line coupled to the target memristor, and senses a current through the target memristor to determine a state of the target memristor. The memory crossbar array includes a plurality of column lines, a plurality of row lines, a plurality of memristors, and a plurality of shorting switches. Each memristor is coupled between a unique combination of one column line and one row line. Each shorting switch has a high impedance resistor and a low impedance transistor, and each shorting switch is coupled to an end of a unique row line.

MEMORY CONTROLLERS

BACKGROUND

[0001] Memory controllers are devices that can operate a memory device, such as memristor-based memories. Memristor-based memories may involve crossbar arrays of memristors. Memristors are devices that can be programmed to different resistive states by applying a programming energy, such as a voltage. After programming, the state of the memristor can be read and remains stable over a specified time period. Thus, memristors can be used to store digital data. For example, a high resistance state can represent a digital “0” and a low resistance state can represent a digital “1.” Large crossbar arrays of memristive elements can be used in a variety of applications, including random access memory, non-volatile solid state memory, programmable logic, signal processing control systems, pattern recognition, and other applications.

BRIEF DESCRIPTION OF THE DRAWINGS

[0002] The following detailed description references the drawings, wherein:

[0003] FIG. 1 is a block diagram of an example memory controller for isolating memristors in a memory crossbar array and a schematic of an example memory crossbar array;

[0004] FIG. 2 is a block diagram of an example system having a memory controller for isolating memristors in a memory crossbar array;

[0005] FIG. 3A is a flowchart of an example method for isolating a target memristor;

[0006] FIG. 3B is a flowchart of an example method for isolating a target memristor including shorting a switch.

DETAILED DESCRIPTION

[0007] Memristors are devices that may be used as components in a wide range of electronic circuits, such as memories, switches, radio frequency circuits, and logic circuits and systems. In a memory structure, a crossbar array of memristors or memristive devices may be used. When used as a basis for memories, memristors may be used to store bits of information, 1 or 0. The resistance of a memristor may be changed by applying an electrical stimulus, such as a voltage or a current, through the memristor. Generally, at least one channel may be formed that is capable of being switched between two states—one in which the channel forms an electrically conductive path (“ON”) and one in which the channel forms a less conductive path (“OFF”). In some other cases, conductive paths represent “OFF” and less conductive paths represent “ON”. Conducting channels may be formed by ions and/or vacancies.

[0008] Using memristors in crossbar arrays may lead to read and/or write failure due to sneak currents passing through the cells that are not selected—for example, cells on the same row or column as a targeted cell. Failure may arise when the total sneak current through untargeted neighboring cells from an applied voltage is higher than the current through the targeted memristor. Using a transistor or selector with each memristor has been proposed to isolate each cell and overcome the sneak current. However, using a transistor or selector with each memristor in a crossbar array limits array density and increases cost, which may impact the commercialization of memristive devices. In some applications, such as memristors on print heads, device architecture modifications may not be an effective solution. Thus, some effort has been spent in identifying alternative solutions for mitigating the sneak current problem.

[0009] Examples disclosed herein provide for memory controllers for isolating memristors of a memory crossbar array. In example implementations, memory controllers have a voltage control module that operates to isolate a target memristor by applying equipotential voltage to all memristors connected to the same row line or the same column line as the target memristor. Without subscribing to any particular theory, little or no current flows through a component when the voltage difference across the component is zero or

minimal. Accordingly, by applying equipotential voltage across the other memristors, the target memristor may be virtually isolated.

[0010] In this manner, isolating a target memristor in a crossbar array may mitigate the impact of sneak currents on reading the targeted memristor. Additionally, the size of crossbar arrays may be minimized by avoiding the use of added selectors, transistors, or other components. These features may allow the creation of highly integrated memory architectures, particularly within certain design and size limitations.

[0011] Referring now to the drawings, FIG. 1 depicts an example memory controller 100 having a voltage control module 110 that operates to isolate a target memristor 127 of a memory crossbar array 120 for a read operation. Memory controller 100 may have a column voltage function 112 for applying a column voltage to a column line 123 coupled to a target memristor 127, a row voltage function 114 for applying a first row voltage to all row lines 124 not coupled to target memristor 127 and applying a second row voltage to a row line, depicted here as row line 125, coupled to target memristor 127, and a current sensing function 116 for sensing a current passing through target memristor 127 to determine the state of target memristor 127. Memory crossbar array 120 may have a plurality of column lines 122, a plurality of row lines 124, a plurality of memristors 126, and a plurality of shorting switches 128.

[0012] Memory controller 100 may be an electrical device or component that, in addition to other functions, operates or controls a memory device. The implementation of memory controller 100 may include hardware-based components, such as a microchip, chipset, or electronic circuit, and software-driven components, such as a processor, microprocessor, or some other programmable device. In some examples, memory controller 100 may be a circuit having a multiplexer that may direct voltage or current to specific lines within an array, such as memory crossbar array 120.

[0013] Memory controller 100 may have voltage control module 110, which may operate to isolate a target memristor of a crossbar array. Voltage control module 100 may include an instruction, set of instructions, process, operation, logic, technique, function, firmware, and/or software executable by memory controller 100. Voltage control module 110 may

isolate target memristor 127 of memory crossbar array 120 by the operation of column voltage function 112, row voltage function 114, and current sensing function 116.

[0014] Memory crossbar array 120 may be a configuration of parallel and perpendicular lines with memory cells coupled between lines at cross-points. Such an architecture is generally referred to as a crossbar or cross-point array. Memory crossbar array 120 may include a plurality of column lines 122, a plurality of row lines 124, a plurality of memristors 126, and a plurality of shorting switches 128. Each memristor 126 may function as a memory cell within memory crossbar array 120.

[0015] Column lines 122 may be electrically conducting lines that carry current throughout memristor crossbar array 120. Column lines 122 may be in parallel to each other, generally with equal spacing. Column lines 122 may sometimes be referred to as bit lines. Depending on orientation, column lines 122 may alternatively be referred to as word lines. Similarly, row lines 124 may be conducting lines that run perpendicular to column lines 122. Row lines 124 may be referred to as word lines in some conventions. In other orientations, row lines 124 may refer to bit lines. Column lines 122 and row lines 124 may be made of conducting materials, such as platinum (Pt), tantalum (Ta), hafnium (Hf), zirconium (Zr), aluminum (Al), cobalt (Co), nickel (Ni), iron (Fe), niobium (Nb), molybdenum (Mo), tungsten (W), copper (Cu), titanium (Ti), tantalum nitrides (TaN_x), or titanium nitrides (TiN_x).

[0016] Memristors 126 may be coupled between column lines 122 and row lines 124, which may mean forming a continuous electrical connection between a column line 122, a memristor 126, and a row line 124. Each memristor 126 may be between a unique combination of one column line 122 and one row line 124. In other words, no two memristors 126 share both a column line 122 and row line 124. In such a manner, each memristor 126 may function as a memory cell in crossbar array 120. A memristor 126 may be an electrical component that may change resistance when a voltage is applied across it or a current is driven through it. Furthermore, a memristor 126 may “memorize” its last resistance. In this manner, each memristor 126 may be set to at least two states.

[0017] Memristors 126 may be based on a variety of materials. Each memristor 126 may be oxide-based, meaning that at least a portion of the memristor is formed from an oxide-containing material. Each memristor 126 may also be nitride-based, meaning that at least a

portion of the memristor is formed from a nitride-containing composition. Furthermore, each memristor 126 may be oxy-nitride based, meaning that a portion of the memristor is formed from an oxide-containing material and that a portion of the memristor is formed from a nitride-containing material. In some examples, a memristor 126 may be formed based on tantalum oxide (TaO_x) or hafnium oxide (HfO_x) compositions. Other example materials of memristors 126 may include titanium oxide, yttrium oxide, niobium oxide, zirconium oxide, aluminum oxide, calcium oxide, magnesium oxide, dysprosium oxide, lanthanum oxide, silicon dioxide, or other like oxides. Further examples include nitrides, such as aluminum nitride, gallium nitride, tantalum nitride, and silicon nitride. In addition, other functioning memristors may be employed in the practice of the teachings herein.

[0018] Each memristor 126 may have electrodes on each end that serve to couple the memristor to a column line 122 and a row line 124. Electrodes may generally have an electrically conducting material in order to create an electrical path with the column line 122 and the row line 124. Example materials for electrodes of memristor 126 may include metals such as platinum or other conducting material such as tantalum nitrides and titanium nitrides.

[0019] Shorting switches 128 may be coupled to the end of row lines 124. A shorting switch 128 may be a device that impacts the amount of current that may pass through a line coupled to the shorting switch. A shorting switch 128 may have a high impedance resistor and a low impedance transistor. A shorting switch 128 may short the row line 124 to which it is coupled by switching the low impedance transistor. Row lines 124 not coupled to target memristor 127 may have the shorting switch set so a current resulting from the first row voltage will go through the high impedance resistor, which may reduce or alter the current going through each row line 124. In one example, shorting switch 128 may have a pass transistor circuit that serves as the logic gate driving the switching function. It should be noted that while example memory crossbar array 120 is shown with shorting switches 128 coupled to the ends of row lines 124, in some other examples, shorting switches 128 may be coupled to column lines 122.

[0020] Voltage control module 110 may isolate target memristor 127 by applying the equipotential principle described above. To do so, voltage control module 110 may utilize the operation of column voltage function 112, row voltage function 114, and current sensing

function 116. Column voltage function 112 may apply a voltage, such as a read voltage, to drive a current to the column line 123 that is coupled to target memristor 127, which is the memory cell being read, for example. In one example, column voltage function 112 directs a multiplexer circuit of memory controller 100 to direct the current to column line 123. However, the current may not solely pass through target memristor 123. Instead, various amounts of current may sneak through the other memristors 126 that are coupled to column line 123.

[0021] To isolate target memristor 123, row voltage function 114 may apply a first row voltage to all row lines 124 that are not coupled to target memristor 127. The row line coupled to target memristor 127 is depicted in FIG. 1 by row line 125. By applying the first row voltage to row lines 124, the voltage drop across the untargeted memristors 126 may be reduced or eliminated, which in turn reduces or eliminates the current flow through each memristor 126. As described above, current is a function of voltage drop by the following equation:

$$I = \Delta V / R \quad [\text{Equation 1}],$$

where:

I is the current across the memristor,

ΔV is the voltage difference across the memristor, and

R is the resistance of the memristor.

[0022] When the voltage difference, ΔV , is zero, the current through memristor 126 is also zero. In some example implementations, the first row voltage applied by row voltage function 114 may be the same voltage as the voltage applied by column voltage function 112. In such examples, ΔV may be zero and the resulting current through the coupled memristor 126 may also be zero. In some other examples, the first row voltage applied by row voltage function 114 may be half of the column voltage applied by column voltage function 112.

[0023] Row voltage function 114 may also apply a second row voltage to row line 125 coupled to target memristor 127. The second row voltage may be a ground voltage. The ground voltage may create a voltage drop across target memristor 127 that is equal or close to the column voltage applied by column voltage function 112. Grounding row line 125

coupled to target memristor 127 may allow controlling the column voltage to drive a desired read current through target memristor 127.

[0024] Current sensing function 116 may sense a current passing through target memristor 127. In some examples, the current may be used to read target memristor 127 by determining the resistance state of target memristor 127. Current sensing function 116 may employ a sensor or sensors connected to column lines 122 or row lines 124 or both. In some implementations, a current that is sensed by current sensing function 116 may include additional currents, such as sneak currents from other row lines 124 as a result of the row voltages applied by row voltage function 114. Current sensing function 116 may filter additional currents and accurately sense the read current for target memristor 127.

[0025] In some implementations, voltage control module 110 may further include a function for shorting the shorting switches 128. Shorting the switch 128 coupled to row line 125 coupled to target memristor 127 may make row line 125 conducting for both the read current from the column voltage and also sneak currents from the first row voltages. Doing so prevents the equipotential effect on target memristor 127. Accordingly, a read current may pass through target memristor 127 by the column voltage applied by column voltage function 112.

[0026] FIG. 2 depicts an example system 200 having a memory controller 220 for isolating memristors 216 in a memory crossbar array 210. Memory crossbar array 210 may have a plurality of column lines 212, a plurality of row lines 214, a plurality of memristors 216, and a plurality of shorting switches 218. Each memristor 216 may be coupled between a unique combination of one column line 212 and one row line 214. Each shorting switch 218 may be coupled to an end of a unique row line 214. Memory controller 220 may have a voltage control module 225 that operates to isolate target memristor 217 in memory crossbar array 210.

[0027] Similar to memory controller 100 of FIG. 1, memory controller 220 may be an electrical device or component that, in addition to other functions, operates or controls a memory device. The implementation of memory controller 220 may include hardware-based components, such as a microchip, chipset, or electronic circuit, and software-driven components, such as a processor, microprocessor, or some other programmable device. In

some examples, memory controller 220 may be a circuit having a multiplexer that may direct voltage or current to specific lines within an array, such as memory crossbar array 210.

[0028] Memory controller 220 may have voltage control module 225, which may operate to isolate a target memristor of a crossbar array. Voltage control module 225 may include an instruction, set of instructions, process, operation, logic, technique, function, firmware, and/or software executable by memory controller 220. Voltage control module 225 may isolate target memristor 217 of memory crossbar array 210 by the operation of column voltage function 225A, row voltage function 225B, and current sensing function 225C.

[0029] Similar to memory crossbar array 120 of FIG. 1, memory crossbar array 210 may be a configuration of parallel and perpendicular lines with memory cells coupled between the lines at cross-points. Column lines 212 may be electrically conducting lines that carry current throughout memristor crossbar array 210. Column lines 212 may be in parallel to each other, generally with equal spacing. Column lines 212 may sometimes be referred to as bit lines. Depending on orientation, column lines 212 may alternatively be referred to as word lines. Relatedly, row lines 214 may be conducting lines that run perpendicular to column lines 212. Row lines 214 may be referred to as word lines in some conventions. In other orientations, row lines 214 may refer to bit lines. Column lines 212 and row lines 214 may be made of conducting materials, such as platinum (Pt), tantalum (Ta), hafnium (Hf), zirconium (Zr), aluminum (Al), cobalt (Co), nickel (Ni), iron (Fe), niobium (Nb), molybdenum (Mo), tungsten (W), copper (Cu), titanium (Ti), tantalum nitrides (TaN_x), or titanium nitrides (TiN_x).

[0030] Memristors 216 may be coupled between column lines 212 and row lines 214, which may mean forming a continuous electrical connection between a column line 212, a memristor 216, and a row line 214. Each memristor 216 may be between a unique combination of one column line 212 and one row line 214. In other words, no two memristors 216 share both a column line 212 and row line 214. In such a manner, each memristor 216 may function as a memory cell in crossbar array 210. A memristor 216 may be an electrical component that may change resistance when a voltage is applied across it or a current is driven through it. Furthermore, a memristor 216 may “memorize” its last resistance. In this manner, each memristor 216 may be set to at least two states. Various types of memristors

may be employed in the practice of the teachings herein, including oxide-based memristors and nitride-based memristors.

[0031] Shorting switches 218 may be coupled to the end of row lines 214. A shorting switch 218 may be a device that impacts the amount of current that may pass through a line coupled to the shorting switch. In some implementations, a shorting switch 214 may have a high impedance resistor and a low impedance transistor. A shorting switch 218 may short the row line 214 to which it is coupled by switching the low impedance transistor. Row lines 214 not coupled to target memristor 217 may have the shorting switch set so a current resulting from the first row voltage will go through the high impedance resistor, which may reduce or alter the current going through each row line 214. In some examples, shorting switch 218 may have a pass transistor circuit that serves as the logic gate driving the switching function. It should be noted that while example memory crossbar array 210 is shown with shorting switches 218 coupled to the ends of row lines 214, in some other examples, shorting switches 218 may be coupled to column lines 212.

[0032] In some implementations, memory crossbar array 210 may further include a plurality of selectors. Each selector may be coupled in series with a unique memristor 216. Selector may be electrical components placed in series with memristors 216 that controls the overall electrical properties of the resulting combinations. In many examples, a selector coupled to memristor 216 may have current-voltage nonlinearity. In other words, when the voltage applied across the selector is changed, the current passing through the selector changes by a factor, "k". Generally, the factor "k" may be a function of voltage. Selectors in memory crossbar array 210 may be any type of selector. Examples may include crested tunnel barrier selectors and non-differential resistance selectors.

[0033] Similar to voltage control module 110 of FIG. 1, voltage control module 225 may isolate target memristor 217 by applying the equipotential principle. To do so, voltage control module 225 may utilize the operation of column voltage function 225A, row voltage function 225B, and current sensing function 225C. Column voltage function 225A may apply a voltage, such as a read voltage, to drive a current to the column line 213 that is coupled to target memristor 217, which is the memory cell being read, for example. In one example, column voltage function 225A directs a multiplexer circuit of memory controller 220 to direct

the current to column line 213. However, the current may not solely pass through target memristor 213. Instead, various amounts of current may sneak through the other memristors 216 that are coupled to column line 213.

[0034] To isolate target memristor 217, row voltage function 225B may apply a first row voltage to all row lines 214 that are not coupled to target memristor 217. The row line coupled to target memristor 217 is depicted in FIG. 2 as row line 215. By applying the first row voltage to row lines 214, the voltage drop across the untargeted memristors 216 may be reduced or eliminated, which in turn reduces or eliminates the current flow through each memristor 216. As previously described, current is a function of voltage drop by Equation 1 above. According to Equation 1, when the voltage difference, ΔV , is zero, the current through a memristor 216 is also zero. In some example implementations, the first row voltage applied by row voltage function 225B may be the same voltage as the voltage applied by column voltage function 225A. In such examples, ΔV may be close to zero and the resulting current through the coupled memristor 216 may also be close to zero. In another example, the first row voltage applied by row voltage function 225B may be half of the column voltage applied by column voltage function 225A.

[0035] Row voltage function 225B may also apply a second row voltage to row line 215 coupled to target memristor 217. The second row voltage may be a ground voltage. The ground voltage may create a voltage drop across target memristor 217 that is equal or close to the column voltage applied by column voltage function 225A. Grounding row line 215 coupled to target memristor 217 may allow controlling the column voltage to drive a desired read current through target memristor 217.

[0036] Current sensing function 225C may sense a current passing through target memristor 217. In some examples, the current may be used to read target memristor 217 by determining the resistance state of target memristor 217. Current sensing function 225C may employ a sensor or sensors connected to column lines 212 or row lines 214 or both. In some implementations, a current that is sensed by current sensing function 225C may include additional currents, such as sneak currents from other row lines 214 as a result of the first row voltages applied by row voltage function 225B. Current sensing function 225C may filter additional currents and accurately sense the read current for target memristor 217.

[0037] In some implementations, voltage control module 225 may further include a function 225D for shorting the shorting switches 218. Shorting the switch 218 coupled to row line 215 coupled to target memristor 217 may make row line 215 conducting for both the read current from the column voltage and also sneak currents from the first row voltages. Doing so prevents the equipotential effect on target memristor 217. Accordingly, a read current may pass through target memristor 217 by the column voltage applied by column voltage function 225A.

[0038] In addition to voltage control module 225, in some examples, memory controller 220 may have an input-output module 230. Similar to voltage control module 225, input-output module 230 may include an instruction, set of instructions, process, operation, logic, technique, function, firmware, and/or software executable by memory controller 220. Input-output module 230 may operate to send and receive data, information, and/or signal between memory controller 220 and the other components of system 200. In addition or as an alternative, in some examples, input-output module 230 may send and receive data, information, and/or signal between system 200 and any devices to which system 200 is connected, operates with, or of which system 200 is a part. For example, input-output module 230 operates to send data to and from system 200 and a computer of which system 200 is a part. In general, input-output module 230 may allow communications between the components of system 200 and between system 200 and other devices or systems.

[0039] FIG. 3A is a flowchart of an example method 300 for isolating a target memristor, which may include block 310 for applying a column voltage to a column line coupled to a target memristor of a memory crossbar array, block 320 for applying a first row voltage to all row lines of the memory array not coupled to the target memristor and a second row voltage to the row line coupled to the target memristor, and block 330 for sensing a current in the row line coupled to the target memristor to determine a state of the target memristor. Although execution of method 300 is herein described in reference to isolating a target memristor by the memory controller 100 of FIG. 1, other suitable parties for implementation of method 300 should be apparent, including, but not limited to, system 200 of FIG. 2.

[0040] Method 300 may start in block 310, where a column voltage is applied to column line 123 coupled to target memristor 127 of memory crossbar array 120. A column voltage

may be applied via a memory controller, for example memory controller 100, by a voltage control module, such as voltage control module 110. A column voltage applied in block 310 may be a read voltage for reading the state of target memristor 127. A read voltage may be used to determine the resistance of target memristor 127.

[0041] After applying a column voltage, method 300 may proceed to block 320, where a first row voltage is applied to all row lines 124 not connected to target memristor 127 and a second row voltage is applied to row line 125 coupled to target memristor 127. Row voltages may be applied via a memory controller, for example memory controller 100, by a voltage control module, such as voltage control module 110. A first row voltage applied in block 320 may be the same voltage as the column voltage applied in block 310. In such instances, the sneak current through non-targeted memristors 126 on column 123 may be eliminated due to equipotential effect. In some other examples, a row voltage may be half the voltage of the column voltage applied in block 310. In such instances, the sneak currents through non-targeted memristors 126 on column 123 may be reduced due to equipotential effect. A second row voltage applied may be a ground voltage. Further details of the equipotential effect are described above in relation to row voltage function 114 of FIG. 1.

[0042] After applying a row voltage, method 300 may proceed to block 330, where a current through target memristor 127 is sensed in order to determine the state of target memristor 127. In some examples, the current may be sensed to read target memristor 127 by determining the resistance state of target memristor 127. Current may be sensed by a sensing function such as current sensing function 116. Current sensing function 116 may employ a sensor or sensors connected to column lines 122 or row lines 124 or both. In some implementations, a current that is sensed by current sensing function 116 may include additional currents, such as sneak currents from other row lines 124 as a result of the row voltages applied in block 310. Current sensing function 116 may filter additional currents and accurately sense the read current for target memristor 127.

[0043] FIG. 3B is a flowchart of an example method 350 for isolating a memristor, which further includes shorting a shorting switch. Method 350 may include method 300 and block 360 for shorting a shorting switch 128. Although execution of method 350 is herein described in reference to isolating target memristor 127 of memory crossbar array 120 as depicted in

FIG. 1, other suitable parties for implementation of method 350 should be apparent, including, but not limited to, system 200 of FIG. 2.

[0044] In block 360, at least one shorting switch 128 may be shorted. Shorting the shorting switch 128 coupled to row line 125, which is in turn coupled to target memristor 127, may make row line 125 conducting for the addressing current from the column voltage. Furthermore, shorting the shorting switch 128 allows the second row voltage applied by row voltage function 114 to prevent or mitigate the equipotential effect on target memristor 127. Accordingly, a sensing current may pass through target memristor 127 by the column voltage applied by column voltage function 112.

CLAIMS

What is claimed is:

1. A memory controller, comprising a voltage control module that operates to isolate a target memristor of a memory crossbar array by applying a column voltage to a column line coupled to the target memristor, applying a first row voltage to all row lines not coupled to the target memristor and a second row voltage to a row line coupled to the target memristor, and sensing a current through the target memristor to determine a state of the target memristor, wherein the memory crossbar array comprises:
 - a plurality of column lines;
 - a plurality of row lines;
 - a plurality of memristors, each memristor coupled between a unique combination of one column line and one row line; and
 - a plurality of shorting switches, each shorting switch coupled to an end of a unique row line, and each shorting switch comprising a high impedance resistor and a low impedance transistor.
2. The memory controller of claim 1, wherein the voltage control module further operates to apply the first row voltage to each row line not coupled to the target memristor via the high impedance resistor of each row line's shorting switch and to apply a ground voltage as the second row voltage to a row line coupled to the target memristor via the low impedance transistor of the row line's the shorting switch.
3. The memory controller of claim 2, wherein the voltage control module further operates to short the shorting switch coupled to the row line coupled to the target memristor.
4. The memory controller of claim 1, wherein the first row voltage is the same as the column voltage.

5. The memory controller of claim 1, wherein the first row voltage is half of the column voltage.
6. A system, comprising:
 - a memory crossbar array, wherein the memory crossbar array comprises a plurality of column lines, a plurality of row lines, and a plurality of memristors, each memristor coupled between a unique combination of one column line and one row line, and a plurality of shorting switches, each shorting switch coupled to an end of a unique row line, and each shorting switch comprising a high impedance resistor and a low impedance transistor; and
 - a memory controller, wherein the memory controller comprises a voltage control module that operates to isolate a target memristor by applying a column voltage to the column line coupled to the target memristor, applying a first row voltage to all row lines not coupled to the target memristor and a second row voltage to a row line coupled to the target memristor, and sensing a current through the target memristor to determine a state of the target memristor.
7. The system of claim 6, wherein the voltage control module further operates to apply the first row voltage to each row line not coupled to the target memristor via the high impedance resistor of each row line's shorting switch and to apply a ground voltage as the second row voltage to a row line coupled to the target memristor via the low impedance transistor of the row line's shorting switch.
8. The system of claim 7, wherein the voltage control module further operates to short the shorting switch coupled to the row line coupled to the target memristor.
9. The system of claim 6, wherein the first row voltage is the same as the column voltage.
10. The system of claim 6, wherein the first row voltage is half of the column voltage.

12. The system of claim 6, wherein the memory controller further comprises an input-output module.
13. A method for isolating a target memristor, comprising:
- applying a voltage to a column line coupled to a target memristor of a memory crossbar array, the memory crossbar array comprising a plurality of column lines, a plurality of row lines, a plurality of memristors, wherein each memristor is coupled between a unique combination of a column line and a row line, and a plurality of shorting switches, each shorting switch coupled to an end of a unique row line and each shorting switching comprising a high impedance resistor and a low impedance transistor;
 - applying a first row voltage to all row lines of the memristor crossbar array not coupled to the target memristor and a second row voltage to a row line coupled to the target memristor; and
 - sensing a current through the target memristor to determine a state of the target memristor.
14. The method of claim 13, further comprising applying the first row voltage to each row line not coupled to the target memristor via the high impedance resistor of each row line's shorting switch and applying a ground voltage as the second row voltage to a row line coupled to the target memristor via the low impedance transistor of the row line's shorting switch.
15. The method of claim 13, further comprising shorting the shorting switch coupled to the row line coupled to the target memristor.

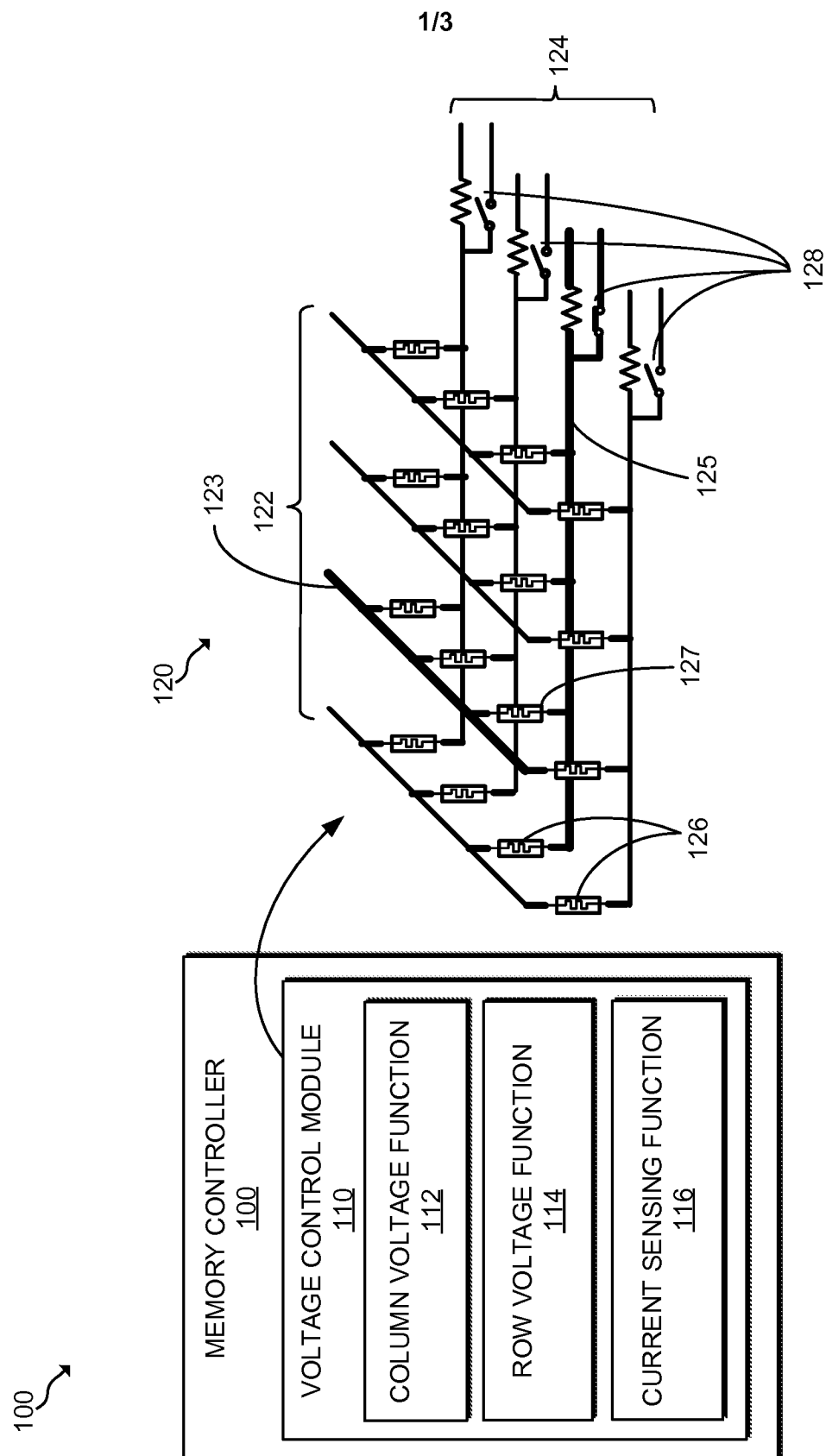


FIG. 1

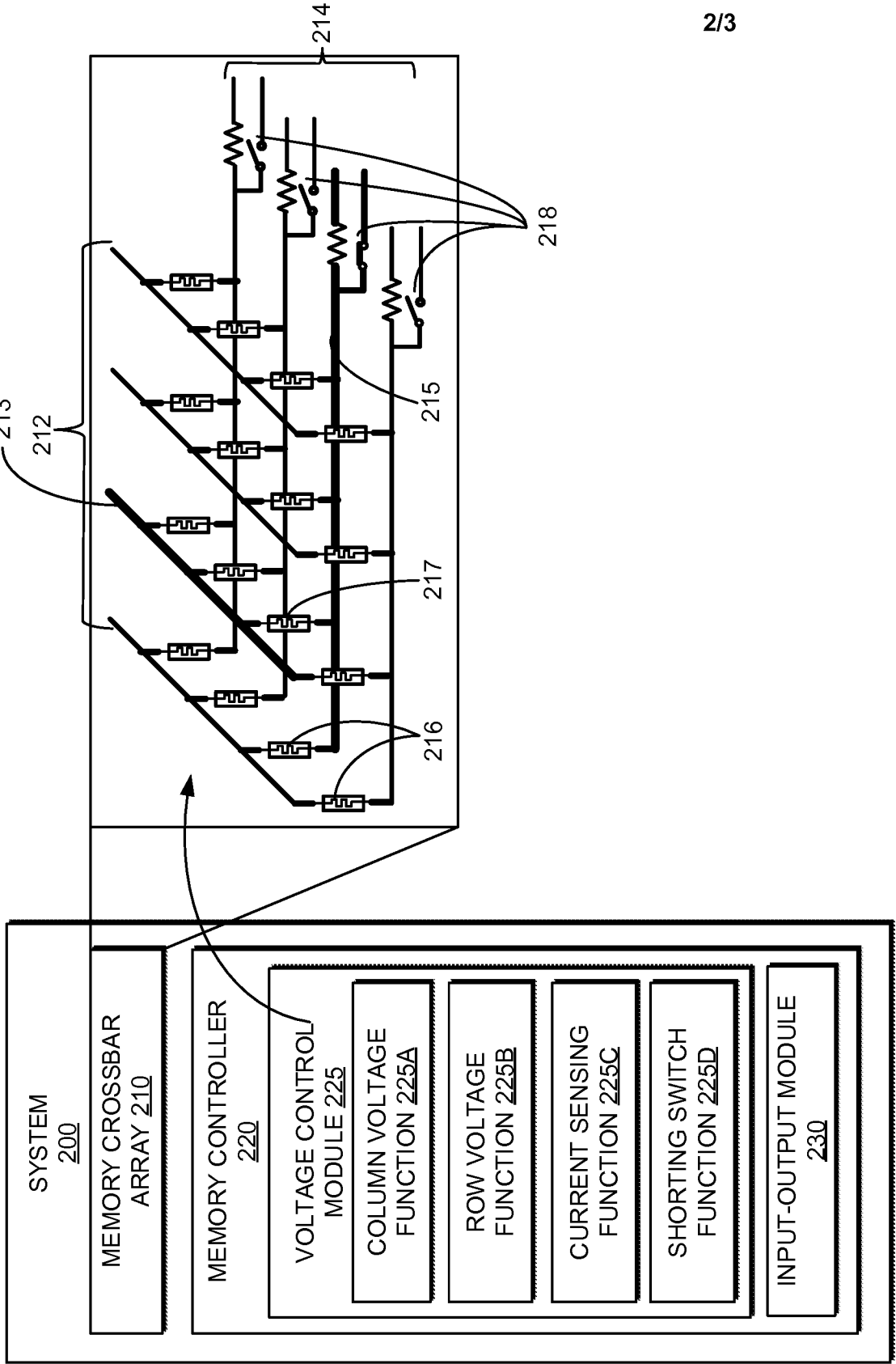


FIG. 2

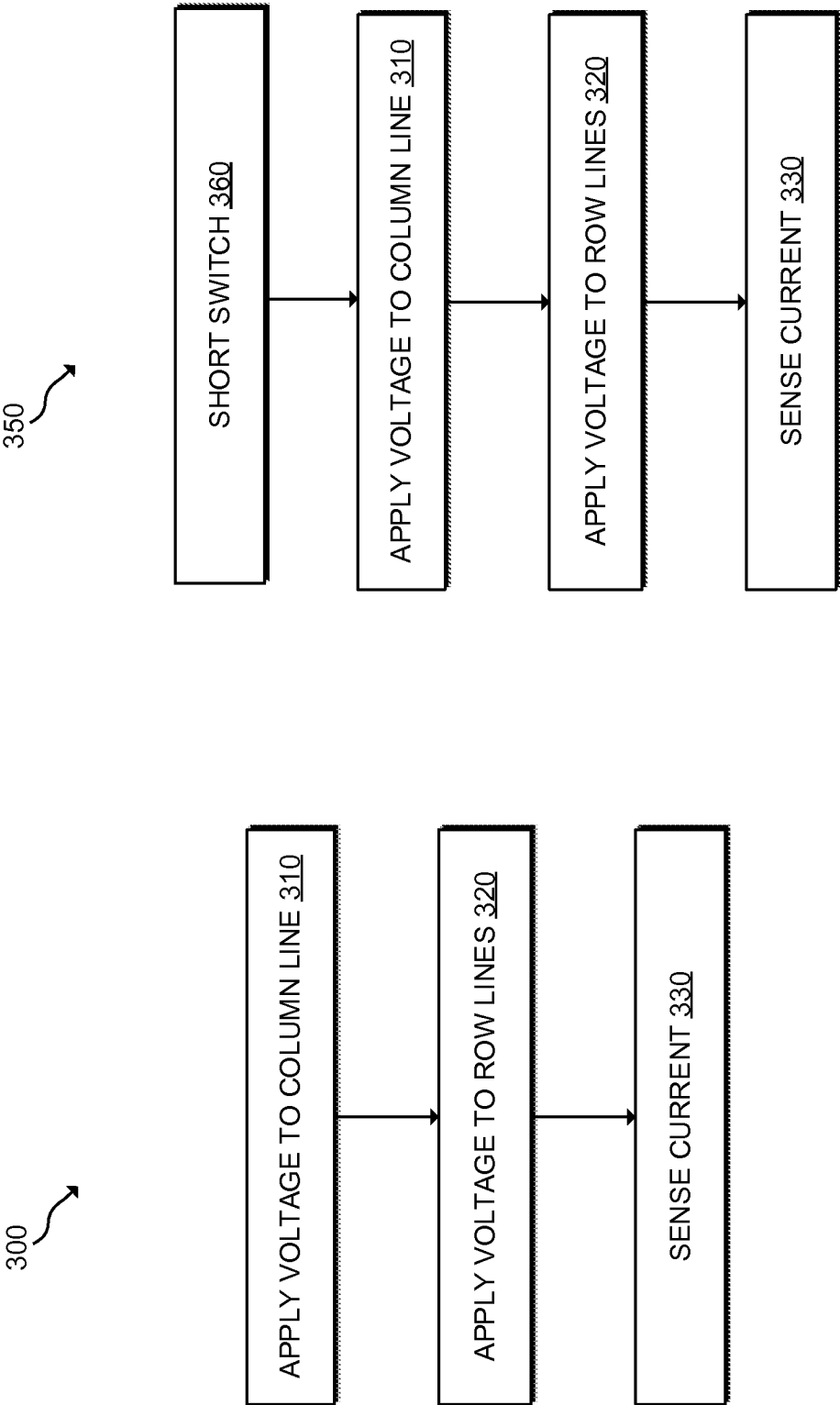


FIG. 3A

FIG. 3B

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2014/040115**A. CLASSIFICATION OF SUBJECT MATTER****G11C 13/00(2006.01)i, G11C 7/10(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G11C 13/00; G06F 7/10; G11C 11/34; G06F 17/30; G11C 7/06; H01L 45/00; G11C 5/02; G11C 11/00; G11C 7/10

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: memristor, memory, crosspoint, crossbar, array, row, column, voltage, sensing, current, switch, resistor, transistor

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2011-0286259 A1 (FREDERICK PERNER) 24 November 2011 See paragraphs [0029], [0031], [0035], [0037], [0042]–[0043], [0053]; claim 1; and figures 2–3.	1–10, 12–15
Y	US 2008-0172385 A1 (BLAISE LAURENT MOUTTET) 17 July 2008 See paragraph [0048]; and figures 1–2.	1–10, 12–15
A	US 2013-0208532 A1 (ROY E MEADE) 15 August 2013 See paragraph [0017]; and figure 1.	1–10, 12–15
A	US 2011-0310656 A1 (FRANZ KREUPL et al.) 22 December 2011 See paragraph [0081]; and figure 3.	1–10, 12–15
A	US 2012-0307542 A1 (CHANG HUA SIAU et al.) 06 December 2012 See paragraph [0023]; and figure 1.	1–10, 12–15



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

27 January 2015 (27.01.2015)

Date of mailing of the international search report

28 January 2015 (28.01.2015)

Name and mailing address of the ISA/KR

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INTERNATIONAL SEARCH REPORT

International application No.

PCT/US2014/040115**Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)**

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:
2. ☒ Claims Nos.: 11
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:
Claim 11 does not comply with PCT Rule 6.1(b), because claim 11 is missing in this application.
3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of any additional fees.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:
4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

- ☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
- ☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
- ☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2014/040115

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