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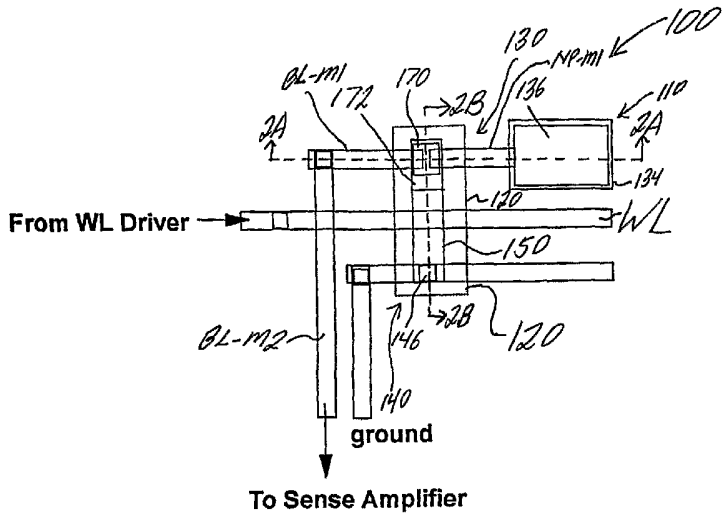
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(54) Title: MICROMACHINED ELECTROCHEMICAL (MEM) RANDOM ACCESS MEMORY ARRAY AND METHOD OF MAKING SAME




(57) Abstract: A micromachined electromechanical random access memory (MEMRAM) array is disclosed which includes a plurality of MEM memory cells, where each MEM memory cell has an MEM switch and a capacitor. The MEM switch includes a contact portion configured for moving from a first position to a second position for reading out a charge stored within the capacitor or for writing the charge to the capacitor. A method is also disclosed for fabricating each MEM memory cell of the MEMRAM array.

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**Declaration under Rule 4.17:**

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# MICROMACHINED ELECTROMECHANICAL (MEM) RANDOM ACCESS MEMORY ARRAY AND METHOD OF MAKING SAME

## Field of the Invention

This invention relates to the field of integrated circuit (IC) design. Specifically, it relates to a random access memory array having a plurality of micromachined electromechanical (MEM) memory cells, where each MEM memory cell includes an MEM switch and a capacitor. This invention also relates to a method of making the MEM random access memory (MEMRAM) array.

## BACKGROUND OF THE INVENTION

Micromachined electromechanical (MEM) switches have been developed for light-emitting display applications. U.S. Patent No. 6,037,719 issued on March 14, 2000 to Yap et al. describes such MEM switches for controlling a plurality of light-emitting devices. Each MEM switch includes a cantilever beam and a control electrode spaced therefrom to deflect the cantilever beam electrostatically in order to close or open the switch.

FIG. 2 of U.S. Patent No. 6,037,719 illustrates a matrix circuit element of a matrix-addressed display. For each light-emitting device, two switches 22, 24 and one storage capacitor 38 are required. The two switches 22, 24 comprise the MEM switch. The first switch 22, called the driving switch, is used to control the current to drive the light-emitting device. Therefore, it determines the light emission intensity of the pixel.

The second switch 24, called the gating switch, is used to control the on/off timing of the pixel. The state of the driving switch 22 is maintained by the storage capacitor 38 coupled to the gate of the driving switch 22.

Since each matrix circuit element includes two switches, i.e., the MEM switch, and one storage capacitor, it is provided that a MEM random access memory (MEMRAM) array can be designed having a plurality of MEM memory cells, where each MEM memory cell has an MEM switch and a capacitor.

It is also provided that a method can be implemented for fabricating each MEM memory cell of the MEMRAM array.

## SUMMARY

An aspect of the present invention is to provide a random access memory array having a plurality of micromachined electromechanical (MEM) memory cells, where each MEM memory cell has an MEM switch and a capacitor.

Another aspect of the present invention is to provide a method for fabricating the MEM random access memory (MEMRAM) array.

Accordingly, a MEMRAM array is disclosed which includes a plurality of MEM memory cells, where each MEM memory cell has an MEM switch and a capacitor. The MEM switch includes a contact portion configured for moving from a first position to a second position for reading out a charge stored within the capacitor or for writing the charge to the capacitor. A preferred method is also disclosed for fabricating each MEM memory cell of the MEMRAM array.

## BRIEF DESCRIPTION OF THE FIGURES

FIG. 1 is a schematic diagram of a micromachined electromechanical (MEM) memory cell according to the present invention;

FIG. 2A is a horizontal cross-sectional view taken along line 2A-2A in FIG. 1;

FIG. 2B is a vertical cross-sectional view taken along line 2B-2B in FIG. 1;

FIG. 3 is a schematic diagram of a 4x4 MEM random access memory (MEMRAM) array according to the present invention; and

FIGS. 4A-4N are cross-sectional views illustrating a preferred process for fabricating an MEM cell according to the present invention.

## DETAILED DESCRIPTION OF THE INVENTION

The present invention provides a random access memory array having a plurality of micromachined electromechanical (MEM) cells, where each MEM memory cell has an MEM switch and a capacitor. The present invention also provides a method for fabricating each MEM memory cell of the MEM random access memory (MEMRAM) array.

The MEMRAM array is possible using MEM switches because compared to the

conventional MOS transistor or switch, the capacitor size of the MEM cell can be significantly reduced. The capacitor size of the MEM cell can be reduced because the leakage rate of the storage charge of the MEM switch is much less than the leakage rate of the storage charge through the junction of the conventional MOS switch or transistor. In fact, the charge leakage path from the MEM capacitor through an off-state MEM switch simply does not exist. Further, the parasitic capacitance of the MEM switch can be used to maintain the charges. Accordingly, one can minimize the leakage rate and reduce the size of a memory cell by using the MEM switch.

**I. Description of the MEM cell**

With reference to FIG. 1, there is shown a schematic diagram of an MEM cell according to the present invention. The MEM cell is designated generally by reference numeral 100 and it includes a capacitor 110 and an MEM switch 120 having a switching element 130 and a fixed end 140 supporting the switching element 130. The MEM switch 120 is tied to ground. The switching element 130 is isolated from the fixed end 140 by an insulating material 150, e.g., a non-conductive beam support.

A wordline WL and a bitline BL traverse the MEM cell 100. The wordline WL is connected to a wordline driver (not shown) and the bitline BL is connected to a sense amplifier (not shown).

The capacitor 110 can be any kind of semiconductor capacitor type, such as planar, trench or stack capacitor. As noted above, the size of the capacitor 110 in an MEM cell can be significantly smaller than that of a capacitor utilized in a conventional DRAM cell. Additionally, if the MEMRAM is built on an SOI substrate, the retention time of each MEMRAM memory cell can be significantly improved.

With continued reference to FIG. 1, during a read operation, when the wordline WL is activated, the corresponding bitline is short to the capacitor 110 and an electrical potential is built up between the wordline WL and the MEM switch 120. When the electrical potential reaches a threshold level, the switching element 130 of the MEM switch 120 is caused to contact a bitline portion BL-M1 due to an electrostatic force. When the switching element 130 is caused to contact the bitline portion BL-M1, the bitline portion BL-M1 is bridged to the capacitor 110 through the MEM switch 120.

When the switching element 130 or cantilever beam of the MEM switch 120 is pulled down, the MEM switch 120 itself does not physically touch the wordline WL or bitline BL. At this time, the charge stored in the capacitor 110 can be read and amplified by a sensing element as known in the art. For example, the sensing element can be any of the conventional single-ended current sensing or direct sensing devices. It can also be a cross- couple differential sense amplifier, etc. It is noted that if a differential sense amplifier is used as the sensing element, a pair of bitlines, one true and one complimentary, are required. After the storage charge is read and sent to a corresponding dataline, a write-back operation is performed to restore the charge in the capacitor 110, as is done for a conventional DRAM memory cell.

A write operation can be performed similarly to the read operation described above. The difference is that the charge now comes from an outside source, for example, from an I/O pad to a dataline passing through a secondary sense amplifier and finally to the capacitor 110 which is addressed by the active wordline WL.

Horizontal and vertical cross-sectional views of the MEMRAM memory cell of FIG. 1 are illustrated by FIGS. 2A and 2B, respectively. The horizontal cross-sectional view illustrates a first portion of bitline BL-M2 formed in M2 (second metal level) traversing in the vertical direction. This first portion of bitline joins via a metal stud 132 the second portion of bitline BL-M1 formed in M1 (first metal level) traversing in the horizontal direction. FIG. 2A also shows a node plate 112 (or bottom electrode) of the capacitor 110 also formed in M1. An insulating (e.g., dielectric) material 134 separates the node plate 112 from a ground plate 136 of the capacitor 110. A gap 160 is presented in between the second portion of bitline BL-M1 and the node plate 112.

The switching element 130 is suspended in the air above the gap 160 between the second portion of bitline BL-M1 and node plate 112. A metallic contact portion 170 of the switching element 130 is formed by a conductive plate (located at the bottom) glued to a non-conductive portion 172 (located at the top).

With reference to FIG. 2B, a cavity area 180 is shown between the switching element

130 and the fixed end 140 of the MEM switch 120. The fixed end 140 has a first fixed end support 142 formed by a first metal, a contact stud 144, and a second fixed end support 146 formed by a second metal. On top of the second fixed end support 146, the non-conductive beam support 150 is provided to hold the two conductive portions 142, 146 of the fixed end 140.

The electrostatic force in the MEM switch 120 is developed due to the potential difference between the second fixed end support 146 of the fixed end 140 and the control electrode (or wordline WL located in the middle). Once the potential reaches the threshold voltage, the contact portion 170 of the switching element 130 is pulled down (as shown by the arc identified by the letter "A" in FIG. 2B) to form a bridge to short the second portion of bitline BL-M1 to the node plate 112 of the capacitor 110.

With reference to FIG. 3, there is shown a schematic diagram of a 4x4 MEMRAM array designated generally by reference numeral 300. Compared to the conventional DRAM array, the MEMRAM array design is much simpler, since there is no need for body bias, and thus associated circuits, such as Vbb charge pumps, etc. are not needed. Also, no triple well is necessary which means lower processing cost. In order to avoid dielectric breakdown, the ground node of the capacitors can all be tied to a ½ Vdd level (not shown).

In the arrangement shown by FIG. 3, capacitors C00 and C01 of MEM cells 302 and 304, respectively, can be accessed by wordline WL0, while capacitors C10 and C11 of MEM cells 306 and 308, respectively, can be accessed by wordline WL1. When a wordline is selected and activated by the decoder and driver circuits, the MEM cells of that row will all be read out simultaneously.

**II. Methodology for fabricating an MEM cell**

A description of a preferred method for fabricating an MEM cell of an MEMRAM array having planar capacitor cells and formed on an SOI substrate will now be provided. The same fabrication method is used for simultaneously fabricating all of the MEM cells of the MEMRAM array. With reference to FIGS. 4A-4N there are shown cross-sectional views for fabricating the MEM cell according to the present invention.

With reference to FIG. 4A, an SOI substrate 400 is used having a buried oxide layer

402 (about 300 nm) and a silicon layer 404 (about 250 nm) for fabricating the MEM cell. It is contemplated that other types of substrates besides semiconductor SOI substrates, such as semiconductor bulk substrates, can be used for fabricating the MEM cell.

With continued reference to FIG. 4A, the MEMRAM array is formed in an area where the silicon layer 404 is etched away. The etched surface is covered by a dielectric material 406, e.g., 20 nm of CVD nitride. A conductive material, such as doped polysilicon, tungsten, gold, platinum, nickel, and palladium, with a thickness of 50 to 100 nm is then deposited and patterned to form the second portion of bitline BL-M1 and the node plate 112 or bottom plate of the capacitor 110.

With reference to FIG. 4B, the dielectric material 134 is deposited and patterned. The MEM cell size can be further reduced if a high-dielectric constant material is used. This dielectric material can be $TiO_2$, $Ta_2O_5$, $Al_2O_3$, or even ferroelectric materials, such as PZT (lead zirconate titanate) having a dielectric constant in the range of 7 to 100.

If the ferroelectric material is used, it is preferable that noble metals, such as platinum or palladium, be used to form the electrode plates. Other ferroelectric materials, such as phase III potassium nitride, and bismuth layered compounds, can all be candidates. One major advantage of using MEM switches is that they are compatible with any high-k material during deposition and annealing. This annealing is typically, however, very detrimental to the conventional MOS transistor devices.

With reference to FIG. 4C, an insulating material 410, e.g., 100 nm CVD oxide, doped glass, etc., is deposited, and the first metal level stud 132 is formed for interconnect. The material for the stud 132 can be tungsten, $TiSi_2$, WSi, TiN, Ti, doped polysilicon, and other suitable materials. A stud similar to stud 132 is also used to form the fixed end 140. The stud 132 must be bound strongly to the first and second metal levels.

With reference to FIG. 4D, the insulating material 410 is patterned and a conductive material is deposited. The conductive material can be doped polysilicon, tungsten, gold, platinum, nickel, palladium, etc. The ground plate 136 of the capacitor 110, the first portion of bitline BL-M2 and the contact portion 170 of the switching element 130 are then formed by RIE (reactive ion etch) patterning.

With reference to FIG. 4E, a thin dielectric material 412 (about 10 to 30 nm), such as CVD nitride and aluminum oxide, is then deposited. Another etch is carried out to define the non-conductive portion 172. The dielectric material used to form the non-conductive portion 172 is not etched in buffered HF, and should be flexible and bound well to the metallic contact portion 170. The dielectric material can also be allowed to cover the ground plate 136 of the capacitor 110, in order for the ground plate 136 not to be "attacked" during a later BHF etching.

A sacrificial oxide layer 414 about 100 nm is then deposited and planarized as shown in FIG. 4G. The planarization can be carried out by a chem-mech polish step.

With reference to FIG. 4H, the oxide coating outside the fabrication region is stripped. A nitride layer 416 is deposited to cover the surface of the MEM cell. Small nitride holes are patterned in the nitride layer 416 which covers an MEM switch region 418, so that later a wet etch can be used to remove the underlying sacrificial oxide layer 414 to release the switching element 130 as described below.

MOS devices, such as nMOS and pMOS, are then formed in the support areas, i.e., the areas where the silicon layer 404 is not etched away, using conventional fabrication methods, including field oxidation, gate formation, source/drain diffusion and silicidation, etc.

With reference to FIG. 4I, an isolation region 420, a junction region 422 and the gate 424 of a typical MOS device are shown. The silicide and the ferroelectric materials can then be annealed at the same time in an oxygen ambient at a temperature range from 450 to 700 degrees Celsius for 30 to 90 minutes. The annealing not only enhances the silicide formation in the MOS device junctions 420, 422, but also recovers the damage of the ferroelectric material.

With reference to FIG. 4J, metallic contact studs 426 are connected to the MOS devices and the MEM cell. An insulating material 427 is then deposited to cover the structure. The metallic contact studs 426 are interconnected by metallic stud 428. The metallic contact studs 426, 428 are preferably formed by either aluminum or copper. A final insulating material 430 is then deposited as shown by FIG. 4K to cover the entire structure, including the metallic

stud 428, in order to make the MEM memory cell structure planar.

With reference to FIGS. 4L-4N, the process of releasing the switching element 130 of the MEM switch 120 is illustrated. First, a resist layer 450 is deposited and patterned as shown in FIG. 4L. The top two insulating material layers 430, 427 are then removed via a directional RIE process as shown by FIG. 4M. The etching process preferably stops at the nitride layer 416.

A BHF wet etch or down stream isotropic etch is then performed to selectively remove the underlying sacrificial oxide layer 414 oxide layer through the patterned nitride holes in order to release the switching element 130 of the MEM switch 120. The non- conductive glue layer 172 of the switching element 130 is not attacked during the etching process, since it is formed by nitride. FIG. 4N illustrates the option of completely removing the nitride layer 416 and the oxide layer 414.

What has been described herein is merely illustrative of the application of the principles of the present invention. For example, the systems described above and implemented as the best mode for operating the present invention are for illustration purposes only. In other words, other arrangements and methods may be implemented by those skilled in the art without departing from the scope and spirit of this invention.

**IN THE CLAIMS:**

We claim:

1. A memory system comprising a plurality of MEM memory cells arranged in an array, wherein each of the plurality of MEM memory cells is configured for storing a charge therein.

2. The memory system according to Claim 1, wherein each MEM memory cell has a switch and a capacitor.

3. The memory system according to Claim 2, wherein the switch includes a contact portion configured for moving from a first position to a second position for reading out the charge stored within the capacitor or for writing the charge to the capacitor.

4. The memory system according to Claim 3, wherein the contact portion shorts a bitline to a plate of the capacitor when said contact portion is in the second position

5. The memory system according to Claim 3, wherein the switch includes a fixed end opposite the contact portion.

6. The memory system according to Claim 1, wherein a plurality of datalines traverse the array.

7. The memory system according to Claim 6, wherein the plurality of datalines include bitlines and wordlines.

8. The memory system according to Claim 7, wherein the bitlines and wordlines are embedded within the plurality of MEM memory cells.

9. The memory system according to Claim 1, wherein each of the plurality of MEM memory cells is connected to at least one respective MOS device.

10. The memory system according to Claim 1, wherein the plurality of MEM memory cells are fabricated on a semiconductor SOI or bulk substrate.

11. The memory system according to Claim 1, wherein each of the plurality of MEM memory cells has a planar cell structure.

12. A micromachined electromechanical random access memory (MEMRAM) array comprising:

a plurality of MEM memory cells, wherein each of the plurality of MEM memory cells is configured for storing a charge therein.

13. The array according to Claim 12, wherein each MEM memory cell has a switch and a capacitor.

14. The array according to Claim 13, wherein the switch includes a contact portion configured for moving from a first position to a second position for reading out the charge stored within the capacitor or for writing the charge to the capacitor.

15. The array according to Claim 14, wherein the contact portion shorts a bitline to a plate of the capacitor when said contact portion is in the second position

16. The array according to Claim 13, wherein the switch includes a fixed end opposite the contact portion.

17. The array according to Claim 12, wherein a plurality of datalines traverse the array.

18. The array according to Claim 17, wherein the plurality of datalines include bitlines and wordlines.

19. The array according to Claim 18, wherein the bitlines and wordlines are embedded within the plurality of MEM memory cells.

20. The array according to Claim 12, wherein each of the plurality of MEM memory cells is connected to at least one respective MOS device.

21. The array according to Claim 12, wherein the plurality of MEM memory cells are fabricated on a semiconductor SOI or bulk substrate.

22. The array according to Claim 12, wherein each of the plurality of MEM memory cells has a planar cell structure.

23. A method for fabricating a micromachined electromechanical random access memory (MEMRAM) array having a plurality of MEM memory cells, the method comprising the steps of:

providing a semiconductor wafer;

fabricating a plurality of datalines on the semiconductor wafer; and

fabricating each of the plurality of MEM memory cells on the semiconductor wafer, wherein at least one dataline traverses each of the plurality of MEM memory cells.

24. The method according to Claim 23, wherein the semiconductor wafer is a semiconductor SOI or bulk wafer.

25. The method according to Claim 22, wherein the step of fabricating each of the plurality of MEM memory cells comprises the steps of:

etching portions of the semiconductor wafer to form a plurality of substrate cavities; and

fabricating each of the plurality of MEM memory cells within a respective substrate cavity.

26. The method according to Claim 22, further comprising the step of encapsulating each of the plurality of MEM memory cells with an insulating material.

27. The method according to Claim 22, further comprising the step of fabricating each of the plurality of MEM memory cells with a planar cell structure.

28. The method according to Claim 26, wherein the step of fabricating each of the plurality of MEM memory cells comprises the step of removing sections of the insulating material and at least one layer below the insulating material to release an MEM switch for each of the plurality of MEM memory cells.

29. The method according to Claim 22, further comprising the step of connecting each of the plurality of MEM memory cells with at least one respective MOS device.

30. The method according to Claim 22, wherein the plurality of datalines include bitlines and wordlines.

31. The method according to Claim 30, wherein the bitlines and wordlines are embedded within the plurality of MEM memory cells.

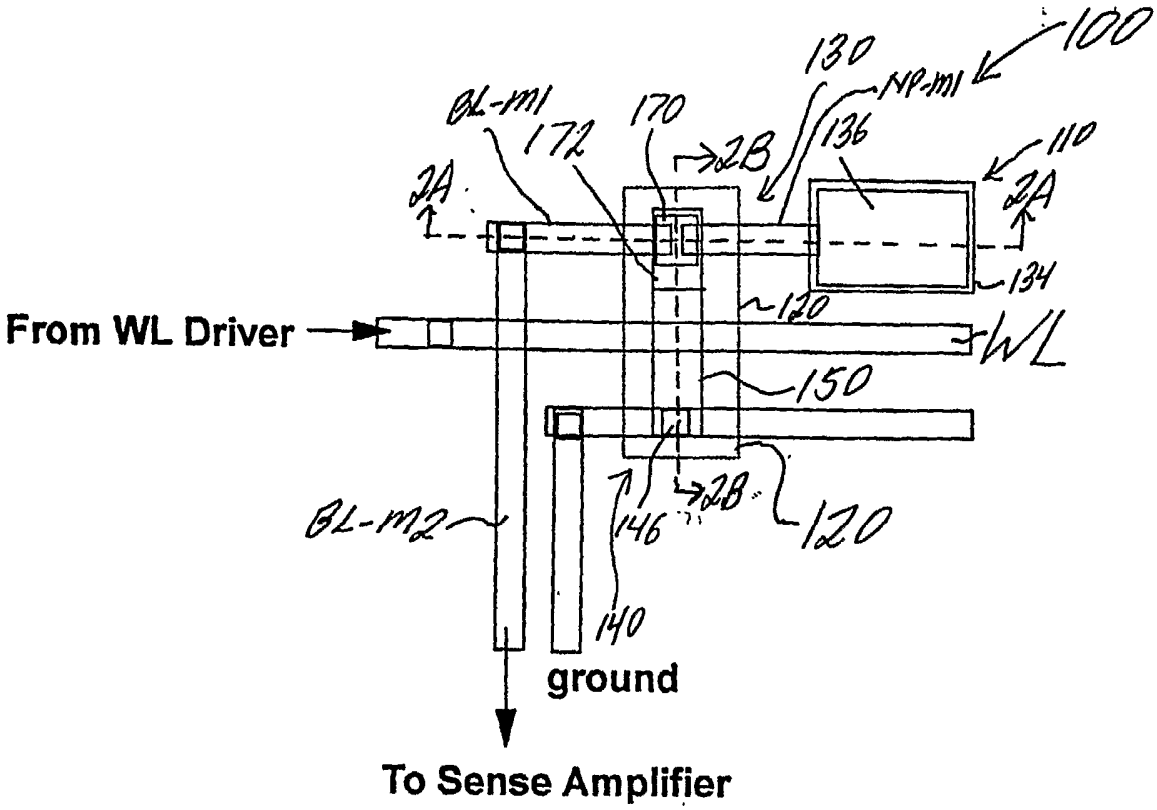



Fig. 1

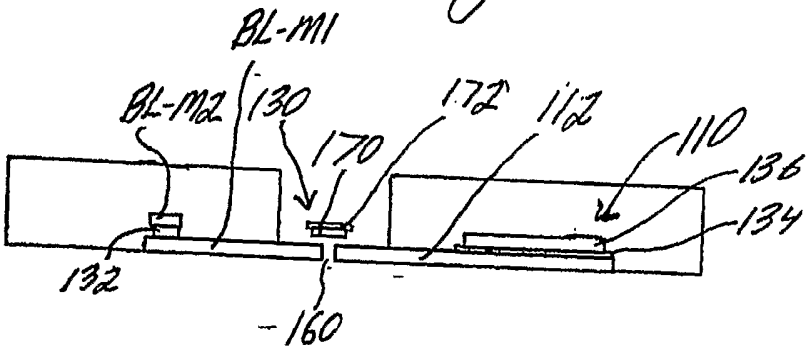



Fig. 2A

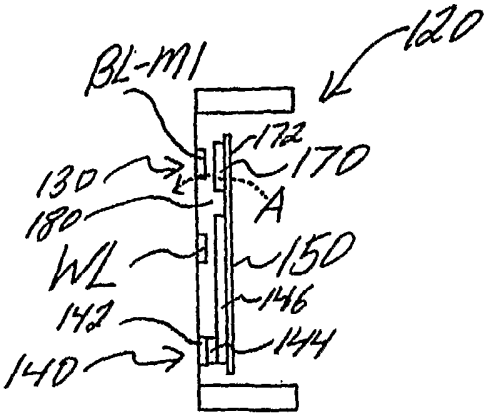



Fig. 2B

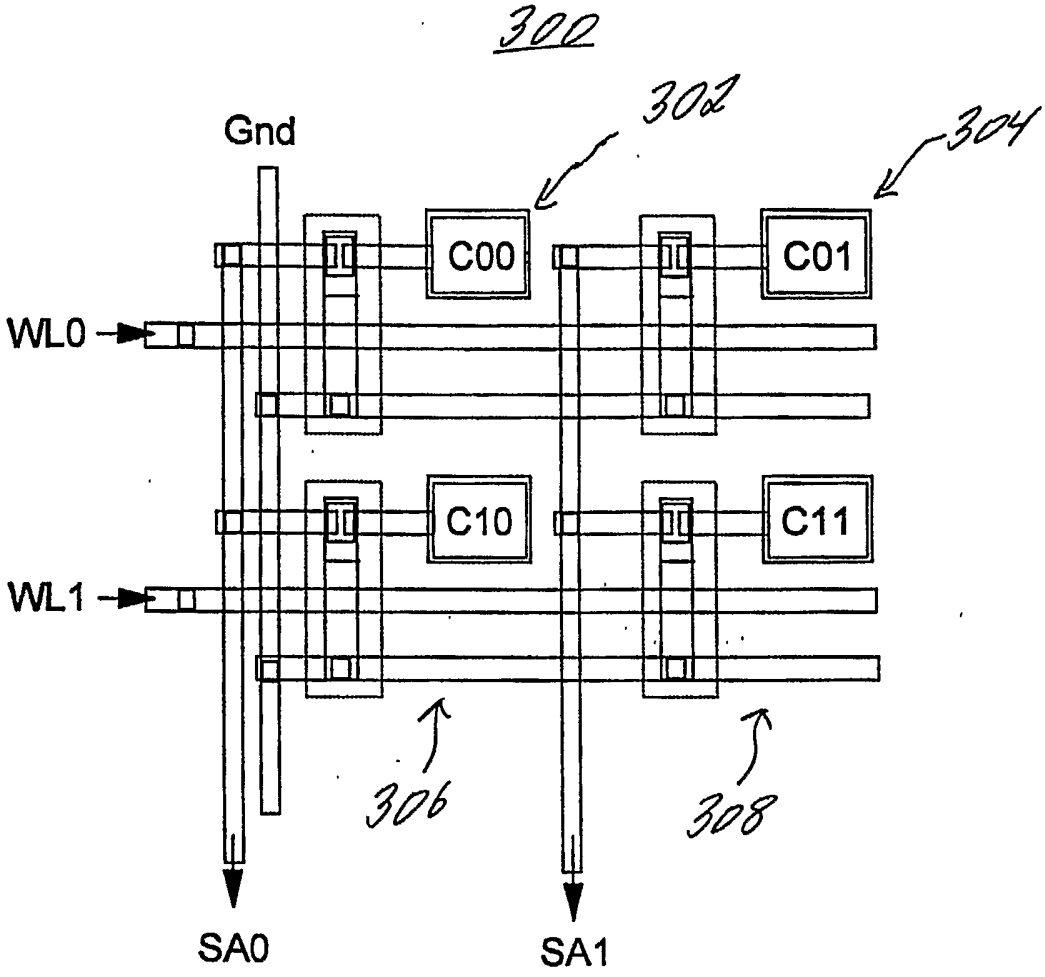



Fig. 3

FIG-4A

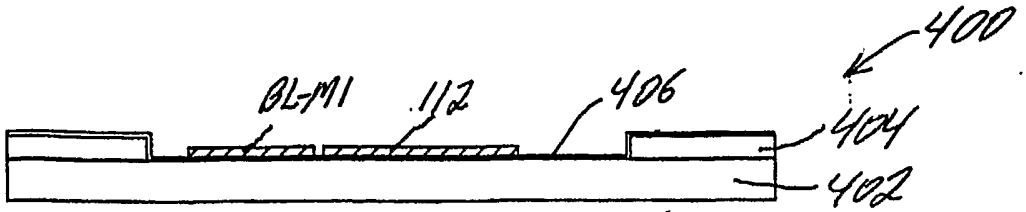



FIG-4B

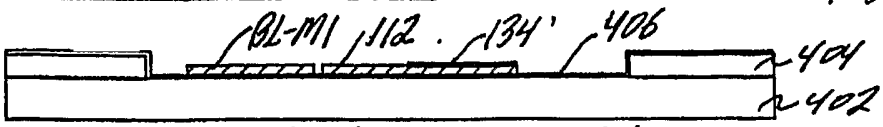



FIG-4C

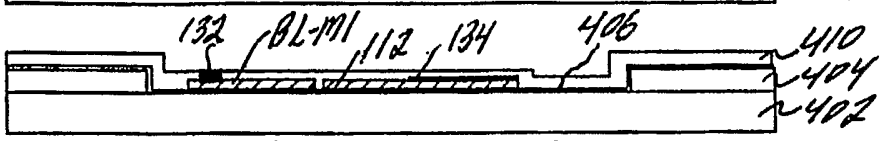



FIG-4D

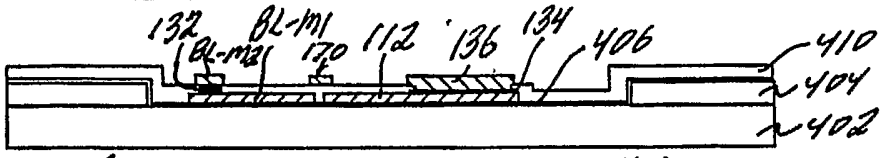



FIG-4E

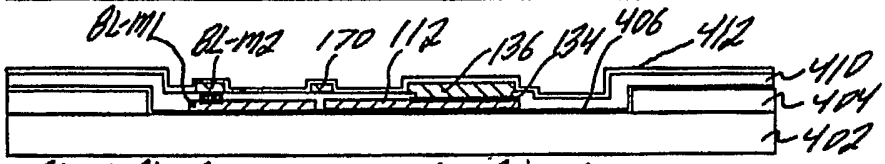



FIG-4F

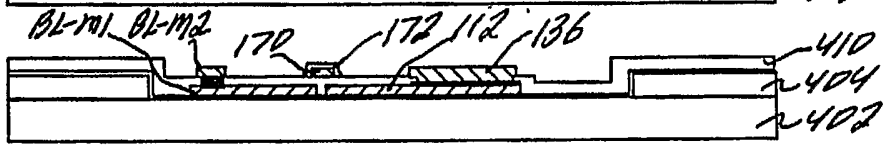



FIG-4G

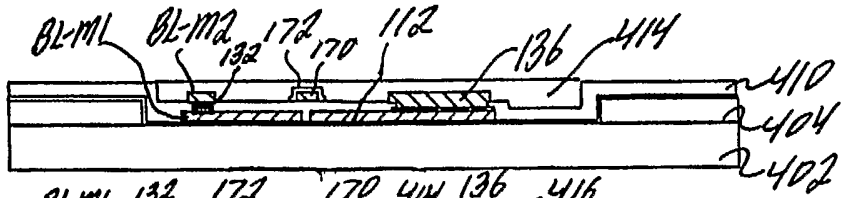



FIG-4H

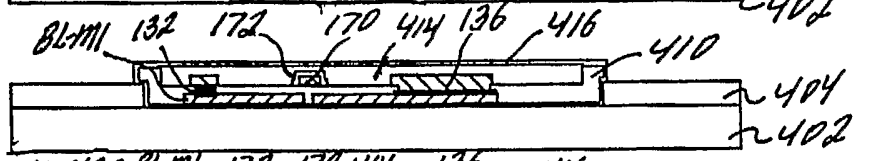



FIG-4I

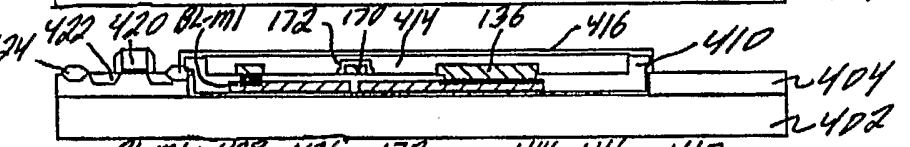



FIG-4J

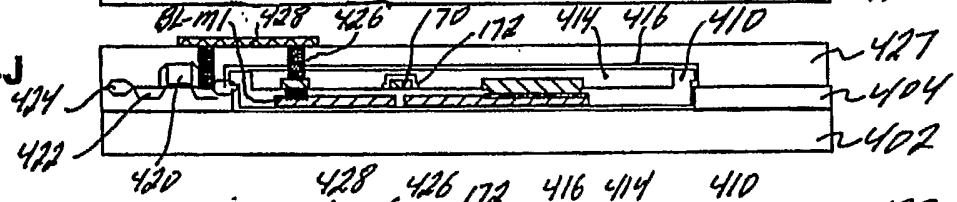



FIG-4K

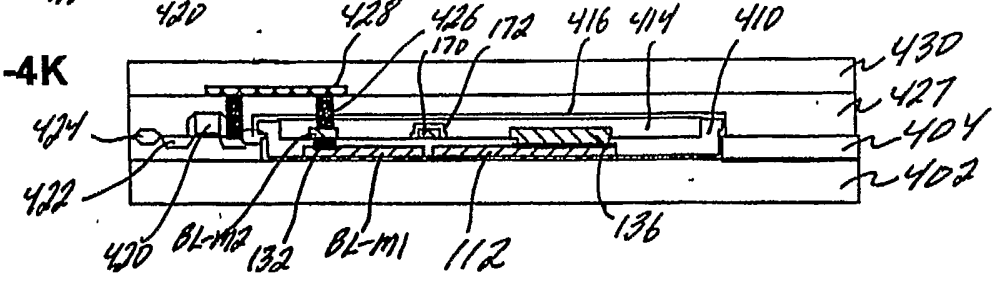


FIG-4L

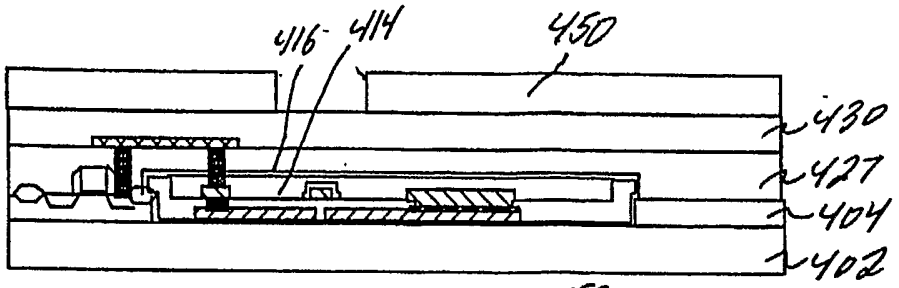



FIG-4M

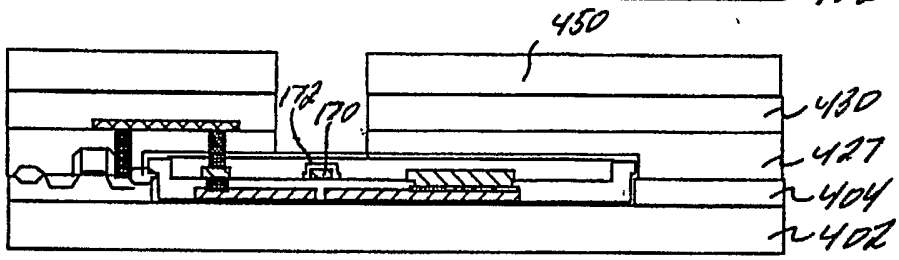
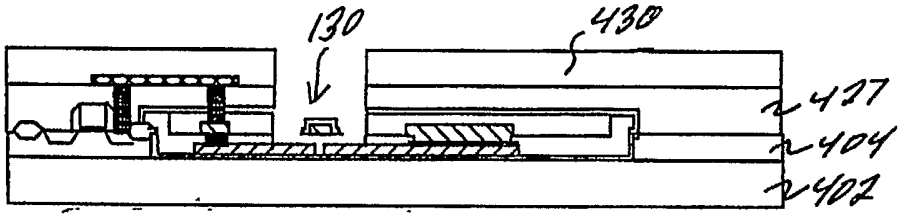



FIG-4N



# INTERNATIONAL SEARCH REPORT

In al Application No
PCT/US 02/40836

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G11C27/00 B81B7/04 B81C1/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G11C B81C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

| Category ° | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| X | US 2002/151132 A1 (HSU LOUIS L ET AL)<br>17 October 2002 (2002-10-17)<br>the whole document | 1-31 |

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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| European Patent Office, P.B. 5818 Patentlaan 2<br>NL - 2280 HV Rijswijk<br>Tel. (+31-70) 340-2040, Tx. 31 651 epo nl,<br>Fax: (+31-70) 340-3016 | Wanzeele, R |

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Inte nal Application No
PCT/US 02/40836

| Patent document cited in search report | Publication date | Patent family member(s) | Publication date |
|---|---|---|---|
| US 2002151132 A1 | 17-10-2002 | NONE | |