(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
18 November 2004 (18.11.2004)

PCT

(10) International Publication Number
WO 2004/100373 A1

(51) International Patent Classification[7]: H03K 7/04

(21) International Application Number:
PCT/US2004/011415

(22) International Filing Date: 14 April 2004 (14.04.2004)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
10/426,263 30 April 2003 (30.04.2003) US

(71) Applicant *(for all designated States except US)*: **EASTMAN KODAK COMPANY** [US/US]; 343 State Street, Rochester, NY 14650-2201 (US).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **LAWLER, Edward, Paul** [US/US]; 61 Heatherwood Road, Fairport, NW 14450 (US). **CHARNESKI, David, Michael** [US/US]; 12 Marjorie Lane, Hilton, NY 14468 (US).

(74) Common Representative: **EASTMAN KODAK COMPANY**; 343 State Street, Rochester, NY 14650-2201 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

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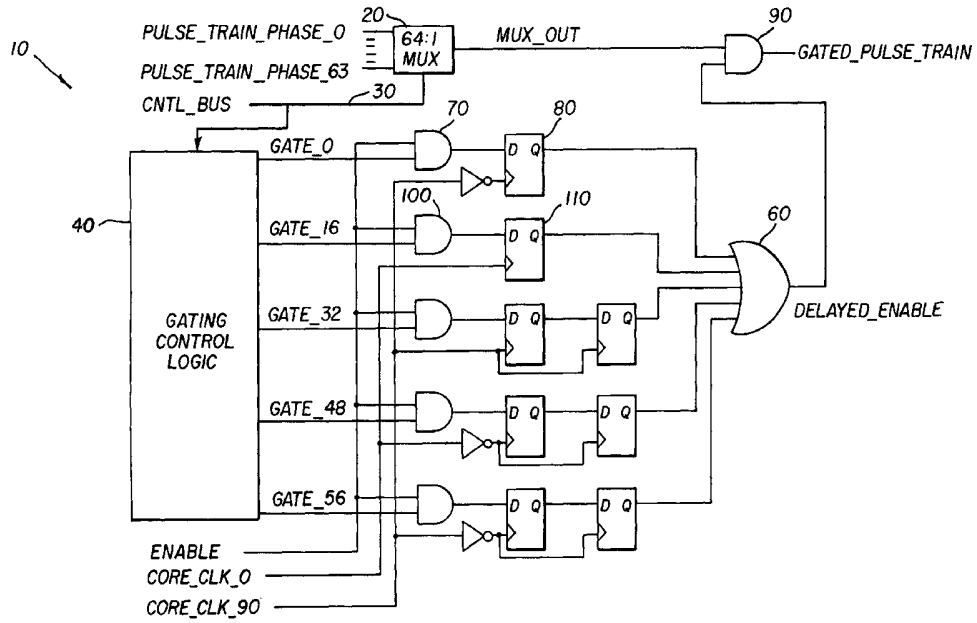
[Continued on next page]

(54) Title: ENABLING METHOD TO PREVENT GLITCHES IN WAVEFORM



(57) Abstract: The present invention includes a system that has been developed to vary the starting and stopping of a pulse train of arbitrary phase without glitches, spurious pulses, or spurious change in duty cycle. This is accomplished by a system for generating a gated periodic waveform, the system includes a generator for generating a periodic waveform of adjustable phase; a device for providing a delayed enable signal based on the phase of the periodic waveform so that the gated periodic waveform can be started and stopped without creating undesirable changes in the gated periodic waveform; and a logic element for generating a gated periodic waveform based on the delayed enable signal and the periodic waveform of adjustable phase.

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EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VC, VN, YU, ZA, ZM, ZW, ARIPO patent (BW, GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG)

— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii)) for all designations*

Published:

— *with international search report*

— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

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ENABLING METHOD TO PREVENT GLITCHES IN WAVEFORM

FIELD OF THE INVENTION

This invention relates generally to electronic imaging systems and, more particularly, to starting and stopping critical systems clocks without creating glitches or spurious pulses.

BACKGROUND OF THE INVENTION

A series of logic-level pulses can typically be created by performing a logical AND of a continuously running pulse train with a positive logic enable signal. To avoid shortened pulses or glitches at turn-on or turn-off, the enable signal should transition from low to high and high to low when the pulse train is low.

If the phase of the continuously running pulse train is varied, the phase of the enable signal must be varied accordingly. However, the enable signal is typically generated by logic running from a non-adjustable system clock of fixed phase. Consequently, a mechanism is needed for varying the phase of the enable signal so that shortened pulses or glitches are not created.

SUMMARY OF THE INVENTION

The present invention is directed to providing a mechanism for varying the phase of the enable signal. Briefly summarized, according to one aspect of the present invention, the invention includes a system for generating a gated periodic waveform, the system includes (a) a generator for generating a periodic waveform of adjustable phase; (b) a device for providing a delayed enable signal based on the phase of the periodic waveform so that the gated periodic waveform can be started and stopped without creating undesirable changes in the gated periodic waveform; and (c) a logic element for generating a gated periodic waveform based on the delayed enable signal and the periodic waveform of adjustable phase.

These and other aspects, objects, features and advantages of the present invention will be more clearly understood and appreciated from a review of the following detailed description of the preferred embodiments and appended claims, and by reference to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a timing diagram showing the various clocks and phases used in the present invention;

Fig. 2 is a logic diagram showing the logic used to create a gated pulse train of the present invention;

Fig. 3 is an alternative embodiment of Fig. 2; and

Fig. 4 is a timing diagram for Fig. 2.

DETAILED DESCRIPTION OF THE INVENTION

In Fig. 1 are shown four 'core clock' phases each having a 90-degree phase separation. These core clocks are used as inputs to an enable delay logic 10 shown in Fig. 2. Also shown in Fig. 1 are 64 free running clock phases, "PULSE_TRAIN_PHASE_0" through "PULSE_TRAIN_PHASE_63", where "PULSE_TRAIN_PHASE_0" is phase aligned with the "CORE_CLK_0", and each successive phase of "PULSE_TRAIN_PHASE_0" through "PULSE_TRAIN_PHASE_63" is shifted by $1/64^{th}$ of the clock period from the previous phase. These will be used as inputs to a multiplexer 20 shown in Fig. 2.

Fig. 2 shows delay logic 10 for an "ENABLE" signal which is generated externally for producing a "GATED_PULSE_TRAIN" signal. The control bus 30 is used by the multiplexer 20 to select a phase of the pulse train to be passed by the multiplexer 20, and is also used by the gating control logic 40 to enable one of the delay paths (Gate 0, Gate 16, Gate 32, Gate 48 and Gate 56). It is instructive to note that only one of these paths is enabled, and the others are disabled and drive a logic 0 to the OR gate 60. The delay path from signal "GATE_0" uses AND gate 70 to allow the system enable signal to pass to flip-flop 80. The clock for flip-flop 80 is the falling edge of "CORE_CLK_90". This

delays the system enable signal by ¾ of the clock period. The output of flip-flop 80 goes to OR gate 60 and then to AND gate 90 where the enabling and disabling of the selected pulse train phase is accomplished.

The delay path from signal "GATE_16" uses AND gate 100 to allow the system enable to pass to flip-flop 110. The clock for flip-flop 110 is the rising edge of "CORE_CLK_0". This delays the system enable by a full clock period and correspondingly delays the enabling and disabling of the selected pulse train at AND gate 90. By performing similar analysis of the delay paths for "GATE_32", "GATE_48", and "GATE_56" it is observed that the enabling and disabling at AND gate 90 is delayed by 1.25, 1.5 and 1.75 clock periods, respectively. It is noted that the flip-flops associated with these gates function substantially similar to flip-flops 80 and 110 to create the delays and will not be discussed in detail herein. It is noted that two flip-flops are in each path to create additional delay as those skilled in the art will readily recognize.

Fig. 3 shows another delay logic 120 for an "ENABLE" signal which is generated externally for producing a "GATED_PULSE_TRAIN" signal. The logic herein is similar to Fig. 2 with the exception that the delay paths are as follows. The delays for signal paths "Gate_0", "Gate_16", "Gate_32", "Gate_48", and "Gate_56" are 1.25, 1.5, 1.75, 2, and 2.25 clock periods respectively. For clarity, similar components are used for the logic 20, 30, 60 and 90 in both Figs. 2 and 3. For other components, those skilled in the art would readily recognize how the new delays are implemented with the flip-flops shown, and as a result, it will not be discussed in detail herein.

Fig. 4 illustrates the timing for Fig. 2. The "ENABLE" signal is generated externally by clocked logic (not shown) using "CORE_CLK_0". In this example the "CNTL_BUS" value has resulted in the "GATE_0" signal path being selected by "GATING CONTROL LOGIC" 40. This results in creating a "DELAYED_ENABLE" signal which is delayed ¾ths of the clock period from "CORE_CLK_0". This causes transition of "DELAYED_ENABLE" at AND gate 90 to occur while signal "MUX_OUT" is low, thus precluding any shortened pulses or glitches when starting or stopping signal "GATED_PULSE_TRAIN".

The invention has been described in detail with particular reference to certain preferred embodiments thereof, but it will be understood that variations and modifications can be effected within the spirit and scope of the invention.

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PARTS LIST

10	enable delay logic
20	multiplexer
30	control bus
40	gating control logic
60	OR gate
70	AND gate
80	flip-flop
90	AND gate
100	AND gate
110	flip-flop
120	another delay logic

CLAIMS:

1. A system for generating a gated periodic waveform, the system comprising:

(a) a generator for generating a periodic waveform of adjustable phase;

(b) a device for providing a delayed enable signal based on the phase of the periodic waveform so that the gated periodic waveform can be started and stopped without creating undesirable changes in the gated periodic waveform; and

(c) a logic element for generating a gated periodic waveform based on the delayed enable signal and the periodic waveform of adjustable phase.

2. The system as in claim 1, wherein the generator generates a plurality of phases for the periodic waveform, and the device for providing the delayed enable signal receives phase information from the generator and creates the delayed enable signal based on the received phase information.

3. The system as in claim 1 further comprising a selector for selecting a waveform from a plurality of waveforms.

4. The system as in claim 3, wherein the selector is a multiplexer.

5. The system as in claim 1, wherein the device for providing the delayed enable signal includes a plurality of enabling logic elements for enabling a delay path from a plurality of delayed paths.

6. The system as in claim 5, wherein the plurality of delayed paths utilizes a plurality of clocks of predetermined phase with respect to a primary enable signal.

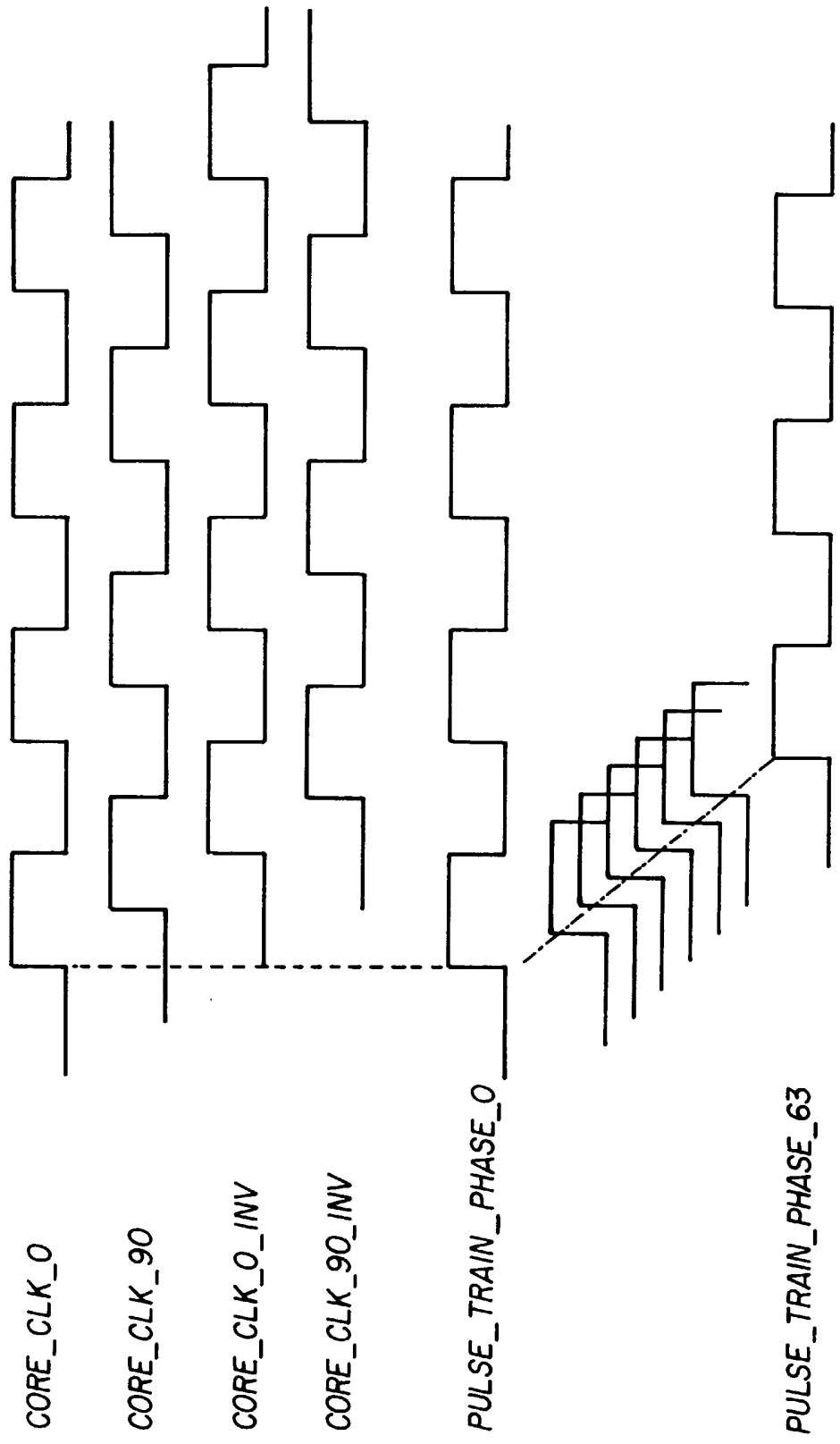
CORE_CLK_0
CORE_CLK_90
CORE_CLK_0_INV
CORE_CLK_90_INV
PULSE_TRAIN_PHASE_0
PULSE_TRAIN_PHASE_63

FIG. 1

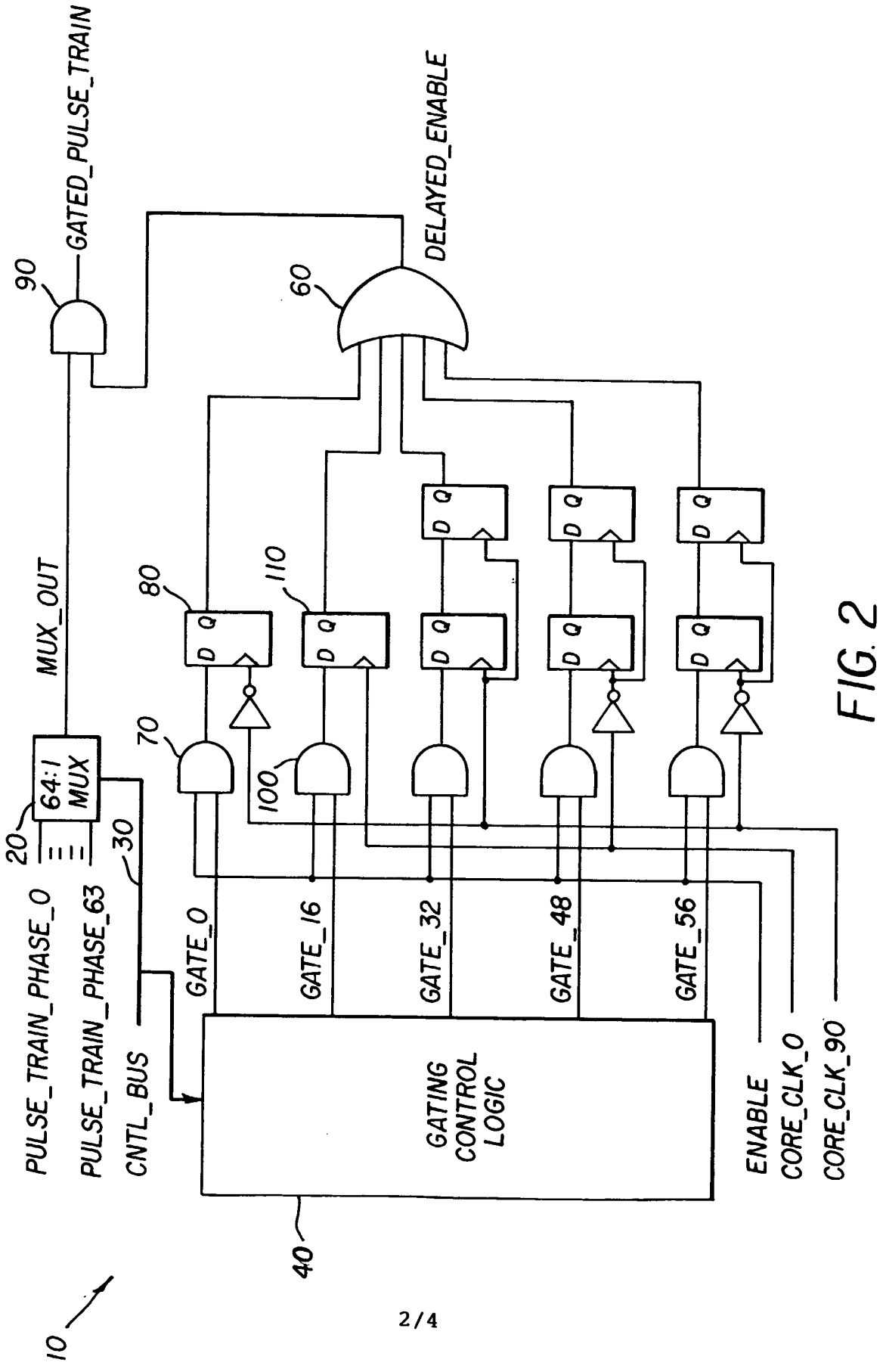
10
20
64:1 MUX
30
40
60
70
80
90
100
110
PULSE_TRAIN_PHASE_0
PULSE_TRAIN_PHASE_63
CNTL_BUS
MUX_OUT
GATED_PULSE_TRAIN
DELAYED_ENABLE
GATE_0
GATE_16
GATE_32
GATE_48
GATE_56
GATING CONTROL LOGIC
ENABLE
CORE_CLK_0
CORE_CLK_90
D Q

FIG. 2

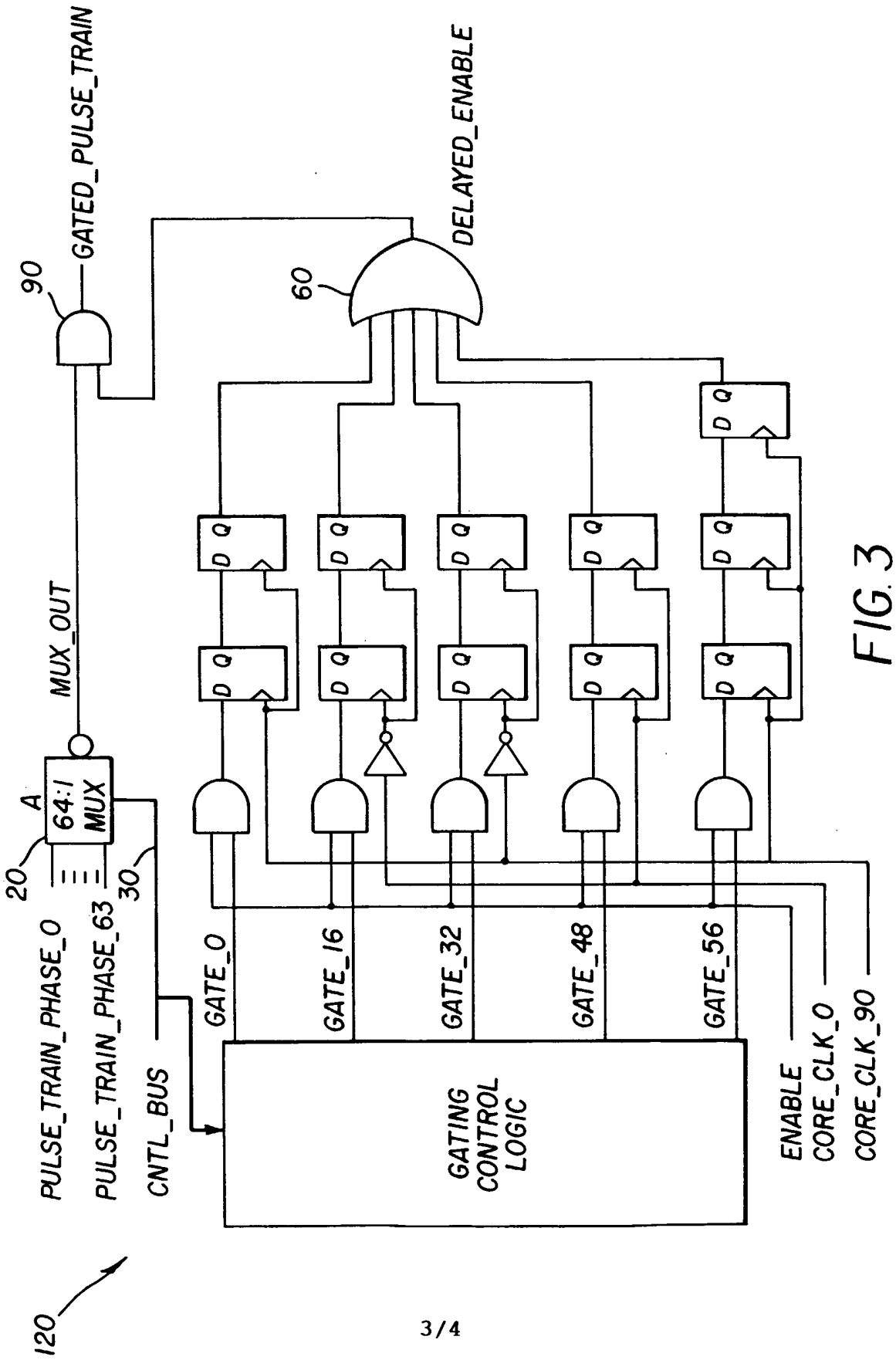
120
PULSE_TRAIN_PHASE_0
PULSE_TRAIN_PHASE_63
CNTL_BUS
20
A
64:1 MUX
30
MUX_OUT
90
GATED_PULSE_TRAIN
60
DELAYED_ENABLE
D Q
GATE_0
GATE_16
GATE_32
GATE_48
GATE_56
GATING CONTROL LOGIC
ENABLE
CORE_CLK_0
CORE_CLK_90

FIG. 3

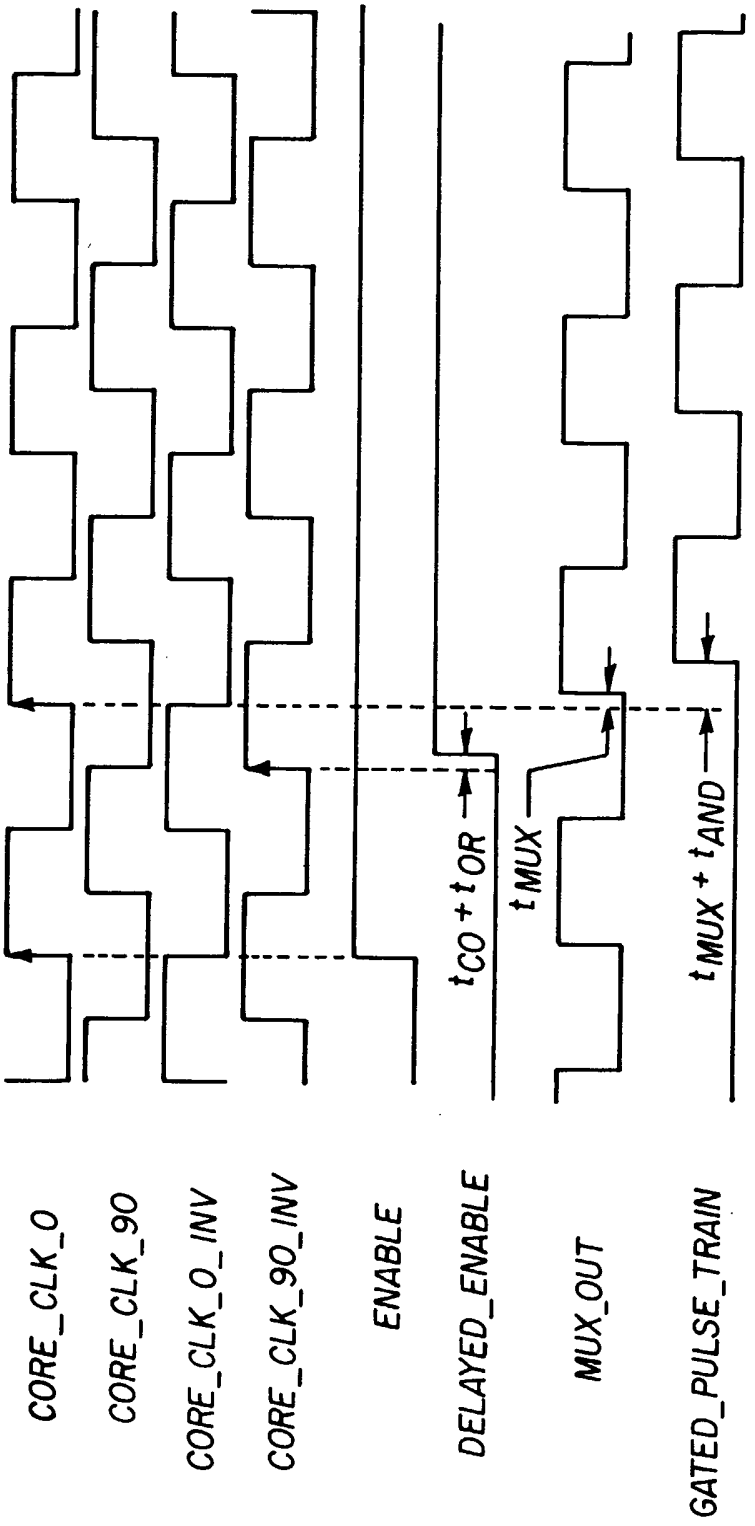
CORE_CLK_0
CORE_CLK_90
CORE_CLK_0_INV
CORE_CLK_90_INV
ENABLE
DELAYED_ENABLE
MUX_OUT
GATED_PULSE_TRAIN
$t_{CO} + t_{OR}$
t_{MUX}
$t_{MUX} + t_{AND}$

FIG 4

INTERNATIONAL SEARCH REPORT

International Application No
[redacted]/US2004/011415

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H03K7/04

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H03K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 1 077 529 A (TEKTRONIX INC) 21 February 2001 (2001-02-21) figures 12,14-16	1-4,6

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
27 September 2004	04/10/2004

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	Brown, J

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/US2004/011415

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		DE 69522779 T2	04-07-2002
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