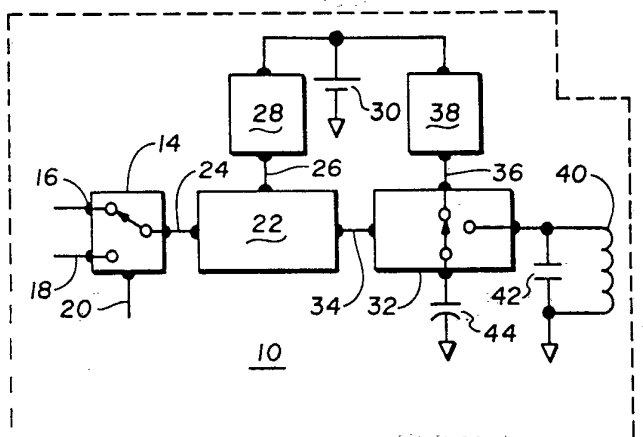




INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification ³ : A61B 5/04	A1	(11) International Publication Number: WO 80/02498 (43) International Publication Date: 27 November 1980 (27.11.80)
(21) International Application Number: PCT/US80/00562 (22) International Filing Date: 14 May 1980 (14.05.80) (31) Priority Application Number: 038,805 (32) Priority Date: 14 May 1979 (14.05.79) (33) Priority Country: US (71) Applicant: MEDTRONIC, INC. [US/US]; 3055 Old Highway Eight, P.O. Box 1453, Minneapolis, MN 55440 (US). (72) Inventor: DUGGAN, Stephen, R.; 4180 120th Street West, Rosemount, MN 55068 (US).		(74) Agents: BREIMAYER, Joseph, F. et al.; Medtronic, Inc., 3055 Old Highway Eight, P.O. Box 1453, Minneapolis, MN 55440 (US). (81) Designated States: DE, FR (European patent), NL. Published With international search report

(54) Title: TELEMETRY TRANSMISSION SYSTEM FOR ANALOG AND DIGITAL DATA FROM AN IMPLANTED SOURCE



(57) Abstract

An improved telemetry transmission system (10) for transmitting electrocardiographic information, indications of the occurrence of the pacing pulse and digitally encoded information from an implanted pacer, drug dispensing device or the like to a remote receiver (12). Two-way telemetry is provided by switch (32) which tunes the tank circuit (40, 42) by means of a capacitor (44) to receive external control signals.

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TELEMETRY TRANSMISSION SYSTEM FOR ANALOG AND DIGITAL
DATA FROM AN IMPLANTED SOURCE

I. DESCRIPTION

5 Background of the Invention

The present invention relates to a telemetry system for transmitting information detected by or relating to electronic devices such as implanted cardiac pacemakers or implanted medication dispensing devices to an external
10 receiver for recording and analysis or for retransmission over phone lines to a remote location.

Adequate evaluation of the operation of implanted electronic prosthetic devices such as pacemakers is necessary to verify their proper operation and to avoid undetected premature performance degradation so that corrective
15 steps may be taken promptly. Although some systems have been previously described which claim to have achieved adequate monitoring of one or more variables in connection with the operation of an implanted pacemaker, those systems
20 have proven to be cumbersome in providing usable information to an external terminal.

In addition, the prior art systems have not generally attempted to solve the problems of transmitting information from a metal encased implantable device. Prior
25 art systems have also failed to consider the compatibility of the telemetry system with a programmable pacemaker or other remotely programmed implantable device which operates at some times in response to an externally generated programming signal.

30 A telemetry patent, 4,026,305, to Tyers, relates



to a telemetry system for transmitting a signal indicating the battery voltage of a pacemaker to an external monitor. The system disclosed in Tyers is not usable for transmission of electrocardiogram information or for digital
5 data. The Tyers system uses a low pass system which includes 60 Hz and 120 Hz.

Further, the problem of minimizing the power consumption of a two-way telemetry system capable of transmission through a metal shield has not been adequately
10 addressed.

The present invention accordingly provides a two-way telemetry system utilizing an improved ultra-low power circuit for transmission of pacemaker EKG, analog data, or stored digital data to an external terminal. The
15 system operates to permit monitoring of the electrical activity on the lead of an implantable pacemaker without attaching external or catheter electrodes to the patient. The receiver uses a bandpass system which operates above the common noise frequencies of 60 Hz and 120 Hz.

20 To receive transmitted data, a receiving coil antenna is placed over the implantable pacemaker and the pacemaker is commanded by applying a programming signal to its circuitry to cause it to send out the electrogram, the pacing pulse, or other data to the remote receiver.

25 The transmitting circuitry of the present invention is compatible with the antenna and receiving circuitry shown in co-pending application entitled Digital Cardiac Pacemaker, filed November 6, 1978, under Serial Number 957,958, naming Ray S. McDonald as the inventor. That
30 application discloses a pacemaker pulse generator which can be remotely programmed.

Brief Description of the Drawings

A preferred embodiment of the present invention is hereafter described with specific reference being made
35 to the following figures in which;

Figure 1 is a simplified block diagram of the



entire telemetry system;

Figure 2 shows the type of damped sinusoid signals transmitted by the system;

Figure 3 is a detailed schematic diagram of the
5 transmitter circuitry;

Figure 4 is a detailed schematic of the receiving circuitry.

Block Diagram of Transmitter

Referring now to Figure 1, there is shown a
10 block diagram of the implantable transmitter 10 and of the receiver 12 used therewith. The dashed line 13 generally designates the skin of the patient in which the transmitter 10 is implanted. The block diagram of the transmitter 10, which is enclosed within a sealed metallic case 13 made of
15 titanium or some similar material. A solid state switch module 14 which receives analog data at an input 16 and digital data at an input 18 is shown within case 13. The sources of the analog and digital data provided to inputs 16 and 18 are discussed more fully below.

20 The analog signal may, in cardiac pacemaker applications, be derived from any of a number of sources. Through appropriate conventional switching, analog signals indicative of the endo or myoelectrogram or pacing artifact may be provided. Typical pacing artifacts are the
25 actual pacing pulse, a voltage indicative of the charging of the pacemaker output stage capacitor or a signal indicative of lead electrode repolarization. Any low voltage 0.1 Hz to 80 Hz bandwidth analog signal lends itself to transmission utilizing the system disclosed.

30 Digital data suitable for transmission is required to be in non-return to zero digital pulses shifted at 10 msec per bit. In digital pacemakers such as the one disclosed in my co-pending application, Serial Number 926,303, filed July 20, 1978, entitled Multimode Adaptable, Implantable Pacemaker, data relating to the operation
35 of the device is located in a number of memory locations



as 8 data bit words. Such digital data can be readily put into asynchronous non-return to zero form with a start bit, 7 or 8 data bits, a parity bit, and a stop bit. The formatting of the data can be accomplished with commercially available UART circuits such as the CDP 1854 UART sold by RCA and other manufacturers.

The digital data input terminal 18 may also be used to generate a calibrating signal for use in calibrating the EKG channel in a recorder connected to the telemetry receiver.

Solid state switch 14 acts in response to a digital/analog control signal on terminal 20 to select either analog or digital data for transmission. Such a signal can be internally generated within a programmable digital pacemaker. The output of the solid state switch 14 is connected to the input of a voltage controlled oscillator 22 through a conductor 24. The voltage controlled oscillator 22 also receives a controlled current on conductor 26 which is regulated by a constant current source 28 driven by a voltage source 30. In the embodiment shown, the supply voltage is nominally 5 volts. Use of low threshold CMOS circuitry in the transmitter 10 would allow use of an even lower nominal voltage for the power source.

The output of the voltage controlled oscillator 22 is connected to control the operation of a further solid state switch 32 through conductor 34. Solid state switch 32 receives a controlled current through conductor 36. The controlled current is supplied by a current regulating circuit 38 which is in turn connected to voltage source 30. The output of the solid state switch 32 is connected to an antenna coil 40 across which is connected a capacitor 42.

The magnitude of the voltage at output of the solid state switch 14 linearly modulates the free running frequency of the voltage controlled oscillator or VCO 22 as a function of the input voltage. In the preferred



embodiment shown, the free running frequency of VCO 22 is 1500Hz and the modulation scale factor is 10Hz per millivolt. The 1500Hz free running frequency was selected to correspond to the center of the band width of a standard
5 telephone system, and the scale factor was selected for compatibility with typical ± 20 mvolt EKG signals.

The output of voltage controlled oscillator 22 on line 34 is used to control the action of the solid state switch 32. When the voltage controlled oscillator 22 has
10 a low output voltage representative of a logic zero, switch 32 is in the position shown in Figures 1 and 3, and connected to receive current from the constant current source 38 and charge capacitor 44. In the specific embodiment shown, the increase of voltage across capacitor 44
15 during the charging cycle is typically in the vicinity of 18 millivolts. When the output of the voltage controlled oscillator 22 is a high voltage corresponding to a logic 1, the solid state switch 32 switches to the other position connecting the capacitor 44 to dump its energy into the
20 tuned parallel combination of capacitor 42 and the antenna coil 40.

It should be pointed out that capacitor 42 tunes antenna coil 40 to the resonant frequency of input programming pulses as discussed in the above-identified Digital
25 Cardiac Pacemaker patent application to Ray S. McDonald. Thus, the antenna coil functions not only as a transmitting antenna as described herein, but also as a receiving antenna when switch 32 is in a position to charge capacitor 44.

30 The tuned combination of capacitors 42 and 44 and coil 40 oscillates at a resonant frequency of 10kHz. It is important to limit the damped sinusoid frequency F1 to approximately 10kHz or less to minimize the attenuation of the signal by the titanium case used to enclose the antenna
35 and circuitry. The damping factor of the equivalent parallel tuned circuit comprising capacitors 42 and 44 and conductor 40 should not exceed 0.2 to assure oscillation of



-6-

the tuned circuit.

The damped sinusoidal voltage created across antenna 40 is important in the operation of the telemetry system and creates a distinct advantage in performance over systems, such as Tyers, which drive the transmitting antenna with a fixed level voltage. In the present invention, use of a damped sinusoidal voltage across antenna 40 creates an electromagnetic field whose maximum strength occurs at the frequency F_1 , which in the preferred embodiment occurs at a frequency of approximately 10 kHz. In contrast, a fixed voltage impressed across an antenna such as 40 would cause the maximum energy to be concentrated at zero frequency and diminish at higher frequencies in accordance with an envelope of $\sin F$ divided by F as is commonly known in the art. All things being equal, a receiver such as 12 which detects this radiated energy must be tuned to a very low frequency to recover the transmitted energy. This is undesirable since the prevalent noise frequencies of 60 Hz and 120 Hz are included in the frequencies.

In the preferred embodiment discussed, a receiver such as 12 which is receiving radiated energy from an antenna driven with damped sinusoidal voltage would be tuned at a frequency F_1 of 10 kHz to avoid reception of the noise frequencies of 60 and 120 Hz. Use of damped sinusoidal frequency modulated signals as disclosed thereby results in a desirable noise-free operation and a more cost-effective system since costly noise filters are not necessary.

Figure 2 illustrates the nature of the voltage waveform across the antenna coil 40 as a function of time. The frequency F_1 is the 10kHz resonant frequency of the antenna 40, its associated capacitor 42 and capacitor 44, while the frequency F_2 represents the 1.5 kHz frequency modulated signal which appears at the output of the voltage controlled oscillator 22.



Schematic of Transmitter

Figure 3 is a detailed schematic of the transmitter circuitry 10 shown in Figure 1 with the components which are shown in Figure 1 similarly numbered. The analog input at terminal 16 is connected to the input terminal of solid state switch 14 through a DC blocking capacitor 46 which has a sufficiently large capacitance to provide a low frequency response sufficient to pass a 0.1Hz sine wave and large enough to prevent distortion of an EKG signal due to differentiation.

The signal after passing through blocking capacitor 46, is connected to the input terminals of the solid state switch 14. The indicated terminal designations for solid state switches 14 and 44 and the terminals for the voltage controlled oscillator 22 are all as specified by the manufacturer. Switch 14 operates to connect either the analog input received at terminal 16 or the digital input received at terminal 18 to the input of terminal 9 of the voltage controlled oscillator 22.

Switch 47 is shown in Figure 3 with its wiper tied to terminals 3 and 6 of switch 14, which are grounded when an analog input is selected. When a digital input signal or a calibration signal is to be received at terminal 18, switch 47 is moved to position B with terminals 3 and 6 tied to a positive voltage. Switch 47 or an associated logic signal such as 20, shown in Figure 1, can be generated by the prosthetic device control logic to cause the transmitter to select a digital or an analog input. Alternatively, switch 47 can be actuated from outside of the body in which the transmitter is implanted by using a magnetic reed switch to switch between input signals.

In the specific circuit shown in Figure 3, the digital input port 18 is connected to an N channel transistor switch module 14. When the voltage at terminal 18 is high, the transistor 48 places a low impedance path across resistor 50, and the voltage change across resistor 50



which is caused by the switching of transistor 48, is coupled through a capacitor 52 through the solid state switch 14.

When solid state switch 14 is in position B to receive digital input data from terminal 18, a path through the switch is provided from the constant current circuit 70 used to provide input bias to the voltage controlled oscillator 22. The bias circuit 70 provides a current of approximately 0.5 microamperes along conductor 54. Since in the preferred embodiment, bias resistors 56 and 58 have a total impedance of approximately 1.5 megohms, and resistor 50 has a resistance of approximately 20 K ohms, the switching of transistor 48 across resistor 50 does not measurably alter the input bias to the voltage controlled oscillator 22 unless the switch of the solid state switch 14 is in position B as shown to select digital data.

The ten millivolt voltage swing across resistor 50 is transmitted through capacitor 52 and switch 14 to the input of the voltage controlled oscillator 22 with a rapid rise time. The digital input can thus be used to calibrate an EKG recorder receiving the signal from the transmitter to provide an output signal indicative of a 10 mv input signal.

Figure 3 also shows a current regulator 28 connected to the power supply 30. In the preferred embodiment shown, the current regulator comprised of PNP transistors 60 and 62 and resistors 64 and 66 is adjusted to provide a constant current of approximately 3.5 microamperes nominal from the collector of transistor 62. Variable resistor 66 is used to adjust the current delivered.

The output of current regulator 28 is delivered to the positive supply voltage terminal of the voltage controlled oscillator 22 and further to the current regulator 70 comprised of transistors 72 and 74 and resistors 76 and 78 which establish a controlled current output from the collector of transistor 74 of 0.5 microamps nominal as a bias current to the input of the voltage controlled



oscillator 22. Capacitor 80 is connected to the output of the current regulator 28 to smooth the supply voltage applied to the voltage controlled oscillator 22. Capacitor 81 is connected between pins 6 and 7 of VCO 22, while resistor 83 is connected between pin 11 and ground.

The regulation and limiting of the current delivered to the voltage controlled oscillator 22 limits the current consumption of the oscillator to a value preset by the constant current source to prevent voltage controlled oscillator 22 from drawing excessive current. By limiting the current supplied to voltage controlled oscillator 22 and to the output switch 32 to an amount slightly above the minimum current at which they will operate the current drain can be minimized and held constant as the voltage 22 of the voltage source 30 decays with time. Since the minimum operating voltage at which devices can operate varies between devices, it is not practical to minimize the current drawn by the various circuits by adjusting the voltage of voltage source 30.

The output of voltage controlled oscillator 22 at pin 4 of oscillator 22 is a 50 percent duty cycle, frequency modulated 1500Hz square wave, which is converted to a damped 10kHz damped sinusoid by the output stage 32 of the transmitter 10 as described below.

Current source 38, which is comprised of transistors 82 and 84 and resistors 86 and 87, supplies a regulated 13 microampere charging current to a 0.22 microfarad capacitor 44 through solid state switch 32 when the switch is in position A as shown in Figure 3. Since the switch 32 is driven from conductor 32 by the 50 percent duty cycle output of VCO 22, the average current is 6.5 microamperes nominal. The current from current regulator 38 charges capacitor 44 to approximately 18 millivolts during the half period of the 1500 Hertz drive signal from the voltage controlled oscillator output 34 when the voltage is low.

During the half period when the VCO 22 has a logic one at its output terminal 4, the switch in solid



state switch 32 is in the B position, which turns the field effect transistor 92 on, providing a low impedance path for capacitor 44 to discharge the energy stored in the previous half cycle into the parallel combination of capacitor 42 and antenna 40. The action of dumping the stored charge in capacitor 44 into the parallel combination of capacitor 42 and inductor antenna 40 causes the antenna voltage to oscillate as a damped sinusoid whose frequency and amplitude are readily controlled by the selection of capacitor values 42 and 44, inductance and resistance of antenna 40 and the charging current from current source 38 according to formulae known to those skilled in the art. The capacitance of capacitor 42 and the inductance of antenna 40 are selected to resonate at a frequency of 175 K Hertz, which is the receiving frequency of the antenna of the device disclosed in the above-identified patent application for Digital Cardiac Pacemaker of Ray S. McDonald.

In the preferred embodiment shown, capacitor 42 has a capacitance of 330 picofarads, capacitor 44 has a value of .22 microfarads, and the inductance of the antenna 40 is approximately one millihenry. Since capacitor 44 is much larger than capacitor 42, inductor 94 and capacitor 42 resonate as they receive the stored energy in capacitor 90 as a damped sinusoid at 10 kilohertz. The frequency of the damped sinusoidal oscillation is controlled primarily by capacitor 44 and inductor 40, while the repetition rate of the pulses is determined by the VCO 22. Note also, that when switch 32 is in position A, the solid state switch 32 and the field effect transistor 92 are connected in such a way as to isolate capacitor 44 from the parallel tuned circuit consisting of capacitor 42 and inductor 40. This design allows the inductor 40 and capacitor 42 to function as a receiving parallel tuned circuit without appreciable attenuation caused by other components in the circuit. Inductor antenna 40 therefore functions not only as a transmitting antenna, but also as a receiving antenna, which may be connected to receiving circuitry at terminal



-11-

43, thereby achieving benefits of lower cost and fewer components by having a dual function. A suitable receiving circuit is shown in the McDonald application identified above.

5 The transmitter 10, when not in operation, does not place a load on antenna 40 which has a significant effect on its ability to receive externally transmitted information at 175 kHz. Tests of the unit indicate that the loading of the transmitter on the antenna is less than
10 0.5 db when the transmitter is not active.

Receiver Circuitry

Referring again to Figure 1, a block diagram of the receiver section 12 is shown. The receiver consists
15 of an antenna section 100 and a tuning capacitor 102 which are connected to a band pass filter 103 which delivers its signal to a phase lock loop circuit 104 which provides its output signal to an amplifier 106 which drives a loud speaker 108 or some other indicating means.

20 A more detailed schematic of the circuitry of the receiving section 12 is shown in Figure 4. The antenna in a preferred embodiment is wound from 1500 turns of #30AWG wire in a loop having a diameter of approximately 10 centimeters. The inductance of the coil is approximately
25 0.396 henrys, and the coil was tuned with a shunt capacitor 102 to resonate at 10 kHz.

The antenna output is connected through a coupling capacitor 110 and a resistor 112 to the input of the first stage 114 of the band pass amplifier shown in Figure 1, as
30 block 103. Each stage of the amplifier provides independent control of low frequency cutoff and high frequency cutoff frequencies and provides a single order or six decibels per octave attenuation beyond the respective cut-off frequencies. The low frequency break point is deter-
35 mined by the values of resistor 112 and capacitor 110 while the high pass break point is determined by feed back resistor 116 and capacitor 118 for the first amplifier 114.



-12-

Similarly, the low frequency break point is determined by the values of resistor 122 and capacitor 120 while the high frequency break point is determined by the values of resistor 126 and its stray capacitance for amplifier
5 stage 124.

The particular advantage of the band pass amplifier configuration shown in Figure 4 is that the amplifier's pulse response does not produce an oscillatory output because the poles of the amplifier Bode plot are always
10 real rather than imaginary. This characteristic of the band pass amplifier is important in the disclosed receiver, since the received information signal from the transmitter is a damped sinusoid pulse.

The output of amplifier 114 is connected through
15 a capacitor 120 and a resistor 122 to the input of the second band pass amplifier stage 124 which has a feed back resistor 126 connected between its output and its noninverting input terminals. The output of the second stage 124 of the band pass amplifier 103 is connected through a
20 capacitor 128 to the input terminal of the phase lock loop circuit 104 and to one end of a grounded resistor 130.

The phase lock loop circuit is connected in an FM demodulation circuit arrangement. When the input 2 to the phase lock loop circuit 104 is grounded, the output
25 frequency at terminals 4 and 5 is 1500Hz. The pin designations are those indicated by the manufacturer. The FM demodulator circuit and its characteristics are described in further detail in Signetic Analog Manual, dated 1976, at Page 623.

30 Resistor 132 is an adjustable resistor used to set the phase lock loop circuit at 1500 Hz with its input at terminal 2 grounded. The oscillator output of the phase lock loop 104 is connected to a resistor 140 which provides the base drive to a grounded emitter NPN transistor 142, which in turn, drives a loud speaker or similar
35 transducer 144 through a resistor 146. The capture range of the VCO as configured in Figure 4 is plus or minus



-13-

434 Hz, while the lock range is plus or minus 2kHz. Since the transmitter 10 has a voltage controlled oscillator scale factor of 10Hz per millivolt deviation, the receiver circuit has the ability to receive an EKG signal of plus 5 or minus 43 millivolts.

The output stage, including transistor 142, amplifies the 1500 Hertz FM square wave at the output of the voltage controlled oscillator to drive a small transducer 144 such as a one inch speaker which can then be 10 positioned near a conventional telephone handset to transmit the 1500 Hz frequency modulated signal to a remote EKG machine or a digital data recorder.

Speaker 144 is connected to a telephone to transmit the frequency modulated signal over telephone 15 lines, a receiver such as the Model 9401 Teletrace R receiver manufactured by Medtronic, Inc. can be used to demodulate the signal and provide an EKG trace. Alternatively, an analog signal representation can be directly obtained from the phase lock loop circuit on terminal 148.

20 Digital data can be received and converted to non-return to zero pulses which may then be decoded into numerals and characters using known terminal devices.

The preferred embodiment of the telemetry system disclosed above has been found to work well with the 25 following values or part designations.

<u>Resistors</u>	<u>Ohms</u>
50	20 K
56	1.3 M
58	200 K
30 64, 78, 86	10 M
66	100 K variable in series with 75 K fixed
76	820 K
83, 112, 122, 130	100 K
35 116	2.2 M
126	4.7 M



-14-

132	10 K variable
140	15 K
146	100
87	100 K variable
5 <u>Capacitors</u>	<u>Microfarads</u>
42	0.000330
44	0.22
46, 80	1.0
102	
10 118	0.000005
110, 120	0.000200
52, 128	0.1
134	0.47
136	.001
15 81	0.000170
138	0.047
<u>Transistors</u>	
60, 62, 72, 74, 82, and 84	2N3799
20 48	3N171
92	2N6661
142	2N2222
<u>Circuits</u>	
switch 14	TA 6178 RCA
25 switch 32	CD 4007 RCA
voltage controlled oscillator 22	CD 4046 RCA
amplifiers 114, 124	LM 318 National
phase lock loop 104	NE 565 Signetics

30 Having described the invention by way of the above examples and general description, the subject matter in which exclusive rights are claimed is defined as follows:



II. CLAIMS

1. A telemetry system utilizing an implantable transmitter for transmitting data from at least one location within a living body to an external receiver, said system
5 comprising, in combination:

an implantable transmitter for transmitting a frequency modulated signal indicative of some value of data at a location within a living body;
and

10 a receiver tuned to receive said frequency modulated output from said implantable transmitter and to extract a signal therefrom to provide an output signal indicative of said data.

2. The invention of Claim 1 wherein said transmitter and
15 receiver are constructed and arranged to have a signal passband which does not include 60 Hz signals.

3. In the telemetry system of Claim 1; an implantable transmitter for transmitting data from at least one location within a living body to an external receiver, said
20 transmitter comprising, in combination:

input means for receiving a signal from said location and providing an electrical signal representative of said data;

25 modulator means for receiving said electrical signal and generating an alternating signal having a period which differs from a predetermined nominal by an amount determined by some characteristic of said electrical signal;

antenna means; and

30 output means responsive to the alternating signal produced by said modulated means to drive said antenna means with a series of fixed frequency damped sinusoidal signals occurring at time intervals corresponding to the period of the alternating signal produced by said modulator means.
35



-16-

4. The invention of Claim 3 wherein said output means drives said antenna means with damped sinusoidal signals having a frequency of approximately 10 kHz.
5. The invention of Claim 4 wherein said antenna means is constructed and arranged to receive information from an external transmitter in the time intervals between applications of damped sinusoidal signals to said antenna means.
6. The invention of Claim 5 wherein said antenna means resonates at approximately 175 K Hz when receiving signals from an external transmitter.
7. The invention of Claims 3 or 4 wherein the predetermined nominal period of the output of said modulator means is approximately 1500 Hz.
8. The invention of Claim 7 wherein the variation of the alternating signal at the output of said modulator means from the predetermined nominal is 10 Hz per millivolt.
9. The invention of Claim 3 wherein the input means is connected to receive a digitally encoded asynchronous signal, said modulator means includes bias means for varying the input voltage to the input of said modulating means by a predetermined increment in response to the presence or absence of pulses received by said input means.
10. The invention of Claim 9 wherein the variation in voltage applied to the input of said modulator means in response to the absence or presence of pulses received by said input means is 10 millivolts.
11. The invention of Claim 3 wherein said modulator means is a voltage controlled oscillator.
12. The invention of Claim 11 wherein current limiting



-17-

means limit the current delivered to power said voltage controlled oscillator to an amount slightly exceeding the minimum current at which said voltage controlled oscillator may be operated.

5 13. The invention of Claim 11 wherein the scale factor of said voltage controlled oscillator is 10 Hz per millivolt.

14. The invention of Claim 3 wherein said output means comprises:

current source means;
10 capacitance means; and
switching means controlled by the alternating signal from said modulator means to connect said capacitance means to said current source means during half of the period of said alternating signal from said modulator means, and to connect said capacitance means
15 to said antenna means during the other half of said alternating signal.

15. In the telemetry system of Claim 1, a receiver for receiving data from said implantable transmitter, said
20 receiver comprising:
receiving antenna means;
band pass filter means receiving a signal from said receiving antenna means and delivering an output signal representative of received signals
25 within the pass band; and
a phase lock loop circuit for receiving the output from said band pass filter and producing a demodulated output signal representative of said data.

16. The invention claimed in Claim 15 wherein said phase
30 lock loop circuit provides a demodulated analog output representative of the transmitted data.

17. The invention claimed in Claim 15 wherein said phase



lock loop circuit provides a frequency modulated audio signal or transmission of the frequency modulated data over a phone line to further receiving circuitry.

18. The invention claimed in Claim 15 wherein said band
5 pass filter passes signals having a frequency of 10 kHz
plus or minus 2 kHz.



Fig. 1

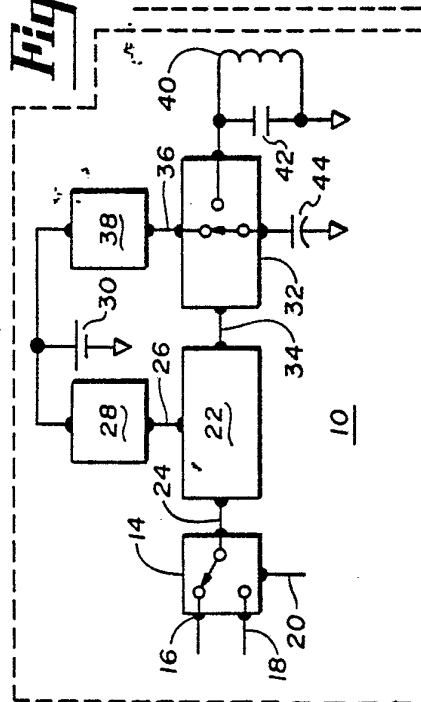


Fig. 2

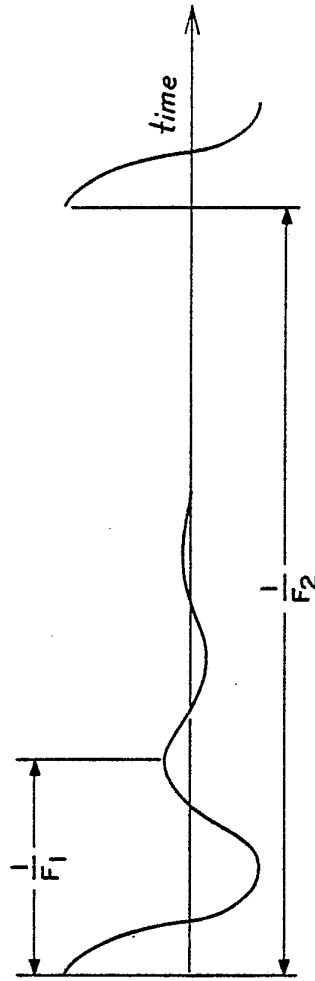
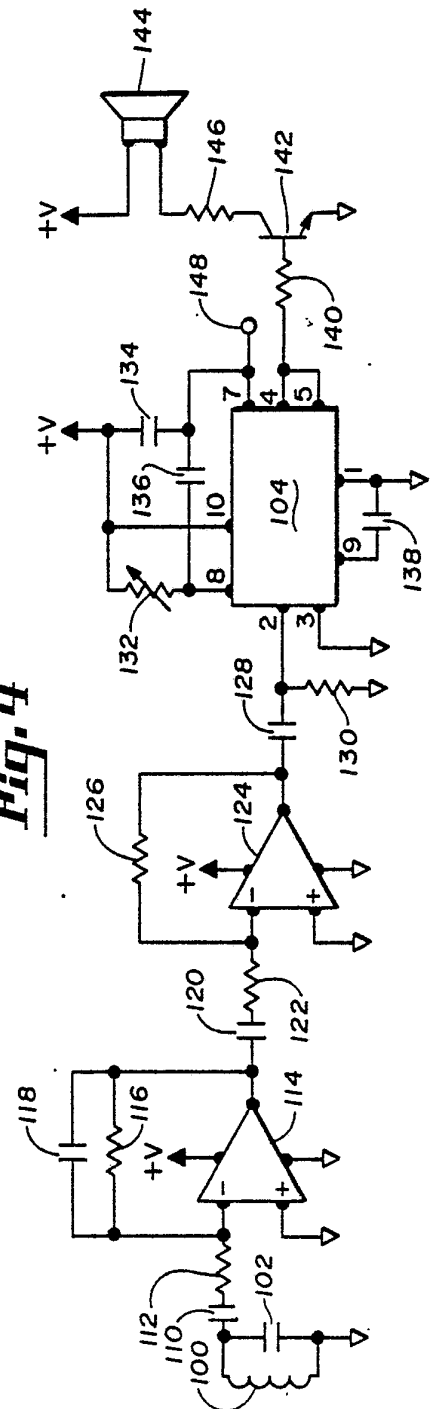
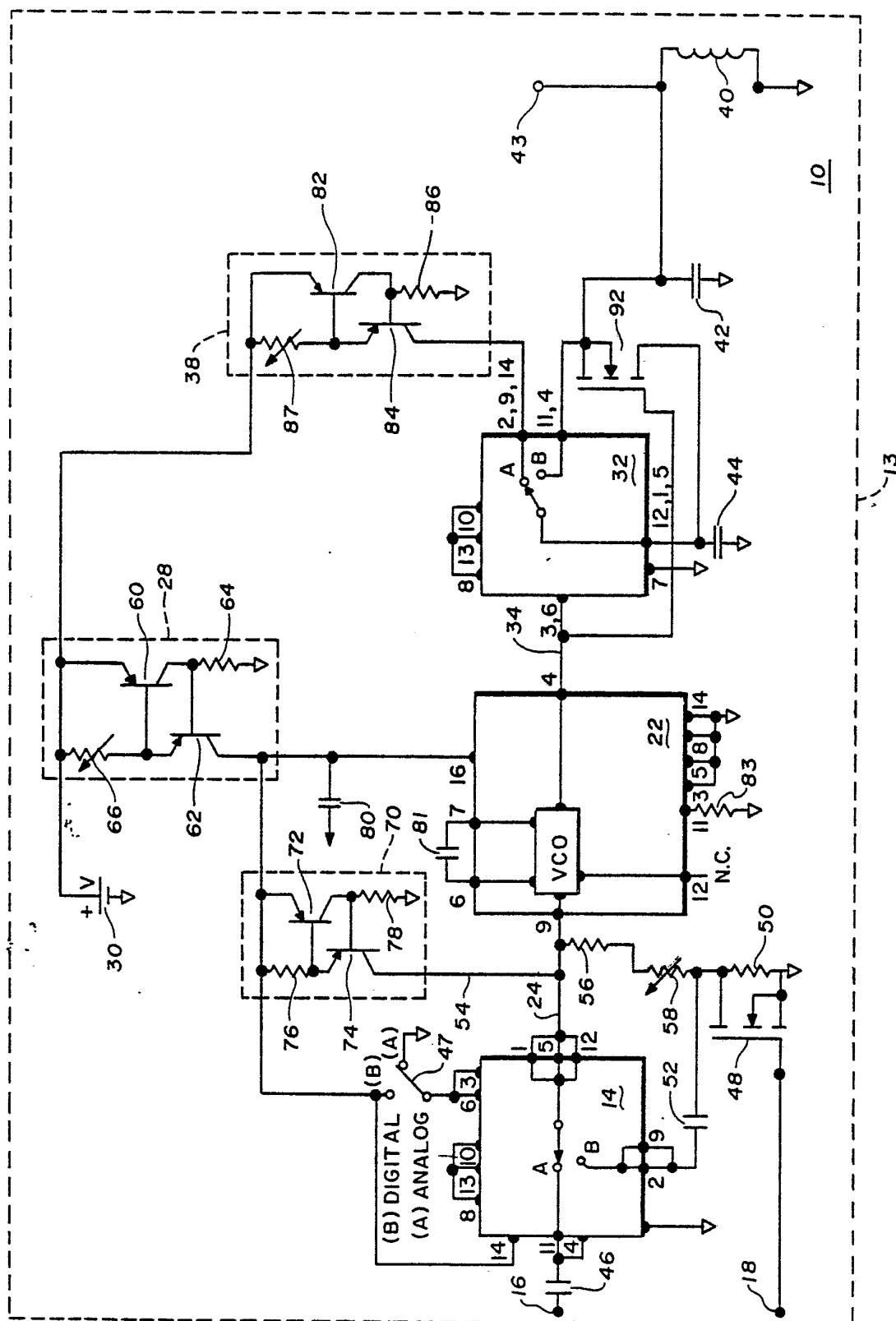


Fig. 4





INTERNATIONAL SEARCH REPORT

International Application No PCT/US 00562

I. CLASSIFICATION OF SUBJECT MATTER (If several classification symbols apply, indicate all) *		
According to International Patent Classification (IPC) or to both National Classification and IPC		
INT. CL. ³ A61B 5/04-US CL. 128/697		
II. FIELDS SEARCHED		
Minimum Documentation Searched ⁴		
Classification System	Classification Symbols	
U.S.	128/260,419P,419PT,696-697,701+903	
Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched ⁵		
III. DOCUMENTS CONSIDERED TO BE RELEVANT ¹⁴		
Category *	Citation of Document, ¹⁶ with indication, where appropriate, of the relevant passages ¹⁷	Relevant to Claim No. ¹⁸
X	US,A, 4,026,305, Published 31 MAY 1977, Brownlee et al	1-18
X	US,A, 2,812,427, Published 05 November 1957, Magondeaux	4-6
X,P	US,A, 4,172,459, Published 30 October 1979, Hepp	5-6
X	US,A, 3,698,398, Published 17 October 1972, Berkovits	14
A	US,A, 3,662,758, Published 16 May 1972, Glover	-
X	US,A, 3,872,455, Published 18 March 1975, Fuller et al	15-18
X	US,A, 4,142,533, Published 06 March 1979, Brownlee et al	17
* Special categories of cited documents: ¹⁵ "A" document defining the general state of the art "E" earlier document but published on or after the international filing date "L" document cited for special reason other than those referred to in the other categories "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but on or after the priority date claimed "T" later document published on or after the international filing date or priority date and not in conflict with the application, but cited to understand the principle or theory underlying the invention "X" document of particular relevance		
IV. CERTIFICATION		
Date of the Actual Completion of the International Search ¹	Date of Mailing of this International Search Report ²	
08 July 80	20 AUG 1980	
International Searching Authority ¹	Signature of Authorized Officer ²⁰	
ISA/US	W.E. Kamm	