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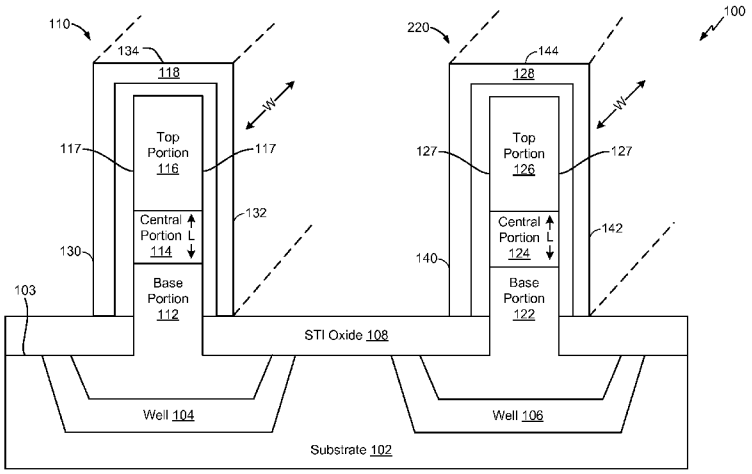

FIG. 1

(57) Abstract: A tunnel field transistor (TFET) device includes a fin structure that protrudes from a substrate surface. The fin structure includes a base portion proximate to the substrate surface, a top portion, and a first pair of sidewalls extending from the base portion to the top portion. The first pair of sidewalls has a length corresponding to a length of the fin structure. The fin structure also includes a first doped region having a first dopant concentration at the base portion of the fin structure. The fin structure also includes a second doped region having a second dopant concentration at the top portion of the fin structure. The TFET device further includes a gate including a first conductive structure neighboring a first sidewall of the first pair of sidewalls. A dielectric layer electrically isolates the first conductive structure from the first sidewall.

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VERTICAL TUNNEL FIELD EFFECT TRANSISTOR

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] The present application claims priority from commonly owned U.S. Non-Provisional Patent Application No. 14/021,795 filed on September 9, 2013, the contents of which is expressly incorporated herein by reference in its entirety.

FIELD

[0002] The present disclosure is generally related to a vertical tunnel field effect transistor.

DESCRIPTION OF RELATED ART

[0003] Advances in technology have resulted in smaller and more powerful computing devices. For example, there currently exist a variety of portable personal computing devices, including wireless computing devices, such as portable wireless telephones, personal digital assistants (PDAs), and paging devices that are small, lightweight, and easily carried by users. More specifically, portable wireless telephones, such as cellular telephones and internet protocol (IP) telephones, may communicate voice and data packets over wireless networks. Further, many such wireless telephones include other types of devices that are incorporated therein. For example, a wireless telephone may also include a digital still camera, a digital video camera, a digital recorder, and an audio file player. Also, such wireless telephones may process executable instructions, including software applications, such as a web browser application, that may be used to access the Internet. As such, these wireless telephones may include significant computing capabilities.

[0004] A semiconductor device for use in wireless communication devices may include transistors (e.g., complementary metal-oxide-semiconductor (CMOS) transistors) that form logic circuits within the semiconductor device. Each CMOS transistor may include a gate, a source region, and a drain region. Upon activation, a gate bias of a traditional CMOS transistor may cause the formation of an accumulation region channel between the source region and the drain region to permit current flow from the source region to the drain region. In contrast, a tunnel CMOS transistor may enable current

flow as a result of band-to-band tunneling in a channel enabled by an applied gate bias. However, because tunnel CMOS transistors are typically planar, such tunnel CMOS transistors may present scaling challenges for sub-22 nanometer (nm) process dimensions and beyond.

SUMMARY

[0005] A vertical tunnel field effect transistor (TFET) and a method of fabrication are disclosed. A fin-type vertical TFET may include a source region and a drain region that are vertically coupled via a channel region. A vertical tunnel may be formed within the channel region to create a conduction path between the source region and the drain region. The length of the vertical tunnel may be dependent on the height of the channel region. The fin-type vertical TFET may also include a gate with an adjustable width. For example, an amount of saturation current that flows through the vertical tunnel may be adjusted (e.g., increased or decreased) in response to changing the width of the gate.

[0006] In a particular embodiment, a tunnel field transistor (TFET) device includes a fin structure that protrudes from a substrate surface. The fin structure includes a base portion proximate to the substrate surface, a top portion, and a first pair of sidewalls extending from the base portion to the top portion. The first pair of sidewalls has a length corresponding to a length of the fin structure. The fin structure also includes a first doped region having a first dopant concentration at the base portion of the fin structure. The fin structure also includes a second doped region having a second dopant concentration at the top portion of the fin structure. The TFET device further includes a gate including a first conductive structure neighboring a first sidewall of the first pair of sidewalls. A dielectric layer electrically isolates the first conductive structure from the first sidewall.

[0007] In another particular embodiment, a method includes fabricating a vertical tunnel field effect transistor (TFET) device. Fabricating the vertical TFET device includes forming a well region, a base portion, a central portion, and a top portion within a substrate. The base portion protrudes from a surface of the well region, and the central portion is formed between the base portion and the top portion. Fabricating the vertical TFET device also includes etching the substrate to form a vertical fin structure. The vertical fin structure includes the base portion, the central portion, and the top portion.

Fabricating the vertical TFET device further includes depositing a dielectric layer on the vertical fin structure and depositing a first gate material on the dielectric layer.

[0008] In another particular embodiment, an apparatus includes means for providing charge carriers to a tunneling channel and means for receiving the charge carriers from the tunneling channel. One of the means for providing or the means for receiving is at a base portion of a fin structure and is adjacent to a substrate surface. The other of the means for providing or the means for receiving is at a top portion of the fin structure. The apparatus also includes means for biasing the tunneling channel to enable band-to-band tunneling at the tunneling channel.

[0009] One particular advantage provided by at least one of the disclosed embodiments is an ability to form band-to-band tunneling currents in channels of tunnel field effect transistors for sub-22 nanometer (nm) process dimensions and beyond. Other aspects, advantages, and features of the present disclosure will become apparent after review of the entire application, including the following sections: Brief Description of the Drawings, Detailed Description, and the Claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] FIG. 1 is a diagram of a particular illustrative embodiment of a vertical tunnel field effect transistor device;

[0011] FIG. 2 is a diagram of another particular illustrative embodiment of a vertical tunnel field effect transistor device;

[0012] FIG. 3 is a diagram illustrating a particular stage of fabricating the vertical tunnel field effect transistor device of FIG. 1;

[0013] FIG. 4 is a diagram illustrating another stage of fabricating the vertical tunnel field effect transistor device of FIG. 1;

[0014] FIG. 5 is a diagram illustrating another particular stage of fabricating the vertical tunnel field effect transistor device of FIG. 1;

[0015] FIG. 6 is a diagram illustrating another stage of fabricating the vertical tunnel field effect transistor device of FIG. 1;

[0016] FIG. 7 is a diagram illustrating another particular stage of fabricating the vertical tunnel field effect transistor device of FIG. 1;

[0017] FIG. 8 is a diagram illustrating another particular stage of fabricating the vertical tunnel field effect transistor device of FIG. 1;

[0018] FIG. 9 is a diagram of a particular illustrative embodiment of a three-dimensional vertical tunnel field effect transistor device;

[0019] FIG. 10 is a flowchart of a particular illustrative embodiment of a method of fabricating a vertical tunnel field effect transistor device;

[0020] FIG. 11 is a block diagram of a wireless communication device including a vertical tunnel field effect transistor device; and

[0021] FIG. 12 is a data flow diagram of a particular illustrative embodiment of a process to manufacture electronic devices that include a vertical tunnel field effect transistor device.

DETAILED DESCRIPTION

[0022] Particular embodiments of vertical tunnel field effect transistor devices and methods of fabrication are presented in this disclosure. It should be appreciated, however, that the concepts and insights applied to the particular embodiments with respect to designs of the vertical tunnel field effect transistor devices and with respect to how to make the vertical tunnel field effect transistor devices may be embodied in a variety of contexts. The particular embodiments presented are merely illustrative of specific ways to design and make the vertical tunnel field effect transistor devices and do not limit the scope of this disclosure.

[0023] The present disclosure describes the particular embodiments in specific contexts. However, features, methods, structures or characteristics described according to the particular embodiments may also be combined in suitable manners to form one or more other embodiments. In addition, figures are used to illustrate the relative relationships between the features, methods, structures, or characteristics, and thus may not be drawn in scale. Directional terminology, such as “top,” “central,” “base,” etc. is used with

reference to the orientation of the figures being described. The components of the disclosure may be positioned in a number of different orientations. As such, the directional terminology is used for purposes of illustration and is not meant to be limiting.

[0024] Referring to FIG. 1, a particular illustrative embodiment of a fin-type vertical tunnel field effect transistor (TFET) device 100 is shown. FIG. 1 shows a cross-sectional view of a portion of the vertical TFET device 100.

[0025] The vertical TFET device 100 includes a substrate 102 and a shallow trench isolation (STI) oxide layer 108. The substrate 102 may be a p-type substrate. In a particular embodiment, the substrate 102 is a silicon (Si) substrate. The STI oxide layer 108 may prevent electrical current leakage between adjacent semiconductor device components. For example, the STI oxide layer 108 may prevent electrical current leakage between the vertical TFET device 100 and another semiconductor device component (e.g., another vertical TFET device).

[0026] The vertical TFET device 100 includes a first vertical TFET 110 that includes a first well region 104, a first base portion 112, a first central portion 114, and a first top portion 116. In a particular embodiment, the first base portion 112, the first central portion 114, and the first top portion 116 are made of a same type of material. For example, the first base portion 112, the first central portion 114, and the first top portion 116 may be made of silicon (Si). In another particular embodiment, the portions 112-116 may be made of at least one III-V material. For example, the portions 112-116 may be made of aluminum arsenide, gallium arsenide, gallium nitride, gallium phosphide, indium antimonide, indium arsenide, indium phosphide, or any combination thereof. In another particular embodiment, the portions 112-116 may be made of at least one II-VI material. The first base portion 112 may be adjacent to (e.g., proximate to) the surface 103 of the substrate 102. The first base portion 112 may correspond to a first doped region having a first dopant concentration, and the first top portion 116 may correspond to a second doped region having a second dopant concentration. The first vertical TFET 110 may also include a first pair of sidewalls 117 extending from the first base portion 112 to the first top portion 116. A first dielectric layer (e.g., a material having a high dielectric constant (k)) may be deposited around the sidewalls 117.

[0027] The first base portion 112, the first central portion 114, the first top portion 116, and the first pair of sidewalls 117 correspond to a first fin structure. The first central portion 114 may correspond to a channel region of the first fin structure, and a channel length (L) may correspond to a height of the first central portion 114. In a particular embodiment, the first top portion 116 may correspond to a drain of the first fin structure and the first base portion 112 may correspond to a source of the first fin structure. In another particular embodiment, the first top portion 116 may correspond to a source of the first fin structure and the first base portion 112 may correspond to a drain of the first fin structure. The first fin structure may protrude from the surface 103 of the substrate 102. The first vertical TFET 110 may also include a first gate 118 that includes a first conductive structure 130 that is adjacent to (e.g., neighboring) at least one sidewall of the first pair of sidewalls 117. The first gate 118 may also include a second conductive structure 132 that is adjacent to (e.g., neighboring) at least one other sidewall of the first pair of sidewalls 117 and a third conductive structure 134 that is adjacent to (e.g., neighboring) the first top portion 116. The third conductive structure 134 may be coupled to the first conductive structure 130 and to the second conductive structure 132. A width (w) of the first gate 118 may be changed to adjust a saturation current of the first vertical TFET 110. The first dielectric layer may electrically isolate the conductive structures 130-134 (e.g., the first gate 118) from the sidewalls 117 and from the first top portion 116, respectively.

[0028] The vertical TFET device 100 also includes a second vertical TFET 120 that includes a second well region 106, a second base portion 122, a second central portion 124, and a second top portion 126. In a particular embodiment, the second base portion 122, the second central portion 124, and the second top portion 126 are made of a same type of material. For example, the second base portion 122, the second central portion 124, and the second top portion 126 may be made of silicon (Si). The second base portion 122 may also be adjacent to (e.g., proximate to) the surface 103 of the substrate 102. The second base portion 122 may correspond to a third doped region having a third dopant concentration, and the second top portion 126 may correspond to a fourth doped region having a fourth dopant concentration. The second vertical TFET 120 may also include a second pair of sidewalls 127 extending from the second base portion 122

to the second top portion 126. A second dielectric layer (e.g., a material having a high dielectric constant (k)) may be deposited around the sidewalls 127.

[0029] The second base portion 122, the second central portion 124, the second top portion 126, and the second pair of sidewalls 127 correspond to a second fin structure. The second central portion 124 may correspond to a channel of the second fin structure, and a channel length (L) may correspond to a height of the second central portion 124. The channel length (L) of the first central portion 114 may be equal to (or substantially equal to) the channel length (L) of the second central portion 124. Alternatively, the first central portion 114 and the second central portion 124 may have different channel lengths (L).

[0030] In a particular embodiment, the second top portion 126 may correspond to a drain of the second fin structure and the second base portion 122 may correspond to a source of the second fin structure. In another particular embodiment, the second top portion 126 may correspond to a source of the second fin structure and the second base portion 122 may correspond to a drain of the second fin structure. The second fin structure protrudes from the surface 103 of the substrate 102. The second vertical TFET 120 may also include a second gate 128 that includes a first conductive structure 140 that is adjacent to (e.g., neighboring) at least one sidewall of the second pair of sidewalls 127. The second gate 128 may also include a second conductive structure 142 that is adjacent to (e.g., neighboring) at least one other sidewall of the second pair of sidewalls 127 and a third conductive structure 144 that is adjacent to (e.g., neighboring) the second top portion 126. The third conductive structure 144 may be coupled to the first conductive structure 140 and to the second conductive structure 142. As further illustrated in FIG. 9, a width of the second gate 128 may be changed to adjust a saturation current of the second vertical TFET 120. The second dielectric layer may electrically isolate the conductive structures 140-144 (e.g., the second gate 128) from the sidewalls 127 and from the second top portion 126, respectively.

[0031] In a particular embodiment, the first vertical TFET 110 and the second vertical TFET 120 are complementary TFETs. For example, the first vertical TFET 110 may be an n-type TFET and the second vertical TFET 120 may be a p-type TFET.

Alternatively, the first vertical TFET 110 may be a p-type TFET and the second vertical TFET 120 may be an n-type TFET.

[0032] Three particular embodiments of the vertical TFET device 100 are described below. In each embodiment, the first vertical TFET 110 is an n-type TFET and the second vertical TFET 120 is a p-type TFET. For example, the first gate 118 may be comprised of a metal having an n-type work function and the second gate 128 may be comprised of a metal having a p-type work function. These embodiments are described for purposes of illustration and are not meant to be limiting. For example, in other embodiments, the first vertical TFET 110 may be an n-type TFET and the second vertical TFET 120 may be a p-type TFET, each vertical TFET 110, 120 may be a p-type TFET, or each vertical TFET 110, 120 may be an n-type TFET.

[0033] In a first particular embodiment, the first well region 104 and the second well region 106 may be doped with an n-type concentration. The first base portion 112 (e.g., the first doped region) may correspond to a source of the first fin structure having a first dopant concentration that includes a P+ concentration. For example, a p+ type silicon may be placed (e.g., implanted) in the substrate 102 and at the bottom of the first fin structure as a source. The first central portion 114 may have a dopant concentration that includes a P- concentration. For example, a p- type silicon may be placed (e.g., implanted) between the first top portion 116 and the first base portion 112 as a channel region. The first top portion 116 (e.g., the second doped region) may correspond to a drain of the first fin structure having a second dopant concentration that includes an N+ concentration. For example, an n+ type silicon may be placed (e.g., implanted) at the top of the first fin structure as a drain. In the first particular embodiment, the second base portion 122 (e.g., the third doped region) may correspond to a drain of the second fin structure having a third dopant concentration that includes a P+ concentration, the second central portion 124 may have a dopant concentration that includes an N- concentration, and the second top portion 126 (e.g., the fourth doped region) may correspond to a source of the second fin structure having a fourth dopant concentration that includes an N+ concentration.

[0034] As variance of a first particular embodiment, the first top portion 116 of the first vertical TFET 110 and the second top portion 126 of the second vertical TFET 120 can

be comprised of different materials than the central portions 114, 124 and the base portions 112, 122. For example, the top portions 116, 126 can be an n-type metal, an n-type polysilicon, etc.

[0035] In a second particular embodiment, the first well region 104 and the second well region 106 may be doped with a p-type concentration. The first base portion 112 (e.g., the first doped region) may correspond to a drain of the first fin structure having a first dopant concentration that includes an N+ concentration. For example, an n+ type silicon may be placed in the substrate 102 and at the bottom of the first fin structure as a drain. The first central portion 114 may have a dopant concentration that includes a P- concentration. For example, a p- type silicon may be placed between the first top portion 116 and the first base portion 112 as a channel region. The first top portion 116 (e.g., the second doped region) may correspond to a source of the first fin structure having a second dopant concentration that includes a P+ concentration. For example, a p+ type silicon may be placed at the top of the first fin structure as a source. In the second particular embodiment, the second base portion 122 (e.g., the third doped region) may correspond to a source of the second fin structure having a third dopant concentration that includes an N+ concentration, the second central portion 124 may have a dopant concentration that includes an N- concentration, and the second top portion 126 (e.g., the fourth doped region) may correspond to a drain of the second fin structure having a fourth dopant concentration that includes a P+ concentration.

[0036] As variance of a second particular embodiment, the first top portion 116 of the first vertical TFET 110 and the second top portion 126 of the second vertical TFET 120 can be comprised of different materials than the central portions 114, 124 and the base portions 112, 122. For example, the top portions 116, 126 can be a p-type metal, a p-type polysilicon, etc.

[0037] In a third particular embodiment, the first well region 104 may be doped with an n-type concentration and the second well region 106 may be doped with a p-type concentration. The first base portion 112 (e.g., the first doped region) may correspond to a source of the first fin structure having a first dopant concentration that includes a P+ concentration. For example, a p+ type silicon may be placed in the substrate 102 and at the bottom of the first fin structure as a source. The first central portion 114 may have a

dopant concentration that includes a P- concentration. For example, a p- type silicon may be placed between the first top portion 116 and the first base portion 112 as a channel region. The first top portion 116 (e.g., the second doped region) may correspond to a drain of the first fin structure having a second dopant concentration that includes an N+ concentration. For example, an n+ type silicon may be placed at the top of the first fin structure as a drain. In the third particular embodiment, the second base portion 122 (e.g., the third doped region) may correspond to a source of the second fin structure having a third dopant concentration that includes an N+ concentration, the second central portion 124 may have a dopant concentration that includes an N- concentration, the second top portion 126 (e.g., the fourth doped region) may correspond to a drain of the second fin structure having a fourth dopant concentration that includes a P+ concentration.

[0038] As variance of the third particular embodiment, the first top portion 116 of the first vertical TFET 110 and the second top portion 126 of the second vertical TFET 120 can be comprised of different materials than the central portions 114, 124 and the base portions 112, 122. For example, the first top portion 116 can be an n-type metal or an n-type polysilicon, and the second top portion 126 can be a p-type metal or a p-type polysilicon, etc.

[0039] A first contact may be coupled to the first base portion 112, a second contact may be coupled to the first top portion 116, and a third contact may be coupled to the first gate 118, as further described with respect to FIG. 9. Voltages applied to each portion 112, 116, 118 via the contacts may cause a first vertical tunneling current to flow between the first top portion 116 and the first base portion 112 via a channel in the first central portion 114. A channel length (L) may defined by the height of the first central portion 114. For example, the length (L) of the channel may correspond to a thickness of a channel film in an embodiment where the first central portion 114 is grown or deposited on the first base portion 112. Similarly, a fourth contact may be coupled to the second base portion 122, a fifth contact may be coupled to the second top portion 126, and a sixth contact may be coupled to the second gate 128. Voltages applied to the each portion 122, 126, 128 via the contacts may cause a second vertical tunneling current to flow between the second top portion 126 and the second base

portion 122 via a channel in the second central portion 124. A channel length (L) may be defined by the height of the second central portion 124.

[0040] It will be appreciated that the first central portion 114 and the second central portion 124 may permit the formation of band-to-band tunneling currents in channels, where the lengths (L) of the channels are independent of the width of the gates 118, 128. The gates 118, 128 may be independently designed and/or adjusted to manage an amount of saturation current supported by the vertical TFETs 110, 120 without affecting the length (L) of the channels. The height of the central portions 114, 124 (e.g., the channel lengths) may also be designed independently of a lithography process used for designing the gates. For example, because the channel is vertical (as opposed to planar), the channel is not limited to a region or a location that is under a planar gate of a field effect transistor.

[0041] Referring to FIG. 2, another particular illustrative embodiment of a fin-type vertical tunnel field effect transistor device 200 is shown. FIG. 2 shows a cross-sectional view of a portion of the vertical TFET device 200.

[0042] The vertical TFET device 200 may include a first vertical TFET 210 and a second vertical TFET 220. The first vertical TFET 210 and the second vertical TFET 220 may correspond to the first vertical TFET 110 of FIG. 1 and the second vertical TFET 120 of FIG. 1, respectively, and may operate in a substantially similar manner. For example, the first vertical TFET 210 may include the first base portion 112, the first central portion 114, the first top portion 116, the first pair of sidewalls 117, the first conductive structure 130, and the second conductive structure 132. The second vertical TFET 220 may include the second base portion 122, the second central portion 124, the second top portion 126, the second pair of sidewalls 127, the first conductive structure 140, and the second conductive structure 142.

[0043] The first vertical TFET 210 may include a first hard mask film 230 that is deposited on the first gate 118 and on the first pair of sidewalls 117. The second vertical TFET 220 may include a second hard mask film 240 that is deposited on the second gate 128 and on the second pair of sidewalls 127. The hard mask films 230, 240 may be deposited during fabrication as described with respect to FIG. 5.

[0044] It will be appreciated that the first top portion 116 and the second top portion 126 of the vertical TFETs 210, 220, respectively, are not covered by a gate material. As a result, contacts may be vertically coupled to the first top portion 116 and to the second top portion 126 from above the fin-type vertical tunnel field effect transistor device 200. Vertically coupling the contacts to the first top portion 116 and to the second top portion 126 may reduce series parasitic resistance in the vertical TFETs 210, 220.

[0045] For ease of illustration, the following description corresponds to fabrication stages for the first particular embodiment of the vertical TFET device 100 described with respect to FIG. 1. However, the fabrication stages may be modified to fabricate the second embodiment, the third embodiment, or any other embodiments.

[0046] Referring to FIG. 3, a particular stage of fabricating the vertical tunnel field effect transistor device of FIG. 1 is shown. During the particular stage shown in FIG. 3, a first photoresist 302 may be patterned on top of the substrate 102. For example, the first photoresist 302 may be patterned to select (e.g., expose) a particular area of the substrate 102 to implant the first vertical TFET 110. After patterning the first photoresist 302, the first vertical TFET 110 may be implanted.

[0047] Implanting the first vertical TFET 110 may include implanting the first well region 104 in the substrate 102 using ion implantation 304. For example, n-type implantation may be performed in the substrate 102 to create the first well region 104. After the first well region 104 is implanted in the substrate 102, the first base portion 112 may be implanted in the first well region 104 using ion implantation 304. For example, P+ implantation may be performed in the first well region 104 to create the first base portion 112. After the first base portion 112 is implanted in the first well region 104, the first central portion 114 may be implanted on top of the first base portion 112 using ion implantation 304. For example, P- implantation may be performed in the substrate 102 and on top of the first base portion 112 to create the first central portion 114. After the first central portion 114 is implanted on the first base portion 112, the first top portion 116 may be implanted on top of the first central portion 114 using ion implantation 304. For example, N+ implantation may be performed in the substrate 102 and on top of the first central portion 114 to create the first top portion 116.

[0048] After the first vertical TFET 110 is implanted, the first photoresist 302 may be removed. For example, the first photoresist 302 may be removed via photoresist stripping to prevent the substrate 102 and the first vertical TFET 110 from being subjected to chemicals used during removal. In a particular embodiment, the first photoresist may be removed via organic photoresist stripping, inorganic photoresist stripping, or dry photoresist stripping.

[0049] FIG. 3 illustrates implantation of the first vertical TFET 110 and FIG. 4 illustrates implantation of the second vertical TFET 120. During the particular stage shown in FIG. 4, a second photoresist 402 may be patterned on top of the substrate 102 and the first vertical TFET 110. For example, the second photoresist 402 may be patterned to select (e.g., expose) a particular area of the substrate 102 to implant the second vertical TFET 120. After patterning the second photoresist 402, the second vertical TFET 120 may be implanted.

[0050] Implanting the second vertical TFET 120 may include implanting the second well region 106 in the substrate 102 using ion implantation 404. For example, n-type implantation may be performed in the substrate 102 to create the second well region 106. After the second well region 106 is implanted in the substrate 102, the second base portion 122 may be implanted in the second well region 106 using ion implantation 404. For example, P+ implantation may be performed in the second well region 106 to create the second base portion 122. After the second base portion 122 is implanted in the second well region 106, the second central portion 124 may be implanted on top of the second base portion 122 using ion implantation 404. For example, P- implantation may be performed in the substrate 102 and on top of the second base portion 122 to create the second central portion 124. After the second central portion 124 is implanted on the second base portion 122, the second top portion 126 may be implanted on top of the second central portion 124 using ion implantation 404. For example, N+ implantation may be performed in the substrate 102 and on top of the second central portion 124 to create the second top portion 126.

[0051] After the second vertical TFET 120 is implanted, the second photoresist 402 may be removed. For example, the second photoresist 402 may be removed via photoresist stripping to prevent the substrate 102, the first vertical TFET 110, the

second vertical TFET 120, or any combination thereof, from being subjected to chemicals used during removal.

[0052] Referring to FIG. 5, another particular stage of fabricating the vertical tunnel field effect transistor device of FIG. 1 is shown. During the particular stage shown in FIG. 5, a first hard mask film 530 may be patterned on the first vertical TFET 110 and a second hard mask film 540 may be patterned on the second vertical TFET 120. For example, the first hard mask film 530 may be deposited on top of the first top portion 116 and the substrate 102. The second hard mask film 540 may be deposited on top of the second top portion 126 and the substrate 102. In a particular embodiment, the first hard mask film 530 and the second hard mask film 540 may be a single hard mask film deposited across the top of the vertical TFET device illustrated in FIG. 4 after the second photoresist 402 is removed.

[0053] The hard mask films 530, 540 may be patterned on top of the first top portion 116 and the second top portion 126, respectively, to protect areas beneath the hard mask films 530, 540 during etching. After patterning the hard mask films 530, 540, the first fin structure and the second fin structure may be etched from the substrate 102. For example, areas of the substrate 102 that are not protected by the hard mask films 530, 540 may be etched down to the well regions 104, 106.

[0054] Referring to FIG. 6, another particular stage of fabricating the vertical tunnel field effect transistor device of FIG. 1 is shown. During the particular stage shown in FIG. 6, the STI oxide layer 108 is deposited. For example, the STI oxide layer 108 may be deposited on the substrate 102, the well regions 104, 106, and the particular areas of the base portions 112, 122 that are not protected by the hard mask films 530, 540. The STI oxide layer 108 may be polished (e.g., via a chemical and mechanical polishing (CMP) process) and recess etched. After the STI oxide layer 108 is etched, the hard mask films 530, 540 may be removed.

[0055] Referring to FIG. 7, another particular stage of fabricating the vertical tunnel field effect transistor device of FIG. 1 is shown. During the particular stage, the material having a high dielectric constant (k) may be deposited on the first fin structure. In addition, the material having a high dielectric constant (k) may be deposited on the second fin structure in a similar fashion. A first gate material 718 (e.g., poly-silicon)

may be deposited and patterned around the first fin structure and a second gate material 728 (e.g., poly silicon) may be deposited and patterned around the second fin structure.

[0056] It will be appreciated that implanting and/or patterning a lightly doped drain (LDD) area may be bypassed by fabricating the vertical tunnel field effect transistor device. Fabricating the vertical tunnel field effect transistor may also relax a requirement for pattering the bottom of the base portions 112, 122 (e.g., source and/or drain regions).

[0057] Referring to FIG. 8, another particular stage of fabricating the vertical tunnel field effect transistor device of FIG. 1 is shown. During the particular stage, an inter-layer dielectric oxide 850 is deposited. After depositing the inter-layer dielectric oxide 850, a CMP process is performed on the inter-layer dielectric oxide 850 to smooth the surface of the inter-layer dielectric oxide 850. The first gate material 718 may be removed and an n-type metal gate may be deposited to create the first gate 118. The second gate material 728 may also be removed and a p-type metal gate may be deposited to create the second gate 128.

[0058] As a result, the first central portion 114 and the second central portion 124 may permit the formation of band-to-band tunneling currents in channels, where the lengths (L) of the channels are independent of the width of the gates 118, 128. The gates 118, 128 may be independently designed and/or adjusted to manage an amount of saturation current supported by the vertical TFETs 110, 120 without affecting the length (L) of the channels. The height of the central portions 114, 124 (e.g., the channel lengths) may also be designed independently of a lithography process used for designing the gates. For example, because the channel is vertical (as opposed to planar), the channel is not limited to a region or a location that is under a planar gate of a field effect transistor.

[0059] Referring to FIG. 9, a particular illustrative embodiment of a three-dimensional vertical tunnel field effect transistor device 900 is shown. The three-dimensional vertical TFET device 900 may correspond to the vertical TFET device 100 of FIG. 1.

[0060] The vertical TFET device 900 may include a first contact 902 coupled to the first base portion 112, a second contact 904 coupled to the first top portion 116, and a third contact 906 coupled to the first gate 118. Voltages applied to each portion 112, 116,

118 via the respective contacts 902-906 may cause the first vertical tunneling current to flow between the first top portion 116 and the first base portion 112 via a channel in the first central portion 114, as described with respect to FIG. 1. The vertical TFET device 900 may also include a fourth contact 908 coupled to the second base portion 122, a fifth contact 910 coupled to the second top portion 126, and a sixth contact 912 coupled to the second gate 128. Voltages applied to each portion 122, 126, 128 via the respective contacts 908-912 may cause the second vertical tunneling current to flow between the second top portion 126 and the second base portion 122 via a channel in the second central portion 124.

[0061] Referring to FIG. 10, a particular illustrative embodiment of a method 1000 of fabricating a vertical tunnel field effect transistor device is shown. The method 1000 of FIG. 10 may be performed to fabricate embodiments of the vertical TFET devices depicted in FIGs. 1-9.

[0062] The method 1000 includes forming a well region, a base portion, a central portion, and a top portion within a substrate, at 1002. For example, in FIG. 3, n-type implantation may be performed in the substrate 102 to create the first well region 104. After the first well region 104 is formed in the substrate 102, the first base portion 112 may be formed in the first well region 104 using ion implantation 304. For example, P+ implantation may be performed in the first well region 104 to create the first base portion 112. The first base portion 112 may protrude from a surface of the first well region 104. After the first base portion 112 is formed in the first well region 104, the first central portion 114 may be formed on top of the first base portion 112 using ion implantation 304. For example, P- implantation may be performed in the substrate 102 and on top of the first base portion 112 to create the first central portion 114. After the first central portion 114 is formed on the first base portion 112, the first top portion 116 may be formed on top of the first central portion 114 using ion implantation 304. For example, N+ implantation may be performed in the substrate 102 and on top of the first central portion 114 to create the first top portion 116.

[0063] A vertical fin structure may be etched, at 1004. For example, in FIG. 5, the hard mask films 530, 540 may be patterned on top of the first top portion 116 and the second top portion 126, respectively, to protect areas beneath the hard mask films 530, 540

during etching. After patterning the hard mask film 530, the first fin structure may be etched. For example, areas that are not protected by the hard mask films 530, 540 may be etched down to the well regions 104, 106. The remaining areas that are protected (e.g., underneath) the hard mask films 530, 540 may correspond to the first vertical fin structure.

[0064] A shallow trench isolation (STI) oxide layer may be formed between the vertical fin structure and a second vertical fin structure, at 1006. For example, in FIG. 6, the STI oxide film 108 may be formed between the structure corresponding to the first vertical TFET 110 and the structure corresponding to the second vertical TFET 120. The STI oxide film 108 may be formed on top of the hard mask films 530, 540 and on top of the top portions 116, 126. A CMP process for planarization may be performed until the hard mask films 530, 540 are reached. A recess etch may be performed and the hard mask films 530, 540 may be removed. The STI oxide layer 108 may be located on top of the surface 103 and between the base portions 112, 122 to isolate the vertical TFETs 110, 120.

[0065] A dielectric layer may be deposited on the vertical fin structure, at 1008. For example, in FIG. 7, the material having the high dielectric constant (k) may be deposited on the first fin structure. The first pair of sidewalls 117 may correspond to a dielectric layer. A first gate material may be deposited on the dielectric layer, at 1010. For example, in FIG. 7, the first gate material 718 (e.g., poly-silicon) may be deposited and patterned around the first pair of sidewalls 117.

[0066] In a particular embodiment, the method 1000 may include patterning a photoresist on the substrate prior to implanting the well region, the base portion, the central portion, and the top portion. For example, referring to FIG. 3, the first photoresist 302 is patterned on top of the substrate 102. For example, the first photoresist 302 may be patterned to select (e.g., expose) a particular area of the substrate 102 to implant the first vertical TFET 110. After patterning the first photoresist 302, the first vertical TFET 110 may be implanted.

[0067] In a particular embodiment, the method 1000 may include depositing a hard mask film on the top portion. For example, referring to FIG. 5, the first hard mask film 530 may be deposited on top of the first top portion 116 and the substrate 102, and the

second hard mask film 540 may be deposited on top of the second top portion 126 and the substrate 102. In a particular embodiment, the first hard mask film 530 and the second hard mask film 540 may be a single hard mask film deposited across the top of the vertical TFET device illustrated in FIG. 4 after the second photoresist 402 is removed.

[0068] In a particular embodiment, the method 1000 may include patterning the hard mask film prior to etching the vertical fin structure from the substrate. For example, referring to FIG. 5, the hard mask films 530, 540 may be patterned on top of the first top portion 116 and the second top portion 126, respectively, to protect areas beneath the hard mask films 530, 540 during etching. After patterning the hard mask films 530, 540, the first fin structure and the second fin structure may be etched. For example, areas that are not protected by the hard mask films 530, 540 may be etched down to the well regions 104, 106.

[0069] In a particular embodiment, the method 1000 may include forming an oxide layer. For example, referring to FIG. 6, the STI oxide layer 108 may be deposited on the substrate 102 (on the well regions 104, 106 and on the particular areas of the base portions 112, 122 that are not protected by the hard mask films 530, 540). The STI oxide layer 108 may be polished using a chemical and mechanical polishing (CMP) process and etched. After the STI oxide layer 108 is etched, the hard mask films 530, 540 may be removed.

[0070] In a particular embodiment, the method 1000 may include depositing an inter-layer dielectric oxide on the first gate material. For example, referring to FIG. 8, the inter-layer dielectric oxide 850 may be deposited on the first gate material 718 and on the STI oxide layer 108. After depositing the inter-layer dielectric oxide 850, a CMP process is performed on the inter-layer dielectric oxide 850 to smooth the surface of the inter-layer dielectric oxide 850.

[0071] In a particular embodiment, the method 1000 may include removing the first gate material and depositing a gate metal. For example, referring to FIG. 8, the first gate material 718 may be removed and an n-type metal gate may be deposited to create the first gate 118. The second gate material 728 may also be removed and a p-type metal gate may be deposited to create the second gate 128.

[0072] As a result, the first central portion 114 and the second central portion 124 may permit the formation of band-to-band tunneling currents in channels, where the lengths (L) of the channels are independent of the width of the gates 118, 128. The gates 118, 128 may be independently designed and/or adjusted to manage an amount of saturation current supported by the vertical TFETs 110, 120 without affecting the length (L) of the channels. The height of the central portions 114, 124 (e.g., the channel lengths) may also be designed independently of a lithography process used for designing the gates. For example, because the channel is vertical (as opposed to planar), the channel is not limited to a region or a location that is under a planar gate of a field effect transistor.

[0073] Referring to FIG. 11, a block diagram of a particular illustrative embodiment of a wireless communication device is depicted and generally designated 1100. The device 1100 includes a processor 1110, such as a digital signal processor (DSP), coupled to a memory 1132 (e.g., a random access memory (RAM), flash memory, read-only memory (ROM), programmable read-only memory (PROM), erasable programmable read-only memory (EPROM), electrically erasable programmable read-only memory (EEPROM), registers, hard disk, a removable disk, a compact disc read-only memory (CD-ROM), or any other form of non-transient storage medium known in the art). The memory 1132 may store instructions 1162 that are executable by the processor 1110. The memory 1132 may store data 1166 that is accessible to the processor 1110.

[0074] The device 1100 includes a vertical tunnel field effect transistor device 1148. In an illustrative embodiment, the vertical tunnel field effect transistor device 1148 may correspond to the vertical tunnel field transistor devices depicted in FIGs. 1-9. The vertical tunnel field effect transistor device 118 may be used to form logic circuits in the processor 1110, other components (e.g., the display controller 1126, the wireless controller 1140, and/or a coder/decoder (CODEC) 1126) of the device 1100, or any combination thereof. In a particular embodiment, the logic circuits may be used for power conservation techniques. FIG. 11 also shows a display controller 1126 that is coupled to the processor 1110 and to a display 1128. The CODEC 1134 may also be coupled to the processor 1110. A speaker 1136 and a microphone 1138 may be coupled to the CODEC 1134. FIG. 11 also indicates that a wireless controller 1140 may be coupled to the processor 1110 and may be further coupled to an antenna 1142 via the RF interface 1152.

[0075] In a particular embodiment, the processor 1110, the display controller 1126, the memory 1132, the CODEC 1134, and the wireless controller 1140 are included in a system-in-package or system-on-chip device 1122. In a particular embodiment, an input device 1130 and a power supply 1144 are coupled to the system-on-chip device 1122. Moreover, in a particular embodiment, as illustrated in FIG. 11, the display 1128, the input device 1130, the speaker 1136, the microphone 1138, the antenna 1142, and the power supply 1144 are external to the system-on-chip device 1122. However, each of the display 1128, the input device 1130, the speaker 1136, the microphone 1138, the wireless antenna 1142, and the power supply 1144 may be coupled to a component of the system-on-chip device 1122, such as an interface or a controller.

[0076] The foregoing disclosed devices and functionalities may be designed and configured into computer files (e.g. RTL, GDSII, GERBER, etc.) stored on computer readable media. Some or all such files may be provided to fabrication handlers who fabricate devices based on such files. Resulting products include semiconductor wafers that are then cut into semiconductor die and packaged into a semiconductor chip. The semiconductor chips are then integrated into electronic devices, as described further with reference to FIG. 12.

[0077] Referring to FIG. 12, a particular illustrative embodiment of an electronic device manufacturing process is depicted and generally designated 1200. Physical device information 1202 is received at the manufacturing process 1200, such as at a research computer 1206. The physical device information 1202 may include design information representing at least one physical property of a semiconductor device, such as a vertical tunnel field effect transistor device (e.g., the vertical tunnel field effect transistor devices illustrated in FIGs. 1-9 and/or a vertical tunnel field effect transistor device formed according to the method 1000 of FIG. 10). For example, the physical device information 1202 may include physical parameters, material characteristics, and structure information that is entered via a user interface 1204 coupled to the research computer 1206. The research computer 1206 includes a processor 1208, such as one or more processing cores, coupled to a computer readable medium such as a memory 1210. The memory 1210 may store computer readable instructions that are executable to cause the processor 1208 to transform the physical device information 1202 to comply with a file format and to generate a library file 1212.

[0078] In a particular embodiment, the library file 1212 includes at least one data file including the transformed design information. For example, the library file 1212 may include a library of devices including a vertical tunnel field effect transistor device (e.g., the vertical tunnel field effect transistor devices illustrated in FIGs. 1-9 and/or a vertical tunnel field effect transistor device formed according to the method 1000 of FIG. 10) provided for use with an electronic design automation (EDA) tool 1220.

[0079] The library file 1212 may be used in conjunction with the EDA tool 1220 at a design computer 1214 including a processor 1216, such as one or more processing cores, coupled to a memory 1218. The EDA tool 1220 may be stored as processor executable instructions at the memory 1218 to enable a user of the design computer 1214 to design a vertical tunnel field effect transistor device (e.g., the vertical tunnel field effect transistor devices illustrated in FIGs. 1-9 and/or a vertical tunnel field effect transistor device formed according to the method 1000 of FIG. 10) using the library file 1212. For example, a user of the design computer 1214 may enter circuit design information 1222 via a user interface 1224 coupled to the design computer 1214. The circuit design information 1222 may include design information representing at least one physical property of a vertical tunnel field effect transistor device (e.g., the vertical tunnel field effect transistor devices illustrated in FIGs. 1-9 and/or a vertical tunnel field effect transistor device formed according to the method 1000 of FIG. 10). To illustrate, the circuit design property may include identification of particular circuits and relationships to other elements in a circuit design, positioning information, feature size information, interconnection information, or other information representing a physical property of a semiconductor device.

[0080] The design computer 1214 may be configured to transform the design information, including the circuit design information 1222, to comply with a file format. To illustrate, the file formation may include a database binary file format representing planar geometric shapes, text labels, and other information about a circuit layout in a hierarchical format, such as a Graphic Data System (GDSII) file format. The design computer 1214 may be configured to generate a data file including the transformed design information, such as a GDSII file 1226 that includes information describing a vertical tunnel field effect transistor device (e.g., the vertical tunnel field effect transistor devices illustrated in FIGs. 1-9 and/or a vertical tunnel field effect transistor

device formed according to the method 1000 of FIG. 10) in addition to other circuits or information. To illustrate, the data file may include information corresponding to a system-on-chip (SOC) that includes a vertical tunnel field effect transistor device (e.g., the vertical tunnel field effect transistor devices illustrated in FIGs. 1-9 and/or a vertical tunnel field effect transistor device formed according to the method 1000 of FIG. 10), and that also includes additional electronic circuits and components within the SOC.

[0081] The GDSII file 1226 may be received at a fabrication process 1228 to manufacture a vertical tunnel field effect transistor device (e.g., the vertical tunnel field effect transistor devices illustrated in FIGs. 1-9 and/or a vertical tunnel field effect transistor device formed according to the method 1000 of FIG. 10), according to transformed information in the GDSII file 1226. For example, a device manufacture process may include providing the GDSII file 1226 to a mask manufacturer 1230 to create one or more masks, such as masks to be used with photolithography processing, illustrated as a representative mask 1232. The mask 1232 may be used during the fabrication process to generate one or more wafers 1234, which may be tested and separated into dies, such as a representative die 1236. The die 1236 includes a vertical tunnel field effect transistor device (e.g., the vertical tunnel field effect transistor devices illustrated in FIGs. 1-9 and/or a vertical tunnel field effect transistor device formed according to the method 1000 of FIG. 10).

[0082] In conjunction with the described embodiments, a non-transitory computer-readable medium stores instructions executable by a computer to perform the method 1000 of FIG. 10. For example, equipment of a semiconductor manufacturing plant may include a computer and a memory and may perform the method 1000 of FIG. 10, such as in connection with the fabrication process 1228 and using the GSDII file 1226. To illustrate, the computer may execute instructions to initiate fabrication of a vertical tunnel field effect transistor, as described with reference to FIGs. 2-8.

[0083] The die 1236 may be provided to a packaging process 1238 where the die 1236 is incorporated into a representative package 1240. For example, the package 1240 may include the single die 1236 or multiple dies, such as a system-in-package (SiP) arrangement. The package 1240 may be configured to conform to one or more

standards or specifications, such as Joint Electron Device Engineering Council (JEDEC) standards.

[0084] Information regarding the package 1240 may be distributed to various product designers, such as via a component library stored at a computer 1246. The computer 1246 may include a processor 1248, such as one or more processing cores, coupled to a memory 1250. A printed circuit board (PCB) tool may be stored as processor executable instructions at the memory 1250 to process PCB design information 1242 received from a user of the computer 1246 via a user interface 1244. The PCB design information 1242 may include physical positioning information of a packaged semiconductor device on a circuit board, the packaged semiconductor device corresponding to the package 1240 including a vertical tunnel field effect transistor device (e.g., the vertical tunnel field effect transistor devices illustrated in FIGs. 1-9 and/or a vertical tunnel field effect transistor device formed according to the method 1000 of FIG. 10).

[0085] The computer 1246 may be configured to transform the PCB design information 1242 to generate a data file, such as a GERBER file 1252 with data that includes physical positioning information of a packaged semiconductor device on a circuit board, as well as layout of electrical connections such as traces and vias, where the packaged semiconductor device corresponds to the package 1240 including a vertical tunnel field effect transistor device (e.g., the vertical tunnel field effect transistor devices illustrated in FIGs. 1-9 and/or a vertical tunnel field effect transistor device formed according to the method 1000 of FIG. 10). In other embodiments, the data file generated by the transformed PCB design information may have a format other than a GERBER format.

[0086] The GERBER file 1252 may be received at a board assembly process 1254 and used to create PCBs, such as a representative PCB 1256, manufactured in accordance with the design information stored within the GERBER file 1252. For example, the GERBER file 1252 may be uploaded to one or more machines to perform various steps of a PCB production process. The PCB 1256 may be populated with electronic components including the package 1240 to form a representative printed circuit assembly (PCA) 1258.

[0087] The PCA 1258 may be received at a product manufacture process 1260 and integrated into one or more electronic devices, such as a first representative electronic device 1262 and a second representative electronic device 1264. As an illustrative, non-limiting example, the first representative electronic device 1262, the second representative electronic device 1264, or both, may be selected from the group of a cellular phone, a wireless local area network (LAN) device, a set top box, a music player, a video player, an entertainment unit, a navigation device, a communications device, a personal digital assistant (PDA), a fixed location data unit, and a computer, into which a vertical tunnel field effect transistor device (e.g., the vertical tunnel field effect transistor devices illustrated in FIGs. 1-9 and/or a vertical tunnel field effect transistor device formed according to the method 1000 of FIG. 10) is integrated. As another illustrative, non-limiting example, one or more of the electronic devices 1262 and 1264 may be remote units such as mobile phones, hand-held personal communication systems (PCS) units, portable data units such as personal data assistants, global positioning system (GPS) enabled devices, navigation devices, fixed location data units such as meter reading equipment, or any other device that stores or retrieves data or computer instructions, or any combination thereof. Although FIG. 13 illustrates remote units according to teachings of the disclosure, the disclosure is not limited to these illustrated units. Embodiments of the disclosure may be suitably employed in any device which includes active integrated circuitry including memory and on-chip circuitry.

[0088] A device that includes a vertical tunnel field effect transistor device (e.g., the vertical tunnel field effect transistor devices illustrated in FIGs. 1-9 and/or a vertical tunnel field effect transistor device formed according to the method 1000 of FIG. 10) may be fabricated, processed, and incorporated into an electronic device, as described in the illustrative process 1200. One or more aspects of the embodiments disclosed with respect to FIGs. 1-11 may be included at various processing stages, such as within the library file 1212, the GDSII file 1226, and the GERBER file 1252, as well as stored at the memory 1210 of the research computer 1206, the memory 1218 of the design computer 1214, the memory 1250 of the computer 1246, the memory of one or more other computers or processors (not shown) used at the various stages, such as at the board assembly process 1254, and also incorporated into one or more other physical

embodiments such as the mask 1232, the die 1236, the package 1240, the PCA 1258, other products such as prototype circuits or devices (not shown), or any combination thereof. Although various representative stages are depicted with reference to FIGs. 1-11 to fabricate a vertical tunnel field effect transistor device, in other embodiments fewer stages may be used or additional stages may be included. Similarly, the process 1200 of FIG. 12 may be performed by a single entity or by one or more entities performing various stages of the process 1200.

[0089] In conjunction with the described embodiments, an apparatus includes means for providing charge carriers to a tunneling region. For example, the means for providing the charge carriers may include the first base portion 112, the first top portion 116, the second base portion 122, and the second top portion 126 depicted in FIGs. 1-9.

[0090] The apparatus may also include means for receiving the charge carriers from the tunneling region. For example, the means for receiving the charge carriers may include the first base portion 112, the first top portion 116, the second base portion 122, and the second top portion 126 depicted in FIGs. 1-9.

[0091] The apparatus may also include means for biasing the tunneling channel to enable band-to-band tunneling at the tunneling channel. For example, the means for biasing the tunneling channel may include the contacts 902-912 of FIG. 9, the voltages applied to the contacts 902-912 of FIG. 9, the processor 1110 of FIG. 10, or any combination thereof.

[0092] Those of skill would further appreciate that the various illustrative logical blocks, configurations, modules, circuits, and algorithm steps described in connection with the embodiments disclosed herein may be implemented as electronic hardware, computer software executed by a processor, or combinations of both. Various illustrative components, blocks, configurations, modules, circuits, and steps have been described above generally in terms of their functionality. Whether such functionality is implemented as hardware or processor executable instructions depends upon the particular application and design constraints imposed on the overall system. Skilled artisans may implement the described functionality in varying ways for each particular application, but such implementation decisions should not be interpreted as causing a departure from the scope of the present disclosure.

[0093] The steps of a method or algorithm described in connection with the embodiments disclosed herein may be embodied directly in hardware, in a software module executed by a processor, or in a combination of the two. A software module may reside in random access memory (RAM), flash memory, read-only memory (ROM), programmable read-only memory (PROM), erasable programmable read-only memory (EPROM), electrically erasable programmable read-only memory (EEPROM), registers, hard disk, a removable disk, a compact disc read-only memory (CD-ROM), or any other form of non-transient storage medium known in the art. An exemplary storage medium is coupled to the processor such that the processor may read information from, and write information to, the storage medium. In the alternative, the storage medium may be integral to the processor. The processor and the storage medium may reside in an application-specific integrated circuit (ASIC). The ASIC may reside in a computing device or a user terminal. In the alternative, the processor and the storage medium may reside as discrete components in a computing device or user terminal.

[0094] The previous description of the disclosed embodiments is provided to enable a person skilled in the art to make or use the disclosed embodiments. Various modifications to these embodiments will be readily apparent to those skilled in the art, and the principles defined herein may be applied to other embodiments without departing from the scope of the disclosure. Thus, the present disclosure is not intended to be limited to the embodiments shown herein but is to be accorded the widest scope possible consistent with the principles and novel features as defined by the following claims.

CLAIMS:

1. A tunnel field effect transistor (TFET) device comprising:

a fin structure protruding from a substrate surface, the fin structure comprising:

a base portion proximate to the substrate surface, a top portion, and a first pair of sidewalls extending from the base portion to the top portion, the first pair of sidewalls having a length corresponding to a length of the fin structure;

a first doped region having a first dopant concentration at the base portion of the fin structure; and

a second doped region having a second dopant concentration at the top portion of the fin structure; and

a gate comprising a first conductive structure neighboring a first sidewall of the first pair of sidewalls, wherein a dielectric layer electrically isolates the first conductive structure from the first sidewall.

2. The TFET device of claim 1, wherein the gate further comprises a second conductive structure neighboring a second sidewall of the first pair of sidewalls, wherein the dielectric layer electrically isolates the second conductive structure from the second sidewall.

3. The TFET device of claim 2, wherein the gate further comprises a third conductive structure neighboring the top portion, wherein the dielectric layer electrically isolates the third conductive structure from the top portion, and wherein the third conductive structure is coupled to the first conductive structure and to the second conductive structure.

4. The TFET device of claim 1, wherein the fin structure further comprises a central portion between the base portion and the top portion.

5. The TFET device of claim 4, wherein the base portion, the top portion, and the central portion are comprised of a first type of material.

6. The TFET device of claim 5, wherein the first type of material is silicon.

7. The TFET device of claim 4, wherein the central portion corresponds to a channel region of the fin structure.

8. The TFET device of claim 7, wherein a channel length corresponds to a height of the central portion.

9. The TFET device of claim 1, wherein a saturation current is adjusted by changing a width of the gate.

10. The TFET device of claim 1, wherein the base portion corresponds to a drain of the fin structure and the top portion corresponds to a source of the fin structure.

11. The TFET device of claim 10, wherein the first dopant concentration includes an n-type concentration and the second dopant concentration includes a p-type concentration.

12. The TFET device of claim 10, wherein the first dopant concentration includes a p-type concentration and the second dopant concentration includes an n-type concentration.

13. The TFET device of claim 1, wherein the first doped region comprises a first material and the second doped region comprises a second material, and wherein the first material is different from the second material.

14. The TFET device of claim 1, wherein the base portion corresponds to a source of the fin structure and the top portion corresponds to a drain of the fin structure.

15. The TFET device of claim 14, wherein the first dopant concentration includes an n-type concentration and the second dopant concentration includes a p-type concentration.

16. The TFET device of claim 14, wherein the first dopant concentration includes a p-type concentration and the second dopant concentration includes an n-type concentration.

17. The TFET device of claim 1, integrated into at least one semiconductor die.

18. The TFET device of claim 1, integrated into a device selected from the group consisting of a communications device, a personal digital assistant (PDA), a navigation device, a fixed location data unit, a set top box, a music player, a video player, an entertainment unit, and a computer.

19. A method comprising:

fabricating a vertical tunnel field effect transistor (TFET) device, wherein

fabricating the vertical TFET device comprises:

forming a well region, a base portion, a central portion, and a top portion within a substrate, wherein the base portion protrudes from a surface of the well region, and wherein the central portion is formed between the base portion and the top portion;

etching the substrate to form a vertical fin structure, wherein the vertical fin structure includes the base portion, the central portion, and the top portion;

depositing a dielectric layer on the vertical fin structure; and

depositing a first gate material on the dielectric layer.

20. The method of claim 19, wherein the central portion corresponds to a channel region of the vertical TFET device.

21. The method of claim 19, wherein the base portion corresponds to a drain of the vertical TFET device and the top portion corresponds to a source of the vertical TFET device.

22. The method of claim 19, wherein the base portion corresponds to a source of the vertical TFET device and the base portion corresponds to a drain of the vertical TFET device.

23. The method of claim 19, wherein fabricating the vertical TFET device further comprises:

patterning photoresist on the substrate prior to implanting the well region, the base portion, the central portion, and the top portion; and

removing the photoresist to expose the top portion, wherein the photoresist is removed via photoresist stripping;

depositing a hard mask film on the top portion; and

patterning the hard mask film prior to etching the vertical fin structure from the substrate.

24. The method of claim 23, wherein fabricating the vertical TFET device further comprises:

forming an oxide layer; and

removing the hard mask film after forming the oxide layer and prior to depositing the dielectric layer on the vertical fin structure.

25. The method of claim 24, wherein forming the oxide layer includes:

depositing the oxide layer;

performing chemical and mechanical polishing (CMP) on the oxide layer; and

etching the oxide layer.

26. The method of claim 19, wherein fabricating the vertical TFET device further includes:

depositing an inter-layer dielectric oxide on the first gate material;

performing chemical and mechanical polishing (CMP) on the inter-layer dielectric oxide;

removing the first gate material;

depositing a gate metal; and

performing CMP on the gate metal.

27. The method of claim 19, wherein fabricating the vertical TFET device is initiated at a processor integrated into an electronic device.

28. A computer-readable storage medium comprising instructions that, when executed by a processor, cause the processor to:

initiate fabricating a vertical tunnel field effect transistor (TFET) device,

wherein fabricating the vertical TFET device comprises:

forming a well region, a base portion, a central portion, and a top portion within a substrate, wherein the base portion protrudes from a surface of the well region, and wherein the central portion is formed between the base portion and the top portion;

etching the substrate to form a vertical fin structure, wherein the vertical fin structure includes the base portion, the central portion, and the top portion;

depositing a dielectric layer on the vertical fin structure; and

depositing a first gate material on the dielectric layer.

29. The computer-readable storage medium of claim 28, wherein the central portion corresponds to a channel region of the vertical TFET device.

30. The computer-readable storage medium of claim 28, wherein the base portion corresponds to a drain of the vertical TFET device and top portion corresponds to a source of the vertical TFET device.

31. The computer-readable storage medium of claim 28, wherein the base portion corresponds to a source of the vertical TFET device and the base portion corresponds to a drain of the vertical TFET device.

32. The computer-readable storage medium of claim 28, wherein the processor is integrated into a device selected from the group consisting of a communications device, a personal digital assistant (PDA), a navigation device, a fixed location data unit, a set top box, a music player, a video player, an entertainment unit, and a computer.

33. A method comprising:

a step for forming a well region, a base portion, a central portion, and a top portion within a substrate, wherein the base portion protrudes from a surface of the well region, and wherein the central portion is formed between the base portion and the top portion;

a step for etching the substrate to form a vertical fin structure, wherein the vertical fin structure includes the base portion, the central portion, and the top portion;

a step for depositing a dielectric layer on the vertical fin structure; and

a step for depositing a first gate material on the dielectric layer.

34. The method of claim 33, wherein the step for implanting, the step for etching, the step for depositing the dielectric layer, and the step for depositing the first gate material are performed by a processor integrated into an electronic device.

35. A method comprising:

receiving a data file including design information corresponding to a semiconductor device; and

fabricating the semiconductor device according to the design information, wherein the semiconductor device includes:

a fin structure protruding from a substrate surface, the fin structure comprising:

a base portion proximate to the substrate surface, a top portion, and a first pair of sidewalls extending from the base portion to the top portion, the first pair of sidewalls having a length corresponding to a length of the fin structure;

a first doped region having a first dopant concentration at the base portion of the fin structure; and

a second doped region having a second dopant concentration at the top portion of the fin structure; and

a gate comprising a first conductive structure neighboring a first sidewall of the first pair of sidewalls, wherein a dielectric layer electrically isolates the first conductive structure from the first sidewall.

36. The method of claim 35, wherein the data file has a Graphic Data System (GDSII) format.

37. The method of claim 35, wherein the data file has a GERBER format.

38. An apparatus comprising:

means for providing charge carriers to a tunneling channel;

means for receiving the charge carriers from the tunneling channel, wherein one of the means for providing or the means for receiving is at a base portion of a fin structure and is adjacent to a substrate surface, and wherein the other of the means for providing or the means for receiving is at a top portion of the fin structure; and

means for biasing the tunneling channel to enable band-to-band tunneling at the tunneling channel.

39. The apparatus of claim 38, wherein the means for providing includes a source of the fin structure.

40. The apparatus of claim 38, wherein the means for receiving includes a drain of the fin structure.

41. The apparatus of claim 38, further comprising a device selected from the group consisting of a set top box, a music player, a video player, an entertainment unit, a navigation device, a communications device, a personal digital assistant (PDA), a fixed location data unit, and a computer, into which the means for providing, the means for receiving, and the means for biasing are integrated.

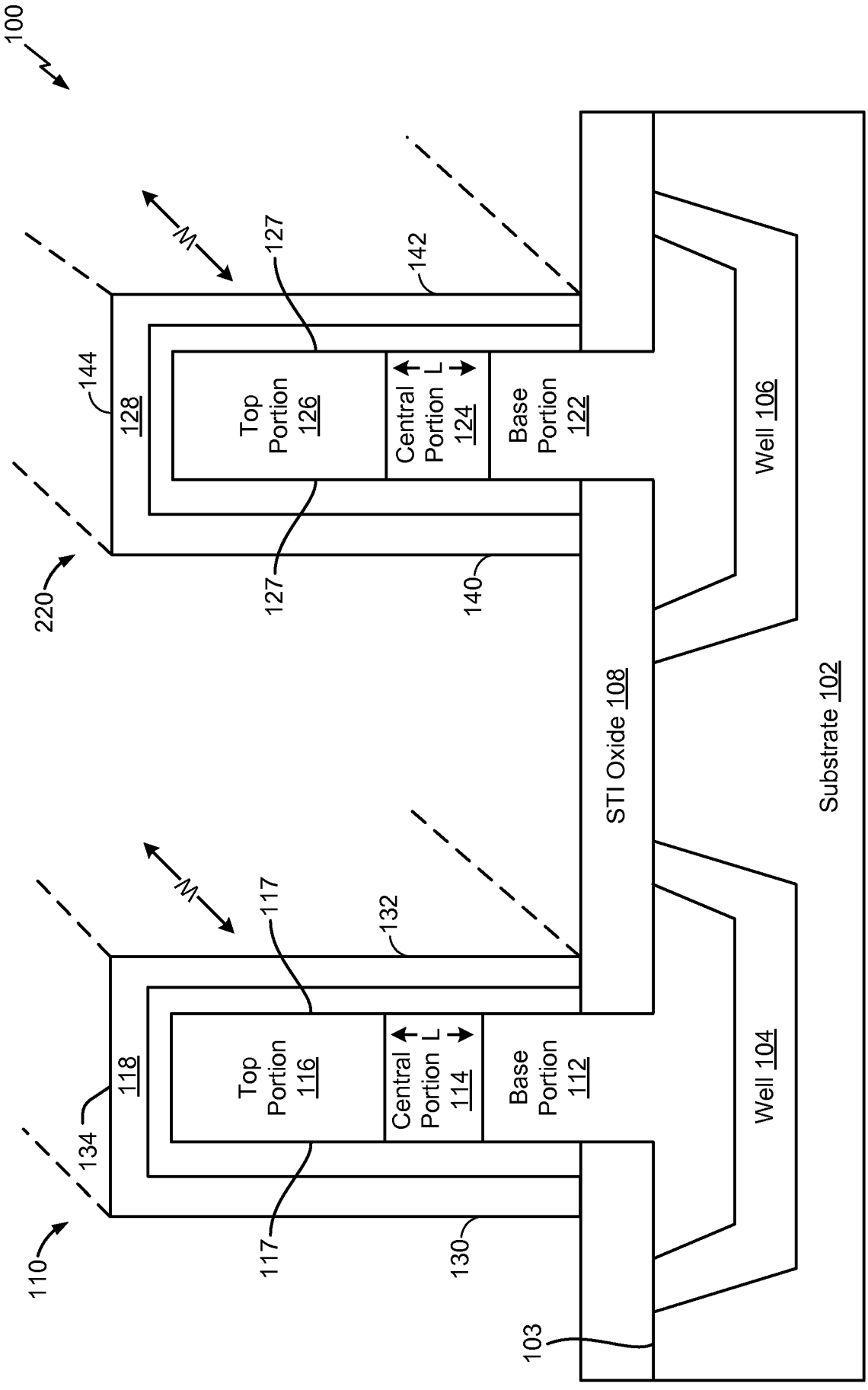
100
W
127
142
144
128
Top Portion 126
Central Portion L 124
Base Portion 122
Well 106
220
127
140
STI Oxide 108
Substrate 102
W
117
132
118
134
Top Portion 116
Central Portion L 114
Base Portion 112
Well 104
110
117
130
103

FIG. 1

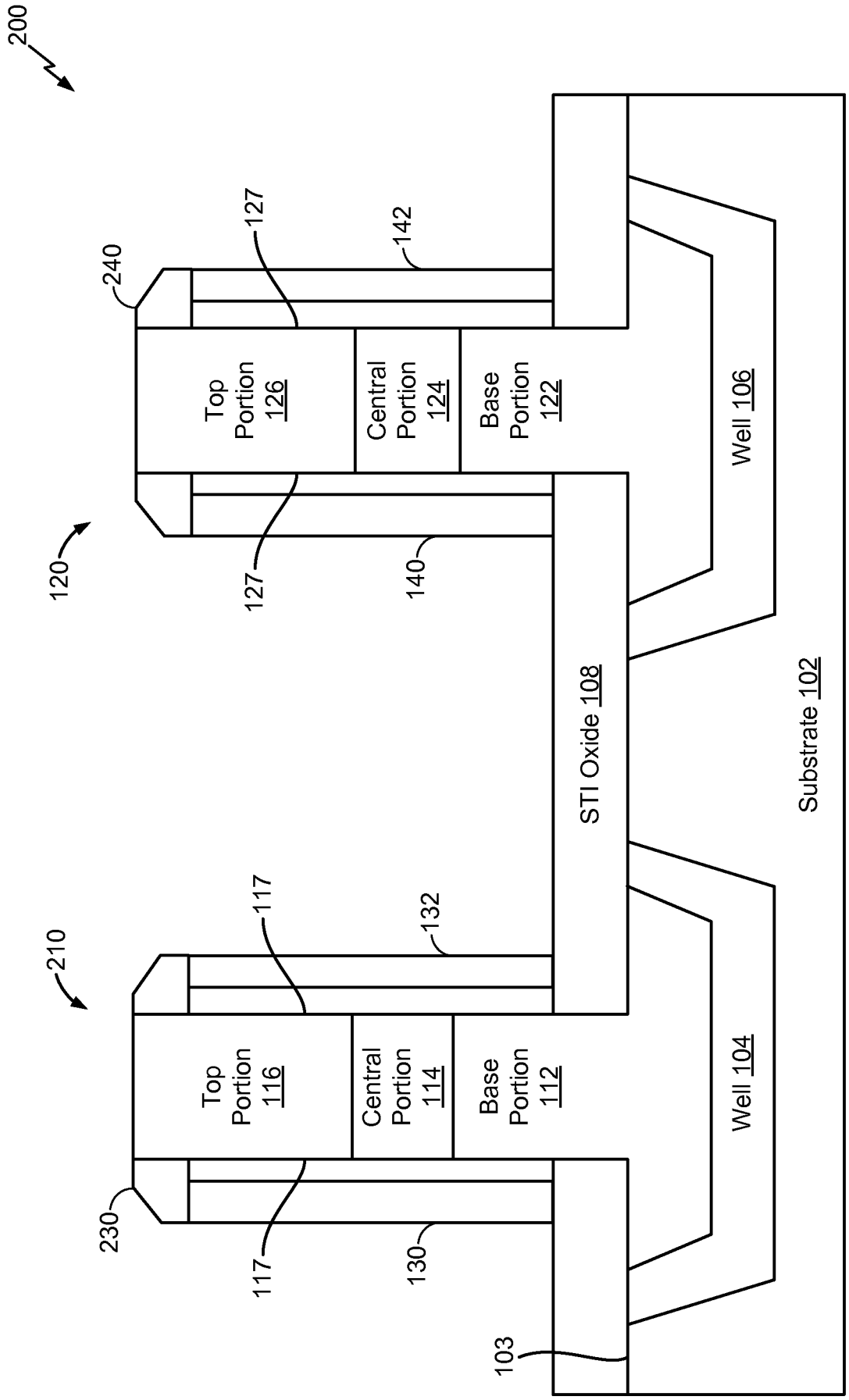
200
240
127
142
120
Top Portion 126
Central Portion 124
Base Portion 122
Well 106
127
140
STI Oxide 108
Substrate 102
210
117
132
Top Portion 116
Central Portion 114
Base Portion 112
Well 104
230
117
130
103

FIG. 2

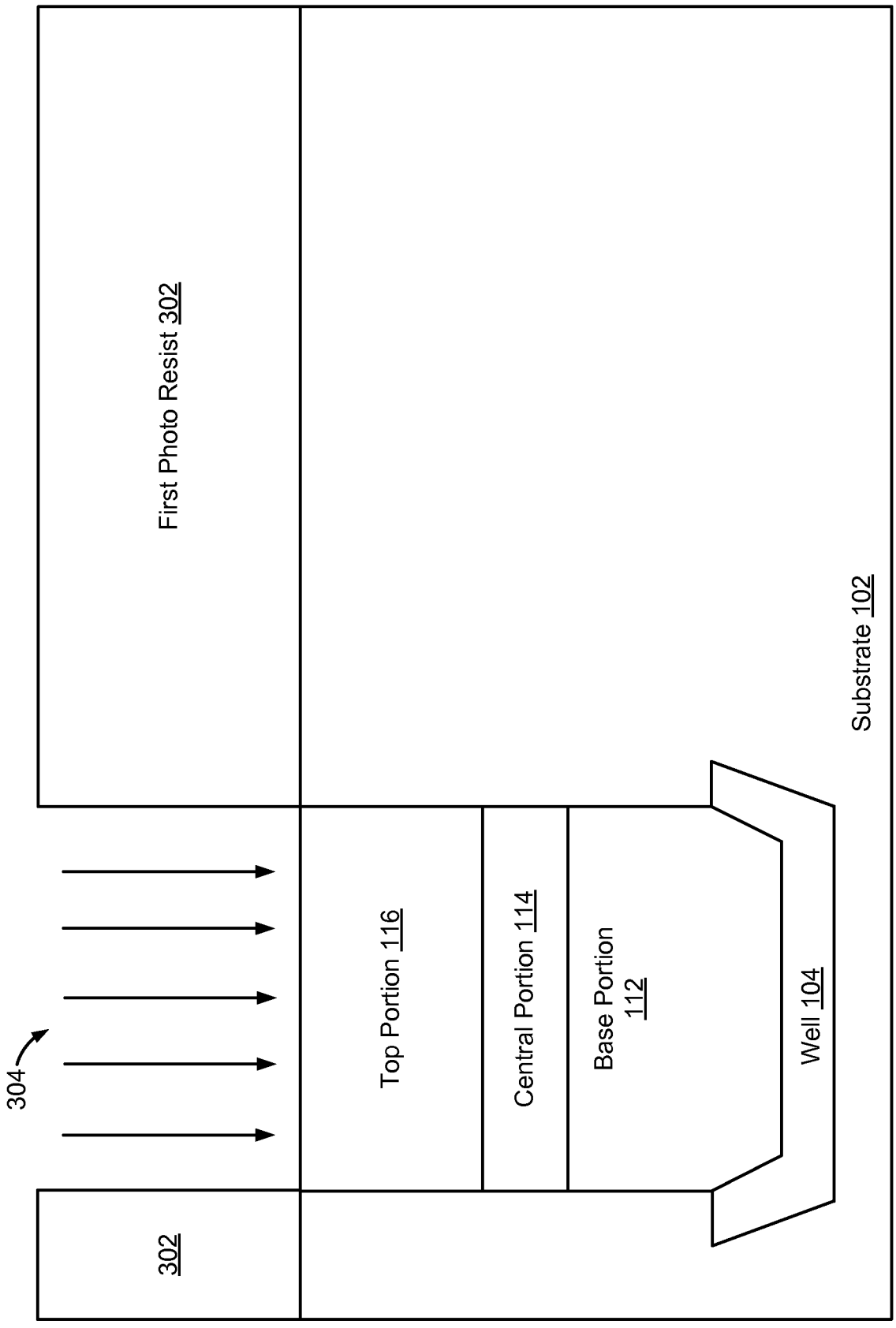
First Photo Resist 302
Substrate 102
304
302
Top Portion 116
Central Portion 114
Base Portion 112
Well 104

FIG. 3

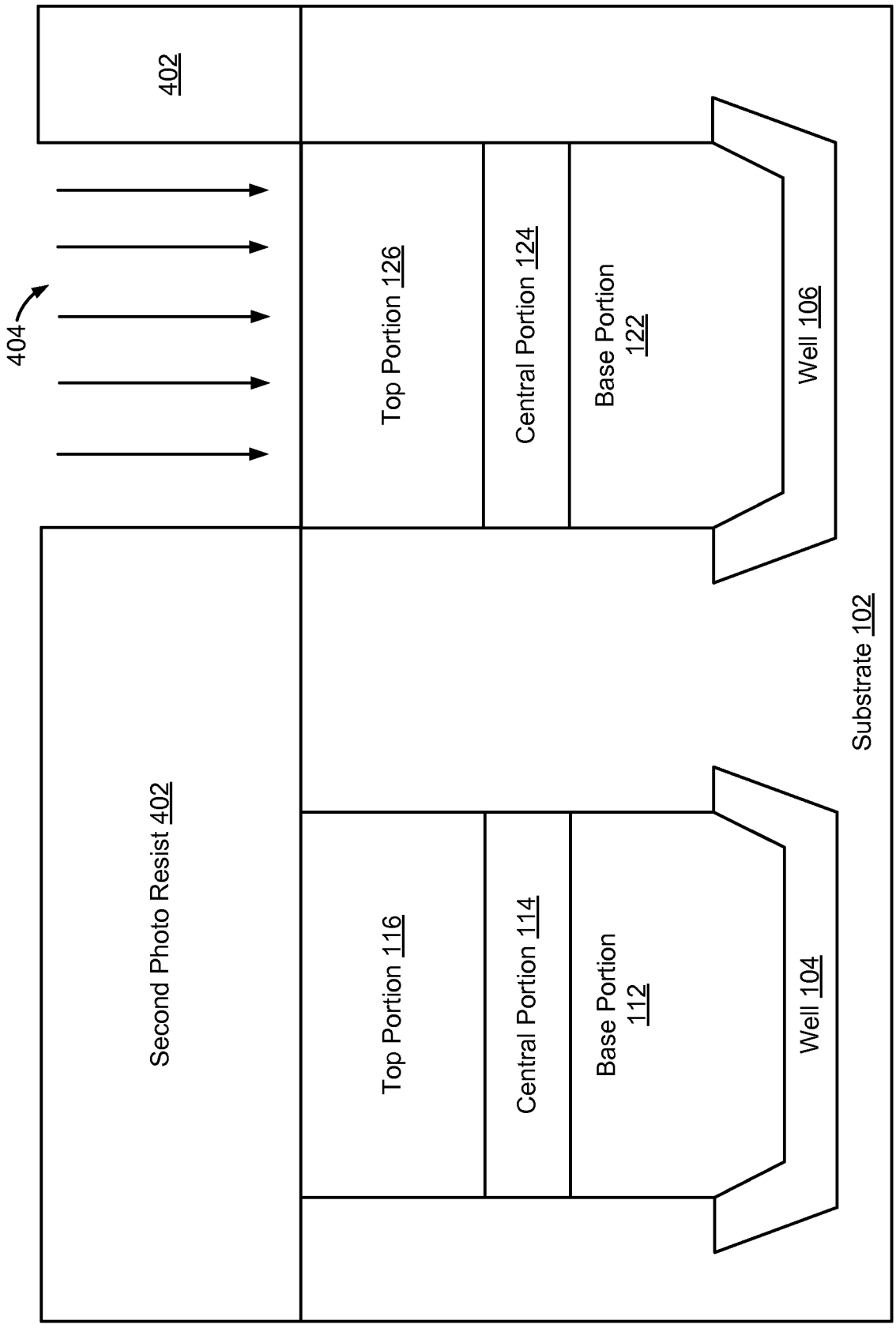
402
404
Top Portion 126
Central Portion 124
Base Portion 122
Well 106
Second Photo Resist 402
Substrate 102
Top Portion 116
Central Portion 114
Base Portion 112
Well 104

FIG. 4

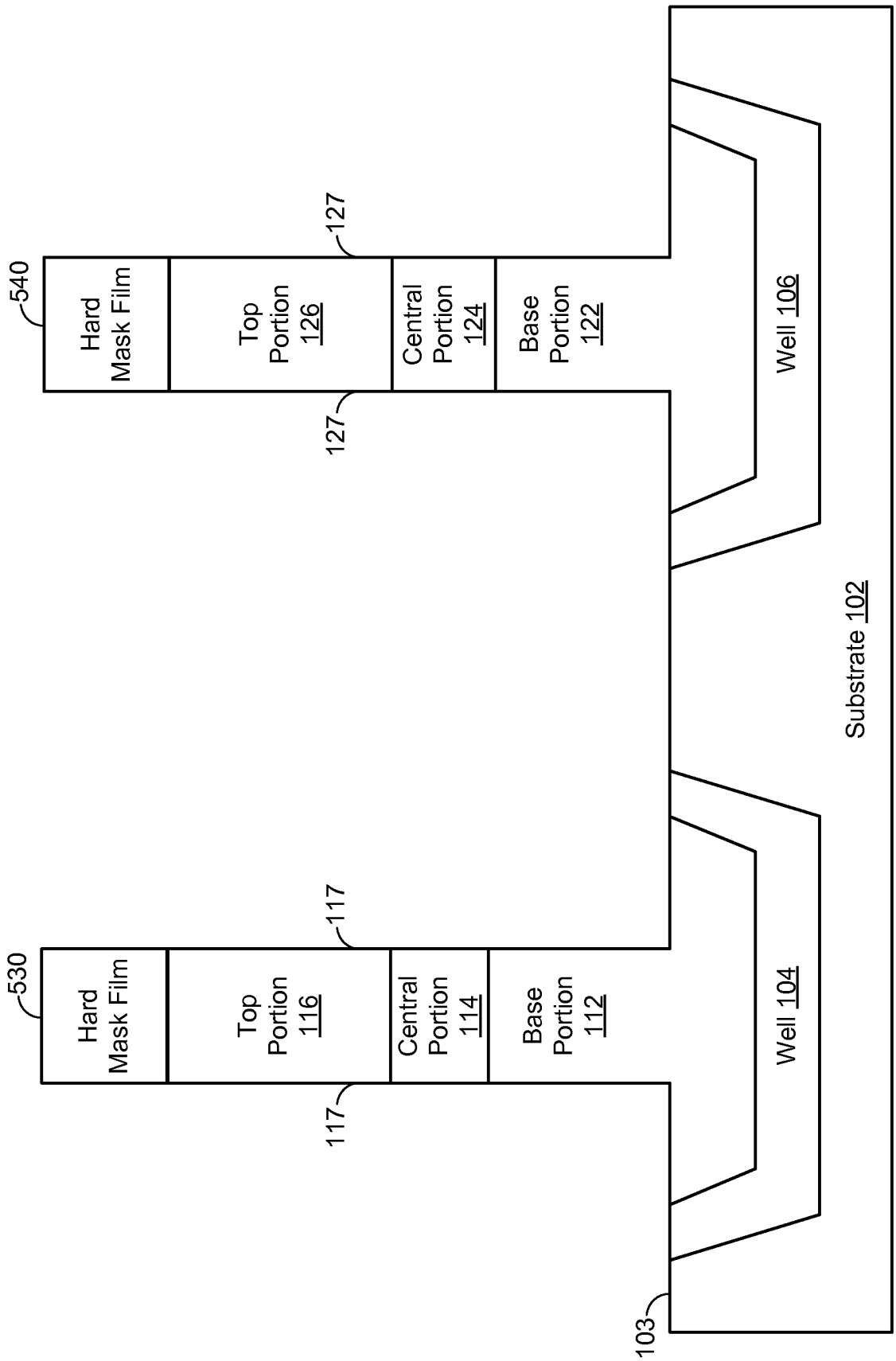
540
Hard Mask Film
Top Portion 126
127
Central Portion 124
Base Portion 122
Well 106
127
530
Hard Mask Film
Top Portion 116
117
Central Portion 114
Base Portion 112
Well 104
117
Substrate 102
103

FIG. 5

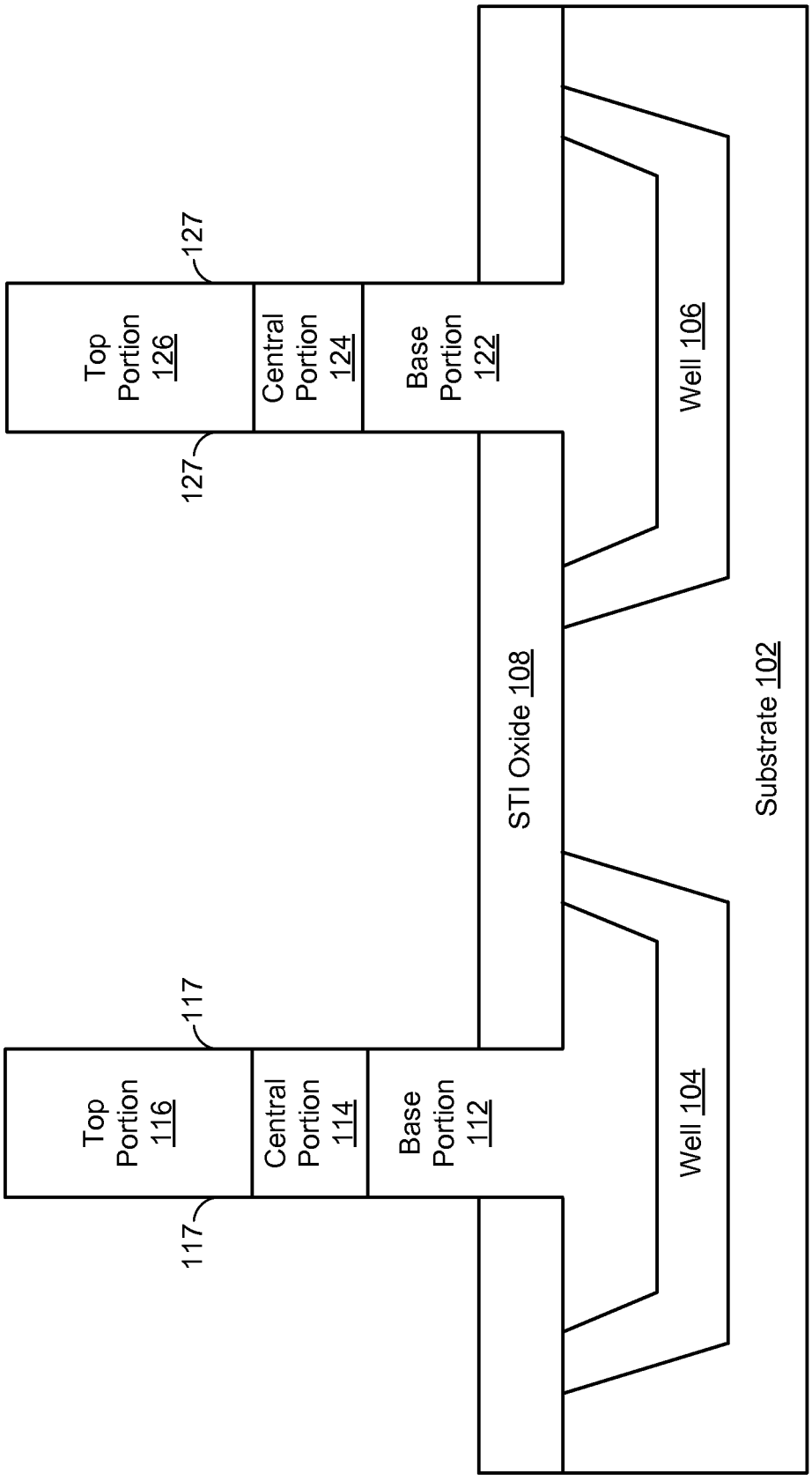
Top Portion 126
Central Portion 124
Base Portion 122
127
127
Well 106
STI Oxide 108
Substrate 102
Top Portion 116
Central Portion 114
Base Portion 112
117
117
Well 104

FIG. 6

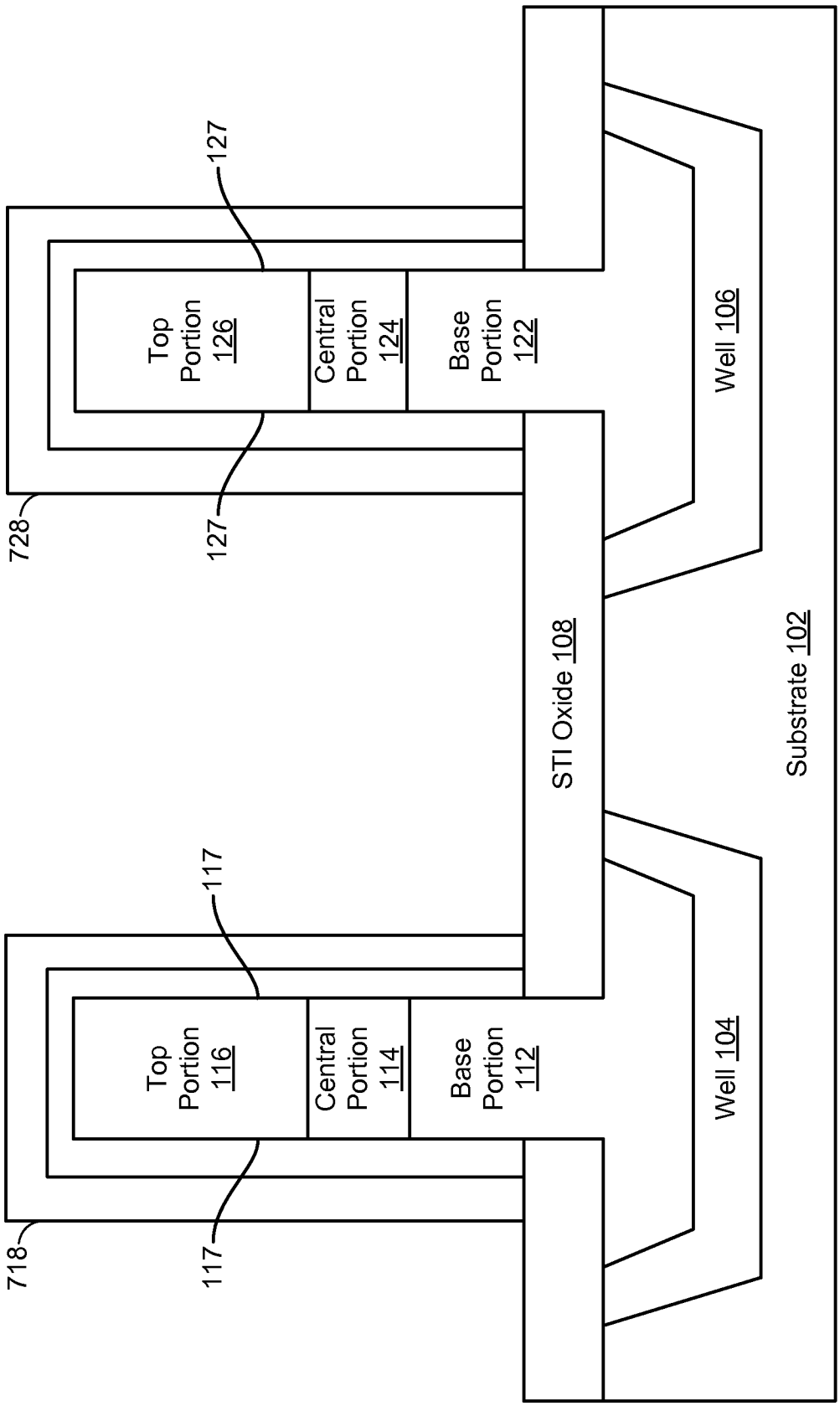
Top Portion 126
Central Portion 124
Base Portion 122
Well 106
127
127
728
STI Oxide 108
Substrate 102
Top Portion 116
Central Portion 114
Base Portion 112
Well 104
117
117
718

FIG. 7

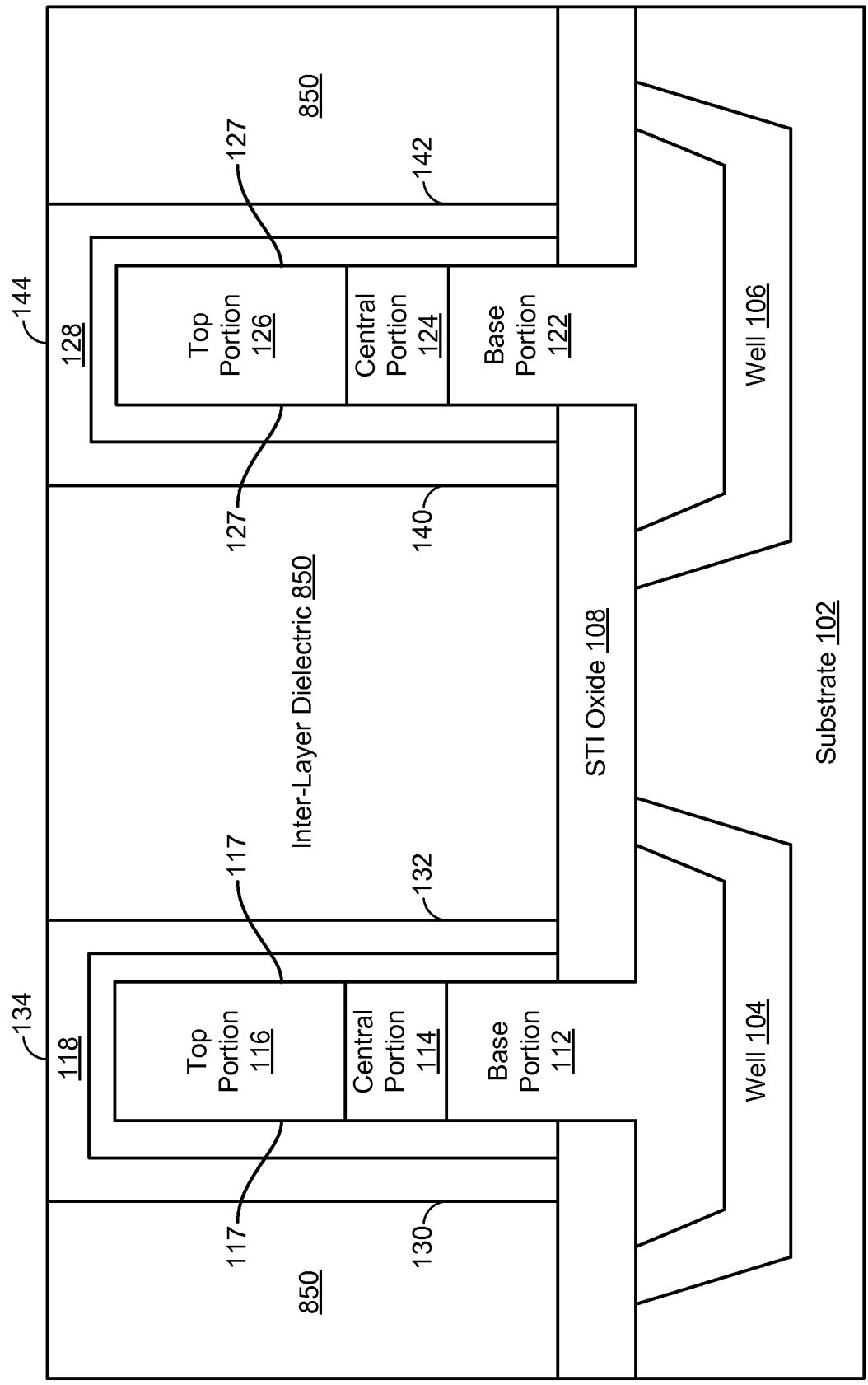
850
127
142
144
128
Top Portion 126
Central Portion 124
Base Portion 122
Well 106
127
140
Inter-Layer Dielectric 850
STI Oxide 108
Substrate 102
117
132
134
118
Top Portion 116
Central Portion 114
Base Portion 112
Well 104
117
130
850

FIG. 8

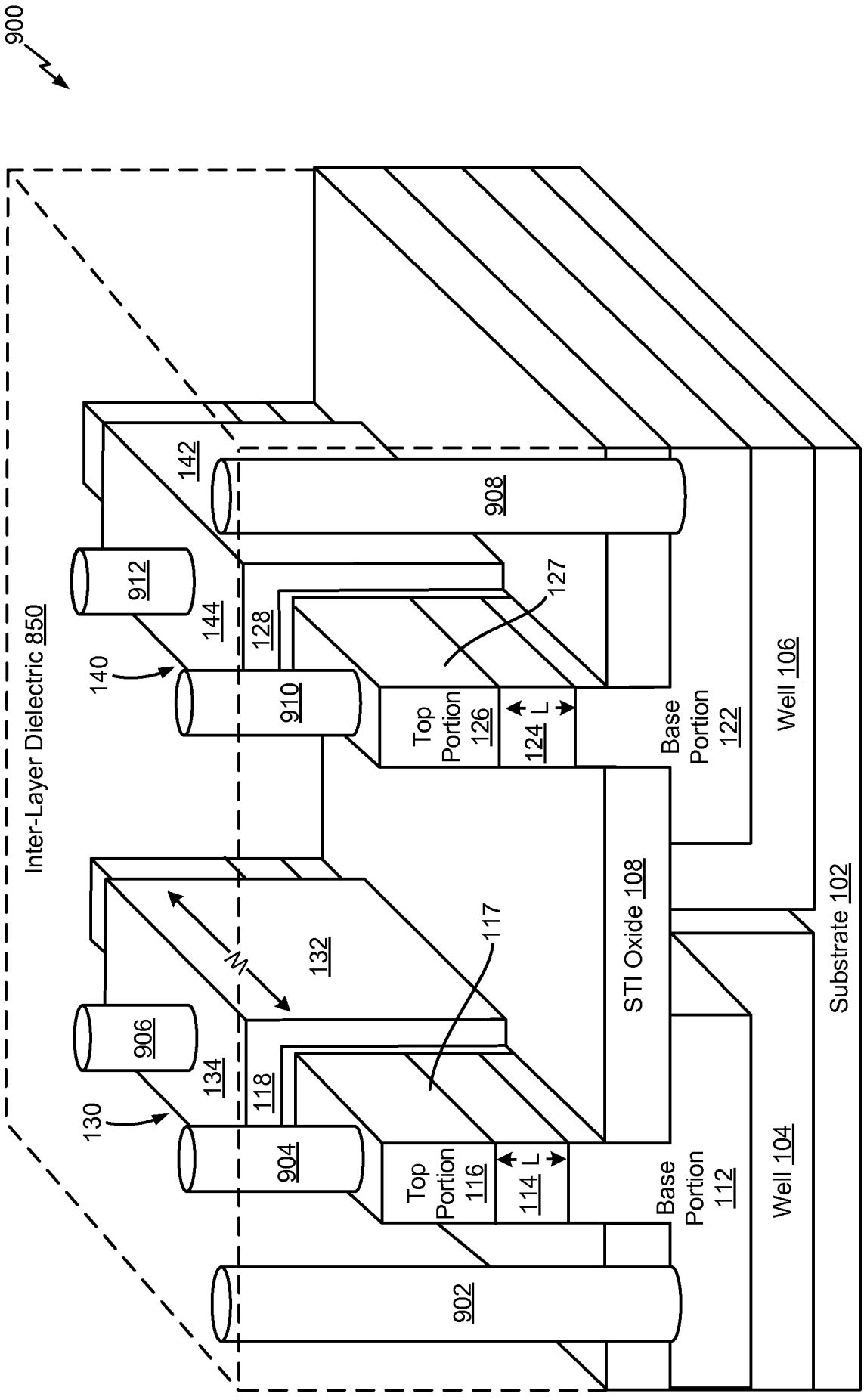
900
Inter-Layer Dielectric 850
142
908
912
144
128
127
140
910
Top Portion 126
124 L
Base Portion 122
Well 106
STI Oxide 108
W
132
117
906
134
118
130
904
Top Portion 116
114 L
Base Portion 112
Well 104
902
Substrate 102

FIG. 9

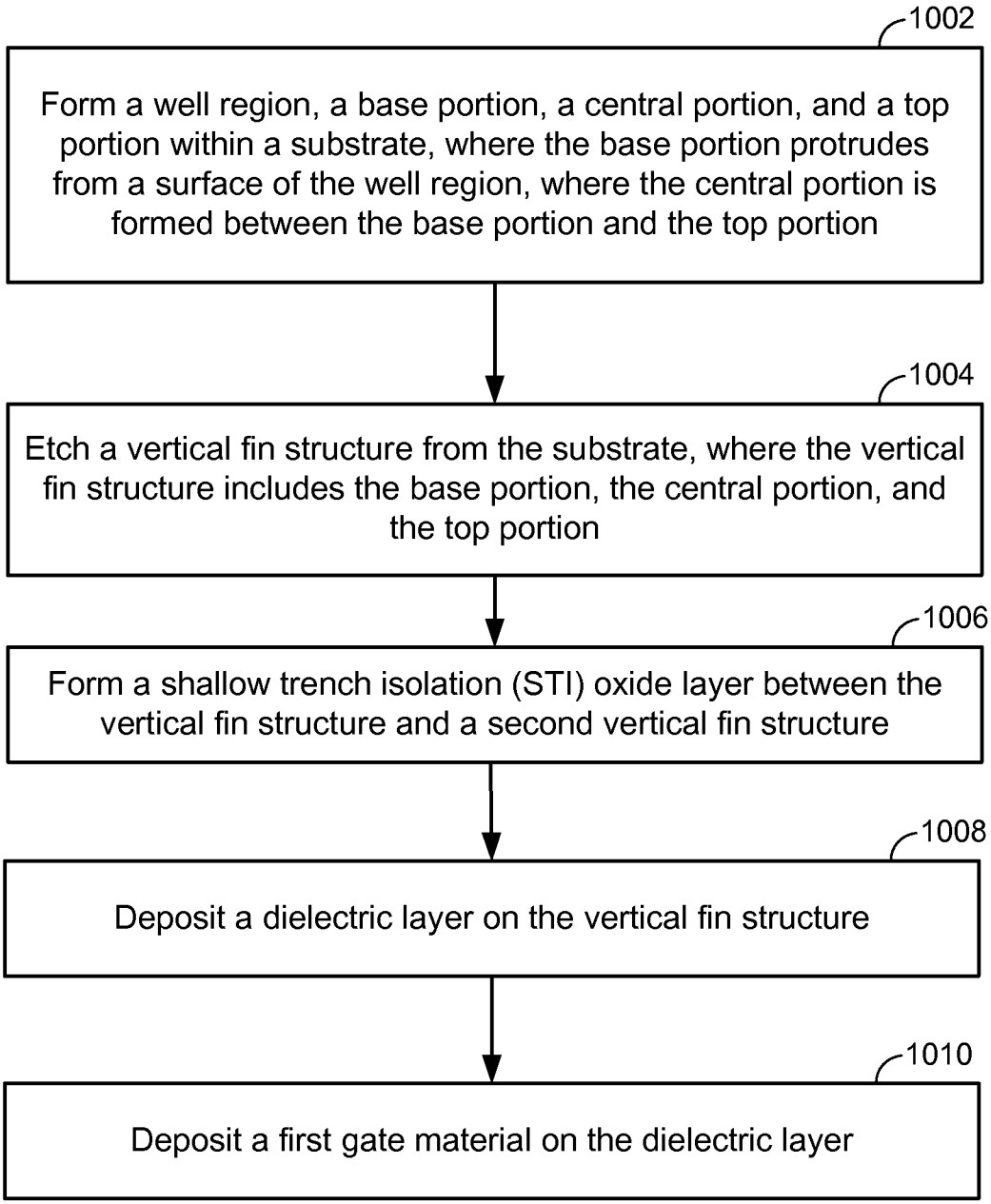
1002
Form a well region, a base portion, a central portion, and a top portion within a substrate, where the base portion protrudes from a surface of the well region, where the central portion is formed between the base portion and the top portion
1004
Etch a vertical fin structure from the substrate, where the vertical fin structure includes the base portion, the central portion, and the top portion
1006
Form a shallow trench isolation (STI) oxide layer between the vertical fin structure and a second vertical fin structure
1008
Deposit a dielectric layer on the vertical fin structure
1010
Deposit a first gate material on the dielectric layer

FIG. 10

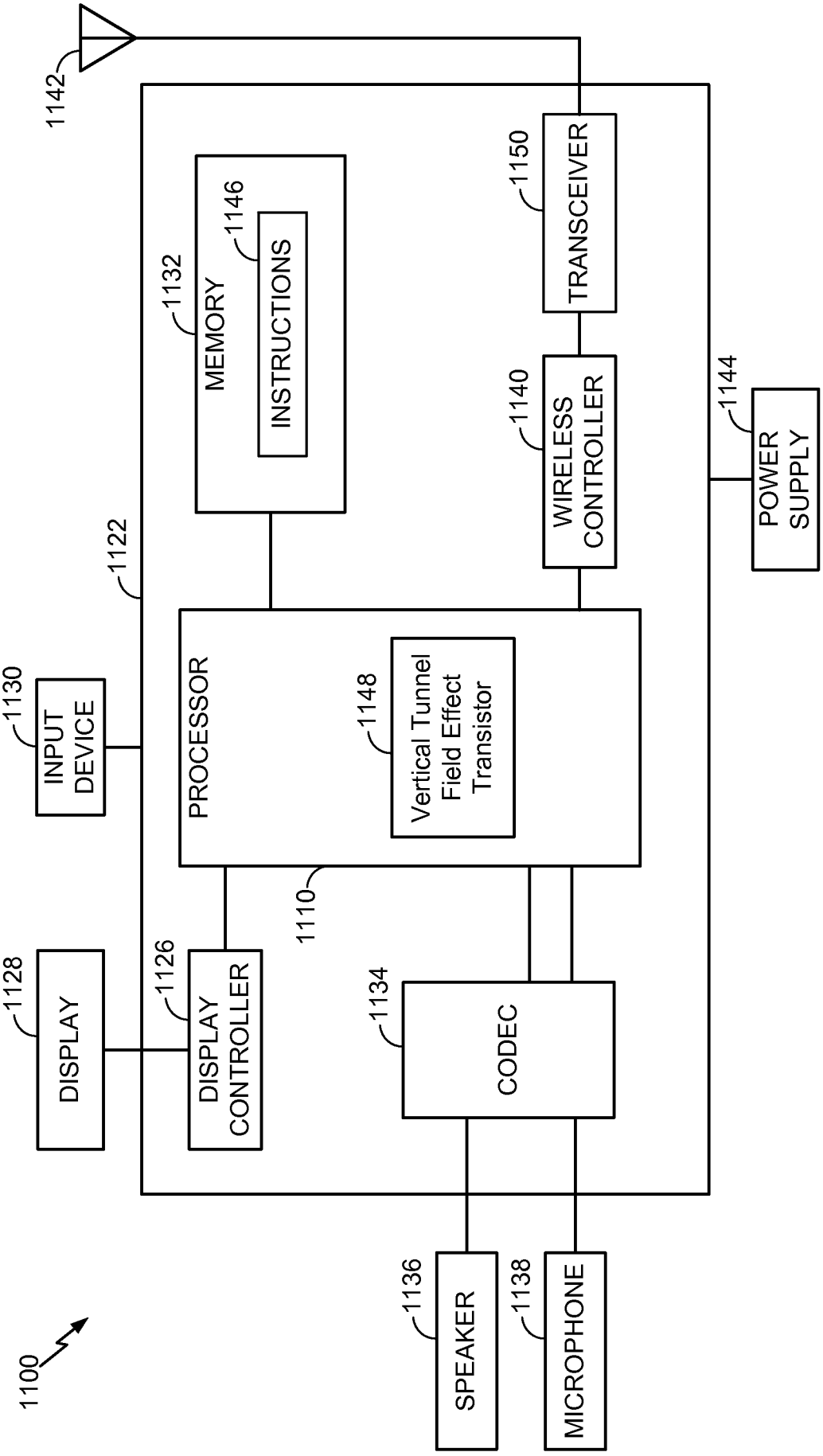
1142
1150
TRANSCEIVER
1146
INSTRUCTIONS
1132
MEMORY
1140
WIRELESS CONTROLLER
1144
POWER SUPPLY
1122
1130
INPUT DEVICE
PROCESSOR
1148
Vertical Tunnel Field Effect Transistor
1110
1128
DISPLAY
1126
DISPLAY CONTROLLER
1134
CODEC
1136
SPEAKER
1138
MICROPHONE
1100

FIG. 11

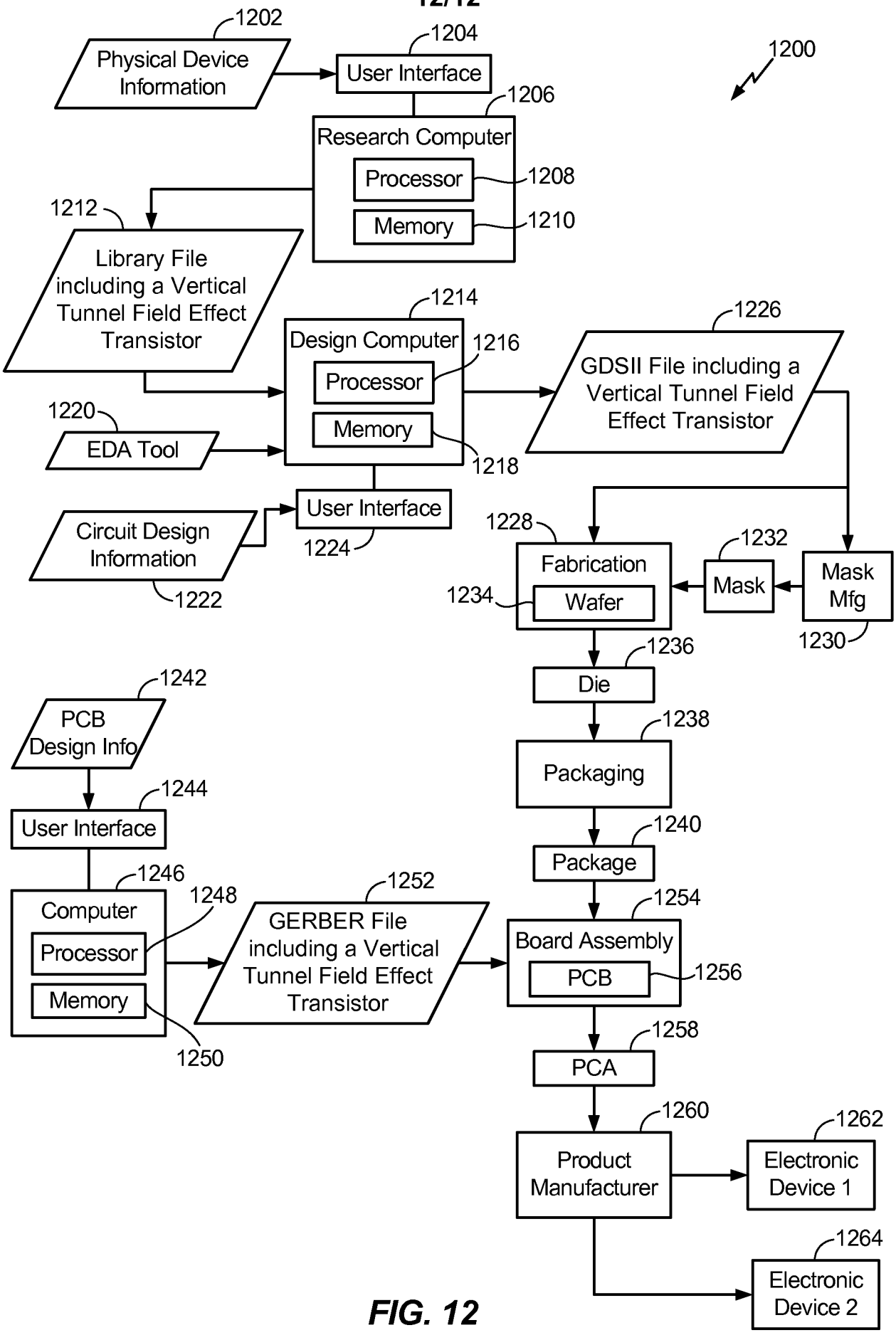
1202
Physical Device Information
1204
User Interface
1200
1206
Research Computer
Processor
1208
Memory
1210
1212
Library File including a Vertical Tunnel Field Effect Transistor
1214
Design Computer
1216
Processor
Memory
1218
1226
GDSII File including a Vertical Tunnel Field Effect Transistor
1220
EDA Tool
User Interface
1224
Circuit Design Information
1222
1228
Fabrication
Wafer
1234
1232
Mask
Mask Mfg
1230
1236
Die
1238
Packaging
1240
Package
1242
PCB Design Info
1244
User Interface
1246
Computer
Processor
Memory
1248
1250
1252
GERBER File including a Vertical Tunnel Field Effect Transistor
1254
Board Assembly
PCB
1256
1258
PCA
1260
Product Manufacturer
1262
Electronic Device 1
1264
Electronic Device 2

FIG. 12

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2014/054066

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L29/739 H01L29/66
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	EP 2 378 557 A1 (IMEC [BE]; UNIV LEUVEN KATH [BE]) 19 October 2011 (2011-10-19) paragraph [0040] - paragraph [0081] figures 1-17	1-22,26, 33,38-41 23-25, 27-32, 34-37

X Y A	US 2007/228491 A1 (FORBES LEONARD [US]) 4 October 2007 (2007-10-04) paragraph [0038] - paragraph [0045] paragraph [0081] figures 6,7,21	1-18, 38-41 35-37 19-34

X Y A	DE 199 43 390 A1 (HANSCH WALTER [DE]) 3 May 2001 (2001-05-03) column 4, line 25 - column 5, line 49 figures 5a-5d	1-18, 38-41 35-37 19-34

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[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
26 November 2014	03/12/2014

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Kostrzewa, Marek

1

Form PCT/ISA/210 (second sheet) (April 2005)

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2014/054066

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2009/121263 A1 (HIKIDA SATOSHI [JP]) 14 May 2009 (2009-05-14) paragraph [0010] paragraph [0044] - paragraph [0077] figures 1A-5B -----	23-25
Y	US 2012/278777 A1 (LIN YI-TANG [TW] ET AL) 1 November 2012 (2012-11-01) paragraph [0003] - paragraph [0004] paragraph [0068] - paragraph [0095] figures 10-13 -----	27-32, 34-37

1

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2014/054066

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP 2378557 A1	19-10-2011	EP 2378557 A1	19-10-2011
		JP 5542728 B2	09-07-2014
		JP 2011238909 A	24-11-2011
		US 2011253981 A1	20-10-2011
US 2007228491 A1	04-10-2007	NONE	
DE 19943390 A1	03-05-2001	NONE	
US 2009121263 A1	14-05-2009	JP 4746600 B2	10-08-2011
		JP 2009111305 A	21-05-2009
		US 2009121263 A1	14-05-2009
US 2012278777 A1	01-11-2012	CN 102779201 A	14-11-2012
		US 2012278777 A1	01-11-2012
		US 2014215420 A1	31-07-2014