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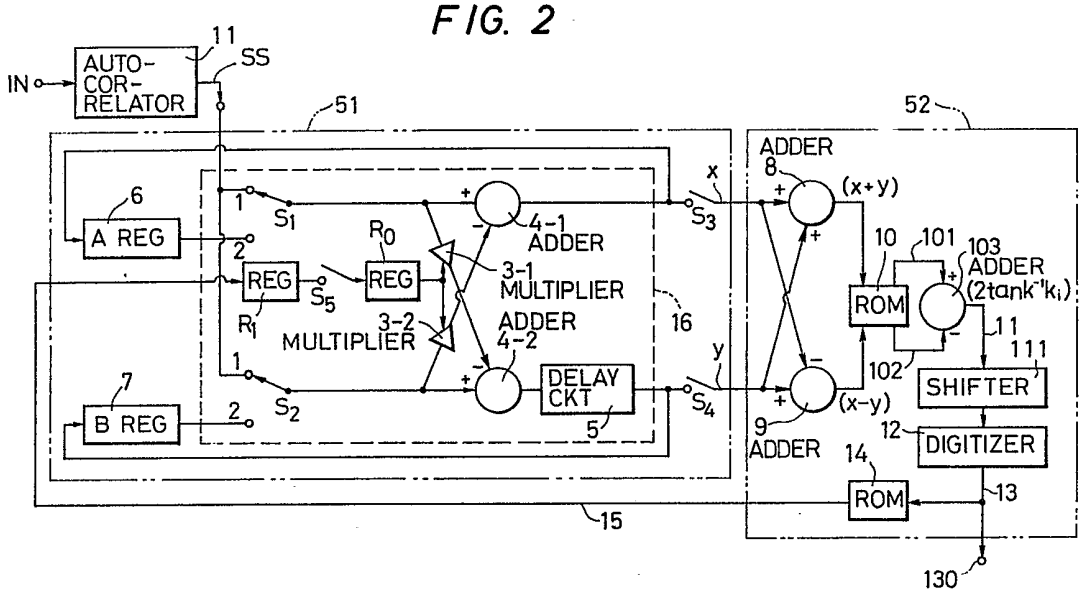
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(54) A Speech Analyzing Device

(57) A speech analyzing device consisting of a data circulation portion (51) of a data circulation type in which two shift registers (6 and 7) and a one-stage digital filter (16) are used repeatedly, and of a partial auto-correlation coefficient computation portion (52) connected to said data circulation portion (51) in cascade. The PARCOR sequence output from said partial auto-correlation coefficient computation portion (52) is fed back to said data circulation portion to sequentially calculate the partial auto-correlation coefficients by means of a process repeating predetermined data circulation.

Certain of the mathematical formulae appearing in the printed specification were submitted in formal form after the date of filing.

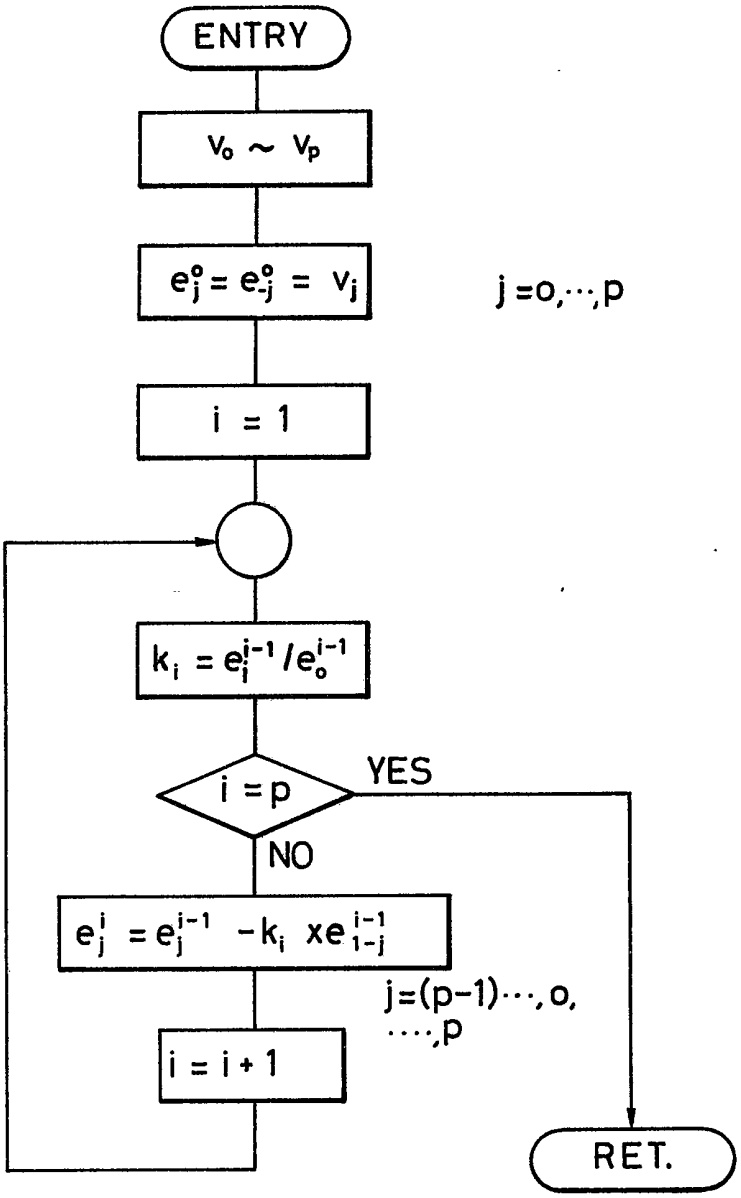
FIG. 2



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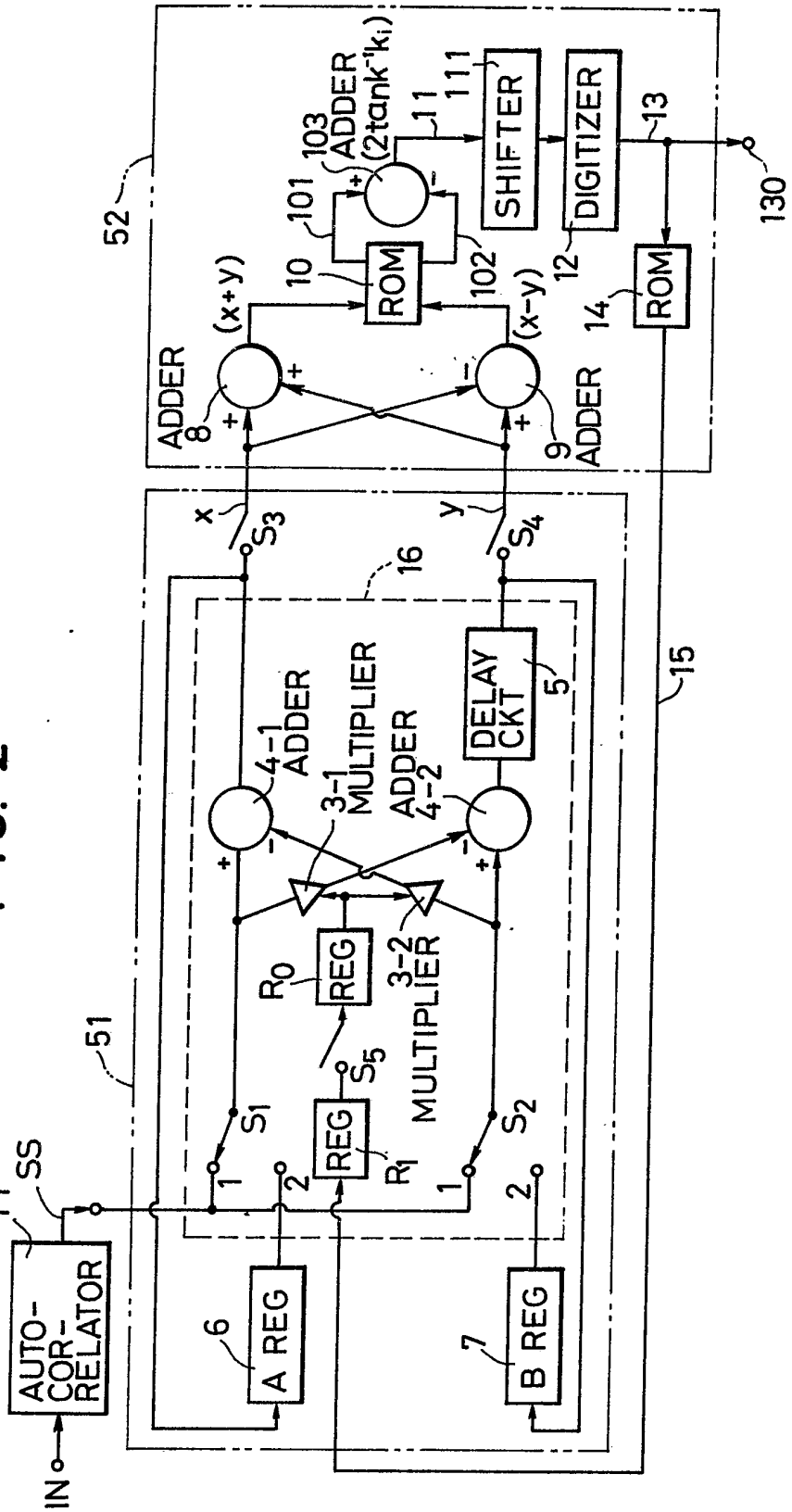
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FIG. 1



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FIG. 2



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FIG. 3(a)

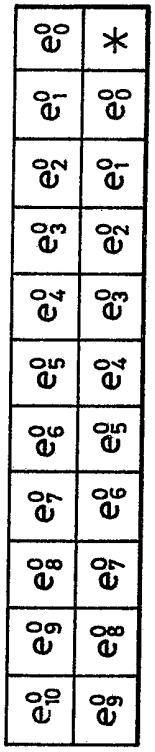


FIG. 3(b)

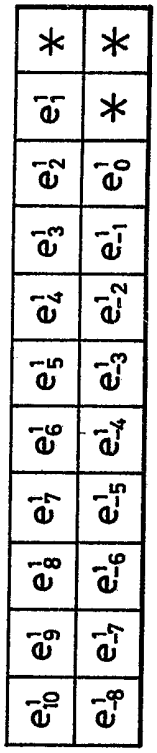
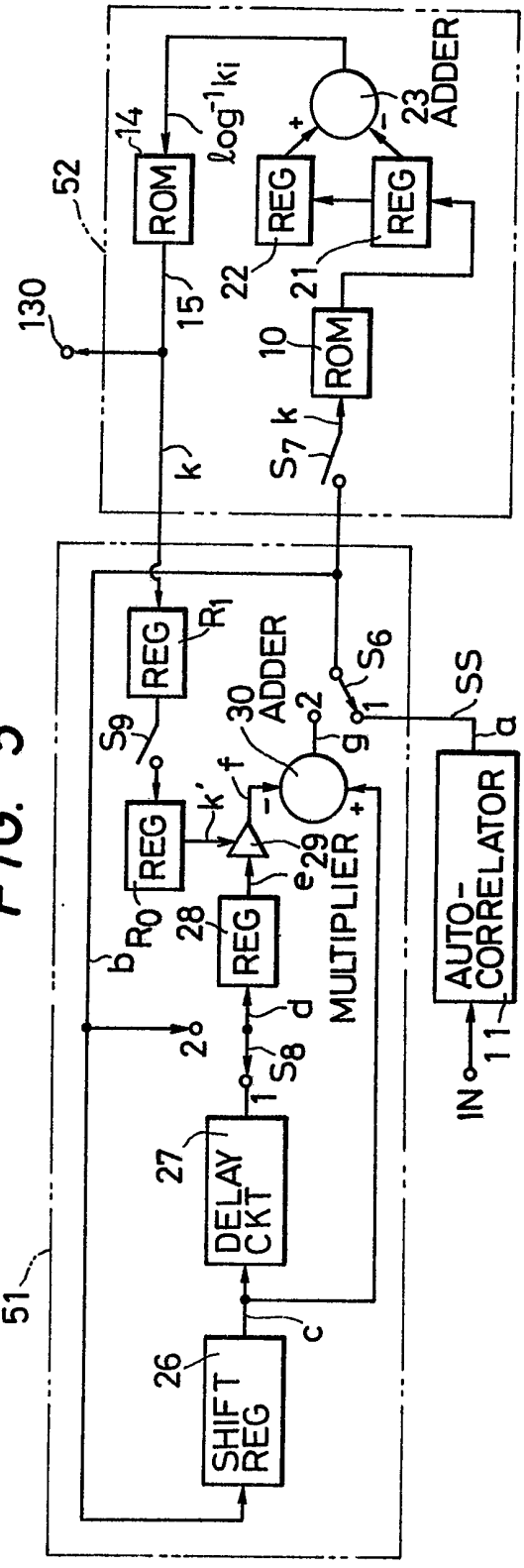
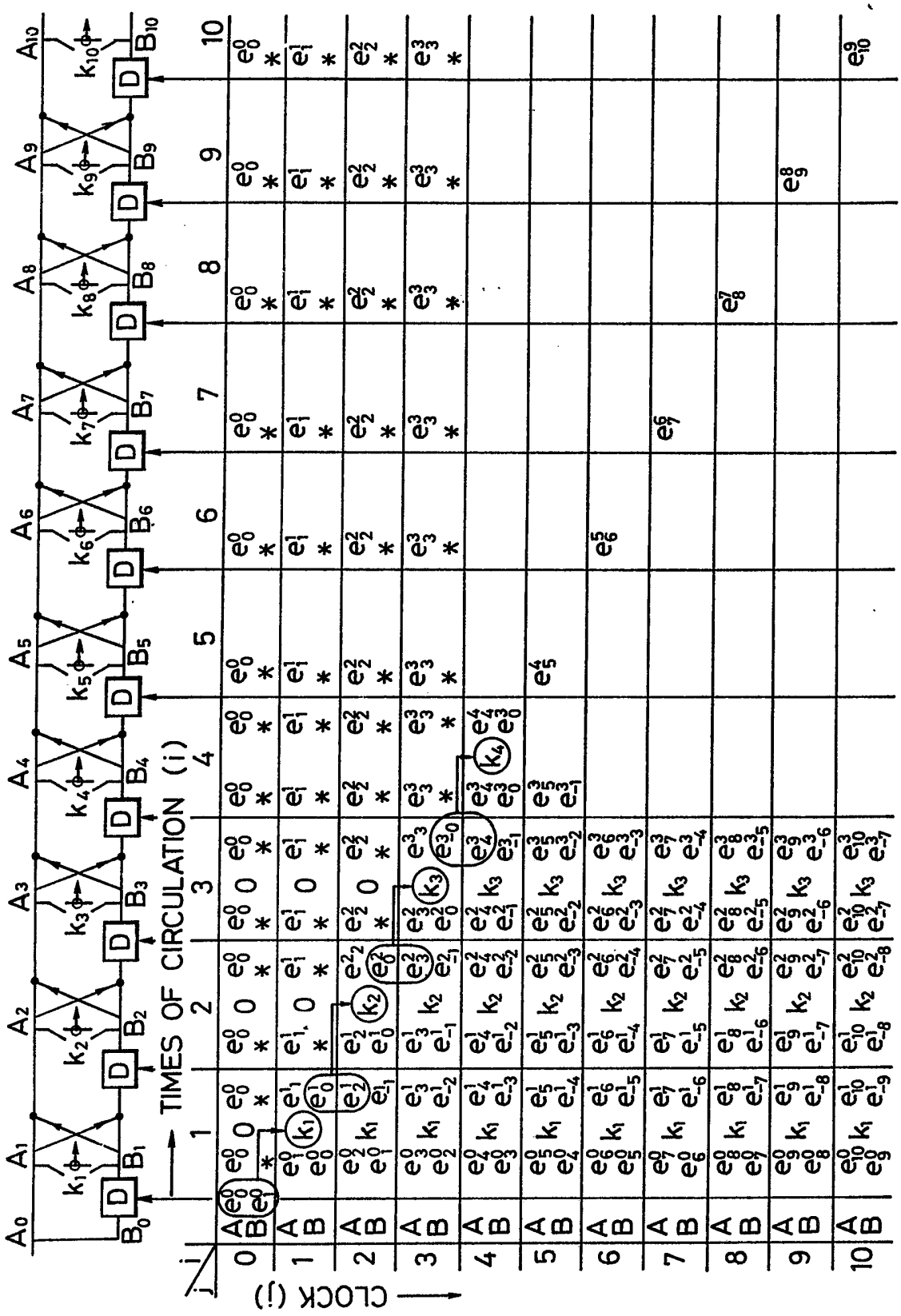


FIG. 5



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FIG. 4



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FIG. 6

T	a	b	c	d	e	k	f	g	h	k	S_8
0	e_1^0	e_1^0							e_1^0		1
1	e_2^0	e_2^0							(S_7		1
2	e_3^0	e_3^0							ON)		1
3	e_4^0	e_4^0									1
4	e_5^0	e_5^0									1
5	e_6^0	e_6^0									1
6	e_7^0	e_7^0									1
7	e_8^0	e_8^0									1
8	e_9^0	e_9^0									1
9	e_{10}^0	e_{10}^0									1
10	e_{-0}^0	e_{-0}^0		e_{-0}^0	↑				e_{-0}^0	↑	2
11	e_{-1}^0	e_{-1}^0		e_{-1}^0	q=4				(S_7	q	2
12	e_{-2}^0	e_{-2}^0		e_{-2}^0					ON)		2
13	e_{-3}^0	e_{-3}^0		e_{-3}^0	↓					↓	2
14	e_{-4}^0	e_{-4}^0		e_{-4}^0	e_{-0}^0	(*)	↑			k_1	2
15	e_{-5}^0	e_{-5}^0		e_{-5}^0	e_{-1}^0	k_1					2
16	e_{-6}^0	e_{-6}^0		e_{-6}^0	e_{-6}^0	k_1	r=5				2
17	e_{-7}^0	e_{-7}^0		e_{-7}^0	e_{-3}^0	k_1					2
18	e_{-8}^0	e_{-8}^0		e_{-8}^0	e_{-4}^0	k_1					2
19	e_{-9}^0	e_{-9}^0		e_{-9}^0	e_{-5}^0	k_1	($*e_{-0}^0$)				2
0		(e_1^1)	e_2^0	e_1^0	e_{-6}^0	k_1	$k_1 e_{-1}^0$	($e_1^1 = e_1^0 - *e_{-0}^0$)			1
1		e_2^1	e_3^0	e_2^0	e_{-7}^0	k_1	$k_1 e_{-2}^0$	$e_2^1 = e_2^0 - k_1 e_{-1}^0$	e_2^1		1
2		e_3^1	e_4^0	e_3^0	e_{-8}^0	k_1	$k_1 e_{-3}^0$	$e_3^1 = e_3^0 - k_1 e_{-2}^0$	(S_7		1
3		e_4^1	e_5^0	e_4^0	e_{-9}^0	k_1	$k_1 e_{-4}^0$	$e_4^1 = e_4^0 - k_1 e_{-3}^0$	ON)		1
4		e_5^1	e_6^0	e_5^0	e_1^0	k_1	$k_1 e_{-5}^0$	$e_5^1 = e_5^0 - k_1 e_{-4}^0$			1
5		e_6^1	e_7^0	e_6^0	e_2^0	k_1	$k_1 e_{-6}^0$	$e_6^1 = e_6^0 - k_1 e_{-5}^0$			1
6		e_7^1	e_8^0	e_7^0	e_3^0	k_1	$k_1 e_{-7}^0$	$e_7^1 = e_7^0 - k_1 e_{-6}^0$			1
7		e_8^1	e_9^0	e_8^0	e_4^0	k_1	$k_1 e_{-8}^0$	$e_8^1 = e_8^0 - k_1 e_{-7}^0$			1
8		e_9^1	e_{10}^0	e_9^0	e_5^0	k_1	$k_1 e_{-9}^0$	$e_9^1 = e_9^0 - k_1 e_{-8}^0$			1
9		e_{10}^1	e_{-0}^0	e_{10}^0	e_6^0	k_1	$k_1 e_1^0$	$e_{10}^1 = e_{10}^0 - k_1 e_{-9}^0$			1
10		e_{-0}^1	e_{-1}^0	e_{-0}^1	e_7^0	k_1	$k_1 e_2^0$	$e_{-0}^1 = e_{-0}^0 - k_1 e_1^0$	e_{-0}^1	↑	2
11		e_{-1}^1	e_{-2}^0	e_{-1}^1	e_8^0	k_1	$k_1 e_3^0$	$e_{-1}^1 = e_{-1}^0 - k_1 e_2^0$	(S_7	q	2
12		e_{-2}^1	e_{-3}^0	e_{-2}^1	e_9^0	k_1	$k_1 e_4^0$	$e_{-2}^1 = e_{-2}^0 - k_1 e_3^0$	ON)		2
13		e_{-3}^1	e_{-4}^0	e_{-3}^1	e_{10}^0	k_1	$k_1 e_5^0$	$e_{-3}^1 = e_{-3}^0 - k_1 e_4^0$		↓	2
14		e_{-4}^1	e_{-5}^0	e_{-4}^1	e_{-0}^1	(*)	$k_1 e_6^0$	$e_{-4}^1 = e_{-4}^0 - k_1 e_5^0$		k_2	2
15		e_{-5}^1	e_{-6}^0	e_{-5}^1	e_{-1}^1	(k_2)	$k_1 e_7^0$	$e_{-5}^1 = e_{-5}^0 - k_1 e_6^0$			2
16		e_{-6}^1	e_{-7}^0	e_{-6}^1	e_{-2}^1	k_2	$k_1 e_8^0$	$e_{-6}^1 = e_{-6}^0 - k_1 e_7^0$			2
17		e_{-7}^1	e_{-8}^0	e_{-7}^1	e_{-3}^1	k_2	$k_1 e_9^0$	$e_{-7}^1 = e_{-7}^0 - k_1 e_8^0$			2
18		e_{-8}^1	e_{-9}^0	e_{-8}^1	e_{-4}^1	k_2	$k_1 e_{10}^0$	$e_{-8}^1 = e_{-8}^0 - k_1 e_9^0$			2
19		e_{-9}^1	e_1^0	e_{-9}^1	e_{-5}^1	k_2	($*e_{-0}^1$)	$e_{-9}^1 = e_{-9}^0 - k_1 e_1^0$			2
0		(e_1^2)	e_2^1	e_1^1	e_{-6}^1	k_2	($k_2 e_{-1}^1$)	($e_1^2 = e_1^1 = *e_{-0}^1$)			1
1		(e_2^2)	e_3^1	e_2^1	e_{-7}^1	k_2	$k_2 e_{-2}^1$	($e_2^2 = e_2^1 - k_2 e_{-1}^1$)			1
2		e_3^2	e_4^1	e_3^1	e_{-8}^1	k_2	$k_2 e_{-3}^1$	$e_3^2 = e_3^1 - k_2 e_{-2}^1$	e_3^2		1
3		e_4^2	e_5^1	e_4^1	e_{-9}^1	k_2	$k_2 e_{-4}^1$	$e_4^2 = e_4^1 - k_2 e_3^1$	(S_7		1
									ON)		

SPECIFICATION

Speech Analyzing Device

The present invention relates to a speech analyzing device, more particularly to an improvement in an analyzing device using a "PARTIAL AUTO-CORRELATION COEFFICIENT". (Hereinafter, this coefficient will be called "PARCOR coefficient" for short and an analyzing system using the coefficient, "PARCOR system".).

About a decade has passed since the PARCOR system speech analysis was devised. Since the principle of this system is well known to those skilled in the art, no further explanation will be given, although reference may be made to an article in "Reports of the meeting by the Acoustical Society of Japan (1976, October, p. 555) by Itakura and Saitoh.

The following devices for determining the PARCOR coefficient k in this PARCOR system, have been proposed:—

(a) a device which incorporates a mini-computer in the device to determine the coefficient k in accordance with the algorithm given by Itakura and Saitoh,

(b) a device which determines the coefficient by a lattice method using a lattice type filter and a correlator disclosed in the above-mentioned report, and

(c) a device by a modified lattice method proposed by Kobayashi and Yamamoto in an article entitled "Operation accuracy of modified lattice type parcor analyzing circuit", in Reports of the meeting by the acoustical society of Japan, (1977, April, p. 257).

The abovementioned lattice method and modified lattice method are suited for the adaptation to a device because they use simple algorithms. However, since the number of steps to be operated becomes large, a hardware construction having high processing capacity is required.

On the other hand, the method proposed by J. Le Roux in an article entitled "A fixed point computation of partial correlation coefficients", in IEEE Transactions on acoustics speech and signal processing, (1977, June p. 257—259) has a characterizing feature in that the number of steps to be processed is small and the operation accuracy is high. To this date, however, no method has been developed to realize the abovementioned method using a simple hardware capable of processing at a high rate.

In view of the problem referred to above, it is an object of the present invention to provide a device which realizes the algorithm proposed by J. Le Roux using a simple hardware construction.

According to the present invention there is provided a speech analyzing device including: a correlator for obtaining an auto-correlation coefficient sequence of input speech signals; a computation portion for obtaining a partial auto-correlation coefficient sequence of said input speech signals; and a data circulation portion receiving as its input said auto-correlation coefficient sequence and said partial auto-correlation coefficient sequence, wherein the output signals of said data circulation portion are employed as the input signals to said computation portion for obtaining said partial auto-correlation coefficient sequence.

The present invention will now be described in greater detail by way of example with reference to the accompanying drawings, wherein:—

Figure 1 is a flow chart showing the procedures for obtaining the PARCOR coefficients in accordance with the algorithm of J. Le Roux;

Figure 2 is a circuit diagram of a first embodiment of a speech analyzing device according to the present invention;

Figures 3, 3(a) and 3(b) are diagrams showing examples of data array stored in A and B registers of Figure 2;

Figure 4 is a diagram showing the change in signals appearing at the outputs of the A and B registers of Figure 2 at every clock pulse;

Figure 5 is a circuit diagram of a second embodiment of a speech analyzing device according to the present invention; and

Figure 6 is a diagram showing the flow of signals appearing at the principal parts of Figure 5 at every clock pulse.

The procedures to obtain the PARCOR coefficients in accordance with the method proposed by J. Le Roux are shown in the flow chart of Figure 1.

First, the auto-correlation coefficients v_o—v_p (where p is the order of the PARCOR coefficients to be determined) are first calculated, and the initial condition is set in the following manner:—

$$e_j o = e_{-j} o = v_j (j = 0, 1, \ldots, p) \ldots (1)$$

The PARCOR coefficients $k_1, k_2, \ldots, k_p$ are sequentially obtained by solving the asymptotic equation:—

$$k_i = e_i^{i-1} / e_o^{i-1}$$

$$e_j^i = e_j^{i-1} - k_i \cdot e_{i-j}^{i-1} \; (j = -(p-1), \ldots, -1, 0, 1, \ldots, p) \ldots (2)$$

The first embodiment of the present invention shown in Figure 2 discloses a device for solving the abovementioned asymptotic equation to determine k_1 by repeated use of two shift registers and a one-stage lattice type digital filter. The second embodiment of the invention shown in Figure 5 discloses a device for solving the asymptotic equation to determine k_1 by utilizing the delay of a shift register and the delay timing of a multiplier. Both of these embodiments make it possible to realize the algorithm proposed by J. Le Roux through an extremely simple hardware construction.

Referring to the first embodiment of the speech analyzing device shown in Figure 2, in which auto-correlation coefficient sequence SS ($v_0, v_1, \ldots, v_p$) is calculated by a known auto-correlator 11 from input speech signals IN to be analyzed. The speech analyzing device comprises a data circulation portion 51 and a PARCOR coefficient computation portion 52. The output from the auto-correlator 11 is applied to the data circulation portion 51.

A register R_0 of a digital filter 16, which is included in the data circulation portion 51, is cleared and switches S_1 and S_2 are placed in the "1" positions before the operation to compute the PARCOR coefficients is started in the data circulation portion 51 and in the PARCOR coefficient computation portion 52.

The auto-correlation coefficient sequence SS ($v_0, v_1, \ldots, v_p$) input to the data circulation portion 51 is stored in a shift register 6 (hereinafter called "A-Reg") and in a shift register 7 (hereinafter called "B-Reg") through multipliers 3—1 and 3—2 (the result of multiplication is 0 because the content of R_0 is 0), adders 4—1 and 4—2 and a 1-data delay circuit 5.

The A-Reg and B-Reg may have such a data length (p-words) as to correspond to the number of orders of the PARCOR coefficients to be determined.

For the sake of simplicity, the operation of Figure 2 will be explained in detail for the case where p=10.

When switches S_3 and S_4 are closed at the instant at which v_1 enters the A-Reg 6, v_0 which is delayed by one-data by the delay circuit 5 enters the input of the B-Reg 7.

Accordingly, since the outputs x and y of the respective switches S_3 and S_4 become:—

$$x=v_1=e_1^0 \text{ and } y=v_0=e_0^0,$$

respectively, the output of adders 8 and 9 in the PARCOR coefficient computation portion 52 become:—

$$(x+y) \text{ and } (x-y),$$

respectively and are applied to a ROM 10.

The logarithmic contents are read from the ROM 10 using (x+y) and (x—y) as the addresses. The results of reading 101 and 102 are subtracted in an adder circuit 103, and the output 11 thereof is as follows:—

$$\log(y+x)-\log(y-x)=\log\frac{y+x}{y-x}=\log\frac{1+\frac{x}{y}}{1-\frac{x}{y}}$$

$$=\log\frac{1+\frac{e_1^0}{e_0^0}}{1-\frac{e_1^0}{e_0^0}}=\log\frac{1+k_1}{1-k_1}$$

$$=2.\tanh^{-1}k_1$$

Thus, a product two times a parameter $\tanh^{-1} k_1$ called "log area ratio" is obtained.

It is known that the influence of quantization is smaller on the log area ratio than on the PARCOR coefficient k when each is quantized.

The abovementioned result is divided by 2 by a shifter 111 (1-bit shift may be made) to obtain $\tanh^{-1} k_1$, which is quantized by a digitizer 12 to obtain a result 13. The result 13 is produced as output at an external terminal 130. Using this result as the address, a reverse conversion table of $\tanh^{-1} k_1$ written in a ROM 14 is read out therefrom to return the log area ratio to the PARCOR coefficient k_1, is fed back to the data circulation portion 51 and is then stored in the register R_1.

Needless to say, it is naturally possible to directly obtain k_1 as $k_1=x/y$.

The switches S_3 and S_4 are opened during the time at which v_2 enters the A-Reg 6. The switches S_1 and S_2 are switched to the "2" position during the time at which $v_0, v_1, \ldots, v_{10}$ are stored in the A-Reg 6 and the B-Reg 7. The switch S_5 is closed and the content of the register R_1 is transferred to the

register R_0. At this time, the contents of the A-Reg 6 and the B-Reg 7 are such as shown in Figure 3(a). Symbol * in the drawing represents meaningless data. Dut to the delay circuit 5, data which each deviated by one word from the corresponding data of the A-Reg 6 are stored in the B-Reg 7. Next, the data are fed out one word by one from both the A-Reg 6 and the B-Reg 7 and multiplication is effected by means of the output of the register R_0 and the multipliers 3—1 and 3—2. The result of multiplication is applied to the adders 4—1 and 4—2 to operate the following equation (3) corresponding to the above referred to equation (2):—

$$\left.\begin{aligned} e_0^1 &= e_0^0 - k_1 \times e_{-1}^0 = v_0 - k_1 \times v_1 \\ e_1^1 &= e_1^0 - k_1 \times e_0^0 = v_1 - k_1 \times v_0 \\ &\cdots\cdots\cdots\cdots \\ e_{10}^1 &= e_{10}^0 - k_1 \times e_9^0 = v_{10} - k_1 \times v_9 \\ &\cdots\cdots\cdots\cdots \\ e_{-9}^1 &= e_{-9}^0 - k_1 \times e_{10}^0 = v_9 - k_1 \times v_{10} \end{aligned}\right\} \quad (3)$$

As a result, the contents of the A-Reg 6 and the B-Reg 7 become such as shown in Figure 3(b).

During this process, e_2^0 is produced as the output from the A-Reg 6 and at the time during which e_1^0 is produced from the B-Reg 7, the input to the switch S_3 is as follows:—

$$e_0^0 - k_1 \times e_1^0 = e_2^1$$

Also, the input to the switch S_4 is as follows:—

$$e_0^0 - k_1 \times e_1^0 = e_0^1$$

which is one period before $(e_1^0 - k_1 \times e_1^0)$ due to the delay circuit 5.

At this time, the switches S_3 and S_4 are closed to obtain $x=e_2^1$ and $y=e_0^1$, and the PARCOR coefficient k_2 can be obtained in the same way as k_1. When e_{10}^1 is stored in the A-Reg 6 and e_{-8}^1 in the B-Reg 7, the switch S_5 is closed whereby k_2 is transferred to the register R_0 to prepare for the operation to obtain k_3.

In the same way, at the time when e_3^1 is produced from the A-Reg 6 and e_{-1}^1 from the B-Reg 7, the input to the switch S_3 becomes e_3^2 and that the switch S_4 becomes e_0^2 which is one period earlier than e_{-1}^2. At this time the switches S_3 and S_4 are closed to obtain $x=e_3^2$ and $y=e_0^2$ and the PARCOR coefficient k_3 can now be obtained.

The operation is continued while extending the time during which the switch S_3 and S_4 remain closed by one data period until k_{10} (or k_p, generally) is computed.

Figure 4 illustrates signal changes of the output portions of the A-Reg 6 and the B-Reg 7 when the PARCOR coefficients $k_1, k_2, \ldots, k_{10}$ are sequentially obtained.

The abscissa represents the number of circulation times (i) of the circulation processing in which the data pass through the digital filter 16 of Figure 2, the operation of the equation (2) is effected and its result is stored in the registers 6 and 7. At the same time, the periods during which the digital filter 16 is repeatedly used and the coefficients $k_1, k_2 \ldots, k_{10}$ are obtained, are illustrated by an exploded view. The ordinate represents the number of transfer clock pulses (j) when the data are transferred in the A-Reg 6 and the B-Reg 7 during each circulation processing.

To take an example of the step where $i=3$ and $j=3$ in Figure 4, e_3^2 and e_0^2 on the left side of the column represent the signals that are output from the adder 4—1 and delay circuit 5 and appear at the output of the two registers 6 and 7 in Figure 2, while C_3^3 and e_{-0}^3 on the right side of the column are calculated as the output of the adders 4—1 and 4—2 of Figure 2 in the following manner:—

$$e_3^3 = e_3^2 - k_3 \times e_0^2$$

$$e_{-0}^3 = e_0^2 - k_3 \times e_3^2$$

The PARCOR coefficients k_i ($i=1, 2, 3, \ldots$) are sequentially obtained using the result of the computation of the preceding steps as represented by arrows. If $i>j$, the data disappear one by one due to the delay circuit 5 whenever the data are repeatedly circulated and hence, do not represent correct values. However, there occurs no problem because e_i^{j-1} and e_0^{j-1} necessary for obtaining k_i are correct values.

In the above referred to operation, since the digitizer 12 is actuated before k_i of the subsequent stage is obtained, the quantization error can be incorporated in the subsequent stage and compensated for in the stage of high order. Hence, the accuracy of analysis as a whole can be improved.

In the ordinary lattice method and modified lattice method, the circuit for obtaining $\tanh^{-1} k$ from x and y is processed in the waveshape range. Hence, the circuit requires four adders, two squarers and two accumulators. By contrast, the present invention can be constructed in an extremely simple manner using only two adders 8 and 9.

In the foregoing description, two sets of the multipliers 3—1, 3—2 and the adders 4—1, 4—2 are required to form the digital filter 16. However, it is possible to use one each multiplier and adder on a time-sharing basis.

Figure 5 shows a circuit diagram of the second embodiment of a speech analyzing device according to the present invention.

In Figure 5, switches S_6 and S_8 are connected to the terminal 1 and the auto-correlation coefficient sequence SS ($v_0, v_1, \ldots, v_p$) is computed by the auto-correlator 11 from input speech signals IN to be analyzed in the same way as in Figure 2.

The auto-correlation coefficient sequence SS is assumed to be produced in the sequence of the equation (4) or (5) by referring to equation (1):—

$$v_0, v_1, \ldots, v_{p-1}, v_1, v_2, \ldots, v_p \quad (4)$$

$$v_1, v_2, \ldots, v_p, v_0, v_1, \ldots, v_{p-1} \quad (5)$$

For the sake of simplicity, the case of equation (5) will now be discussed in greater detail. The case of equation (4) can also be processed in the same way by changing the periods for the switches as will be described later.

From equation (1), equation (5) can be regarded as the following data sequence of 2p;

$$e_1^0, e_2^0, \ldots e_p^0, e_{-0}^0, e_{-1}^0, e_{-2}^0, \ldots e_{-(p-1)}^0 \quad (6)$$

The auto-correlation coefficient sequence SS expressed by the equation (6) is divided into three parts and sent to the switch S_7 in the PARCOR coefficient computation portion 51, to the switch S_8 in the circulation processing portion 52 and to a shift register 26 (consisting of 2p words). A switch S_7 at the input portion of the PARCOR coefficient computation portion 52 is closed during the time at which e_1^0 and e_{-0}^0 appear. The contents written logarithmically in a ROM 10 are read out twice using e_1^0 and e_{-0}^0 as the addresses and the results are sequentially stored in registers 21 and 22. The difference between the read results are computed by an adder 23, and a ROM 14 storing the inverse logarithm of the result is read twice to obtain the PARCOR coefficient k_1.

That is to say:—

$$k_1 = \log^{-1}(\log e_1^0 - \log e_{-0}^0) = \log^{-1}\left(\log \frac{e_1^0}{e_{-0}^0}\right)$$

$$= \frac{e_1^0}{e_{-0}^0}$$

The switch S_7 is normally closed during the time e_1^{i-1} and e_0^{i-1} appear, and the PARCOR coefficient k_i is obtained as:—

$$k_i = \log^{-1}(\log e_i^{i-1} - \log e_0^{i-1}) = \log^{-1}\left(\log \frac{e_i^{i-1}}{e_0^{i-1}}\right)$$

$$= \frac{e_1^{i-1}}{e_0^{i-1}}$$

This can be taken out from the output terminal 130.

In the PARCOR coefficient computation portion 52, the ROM 10 is read out twice and the calculation to obtain the difference is made by the adder 13 to obtain the difference. Further, the ROM 14 is read once, thus yielding 4-bit delay q=4.

The PARCOR coefficient 15 obtained in the PARCOR coefficient computation portion 52 is transferred to the data circulation processing portion 32 and is first stored in the register R_1. On the other hand, the data sequence of equation (6) are sequentially stored in the shift register 26 when the switch S_6 is in the "1" position. When $e_1^0, e_2^0, \ldots, e_p^0$ are stored, the switch S_8 is in the "2" position and subsequent data sequence $e_{-0}^0, e_{-1}^0, \ldots, e_{-(p-1)}^0$ are also stored in the register 28.

The switch S_9 is closed at the time which is one data period later than the time of the appearance of e_{-0}^{0} (generally, e_{-0}^{l}) and k_1 stored in the register R_1 is transferred to the register R_0. Generally, whenever the processing to be later described makes one circulation, the time may further be delayed by one data period. This is because the first result of the data applied to the multiplier 29 is not used.

When k_1 is obtained at the output of the register R_0, the output of the register 28 is e_{-1}^{0} which is next to e_{-0}^{0}. Accordingly, the output of the multiplier 29 is $k_1 \times e_{-1}^{0}$ and is applied to the negative input of the adder 30. The delay by the multiplier 29 can be made $r=z/2-1$ where z is the data length of the shorter data of the two to be multiplied.

Accordingly, in order to adjust the time so that e_2^0 is obtained at the output of the register 26 when $k_1 \times e_{-1}^{0}$ is obtained at the output of the register 29, the following equation may be satisfied:—

$$q+r=p-1 \qquad (7)$$

where q is the delay of the register 28.

The output of the adder 30 at this time is:—

$$e_2^0-k_1 \times e_{-1}^{0}=e_2^1$$

and the result of the equation (2) can thus be obtained.

In the PARCOR analysis, the correlation data is usually 12 to 16-bit while the PARCOR coefficient is 3 to 12 bit. Hence, it is possible to obtain r=5 if z=12.

At the time when e_2^1 is obtained at the output of the adder 30, the switch S_6 is in the "2" position and the switch S_7 is closed whereby $\log(e_2^1)$ is read out from the ROM 10 and stored in the register 21. Further, the switch S_8 is in the "1" position and the switch S_6 is kept in the "2" position until all the PARCOR coefficients are obtained. Accordingly, the output of the shift register 26 is applied to the register 28 through the delay circuit 27 for the one-data period delay.

In the same way $e_2^1, e_3^1, e_4^1, \ldots, e_p^1, e_{-0}^{1}, e_{-1}^{1}, \ldots, e_{-(p-1)}^{1}$ are obtained at the output of the adder 30 in accordance with $e_j^1=e_j^0-k_1 \times e_{1-j}^0$ of the equation (2), and are sequentially stored in the shift register 26.

At the time when e_{-0}^{1} is obtained at the output of the adder 30, the switch S_7 is closed and $\log(e_{-0}^{1})$ is transferred from the ROM 10 to the register 21. In the same way as k_1, k_2 is obtained at the same time by q data periods later than the closure of the switch S_7 and is then stored in the register R_1. At this time the switch S_8 is in the "2" position. At the time when e_{-1}^{1}, which is one period later than e_{-0}^{1}, appears at the output of the register 28 while it is further delayed by the q data periods, the switch S_9 is closed and k_2 is transferred from the register R_1 to R_0. When $k_2 \times e_{-1}^{1}$ is obtained at the output of the multiplier 29 at the time delayed by r data periods, the output of the adder becomes as follows since the output of the shift register 26 is e_2^1.

$$e_2^1-k_2 \times e_{-1}^{1}=e_2^2$$

There is thus obtained the result of equation (2).

In the same way as $e_2^2, e_3^2, e_4^2, \ldots, e_p^2, e_{-0}^{2}, e_{-1}^{2}, \ldots e_{-(p-1)}^{2}$ are obtained at the output of the adder 30 in accordance with $e_j^2=e_j^1-k_2 \times e_{1-j}^1$ of equation (2) and are sequentially stored in the shift register 26.

Thereafter, the operation is continued until k_p is obtained by alternately changing over the switch S_8 between the "1" and "2" positions at p instants so as to circulate the data p time.

In the case of this embodiment (p=10), the delay of the PARCOR coefficient computation portion 52 is 4. In order to apply k_1 to the multiplier 29 at the precise instant, it is convenient to make the register R_0 the same as the register R_1. For under the condition $p=10$, k_j would be delayed by one clock pulse more than necessary at the multiplier 29 if k_i has to pass through the two registers R_0 and R_1 during two successive periods. If $p>10$, it is preferred to use the registers R_0 and R_1 separately in order not to erase k_i obtained at the PARCOR coefficient computation portion 52 and k_{i-1} which is being used at the multiplier 29.

If the PARCOR coefficient computation portion in this embodiment performs the operation in which k is first converted to $\tanh^{-1} k$ and $\tanh^{-1} k$ is quantized and is again returned to k in the same way as in the first embodiment, the delay q in the PARCOR coefficient computation portion becomes great. When $q+r>p-1$, the processing at the data circulation processing portion 51 may be stopped at the following time:—

$$\tau=q+r-(p-1)$$

in order to adjust the timing.

Generally, the total stop time ($\tau \times p$) until k_p is obtained is negligibly smaller in comparison with the time length of the speech to be analyzed. Hence, the abovementioned operation may be carried out without any practical problems occuring.

On the contrary, when the adder 29 is reduced in size and r becomes smaller as expressed by the following relation:—

$$q+r<p-1$$

the operation by the PARCOR coefficient computation portion 52 may be stopped at the following clock pulse:—

$$-\tau=(p-1)-(q+r)$$

The foregoing explains the case where the auto-correlation coefficience sequence is given by equation (5). When it is given by equation (4), the time during which the switch S_7 is closed is so changed as to obtain predetermined data and the polarity of the input to the adder 23 is reversed.

Figure 6 illustrates the flow of signals at the portions (a, b, c, d, e, f, g, h, k, k') of Figure 5 at every instant (T).

This is the case where $p=10$, $q=4$ and $r=5$. The data are circulated at every T=0~19 and the switch S_8 is alternately switched from one position to the other at the instants when $p=10$.

Values in parentheses represent the operation that is not necessary for the subsequent computation. By utilizing these characteristics, k_i can be obtained and the processing can be made even if the first data (represented by *) appearing at k' as the input to the multiplier 29 is not in time for the time of the operation of equation (2).

As represented in the column h, the instants between which the switch S_7 is closed are T=0 and T=10 between e_1^0 and e_{-0}^0 to obtain k_1 and has an interval of 10 periods. Between e_2^1 and e_{-2}^{1} to obtain k_2, however, the instants are between T=1 and T=10 and the interval becomes 9 periods. Similarly, the interval between e_{i+1}^{i} and e_0^i to obtain k_i becomes smaller by one period whenever the data makes one circulation.

As will be appreciated by those skilled in the art, the present invention makes it possible to realize the algorithm proposed by J. Le Roux through an extremely simplified hardware construction.

Claims

1. A speech analyzing device including: a correlator for obtaining an auto-correlation coefficient sequence of input speech signals; a computation portion for obtaining a partial auto-correlation coefficient sequence of said input speech signals; and a data circulation portion receiving as its input said auto-correlation coefficient sequence and said partial auto-correlation coefficient sequence, wherein the output signals of said data circulation portion are employed as the input signals to said computation portion for obtaining said partial auto-correlation coefficient sequence.

2. A speech analyzing device according to Claim 1, wherein said data circulation portion comprises:

two independent shift registers;

a digital filter using either one of two output signals from said shift registers and said partial autocorrelation coefficient sequence from said computation portion as its input signals; and

two switching circuits for selecting two output signals from said digital filter at predetermined timings, respectively;

said two output signals from said digital filter being fed back to the corresponding input of said shift registers, respectively;

said output signals of said two switching circuits being used as the input signals to said computation portion for obtaining said partial auto-correlation coefficient sequence.

3. A speech analyzing device according to claim 1, wherein said data circulation portion comprises:—

an addition circuit;

a first switching circuit for selecting either said auto-correlation coefficient sequence from said correlator or output signals from said addition circuit;

a first shift register for storing the output signal from said first switching circuit:

A second switching circuit for selecting either the output signal of said first shift register or that of said first switching circuit at a predetermined time;

a second shift register for storing the output of said second switching circuit;

a third shift register for storing the output signal of said partial auto-correlation coefficient computation portion receiving the output signal of said first switching circuit as its input signal; and

a multiplier for multiplying a signal corresponding to the output of said third register and the output signal of said second register;

the output signal of said multiplier and that of said first register being applied as input signals to said addition circuit.

4. A speech analyzing device constructed and arranged to operate substantially as herein described with reference to and as illustrated in Figure 2 or Figure 5 of the accompanying drawings.

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