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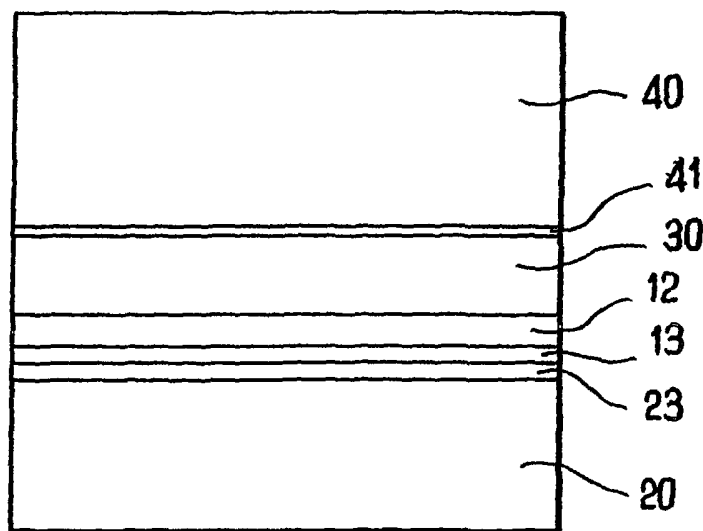
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**GHYSELEN, Bruno** [FR/FR]; 58, rue Georges Maeder, *ance Notes on Codes and Abbreviations" appearing at the begin-*  
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(54) Title: A METHOD OF FABRICATING A SUBSTRATE COMPRISING A USEFUL LAYER OF A MONOCRYSTALLINE SEMICONDUCTOR MATERIAL



(57) Abstract: A method for manufacturing a substrate comprising a useful layer (30) of at least one monocrystalline semiconductor material on a support (40) involves an epitaxial growing of the monocrystalline semiconductor material on a nucleation layer (12). The nucleation layer is provided on an intermediate support (20) in the form of a thin layer of nucleation material taken from a source substrate (10). The following steps are performed: selecting the material of intermediate support so that it can be chemically etched by a given etching medium, it is liable to thermal dissociation when exposed to the temperature of epitaxial growing, and it is less expensive than materials which are less liable to thermal dissociation at said temperature of epitaxial growing, selecting the material of the nucleation layer so that it forms a barrier against the diffusion

of elements deriving from the thermal dissociation of the material of the intermediate support (20) to the intermediate support (20); growing the or each monocrystalline semiconductor material of the useful layer (30) on said nucleation layer (12); bonding the useful layer (30) to a final support (40) at the face of said useful layer opposite to the intermediate support; and exposing said intermediate support (20) to said etching medium to remove it by chemical etching substantially without affecting the useful layer. Application to producing optoelectronic components such as LEDs based on thin layer metallic nitrides.



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A METHOD OF FABRICATING A SUBSTRATE COMPRISING A USEFUL LAYER OF A MONOCRYSTALLINE SEMICONDUCTOR MATERIAL

The present invention relates to a method of  
5 fabricating a support carrying a substrate comprising a  
useful layer of monocrystalline semiconductor material,  
especially a wide band gap material, and in particular a  
gallium nitride (GaN), aluminium nitride (AlN), or some  
other mono or poly-metallic nitride substrate, or a diamond  
10 substrate.

Technologies based on GaN, AlN, and compounds thereof  
currently suffer from a dearth of large-sized bulk  
substrates of such materials.

The most widely known technique for producing a bulk  
15 GaN substrate consists in depositing said material on a  
substrate by hetero-epitaxy.

In order to produce deposited material with good  
crystal quality, the material of the substrate must present  
little lattice mismatch relative to the epitaxial  
20 monocrystal. Because of the high temperatures involved in  
hetero-epitaxy, it is also necessary for the thermal  
expansion coefficient of the substrate material to be  
relatively close to that of the epitaxial monocrystal.  
Finally, said substrate must be mechanically and chemically  
25 stable at the temperatures under consideration in order to  
obtain good crystal quality. Naturally, the surface  
condition and the good crystal quality of the starting  
substrate are also important factors.

Materials that are currently recognized as good  
30 candidates having regard to the above criteria are sapphire  
and silicon carbide (SiC), although they are far from being  
optimal as regards their lattice parameters and their  
expansion coefficients.

The growth of layers of GaN on substrates of zirconium  
35 oxide ZnO, or lithium gallium oxide LiGaO<sub>2</sub>, or lithium  
aluminium oxide LiAlO<sub>2</sub> (see the article "Growth of III-  
Nitrides on ZnO, LiGaO<sub>2</sub> and LiAlO<sub>2</sub> substrates", Mackenzie et

al., J. Electrochem. Soc., vol. 145, N° 7, July 1998, p. 2581) or of neodymium gallium oxide  $\text{NdGaO}_3$  (see the article "GaN bulk substrates for GaN based LEDs and LDs", Oda et al., Phys. Stat. Sol., (a) 180, 51 (2000)), has also been  
5 described, said materials having been selected for their small lattice mismatch relative to GaN and their small coefficient of expansion difference compared with GaN.

However, those substrates are oxides with high temperature chemical stability that is poorer than that of  
10 SiC or of sapphire. Said problem with stability manifests itself in the form of dissociation and diffusion of the metal and/or oxygen component elements of the oxide towards the epitaxial layer. In the case of a ZnO substrate, the article "Impurity contamination of GaN epitaxial films from  
15 the sapphire, SiC, and ZnO substrates", Popovici et al., Appl. Phys. Lett., 71(23), 8 December 1997, demonstrates contamination by zinc and by oxygen in the case of a ZnO substrate, and that contamination compromises the quality and purity of the epitaxial layer.

20 Further, once the layer or layers intended to form the substrate have been formed, in the majority of cases the support on which growth has been carried out has to be removed, which necessitates either chemical etching of said support and thus its loss even if it is produced from an  
25 expensive material, thereby increasing the cost of the process, or by rupture between the layers formed by epitaxial growth and said support.

More generally, it has been proven that, for the purpose of temporary support removal, the chip  
30 manufacturers would mostly prefer an etching technique than a rupture technique. This is mainly because in the industry of semiconductors, etching techniques have been well mastered for years and most often do not require any significant investment, while ruptures techniques might be  
35 difficult to control and/or require significant additional investment and add complexity to the whole process.

In parallel, an etching approach would be economically valuable only if the material of the support is reasonably inexpensive, but such inexpensive materials, such as gallium arsenide GaAs, bring other drawbacks.

5 In this regard, the paper "Preparation of large freestanding GaN substrates by Hydride Vapor Phase Epitaxy using GaAs as a starting substrate", Motoki et al., Jpn. J. Appl. Phys., Vol. 41 (2001), p. 140-143, proposes using a gallium arsenide GaAs substrate on which to grow GaN by  
10 hetero-epitaxy. However, when heated to the high temperatures involved in epitaxy, GaAs undergoes surface dissociation, which causes arsenic to evaporate, which is likely to contaminate the GaN monocrystal.

An aim of the present invention is to overcome the  
15 limitations of the prior art and to propose a method for manufacturing a substrate by hetero-epitaxial growth in which a low cost intermediate support can be eliminated by etching while leaving the useful layer substantially unaffected by elements dissociated from said intermediate  
20 support.

In a first aspect, the present invention provides a method for manufacturing a substrate comprising a useful layer of at least one monocrystalline semiconductor material on a support, said method involving an epitaxial  
25 growing of the monocrystalline semiconductor material on a nucleation layer, said nucleation layer being provided on an intermediate support in the form of a thin layer of nucleation material taken from a source substrate, the method comprising the following steps:

30 selecting the material of intermediate support so that it can be chemically etched by a given etching medium, it is liable to thermal dissociation when exposed to the temperature of epitaxial growing, and it is less expensive than  
35 materials which are less liable to thermal dissociation at said temperature of epitaxial growing,

selecting the material of the nucleation layer so  
that it forms a barrier against the diffusion of  
elements deriving from the thermal  
dissociation of the material of the intermediate  
5 support;  
applying the nucleation layer to the intermediate  
support;  
growing the or each monocrystalline semiconductor  
material of the useful layer on said nucleation  
10 layer;  
bonding the useful layer to a final support at  
the face of said useful layer opposite to the  
intermediate support; and  
exposing said intermediate support to said  
15 etching medium to remove it by chemical etching  
substantially without affecting the useful layer.  
substantially without affecting the useful layer.

Certain preferred, but non-limiting features of the  
method are as follows:

- 20 • the first step is carried out by forming a source  
substrate comprising a detachment zone at a  
certain depth, by bonding the source substrate to  
the intermediate support, and by carrying out a  
treatment on the zone forming the detachment site  
25 to detach a thin layer from the source substrate;
- the detachment zone is produced by implanting  
atomic species;
- said detachment treatment comprises applying  
stresses included in the group formed by thermal  
30 stresses and mechanical stresses;
- the nucleation layer is applied to the  
intermediate support by molecular bonding;
- before applying the nucleation layer to said  
intermediate support, a bonding layer is  
35 deposited on at least one of these two parts;
- the intermediate support is selected from the  
group formed by silicon, gallium arsenide, zinc

oxide, lithium gallium oxide, and lithium aluminium oxide;

- the useful layer comprises at least one mono or poly-metallic nitride;
- 5     • the useful layer is constituted by gallium nitride, and the material of the nucleation layer is selected from the group formed by silicon carbide, gallium nitride and sapphire; and
- 10    • the final support comprises a radiation-reflective coating on its surface receiving the useful layer.

In a second aspect, the present invention provides a method for manufacturing a substrate comprising a useful layer of at least one monocrystalline semiconductor material on a support, said method involving an epitaxial growing of the monocrystalline semiconductor material on a nucleation layer, said nucleation layer being provided on an intermediate support in the form of a thin layer of nucleation material taken from a source substrate, the method comprising the following steps:

- selecting the material of intermediate support so that it can be chemically etched by a given etching medium, it is liable to thermal dissociation when exposed to the temperature of epitaxial growing, and it is less expensive than materials which are less liable to thermal dissociation at said temperature of epitaxial growing,
- selecting a barrier material capable of forming a barrier against the diffusion of elements deriving from the thermal dissociation of the material of the intermediate support;
- providing one face of the intermediate support with a barrier layer made of the barrier material and with the nucleation layer;

growing the or each monocrystalline semiconductor material of the useful layer on said nucleation layer;

5 bonding the useful layer to a final support at the face of said useful layer opposite to the intermediate support; and

10 exposing said intermediate support to said etching medium to remove it by chemical etching substantially without affecting the useful layer which is protected by the barrier layer.

Preferred but non-limiting features of said second method are as follows:

- 15 • the barrier layer and/or nucleation layer is/are formed by providing a source substrate comprising a zone forming a detachment site at a certain depth, by bonding the source substrate to the intermediate support, and by carrying out a treatment on the zone forming the detachment site to detach the layer in question from the source substrate;
- 20 • the barrier layer is applied to the intermediate support and/or the nucleation layer is applied to the barrier layer by molecular bonding;
- 25 • before applying the barrier layer and/or the nucleation layer by bonding, a layer of adhesive is deposited on at least one of the faces to be bonded.

30 Other aspects, aims and advantages of the present invention become clear from the following description of a preferred implementation, given by way of non-limiting example and made with reference to the accompanying drawings in which Figures 1A to 1G illustrate the successive steps of a method in accordance with the invention.

35 Referring to Figures 1A to 1G, Figure 1A shows a source substrate 10, for example of monocrystalline silicon carbide SiC, in which ions, for example hydrogen ions, have

been implanted at a certain depth using an ionic bombardment machine, a plasma implantation machine, etc. Said implantation defines a thin layer 12 from the remainder of the source substrate, the main concentration of hydrogen ions being indicated at 14. Typically, 5 implantation is carried out to a depth in the range 200 nanometers (nm) to 1000 nm, using ions with energy in the range 50 kilo electron volts (keV) to 200 keV, and an implantation dose in the range  $5 \times 10^{16}$  ions per square 10 centimeter (ions/cm<sup>2</sup>) to  $1 \times 10^{17}$  ions/cm<sup>2</sup>.

Referring to Figure 1B, substrate 10 carrying layer 12 is then bonded by molecular bonding to a substrate forming a growth support 20 formed here from monocrystalline gallium arsenide GaAs. Said substrate 20 typically has a 15 thickness in the range 400 micrometers ( $\mu\text{m}$ ) to 800  $\mu\text{m}$ . Optionally, the faces of substrate 10 and substrate 20 to be assembled together have been provided with bonding layers 13, 23, in particular of silicon oxide SiO<sub>2</sub> or silicon nitride Si<sub>3</sub>N<sub>4</sub>, in a manner that is known per se. 20 Said bonding layers, when formed from SiO<sub>2</sub> on Si, are advantageously formed by thermal oxidation, or alternatively, by deposition. The bonding energy of the bonding interface is brought to the required level by heat treatment, typically at a temperature of more than 300°C 25 for a period that is typically 2 hours.

Stresses, in particular thermal and/or mechanical stresses, but which could be of some other nature, are exerted so as to detach the assembly constituted by the substrate 20 and the layer 12 from the remainder of the substrate 10 at the implanted zone 14, using the known 30 Smart-Cut® technique developed by the Applicant. To this end, a heat treatment is typically carried out at a temperature in the range 800°C to 900°C for a period in the range 30 minutes to 3 hours. Such heat treatment can be 35 combined with that used to strengthen the bonding interface.

As illustrated in Figure 1C, a structure comprising a GaAs growth support 20 carrying a thin nucleation layer 12 of monocrystalline SiC is obtained. The free surface of said layer can undergo polishing/cleaning and in particular  
5 chemical-mechanical polishing or ion beam smoothing intended to allow good-quality epitaxial growth to be performed thereon.

A metal organic chemical vapor deposition (MOCVD) hetero-epitaxy technique is carried out on this surface to  
10 produce a stack of deposits of gallium nitride GaN with different types of doping, said technique being known to produce a GaN stack 30 of good crystal quality.

Such an operation is carried out at a temperature of the order of 1050°C to 1100°C, at which temperature partial  
15 dissociation of the GaAs forming the support 20 is observed. However, the presence of the SiC nucleation layer 12, which forms a barrier layer against the diffusion of atoms of arsenic or gallium towards the deposited layer 30, prevents disturbance of the crystal quality and the  
20 purity of said layer 30.

Said stack is typically a few microns thick, i.e., it is a thin layer, as opposed to the thick layers with a minimum thickness of about 200 µm to 300 µm, rendering the stack self-supporting.

25 Figure 1D shows the resulting structure.

After growth of the GaN stack 30, the assembly constituted by layers 20, 23, 13, 12 and 30 is applied to a target substrate 40 of monocrystalline or polycrystalline silicon intended to constitute the final support of the GaN  
30 useful layer.

At its surface receiving the useful GaN layer, said final support 40 advantageously has metallization 41 allowing the final support to constitute a reflector for visible or UV radiation emitted by the electroluminescent  
35 components which have been formed in the useful layer 30. This metallization is preferably formed by cathode sputtering or vacuum evaporation of gold, tin, or palladium

(or of any suitable alloy) with a thickness of 500 nm, for example.

The free surface of the GaN stack 30 undergoes polishing treatment, typically a chemical-mechanical  
5 polishing or ion beam smoothing intended to endow it with a flatness that is suitable for molecular bonding with the target substrate 40, which itself must have a satisfactory flatness produced prior to metallization.

10 The thickness of substrate 40 is typically in the range 300  $\mu\text{m}$  to 500  $\mu\text{m}$ .

Fixing is achieved in this case by molecular bonding or by eutectic bonding (which means that polishing can be dispensed with), if necessary supplying heat energy at a temperature in the range 200°C to 350°C for several hours  
15 to produce the desired bonding forces.

If necessary, prior to said fixing operation, the GaN stack 30 can undergo all or some treatments for producing components such as blue or green LEDs, laser diodes, etc.

20 The assembly is then exposed to chemical etching with a solution composed of a mixture of HF, HNO<sub>3</sub>, CH<sub>3</sub>COOH, and H<sub>2</sub>O in proportions of 1:3:3:5 to etch the intermediate GaAs support 20 and remove it completely.

The final step consists of removing, preferably by ionic etching, the nucleation layer and, if appropriate,  
25 the bonding layers 13 and 23 if they have not been removed chemically. During this operation, it is also possible to remove a portion of the epitaxial layers that have been formed, in particular to remove initial epitaxial layers containing defects.

30 The method described above can be endowed with a variety of variants.

Firstly, the choice of nucleation layer 12 is principally conditioned by the search for a compromise between the lattice parameter, thermal expansion  
35 coefficient, stability at high temperatures, ability to form a barrier layer against the diffusion of elements from possible partial decomposition of the layer forming the

intermediate support. Preferably, either SiC as indicated above is selected, or GaN, or even sapphire is selected.

In contrast, the material of the intermediate support 20 is not critical as regards lattice parameter, but it is selected principally as a result of finding a compromise between its thermal expansion coefficient compared with that of the material of the epitaxial layer, the stability of the epitaxial layer to high temperatures, and in particular the facility with which it is removed chemically.

Apart from GaAs, silicon, certain oxides such as ZnO, or LiGa<sub>2</sub> or NdGaO<sub>3</sub> can in particular be used.

Further, the material deposited by epitaxial growth to form the useful layer or layers of the substrate is typically a stack of differently doped layers of GaN, in a manner that is known per se. However, it can also be a stack of a variety of other metal nitrides such as AlN or GaAlN, etc.

Finally, the final support 40 can be constituted by any support are selected as a function of a compromise between its ability to receive the metallization 41 if appropriate, its ability to receive the deposited layer 30 by bonding or any other technique, its properties in terms of mechanical and chemical stability during treatments for producing components in the stack of layers 30, its thermal properties, its fabrication cost, etc.

In a variant, not shown, it is possible to form two distinct layers, deposited on or applied to the intermediate support, one forming a barrier to the diffusion of elements deriving from dissociation of the material of the intermediate support, and the other, outer layer, forming a nucleation layer. It should be noted in this respect that the barrier layer can be formed, deposited or applied either onto the source substrate 10, or onto the intermediate support 20, prior to bonding.

## EXAMPLE

A 500 nm thick layer of SiO<sub>2</sub> is produced on one face of a monocrystalline SiC source substrate by thermal oxidation. Hydrogen ions are then implanted with an energy of 100 keV and using a dose of  $8 \times 10^{16}$  ions/cm<sup>2</sup> into the source substrate using ion bombardment equipment.

A 500 μm thick monocrystalline GaAs substrate intended to form the intermediate support is also prepared, and one face of the substrate is coated with a 500 nm thick SiO<sub>2</sub> layer by chemical vapor deposition.

Surface activation is then carried out, for example by chemical-mechanical polishing, to smooth the surfaces and provide them with a certain hydrophilic nature.

The faces of the source substrate and the intermediate support substrate are then brought together and bonded, and a suitable bonding energy is obtained by heat treatment at 350°C for a period of 2 hours.

This assembly then undergoes heat treatment at 900°C for a period of one hour to obtain detachment at the implanted zone.

The face of the layer 12 is then polished at the detachment location using ionic smoothing by ion cluster smoothing.

Different GaN layers are then deposited by epitaxial growth. Typically, said GaN stack 30 has the following succession of layers:

- an 8 nm AlN buffer layer;
- a 1 μm GaN layer.

After said operation, the free face of the stack 30 is polished by an ion cluster technique

Meanwhile, a monocrystalline silicon substrate with a normal commercial grade of surface polishing and a thickness of 500 μm is coated with a metallization based on indium/palladium over a thickness of 400 nm.

The intermediate support 20 carrying the stack 30 and the substrate 40 carrying the metallization 41 are then bonded together by molecular bonding, the bonding interface

being reinforced by heat treatment at 350°C for a period of 2 hours.

The GaAs intermediate support is then etched by immersion in an etching solution composed of a mixture of  
5 HF, HNO<sub>3</sub>, CH<sub>3</sub>COOH, and H<sub>2</sub>O in proportions of 1:3:3:5, peripheral etching of the metallic layer 41 being minor and without consequence.

Said etching finishes at the SiC layer 12.

This latter layer is then removed, for example by  
10 SF<sub>6</sub>/O<sub>2</sub> reactive ionic etching.

Clearly, the present invention is not limited to the implementation described and shown in the drawings, and the skilled person is capable of providing variants and modifications.

CLAIMS

1. A method for manufacturing a substrate comprising a useful layer (30) of at least one monocrystalline semiconductor material on a support (40), said method involving an epitaxial growing of the monocrystalline semiconductor material on a nucleation layer (12), said nucleation layer being provided on an intermediate support (20) in the form of a thin layer of nucleation material taken from a source substrate (10), the method comprising the following steps:
- selecting the material of intermediate support so that it can be chemically etched by a given etching medium, it is liable to thermal dissociation when exposed to the temperature of epitaxial growing, and it is less expensive than materials which are less liable to thermal dissociation at said temperature of epitaxial growing,
  - selecting the material of the nucleation layer so that it forms a barrier against the diffusion of elements deriving from the thermal dissociation of the material of the intermediate support;
  - applying the nucleation layer (12) to the intermediate support (20);
  - growing the or each monocrystalline semiconductor material of the useful layer (30) on said nucleation layer (12);
  - bonding the useful layer (30) to a final support (40) at the face of said useful layer opposite to the intermediate support; and
  - exposing said intermediate support (20) to said etching medium to remove it by chemical etching substantially without affecting the useful layer.
2. A method according to claim 1, characterized in that the first step is carried out by forming a source substrate

- (10) comprising a detachment zone (14) at a certain depth, by bonding the source substrate to the intermediate support, and by carrying out a treatment on the zone forming the detachment site to detach a thin layer (12)  
5 from the source substrate.
3. A method according to claim 2, characterized in that the detachment zone (14) is produced by implanting atomic  
10 species.
4. A method according to claim 3, characterized in that said detachment treatment comprises applying stresses included in the group formed by thermal stresses and mechanical stresses.  
15
5. A method according to any one of claims 1 to 4, characterized in that the nucleation layer (12) is applied to the intermediate support (20) by molecular bonding.
- 20 6. A method according to claim 5, characterized in that before applying the nucleation layer (12) to said intermediate support (20), a bonding layer (13; 23) is deposited on at least one of said two parts.
- 25 7. A method according to any one of claims 1 to 6, characterized in that the intermediate support (20) is selected from the group formed by silicon, gallium arsenide, zinc oxide, lithium gallium oxide and lithium aluminium oxide.
- 30 8. A method according to any one of claims 1 to 7, characterized in that the useful layer (30) comprises at least one mono or poly-metallic nitride.
- 35 9. A method according to any one of claims 1 to 8, characterized in that the useful layer (30) is constituted by gallium nitride, and in that the material of the

nucleation layer (12) is selected from the group formed by silicon carbide, gallium nitride and sapphire.

10. A method according to any one of claims 1 to 9,  
5 characterized in that the final support (40) comprises a radiation-reflective coating (41) on its surface receiving the useful layer (30).

11. A method for manufacturing a substrate comprising a  
10 useful layer (30) of at least one monocrystalline semiconductor material on a support (40), said method involving an epitaxial growing of the monocrystalline semiconductor material on a nucleation layer (12), said nucleation layer being provided on an intermediate support  
15 (20) in the form of a thin layer of nucleation material taken from a source substrate (10), the method comprising the following steps:

selecting the material of intermediate support so that it can be chemically etched by a given  
20 etching medium, it is liable to thermal dissociation when exposed to the temperature of epitaxial growing, and it is less expensive than materials which are less liable to thermal dissociation at said temperature of epitaxial  
25 growing,  
selecting a barrier material capable of forming a barrier against the diffusion of elements deriving from the thermal dissociation of the material of the intermediate support;  
30 providing one face of the intermediate support (20) with a barrier layer made of the barrier material and with the nucleation layer (12),  
growing the or each monocrystalline semiconductor material of the useful layer (30) on said  
35 nucleation layer (12);

bonding the useful layer (30) to a final support (40) at the face of said useful layer opposite to the intermediate support; and  
exposing said intermediate support (20) to said  
5 etching medium to remove it by chemical etching substantially without affecting the useful layer which is protected by the barrier layer.

12. A method according to claim 11, characterized in that  
10 the barrier layer and/or the nucleation layer is/are formed by providing a source substrate (10) comprising a zone (14) forming a detachment site at a certain depth, by bonding the source substrate to the intermediate support (20), and  
by carrying out a treatment on the zone forming the  
15 detachment site to detach the layer in question from the source substrate.

13. A method according to claim 12, characterized in that  
20 the detachment zone (14) is produced by implanting atomic species.

14. A method according to claim 13, characterized in that  
said detachment treatment comprises applying stresses  
included in the group formed by thermal stresses and  
25 mechanical stresses.

15. A method according to any one of claims 11 to 14,  
characterized in that the barrier layer is applied to the  
intermediate support (20) and/or the nucleation layer (12)  
30 is applied to the barrier layer by molecular bonding.

16. A method according to claim 15, characterized in that  
before applying the barrier layer and/or the nucleation  
layer (12) by bonding, a layer of adhesive (13; 23) is  
35 deposited on at least one of the faces to be bonded.

17. A method according to claim 11, characterized in that the barrier layer and/or the nucleation layer (12) is/are formed by a deposition technique.
- 5 18. A method according to any one of claims 11 to 17, characterized in that the intermediate support is selected from the group formed by silicon, gallium arsenide, zinc oxide, lithium gallium oxide and lithium aluminium oxide.
- 10 19. A method according to any one of claims 11 to 18, characterized in that the useful layer comprises at least one mono or poly-metallic nitride.
- 15 20. A method according to any one of claims 11 to 19, characterized in that the useful layer is constituted by gallium nitride, and in that the material of the nucleation layer is selected from the group formed by silicon carbide, gallium nitride and sapphire.
- 20 21. A method according to any one of claims 11 to 20, characterized in that the final support comprises a radiation-reflective coating 41 on its surface receiving the useful layer (30).

FIG. 1A

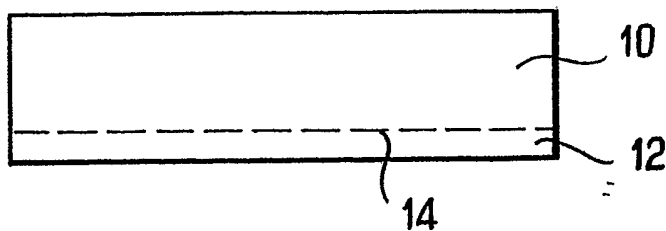


FIG. 1B

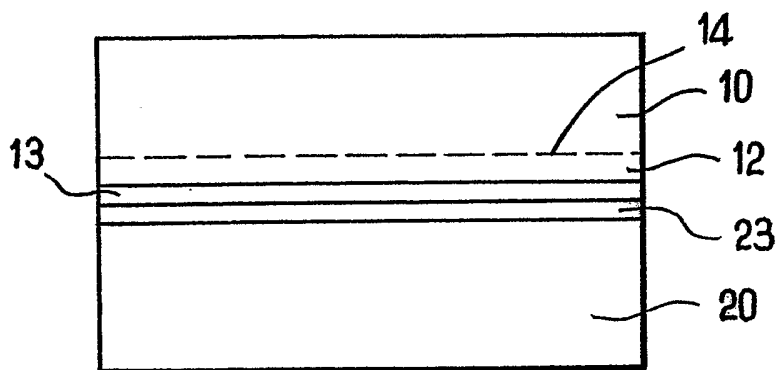


FIG. 1C

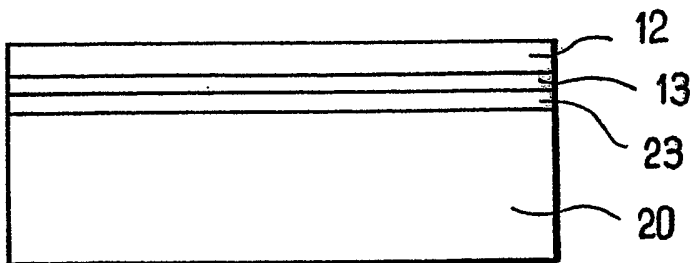


FIG. 1D

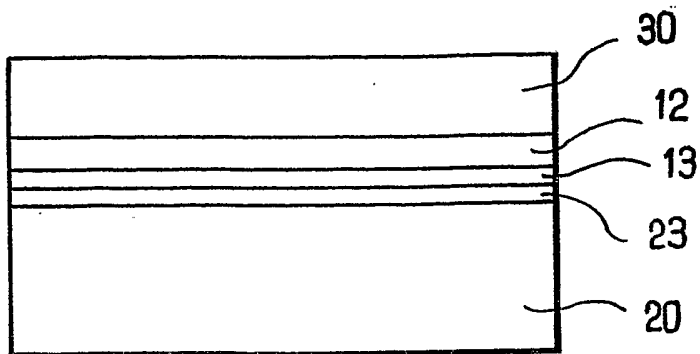


FIG. 1E

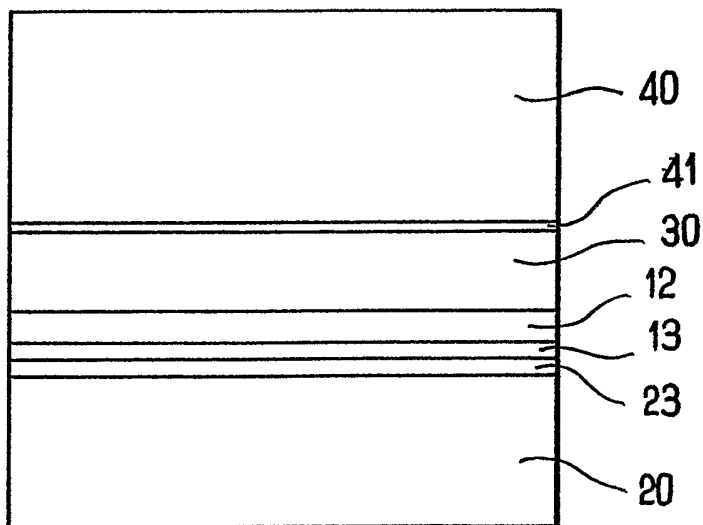


FIG. 1F

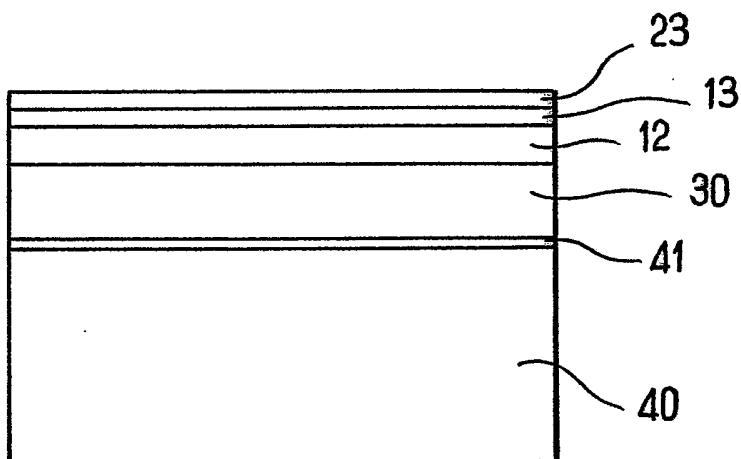
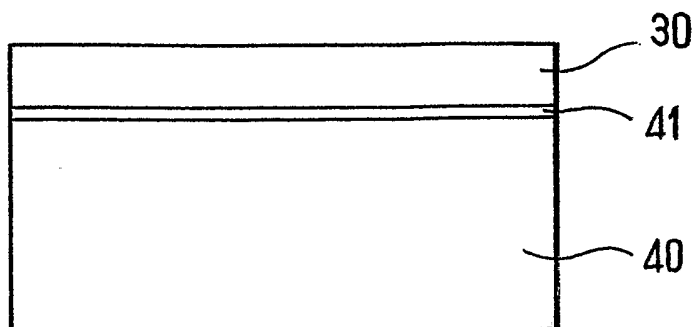


FIG. 1G



INTERNATIONAL SEARCH REPORT

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<b>A. CLASSIFICATION OF SUBJECT MATTER</b> IPC 7 H01L21/76 H01L21/76 H01L21/04 H01L21/20				
According to International Patent Classification (IPC) or to both national classification and IPC				
<b>B. FIELDS SEARCHED</b> Minimum documentation searched (classification system followed by classification symbols) IPC 7 H01L				
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched				
Electronic data base consulted during the international search (name of data base and, where practical, search terms used) EPO-Internal, WPI Data, PAJ, INSPEC, IBM-TDB				
<b>C. DOCUMENTS CONSIDERED TO BE RELEVANT</b>				
Category <sup>o</sup>	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.		
X	WO 02 43112 A (GHYSELEN BRUNO ;LETERTRE FABRICE (FR); S O I TEC SILICON ON INSULA) 30 May 2002 (2002-05-30) abstract; claims; figures page 9, line 2 - line 16 page 13, line 17 - line 18 ---	1-21		
X	WO 02 43124 A (GHYSELEN BRUNO ;LETERTRE FABRICE (FR); S O I TEC SILICON ON INSULA) 30 May 2002 (2002-05-30) abstract; claims; figures page 6, line 28 -page 7, line 13 ---	1-21		
Y	WO 02 37556 A (COMMISSARIAT ENERGIE ATOMIQUE ;ASPAR BERNARD (FR); JALAGUIER ERIC) 10 May 2002 (2002-05-10) abstract; claims; figures page 15, line 23 - line 32 ---	1-21		
-/--				
<input checked="" type="checkbox"/> Further documents are listed in the continuation of box C. <input checked="" type="checkbox"/> Patent family members are listed in annex.				
<sup>o</sup> Special categories of cited documents : <table border="0" style="width: 100%;"> <tr> <td style="width: 50%; vertical-align: top;">                     "A" document defining the general state of the art which is not considered to be of particular relevance                      "E" earlier document but published on or after the international filing date                      "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)                      "O" document: referring to an oral disclosure, use, exhibition or other means                      "P" document published prior to the international filing date but later than the priority date claimed                 </td> <td style="width: 50%; vertical-align: top;">                     "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention                      "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone                      "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.                      "&amp;" document member of the same patent family                 </td> </tr> </table>			"A" document defining the general state of the art which is not considered to be of particular relevance "E" earlier document but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document: referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed	"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art. "&" document member of the same patent family
"A" document defining the general state of the art which is not considered to be of particular relevance "E" earlier document but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document: referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed	"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art. "&" document member of the same patent family			
Date of the actual completion of the international search <p style="text-align: center;">29 September 2003</p>		Date of mailing of the international search report <p style="text-align: center;">07/10/2003</p>		
Name and mailing address of the ISA European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016		Authorized officer <p style="text-align: center;">Wirner, C</p>		

## INTERNATIONAL SEARCH REPORT

International Application No  
PCT/IB 03/03068

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT		
Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	FR 2 787 919 A (THOMSON CSF) 30 June 2000 (2000-06-30) abstract; claims; figures -----	1-21
A	US 5 759 908 A (STECKL ANDREW J ET AL) 2 June 1998 (1998-06-02) abstract; claims; figures -----	1-21

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International Application No

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