(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
11 October 2007 (11.10.2007)

PCT

(10) International Publication Number
WO 2007/114663 A1

(51) International Patent Classification:
H04N 7/24 (2006.01) *H04N 7/64* (2006.01)

(21) International Application Number:
PCT/KR2007/001667

(22) International Filing Date: 5 April 2007 (05.04.2007)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
60/789,603 6 April 2006 (06.04.2006) US
11/692,509 28 March 2007 (28.03.2007) US

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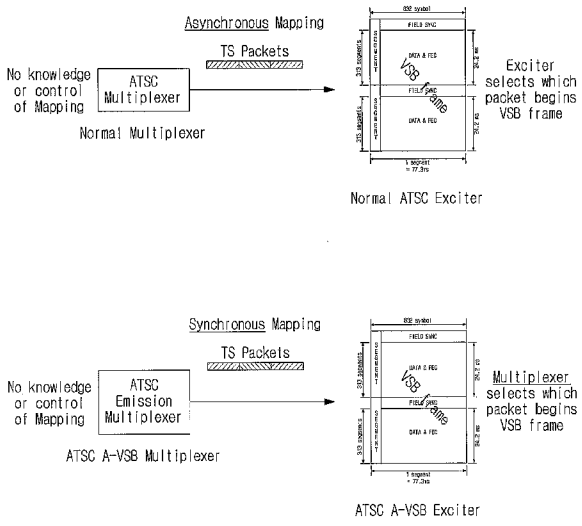
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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, MT, NL, PL,

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(54) Title: METHOD AND APPARATUS FOR TRANSMITTING DIGITAL BROADCASTING SIGNAL IN ADVANCED-VSB (A-VSB) SYSTEM IN WHICH TRANSPORT PACKET WITHOUT ADAPTATION FIELD IS PROVIDED AT FIXED LOCATION IN DATA FIELD SLICES



(57) Abstract: A method of processing a digital broadcasting signal includes generating a transport stream including a plurality of transport packets; selecting one of the transport packets as a starting packet to be mapped into a first data segment of an encoded data frame; and constructing deterministic data frames in the transport stream beginning with the starting packet; wherein at least one of the 52 transport packets does not have an adaptation field; wherein all remaining ones of the 52 transport packets do have an adaptation field; and wherein the at least one transport packet that does not have an adaptation field is provided at a fixed location in each of the slices.

WO 2007/114663 A1

PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

Description

METHOD AND APPARATUS FOR TRANSMITTING DIGITAL BROADCASTING SIGNAL IN ADVANCED-VSB (A-VSB) SYSTEM IN WHICH TRANSPORT PACKET WITHOUT ADAPTATION FIELD IS PROVIDED AT FIXED LOCATION IN DATA FIELD SLICES

Technical Field

[1] Aspects of the invention relate in part to enhancements to the Advanced Television Systems Committee (ATSC) Digital Television (DTV) System.

Background Art

[2] The ATSC DTV system uses an 8-symbol vestigial sideband (8-VSB) transmission system which is susceptible to reception problems in certain applications and under certain conditions, such as in mobile applications and in communication over channels subject to Doppler fading.

[3] An enhanced version of the 8-VSB system called the Enhanced-VSB (E-VSB) system has been developed. The E-VSB system enables an enhanced or robust data stream to be transmitted. This enhanced or robust data stream is intended to solve some of the reception problems that occur in the 8-VSB system. However, the E-VSB system is still susceptible to reception problems. Aspects of the invention have been developed in part in an effort so solve the reception problems that occur in the 8-VSB and E-VSB systems, and includes an enhanced version of these systems known as the Advanced-VSB (A-VSB) system.

Disclosure of Invention

Technical Solution

[4] According to an aspect of the invention, a method of processing a digital broadcasting signal includes generating a transport stream including a plurality of transport packets, each of the transport packets having 187 bytes, each of the bytes having 8 bits, the 187 bytes including 3 packet identifier (PID) bytes; selecting one of the transport packets as a starting packet to be mapped into a first data segment of an encoded data frame; and constructing deterministic data frames in the transport stream beginning with the starting packet, each of the deterministic data frames having 2 data fields, each of the data fields having 6 slices, each of the slices having 52 transport packets; wherein at least one of the 52 transport packets does not have an adaptation field and has 187 bytes, each of the bytes having 8 bits, the 187 bytes including 3 PID bytes, followed by 184 data bytes; wherein all remaining ones of the 52 transport

packets each have 187 bytes, each of the bytes having 8 bits, the 187 bytes including 3 PID bytes, followed by 2 adaptation field (AF) header bytes specifying an adaptation field having a length of N bytes, followed by N adaptation field bytes, followed by 182-N data bytes; and wherein the at least one transport packet that does not have an adaptation field is provided at a fixed location in each of the slices.

[5] Additional aspects and/or advantages of the invention will be set forth in part in the description which follows and, in part, will be obvious from the description, or may be learned by practice of the invention.

Advantageous Effects

[6] While described in the context of an ATSC system for use in digital television, it is understood that aspects of the invention can be used in other transmission systems.

[7] Furthermore, statistical multiplexing has proven very efficient for transmitting multiple streams over a single channel, and most broadcasters have adopted it or can be expected to adopt it in the future. Statistical multiplexing is a packet mode communication system, as is A-VSB according to an aspect of the invention, and thus offers another opportunity for implementing A-VSB.

Brief Description of the Drawings

[8] These and/or other aspects and advantages of the invention will be become apparent and more readily appreciated from the following description of embodiments of the invention, taken in conjunction with the accompanying drawings of which:

[9] FIG. 1 shows asynchronous and synchronous mappings of ATSC transport stream (TS) packets to a VSB frame according to an aspect of the invention, with the synchronous mapping producing a deterministic frame (DF) according to an aspect of the invention;

[10] FIG. 2 shows a block diagram of pre-coders/trellis encoders used to illustrate an aspect of the invention;

[11] FIG. 3 shows a normal VSB and an A-VSB frame according to an aspect of the invention;

[12] FIG. 4 shows a circuit for performing a deterministic trellis reset (DTR) according to an aspect of the invention;

[13] FIG. 5 shows a block diagram of an ATSC DTV transmitter using a supplementary reference sequence (SRS) according to an aspect of the invention;

[14] FIG. 6 shows a block diagram of an ATSC emission multiplexer using SRS according to an aspect of the invention;

[15] FIG. 7 shows a normal TS packet syntax according to an aspect of the invention;

[16] FIG. 8 shows a TS packet without SRS according to an aspect of the invention;

[17] FIG. 9 shows a normal transport stream according to an aspect of the invention;

[18] FIG. 10 shows a normal TS packet syntax with an adaptation field according to an aspect of the invention;

[19] FIG. 11 shows an SRS-carrying TS packet according to an aspect of the invention;

[20] FIG. 12 shows a transport stream with SRS packets according to an aspect of the invention;

[21] FIG. 13 shows a block diagram of an SRS stuffer according to an aspect of the invention;

[22] FIG. 14 shows a transport stream carrying SRS according to an aspect of the invention;

[23] FIG. 15 shows a transport stream carrying SRS with parity added by the Reed-Solomon encoder in FIG. 5 according to an aspect of the invention;

[24] FIG. 16 shows an ATSC byte interleaver output for N = 26(SRS)+2(AF header) according to an aspect of the invention;

[25] FIG. 17 shows the meaning of "0th bytes [0,..,-51 packets]" according to an aspect of the invention;

[26] FIG. 18 conceptually shows how an ATSC byte interleaver converts 52 segments each containing 26 bytes of SRS pattern data in a transport stream into 26 segments each containing 52 contiguous bytes of SRS pattern data in a transmission stream;

[27] FIG. 19 shows a block diagram of a trellis-coded modulation (TCM) encoder block with parity correction according to an aspect of the invention;

[28] FIG. 20 shows a detailed block diagram of the TCM encoder block in FIG. 19 according to an aspect of the invention;

[29] FIG. 21 shows one slice (52 segments) of a deterministic frame (DF) template for use with SRS according to an aspect of the invention;

[30] FIG. 22 shows pattern byte values stored in an SRS pattern memory according to an aspect of the invention;

[31] FIG. 23 shows an ATSC byte interleaver output when 35 bytes of SRS pattern data are used which shows why more than 27 bytes of SRS pattern data cannot be used;

[32] FIG. 24 shows how a slice boundary cuts off the region labeled "C" in FIG. 16 in segments 5 through 9;

[33] FIG. 25 shows an ATSC byte interleaver output for 27 bytes of SRS pattern data (the maximum permissible number of bytes of pattern data) appearing in segments 5 through 31;

[34] FIG. 26 shows one slice (52 segments) of a deterministic frame (DF) template for use with SRS according to an aspect of the invention that includes a {Null, PAT, PMT} packet without an adaptation field is provided at a fixed location in a frame;

[35] FIG. 27 conceptually shows a harmonized ATSC single-frequency network (SFN) functionality;

[36] FIG. 28 shows a system configuration for a harmonized SFN and A-VSB functionality;

[37] FIG. 29 shows insertion of a VSB frame initialization packet (VFIP) in a last (623rd) TS packet in a VSB frame;

[38] FIG. 30 shows byte mapping in an ATSC 52-segment interleaver;

[39] FIG. 31 shows positions of bytes of a VFIP in the ATSC 52-segment interleaver;

[40] FIG. 32 shows byte positions in a VFIP used for deterministic trellis reset (DTR);

[41] FIG. 33 conceptually shows a 1 PPS counter used in an SFN;

[42] FIG. 34 shown SFN synchronization timelines showing timing syntax and semantics for an ATSC SFN;

[43] FIG. 35 shows a block diagram of an ATSC DTV transmitter modified for use with a turbo stream according to an aspect of the invention;

[44] FIG. 36 shows a block diagram of the ATSC emission multiplexer (MUX) for use with a turbo stream in the turbo-modified ATSC DTV transmitter in FIG. 35 according to an aspect of the invention;

[45] FIG. 37 shows a turbo transport stream input to the turbo pre-processor in FIG. 36 according to an aspect of the invention;

[46] FIG. 38 shows a block diagram of the turbo pre-processor in FIG. 36 according to an aspect of the invention;

[47] FIG. 39 shows a turbo transport stream with parity added by the Reed-Solomon (RS) encoder in the turbo pre-processor in FIG. 38 according to an aspect of the invention;

[48] FIG. 40 shows an expansion of one byte to two bytes performed on the turbo transport stream with parity by the placeholder-maker in the turbo pre-processor in FIG. 38 in a 1/2 rate encoding mode according to an aspect of the invention;

[49] FIG. 41 shows an expansion of one byte to four bytes performed on the turbo transport stream with parity by the placeholder-maker in the turbo pre-processor in FIG. 38 in a 1/4 rate encoding mode according to an aspect of the invention;

[50] FIG. 42 shows an expanded turbo transport stream output from the turbo pre-processor in FIG. 38 according to an aspect of the invention;

[51] FIG. 43 shows a transport stream carrying turbo data that is input to the randomizer in the turbo-modified ATSC DTV transmitter in FIG. 35 according to an aspect of the invention;

[52] FIG. 44 shows a transport stream carrying turbo data with parity added by the Reed-Solomon (RS) encoder in the turbo-modified ATSC DTV transmitter in FIG. 35 according to an aspect of the invention;

[53] FIG. 45 shows a block diagram of the turbo post-processor in the turbo-modified ATSC DTV transmitter in FIG. 35 according to an aspect of the invention;

[54] FIG. 46 shows a block diagram of the outer encoder in the turbo post-processor in

FIG. 45 according to an aspect of the invention;

[55] FIG. 47 shows inputs and outputs of the outer encoder in FIGS. 45 and 46 in a 1/2-rate encoding mode according to an aspect of the invention;

[56] FIG. 48 shows inputs and outputs of the outer encoder in FIGS. 45 and 46 in a 1/4-rate encoding mode according to an aspect of the invention;

[57] FIG. 49 shows a graphical explanation of a bit interleaving rule for an interleaving length of 4 used by the outer interleaver in the turbo post-processor in FIG. 45 according to an aspect of the invention;

[58] FIG. 50 shows one slice (52 segments) of a deterministic frame (DF) template for use with turbo stream mode 2 or 4 according to an aspect of the invention;

[59] FIG. 51 shows one slice (52 segments) of a deterministic frame (DF) template for use with turbo stream mode 5 or 6 according to an aspect of the invention;

[60] FIG. 52 shows one slice (52 segments) of a deterministic frame (DF) template for use with both SRS and turbo stream mode 2 or 4 according to an aspect of the invention;

[61] FIG. 53 shows one slice (52 segments) of a deterministic frame (DF) template for use with both SRS and turbo stream mode 5 or 6 according to an aspect of the invention;

[62] FIG. 54 shows an A-VSB mode signaling bit structure used in an A-VSB mode signaling scheme according to an aspect of the invention;

[63] FIG. 55 show Walsh codes of (16) bits used in the A-VSB mode signaling scheme according to an aspect of the invention;

[64] FIG. 56 shows a diagram of an ATSC 52-segment byte interleaver used according to an aspect of the invention;

[65] FIG. 57 shows a first stage of manipulation of 52 input packets with SRS in the byte interleaver in FIG. 56 according to an aspect of the invention;

[66] FIG. 58 shows a second stage of manipulation of the 52 input packets with SRS in the byte interleaver in FIG. 56 according to an aspect of the invention;

[67] FIG. 59 shows a third stage of manipulation of the 52 input packets with SRS in the byte interleaver in FIG. 56 according to an aspect of the invention;

[68] FIG. 60 shows a mapping of 52 input packets performed by the byte interleaver in FIG. 56 according to an aspect of the invention;

[69] FIG. 61 shows a mapping of 104 input packets performed by the byte interleaver in FIG. 56 according to an aspect of the invention; and

[70] FIG. 62 shows a detail of a mapping performed by the byte interleaver in FIG. 56 when 26 bytes are used for SRS according to an aspect of the invention.

Best Mode for Carrying Out the Invention

[71] Reference will now be made in detail to embodiments of the invention, examples of which are shown in the accompanying drawings, wherein like reference numerals refer

to like elements throughout. The embodiments are described below in order to explain the present invention by referring to the figures.

[72] Aspects of the invention described below include deterministic frame (DF), deterministic trellis reset (DTR), supplementary reference sequence (SRS), single-frequency network (SFN), and turbo stream. These aspects of the invention are described in the context of the ATSC DTV 8-VSB system as part of an Advanced-VSB (A-VSB) system, but are not limited to use in such a context.

[73] The following description presumes a familiarity with the Advanced Television Systems Committee (ATSC) Digital Television (DTV) System which incorporates aspects of the MPEG-2 system, details of which are described in the corresponding standards. Examples of such standards which may be relevant are ATSC A/52B, Digital Audio Compression Standard (AC-3, E-AC-3), Revision B, 14 June 2005; ATSC A/53E, ATSC Digital Television Standard (A/53), Revision E, 27 December 2005; Working Draft Amendment 2 to ATSC Digital Television Standard (A/53C) with Amendment 1 and Corrigendum 1; ATSC A/54A, Recommended Practice: Guide to the Use of the ATSC Digital Television Standard, 4 December 2003; ATSC A110/A, Synchronization Standard for Distributed Transmission, Revision A, 19 July 2005; ISO/IEC IS 13818-1:2000(E), Information technology-Generic coding of moving pictures and associated audio information: Systems (second edition) (MPEG-2); and ISO/IEC IS 13818-2:2000(E), Information technology-Generic coding of moving pictures and associated audio information: Video (second edition) (MPEG-2), the contents of which are incorporated herein by reference in their entirety.

[74] Deterministic frame and deterministic trellis reset prepare the 8-VSB system to be operated in a deterministic manner. In the A-VSB system, the emission multiplexer has knowledge of and signals the start of the 8-VSB frame to the A-VSB exciter. This a priori knowledge of the emission multiplexer allows intelligent multiplexing to be performed according to an aspect of the invention.

[75] An absence of adequate equalizer training signals has encouraged receiver designs with an over-dependence on blind equalization techniques. SRS offers a system solution with adequate equalizer training signals coupled with the latest algorithmic advances in receiver design principles to achieve new levels of performance in dynamic environments. SRS improves normal stream reception. However, it is understood that other training sequences can be used in other aspects of the invention.

[76] SFN functionality is provided in the A-VSB system as a fully harmonized approach that works with the other A-VSB features.

[77] Turbo stream according to aspects of the invention provides a new level of error correction capability. This brings robust reception in terms of lower SNR receiver threshold and improvements in multi-path environments. Normal stream reception in a

legacy receiver is not affected by turbo stream.

[78] An initial application of the A-VSB system might be to address reception issues of main stream services in fixed or portable modes of operation in ATSC DTV applications. The A-VSB system is backward compatible and will offer terrestrial broadcasters options to leverage technological change and meet changing consumer expectations going forward.

[79] Deterministic frame (DF) is one element of the A-VSB system, and its purpose is to make the mapping of ATSC transport stream packets a synchronous process. Currently, this mapping is an asynchronous process. The current ATSC multiplexer at a studio produces a fixed-rate transport stream with no knowledge of the 8-VSB physical layer frame structure or mapping of packets. This situation is shown in the top half of FIG. 1.

[80] The normal (A/53) ATSC exciter randomly picks a packet to map into the first segment of a VSB frame. No knowledge of this decision (and hence the temporal position of any transport stream packet in the VSB frame) is known to the upstream multiplexer. In the ATSC A-VSB system disclosed herein, the emission multiplexer makes a deliberate decision of which packet the ATSC exciter should map into the first segment of the VSB frame. This decision is then signaled to the A-VSB exciter which operates as a slave to the emission multiplexer. The starting packet coupled with knowledge of the fixed VSB frame structure, gives the emission multiplexer knowledge of every packet's position in the VSB frame. This situation is shown in the bottom half of FIG. 1. This fundamental change in the selection of the starting packet is called "deterministic frame" (DF). Briefly stated, the A-VSB emission multiplexer will work in harmony with the A-VSB exciter to perform intelligent multiplexing. The DF allows special pre-processing in the emission multiplexer and synchronous post-processing in the exciter.

[81] The deterministic frame enables the use of an emission multiplexer and an A-VSB exciter. The emission multiplexer shown in the bottom half of FIG. 1 is a special-purpose ATSC multiplexer that is used at a studio or a network operations center (NOC) and directly feeds one or more 8-VSB transmitters all having an A-VSB exciter. Hence the term "emission" multiplexer is used. However, other multiplexers may be used and need not be special-purpose multiplexers.

[82] The first compatible change in the ATSC system design is the required locking of both the emission multiplexer transport stream clock and the symbol clock of the A-VSB exciter to a universally available frequency reference. The 10 MHz reference from a GPS receiver is used for this purpose in the example disclosed herein. Locking both the symbol and transport stream clocks to an external reference provides the needed stability and buffer management in a simple, straightforward manner. One

additional benefit to legacy and new ATSC receivers will be a stable ATSC symbol clock, without the jitter that can occur with the current system design. The preferred transport stream interface supported on the emission multiplexer and the A-VSB exciter will be asynchronous serial interface (ASI). However, other clocks and other interfaces can be used.

[83] The emission multiplexer is considered to be a master, and its syntax and semantics will signal to the A-VSB exciter operating as a slave which transport stream packet shall be used as the first VSB data segment in a VSB frame. Since the system is operating with synchronous clocks, the system knows with 100% certainty which 624 transport stream (TS) packets make up a VSB frame with the A-VSB exciter slaved to the syntax and semantics of the emission multiplexer. A simple frame counter that counts 624 TS packets numbered 0 through 623 is provided in the emission multiplexer. When SFN is used as described below, DF is achieved through the insertion of a VSB frame initialization packet (VFIP) in the last (623rd) TS packet in a VSB frame as described in detail below. However, if SFN is not used, then another simple syntax can be used. One example of such a simple syntax is the data frame cadence signal (CS) described in ATSC A/110 which is inserted in a transport stream by inverting the value of a MPEG-2 packet sync byte once every 624 packets. The normal value of the MPEG-2 packet sync byte is 0x47, and the inverted value of the MPEG-2 packet sync byte is 0xB8. This syntax can be applied to aspects of the invention by inserting in each encoded data frame a frame construction starting signal indicating that construction of a new frame is be started by inverting the value of a data segment sync byte once every 624 data segments beginning in a first one of the encoded data frames with a selected one of the data segments corresponding to a transport packet that was selected as a starting packet to be mapped into a first data segment of the first one of the encoded data frames. The ATSC VSB frame can be viewed by the emission multiplexer as being divided into 12 groups or slices each having (52) data segments.

[84] Deterministic trellis reset (DTR) is another element of the A-VSB system, and is an operation that resets the trellis-coded modulation (TCM) encoder states (pre-coder and trellis encoder states) in the ATSC exciter to a known deterministic state at selected temporal locations in the VSB frame. FIG. 2 shows that the states of the (12) pre-coder/trellis encoders are random. No external knowledge of these states can be obtained due to the random nature of these states in the current A/53 exciter. The DTR provides a mechanism to force all TCM encoders to a zero state (a known deterministic state).

[85] FIG. 4 shows a circuit of (1 of 12) modified TCM encoders used in an 8-trellis VSB (8T-VSB) system. Two new multiplexer (MUX) circuits have been added to existing

logic gates in the circuit shown. When the reset input is inactive (Reset = 0), the circuit operates as a normal 8-VSB encoder. When the reset input is active (Reset = 1), the circuit performs a state reset operation as described below in conjunction with the following Table 1.

[86] Table 1

[Table 1]

[Table]

Trellis Reset Table

Resetat t = 0	(S0 S1 S2)at t = 0	(X0 X1)at t = 0	(S0 S1 S2)at t = 1	(X0 X1)at t = 1	(S0 S1 S2)Next Stateat t = 2	Output(Z2 Z1 Z0)
1	0,0,0	0,0	0,0,0	0,0	0,0,0	000
1	0,0,1	0,1	0,0,0	0,0	0,0,0	000
1	0,1,0	0,0	1,0,0	1,0	0,0,0	000
1	0,1,1	0,1	1,0,0	1,0	0,0,0	000
1	1,0,0	1,0	0,0,0	0,0	0,0,0	000
1	1,0,1	1,1	0,0,0	0,0	0,0,0	000
1	1,1,0	1,0	1,0,0	1,0	0,0,0	000
1	1,1,1	1,1	1,0,0	1,0	0,0,0	000

[87] The truth table of the two XOR gates in FIG. 4 states that "when both inputs are at like logic levels (either 1 or 0), the output of the XOR gate is always 0 (zero)". Note that there are three D latches (S0, S1, S2) in FIG. 4 that form the memory of the TCM encoder. These can be in one of two possible states, (0 or 1). Therefore, as shown the second column in Table 1, there are (8) possible starting states of the TCM encoder memory. Table 1 shows the logical outcome when the reset input is held active (Reset = 1) for two consecutive symbol clock periods. Regardless of the starting states of the TCM encoder memory, the states are forced to a known zero state (S0=S1=S2=0) after two symbol clock periods. This is shown in the next-to-last column labeled "Next State". Hence, a deterministic trellis reset (DTR) can be forced over two symbol clock periods.

[88] Additionally, zero-state forcing inputs (X0, X1 in FIG. 4) are available. These are TCM encoder inputs which force the TCM encoder states to zero, and they are produced during the two symbol clock periods. The DTR operation can be explained as follows. At the moment of reset, that is, when the reset input becomes active (Reset = 1), the two multiplexers disconnect the normal inputs (D0, D1 in FIG. 4) from the

TCM encoder and connect the zero-state forcing inputs to the TCM encoder for the next two symbol clock periods. Then TCM encoder states are forced to zero by the zero-state forcing inputs. These zero-state forcing inputs play an important role in correcting parity errors induced by a DTR operation as described later.

[89] The appropriate moment to reset the TCM encoder states depends on the application. Some applications for DTR are described below.

[90] If introduced immediately after a DTR operation, a selected bit sequence, based on the known starting states of the TCM encoder, will generate a known pattern of symbols. This is used to generate a supplementary reference sequence (SRS) as described later. The appropriate moment to reset the TCM encoder states is thus the first 2 symbols (4 bits) from each TCM Encoder (1 of 12) that process SRS. This process will create a pattern known to a receiver in known locations of the VSB frame, which will enable the equalizer of the receiver to identify the pattern.

[91] In a single-frequency network (SFN) as described later, the DTR operation is synchronous with DTR stuff bytes carried in the VSB frame initialization packet (VFIP) to cause all of the pre-coder/trellis encoders in all of the exciters in the SFN to assume the same states. Each one of the 12 stuff bytes in the VFIP maps to (1 of 12) pre-coder/trellis encoders in a deterministic fashion.

[92] Although several examples of applications for DTR have been described, the use of DTR is not limited to these applications, and DTR can be used in any application which requires that TCM encoder states be reset to known states at a particular time.

[93] Supplementary reference sequence (SRS) is another element of the A-VSB system. The current ATSC 8-VSB system needs improvement to provide reliable reception in fixed, indoor, and portable environments susceptible to dynamic multi-path interference. The basic principle of SRS is to periodically insert a special known sequence in a deterministic VSB frame in such a way that a receiver equalizer can utilize this known sequence to mitigate dynamic multi-path interference and other adverse channel conditions and adapt itself to a dynamically changing channel.

[94] When the TCM encoder states have been forced to a known deterministic state by a DTR, an appended precalculated known sequence of bits (an SRS pattern) is then processed immediately in a predetermined way at specific temporal locations at the interleaver input of the frame. The resulting symbols at the interleaver output, due to the way the ATSC interleaver functions, will appear as known contiguous symbol patterns in known locations in the VSB frame, which will be available to the receiver as an additional equalizer training sequence. FIG. 3 shows the normal VSB frame on the left and the A-VSB frame on the right with SRS turned on. The A-VSB frame has frequently appearing SRS available to a new A-VSB design ATSC receiver. The data to be used in transport stream packets to create this known symbol sequence is

introduced into the system in a backward compatible way using existing standard mechanisms. This data is carried in the MPEG-2 adaptation field. Hence, existing standards are leveraged, and compatibility is assured.

[95] The RS encoder preceding the interleaver calculates the RS parity. Due to resetting the TCM encoders, the calculated RS parity bytes are wrong and need to be corrected. Thus, an additional processing step corrects parity errors in selected packets. All packets with parity errors will have their RS parity re-encoded. A (52) segment byte interleaver with unique time dispersion properties that generates contiguous SRS pattern bytes is leveraged to have adequate time to re-encode parity bytes. The time required to do this constrains the maximum number of SRS pattern bytes.

[96] To add the SRS feature to the ATSC DTV RF transmission system (the VSB system), an ATSC DTV transmitter is modified as shown in FIG. 5 according to an aspect of the invention. The A-VSB emission multiplexer and TCM blocks are modifications of existing blocks to perform SRS processing, and a new SRS stuffer block is provided. The A-VSB emission multiplexer scheduling algorithm takes into consideration a predefined deterministic frame template for SRS. The generated packets are prepared for SRS post-processing in an A-VSB exciter.

[97] The packets are first randomized, and then the SRS stuffer fills the stuffing area in the adaptation fields of packets with a predefined sequence (SRS pattern data). The stuffing area means an area in which some data are stuffed. For example, the stuffing area may include a Private data flag. Along with all data packets the SRS-containing packets are also processed for forward error corrections with the (207, 187) Reed-Solomon code. After byte interleaving, the packets are encoded in the 2/3 rate trellis encoder block. At every SRS-appearing instant, the deterministic trellis reset (DTR) is performed to generate a known symbol output.

[98] DTR necessarily entails some symbol changes (2 symbols for each TCM encoder) at the SRS-appearing instant. Since these changes occur after Reed-Solomon encoding, the previously calculated RS parity bytes are no longer correct. In order to correct these erroneous parity bytes, the parity bytes are recalculated and the recalculated parity bytes replace the old parity bytes in the TCM with DTR block in FIG. 5. The following blocks are generally the same as the standard ATSC VSB exciter and the data pass through them. Now each block in FIG. 5 will be examined one by one.

[99] An example of an A-VSB emission multiplexer for SRS is shown in FIG. 6. In principle, the service multiplexer for SRS in FIG. 6 places adaptation fields (AF) in all TS packets for later SRS processing. The MPEG-2 TS packet syntax is shown in FIG. 7 according to an aspect of the invention. An MPEG-2 TS packet without AF is depicted in FIG. 8 according to an aspect of the invention which complies with the syntax shown in FIG. 7. This packet has a 1-byte MPEG-2 sync, a 3-byte header, and

184 bytes of payload (resulting in a total 188-byte length). A transport stream with packets without AF is shown in FIG. 9 according to an aspect of the invention.

[100] The adaptation field control in the TS header turns on an adaptation field having a length of (N) bytes which includes a 2-byte adaptation field header, leaving (N-2) bytes to carry SRS pattern data. The packet syntax with AF is shown in FIG. 10 according to an aspect of the invention. The adaptation field is mainly used to adjust a payload size during packetized elementary stream (PES) encapsulation and to carry the PCR and so on. A typical SRS packet is depicted in FIG. 11 according to an aspect of the invention, and a transport stream with SRS packets is depicted in FIG. 12 according to an aspect of the invention, which will be an output of the service multiplexer for SRS shown in FIG. 6.

[101] The frame structure for SRS will now be described. An 8-VSB Frame has 2 data fields. Each data field has a data field sync segment and 312 data segments. A VSB slice is defined as a group of 52 data segments. Since a VSB frame has 2*312/52=12 slices, this 52 data segment granularity fits well with the special characteristics of the ATSC 52 segment VSB interleaver used in the ATSC DTV 8-VSB transmission system.

[102] In a real situation, there are several other pieces of information that must be carried in an adaptation field along with SRS in order to be compatible with the MPEG-2 standard. These other pieces of information can be a program clock reference (PCR), an original program clock reference (OPCR), a splice counter, private data, and so on. From the ATSC and MPEG-2 perspective of an emission multiplexer, the PCR and the splice counter must be carried when needed along with the SRS. This imposes a constraint during TS packet generation since the PCR is located where the first 6 SRS pattern bytes would be stuffed. This constraint can easily be accommodated by using the deterministic frame (DF) element of the A-VSB system. Since the A-VSB frame structure must be deterministic, positions of data segments with PCR are fixed. An exciter designed for SRS knows the temporal position of the PCR and the splice counter, and properly stuffs the SRS pattern bytes to avoid overwriting the PCR and the splice counter. FIG. 21 shows one slice (52 segments) of a deterministic frame (DF) template for use with SRS according to an aspect of the invention. The SRS DF template stipulates that the 15-th (19-th) segment in every slice can be a PCR (splice counter)-carrying packet. This is based on the fact that broadcasters generally use only the PCR and splice counter of the MPEG-2 standard. However, the MPEG-2 standard provides for many other types of data to be transmitted in the TS packets, such as OPCR, adaptation field extension length, private data, etc., and if such data is required by broadcasters in the future, the SRS DF template may be modified to protect such data from being overwritten by SRS pattern data.

[103] The MPEG-2 standard requires that a PCR-carrying packet appear in the transport stream at least once every 100 ms. The ATSC standard uses MPEG-2 transport packets, and has the same requirement that a PCR-carrying packet appear in the transport stream at least once every 100 ms. The Digital Video Broadcasting (DVB) standard, which is an alternative to the ATSC standard, and which, like the ATSC standard, uses MPEG-2 transport streams, requires that a PCR-carrying packet appear in the transport stream at least once every 40 ms. When using SRS in the A-VSB system described herein, the 15th segment in every slice of the transport stream is a PCR-carrying packet. Each slice takes 4.03 ms, so a PCR-carrying packet appears every 4.03 ms, thus far exceeding the requirements of the MPEG-2, ATSC, and DVB standards.

[104] Obviously, a normal payload data rate with SRS will be reduced depending on (N-2) bytes of SRS pattern data in FIG. 14. (N-2) can be 0 through 26, with 0 (no SRS) being normal ATSC 8-VSB. The recommended (N-2) bytes of SRS pattern data are {10, 20, 26} bytes. The following Table 2 lists four SRS modes {0, 1, 2, 3} corresponding to (N-2) bytes of {0, 10, 20, 26}, wherein "Mbps" means megabits per second. However, other modes can be defined in other aspects of the invention.

[105] Table 2

[Table 2]

[Table]

Recommended SRS-n

SRS Mode	Mode 0	Mode 1	Mode 2	Mode 3
SRS Length	0 byte	10 bytes	20 bytes	26 bytes
Payload Loss	0 Mbps	1.24 Mbps	2.27 Mbps	2.89 Mbps

[106]

[107] SRS modes are signaled to the exciter from the emission multiplexer, and are Walsh coded in bytes reserved for A-VSB in the data field sync segment. The detailed signaling scheme is described below in the section entitled "A-VSB Mode Signaling Scheme". Table 2 shows also the payload loss associated with each mode. Since 1 slice takes 4.03 ms, the payload loss due to SRS of 10 bytes is 1.24 Mbps as calculated by the following expression:

[108] MathFigure 1

[Math.1]

$$\frac{(10+2)bytes \cdot 52 packets}{4.03ms} \cdot 8 = 1.24Mbps$$

[109] Similarly, the payload loss due to SRS of 20 bytes is 2.27 Mbps, and the payload loss due to SRS of 26 bytes is 2.89 Mbps.

[110] The basic operation of the SRS stuffer is to fill the SRS pattern bytes to the stuffing area of AF in each TS packet. In FIG. 13, the SRS pattern memory is activated by the control signal at SRS stuffing time. The control signal also switches the output of the SRS stuffer to the SRS pattern memory. FIG. 14 depicts the transport stream carrying SRS pattern bytes in the AF according to an aspect of the invention.

[111] The SRS stuffer must not overwrite a PCR when a PCR-carrying packet is sent in a multiplex stream. Since the exciter knows that the 15-th packet in a slice from the emission multiplexer carries a PCR, the SRS stuffer can protect a PCR of the packet. Similarly, the SRS stuffer can also protect a splice counter. However, it is understood that other packet elements can be designated for protection in other aspects of the invention.

[112] FIG. 22 shows pattern byte values stored in an SRS pattern memory. These values are designed to give a good performance for equalization in a receiver. The values in the light gray diagonal band, ranging from 0 to 15, are fed to the TCM encoders at DTR. The 4 MSBs of these bytes having values 0~15 are effectively replaced with the zero-state forcing inputs in an exciter.

[113] Depending on the selected SRS mode, different ones of these SRS pattern byte values are used. For example, in SRS mode 1, 10 bytes of SRS pattern data per packet are used which results in the values in the 4th to the 13th column in FIG. 22 being used. In SRS mode 2, the values from the 4th to the 23rd column are used. In SRS mode 3, the values from the 4th to the 29th column are used. However, other values can be used in other aspects of the invention.

[114] A transport stream carrying SRS is then fed to the Reed-Solomon (RS) encoder in FIG. 5. The output of the RS encoder is shown in FIG. 15, which is an example of a parity-attached version of an SRS-carrying transport stream according to an aspect of the invention.

[115] FIG. 16 shows the output of the byte interleaver in FIG. 5. See the discussion below in the section entitled "ATSC Byte Interleaver Mapping" to understand the exact byte interleaver mapping. FIGS. 57-62 discussed in that section graphically show how to manipulate the input bytes to obtain the final interleaved bytes.

[116] The region labeled "A" in FIG. 16 contains SRS pattern bytes, while the regions labeled "B" contain parity bytes. The region labeled "C" contains bytes to be replaced by DTR, and the regions labeled "D" contain the parity bytes to be recalculated in order to correct the parity mismatch introduced by DTR. The region labeled "E" contains adaptation field header bytes. FIG. 17 explains how to interpret "0th bytes [0, -1, -2,...,-51 packets]" in FIG. 16. A negative packet number means nothing but a

relative order among packets. The -1-th packet is the packet preceding the 0-th packet.

[117] Note that (N) bytes of SRS pattern data contained in 52 segments in FIG. 16 are arranged vertically by the ATSC byte interleaver mapping, resulting in (N) segments each containing 52 contiguous bytes of SRS pattern data. The 52 contiguous bytes of SRS pattern data in each of the (N) segments serve as a training sequence that is used by an SRS-aware equalizer in a receiver.

[118] More specifically, the SRS DF template in FIG. 21 shows that each one of the 52 segments contains 10, 20, or 26 bytes of SRS pattern data in the transport stream. The ATSC byte interleaver converts this arrangement of SRS pattern data in the transport stream into 10, 20, or 26 segments each containing 52 contiguous bytes of SRS pattern data in the transmission stream. FIG. 16 shows an example where 52 segments each containing 26 bytes of SRS pattern data in the transport stream have been converted into 26 segments numbered 5 through 30 each containing 52 contiguous bytes of SRS pattern data in the transmission stream. As can be seen from FIG. 16, the ATSC byte interleaver converts the 52 segments each containing 207 total bytes in the transport stream into 207 segments each containing 52 bytes in the transmission stream. This conversion process is shown conceptually in FIG. 18 in which the top portion corresponds to FIG. 15, the small block in the middle labeled "Byte Interleave" corresponds to the block labeled "Byte Interleave" in FIG. 5, and the bottom portion corresponds to FIG. 16.

[119] FIG. 3 shows an A-VSB frame on the right with SRS turned on. Each of the 12 rhombus-shaped areas in FIG. 3 corresponds to the combination of the regions labeled "A" and "C" in FIG. 3, and contains portions of 10, 20, or 26 segments each containing 52 contiguous bytes of SRS pattern data, or 208 contiguous symbols since 1 byte equals 4 symbols. Thus, a known sequence of 52 contiguous bytes or 208 contiguous symbols of SRS pattern data appears in 120, 240, or 312 segments out of the 626 segments in an A-VSB frame for use as a training sequence by a receiver equalizer. This frequent training of the receiver equalizer is very effective in mitigating dynamic multi-path interference and other adverse channel conditions and adapting to a dynamically changing channel.

[120] FIG. 19 shows a block diagram of a TCM encoder block with parity correction. The RS re-encoder receives zero-state forcing inputs from the TCM encoder block. After synthesizing an RS code information word from the zero-state forcing inputs, the RS re-encoder calculates parity bytes. When the parity bytes to be replaced arrive, these parity bytes are replaced by the values generated by the exclusive-OR of these parity bytes and the recalculated parity bytes from the RS re-encoder.

[121] The trellis encoder block shown in FIG. 19 includes a 12-way data splitter, 12 TCM encoders, and a 12-way data de-splitter as shown in FIG. 20. TCM encoder behavior is

described in Annex D of ATSC A/53E previously referred to above. The 12 trellis encoders for A-VSB have DTR functionality. The zero-forcing inputs are fed to the next block, which calculates the re-encoded parity bytes. However, it is understood that other types of TCM encoders can be used in other aspects of the invention.

[122] As discussed above, the number (N-2) of bytes of SRS pattern data can be 0 through 26 bytes, with recommended modes being 10, 20, and 26 bytes. Actually, up to 27 bytes of SRS pattern data can be used, but it is preferable to use a maximum of 26 bytes of SRS pattern data to provide a safety margin for recalculating parity bytes to correct for the parity mismatch introduced by deterministic trellis reset (DTR) referred to above. When DTR is performed, the 4 MSBs of the SRS pattern byte values shown in the light gray diagonal band in FIG. 22 are effectively replaced with the zero-state forcing inputs in an exciter to reset the TCM encoders. This introduces a parity mismatch, and the parity bytes corresponding to these SRS pattern bytes must be re-calculated in the RS re-encoder in FIG. 19.

[123] FIG. 23 shows an ATSC byte interleaver output which shows why more than 27 bytes of SRS pattern data cannot be used. FIG. 23 is the same as FIG. 16, except that 35 bytes of SRS pattern data are used in FIG. 23, while 26 bytes of SRS pattern data are used in FIG. 16. As in FIG. 16, the region labeled "A" in FIG. 23 contains SRS pattern bytes, while the regions labeled "B" contain parity bytes. The region labeled "C" contains bytes to be replaced by DTR, and the regions labeled "D" contain the parity bytes to be recalculated in order to correct the parity mismatch introduced by DTR. The region labeled "E" contains adaptation field header bytes. As can be seen from FIG. 23, in the segments numbered 32 through 39 corresponding to bytes 28 through 35 of the 35 bytes of SRS pattern data, the SRS pattern bytes in the region labeled "A" appear after the parity bytes to be recalculated in the region labeled "D". This means that the parity bytes to be recalculated in the region labeled "D" corresponding to bytes 28 to 35 of the 35 bytes of SRS pattern data have already passed through the TCM encoder block shown in FIG. 19, making it impossible to recalculate any of the parity bytes to be recalculated in the region labeled "D" for bytes 28 through 35 of the 35 bytes of SRS pattern data.

[124] As can be seen from FIG. 16, the region labeled "C" that contains bytes to be replaced by DTR contains fewer bytes in segments 5 through 9 than in segments 10 through 31. Specifically, the region labeled "C" contains 7 bytes in segment 5, 8 bytes in segment 6, 9 bytes in segment 7, 10 bytes in segment 8, 11 bytes in segment 9, and 12 bytes in each of segments 10 through 31. This is because a slice boundary cuts off the region labeled "C" in segments 5 through 9. A slice boundary is a boundary in the transmission stream between data obtained from two 52-segment slices of data in the transport stream. Thus, if the region labeled "C" contained 12 bytes in each of

segments 5 through 9, some of these bytes would come from one slice and the other bytes would come from another slice. For example, in segment 5, 7 bytes would come from one slice and 5 bytes would come from another slice. Each of the bytes in the region labeled "C" resets one of the 12 trellis encoders in FIG. 2 during DTR. Parity bytes corresponding to the bytes in the region labeled "C" must be recalculated in order to correct the parity mismatch introduced by DTR. This cannot be done for all of the bytes in the other slice because the corresponding parity bytes appear beforehand in the transmission stream as a result of the operation of the ATSC byte interleaver. Since segments 5 to 9 do not contain 12 bytes to be replaced by DTR, it is not possible to initialize all 12 of the trellis encoders in FIG. 2 during DTR for segments 5 to 9. Thus, in segment 5, 7 of the 12 trellis encoders in FIG. 2 are reset during DTR. In segment 6, 8 of the 12 trellis encoders are reset. In segment 7, 9 of the 12 trellis encoders are reset. In segment 8, 10 of the 12 trellis encoders are reset. In segment 9, 11 of the 12 trellis encoders are reset. In each of segments 10 through 31, all 12 of the trellis encoders are reset.

[125] FIG. 24 shows how a slice boundary cuts off the region labeled "C" in FIG. 16 in segments 5 through 9. In FIG. 24, the region labeled "InitializedStuffByte" corresponds to the region labeled "C" in FIG. 16. The slice boundaries are the diagonal lines formed by the bytes from the -50th and -51st TS packets.

[126] FIG. 25 shows an ATSC byte interleaver output for 27 bytes of SRS pattern data (the maximum permissible number of bytes of pattern data) appearing in segments 5 through 31. The region labeled "A" contains trellis encoder initialization bytes that are used to reset the 12 trellis encoders in FIG. 2 during deterministic trellis reset (DTR). The region labeled "B" contains trellis encoder input bytes for generating an SRS training sequence in the transmission stream. The regions labeled "C" contain bytes corresponding to trellis encoders that cannot be initialized in segments 5 through 9. The regions labeled "D" in segments 5 through 10 contain the 6 PCR bytes that are carried in the 15th packet in the transport stream as shown in FIG. 21. The bytes in the regions "D" in segments 5 through 9 correspond to trellis encoders that cannot be initialized. The 12 characters 1 through 9, A, B, and C in FIG. 25 identify the 12 trellis encoders numbered #0 through #11 in FIG. 2. That is, character 1 identifies trellis encoder #0, character 2 identifies trellis encoder #1, and so on, up to character C identifies trellis #11.

[127] As can be seen from the regions labeled "C" and "D" in FIG. 25, in segment 5 (corresponding to byte 1 of the SRS pattern data), the five trellis encoders identified by characters C, 5, 6, 7, and 8 cannot be initialized. In segment 6 (corresponding to byte 2 of the SRS pattern data), the four trellis encoders identified by characters 9, A, B, and C cannot be initialized. In segment 7 (corresponding to byte 3 of the SRS pattern data),

the three trellis encoders identified by characters 6, 7, and 8 cannot be initialized. In segment 8 (corresponding to byte 4 of the SRS pattern data), the two trellis encoders identified by characters 3 and 4 cannot be initialized. In segment 9 (corresponding to byte 5 of the SRS pattern data), the one trellis encoder identified by character C cannot be initialized. In segments 10 through 31 (corresponding to bytes 6 through 27 of the SRS pattern data), all 12 of the trellis encoders can be initialized. The various trellis encoders that cannot be initialized in segments 5 through 9 cannot be used to encode SRS pattern data in those segments because the encoded SRS pattern data would not match the known sequence of SRS pattern data that is expected by the receiver equalizer as a result of the inability to initialize the trellis encoders. Therefore, the SRS stuffer in FIG. 5 is designed not to overwrite the bytes in the regions labeled "C" in FIG. 25 when it stuffs the SRS pattern bytes into the adaptation fields in the transport stream. That is, the SRS stuffer does not fill these bytes with SRS pattern bytes stored in the SRS pattern memory as shown in FIG. 22. Also, the SRS stuffer is designed not to overwrite the bytes in the region labeled "D" in FIG. 25 that contain the 6 PCR bytes that are carried in the 15th packet in the transport stream.

[128] As can be seen from the deterministic frame (DF) template for use with SRS shown in FIG. 21, all segments or packets have an adaptation field. However, the current ATSC constraints on the MPEG-2 standard prevent all packets from having an adaptation field. For example, a packet identified by a program_map_PID (packet identifier) value cannot have an adaptation field for any purpose other than for signaling with the discontinuity_indicator that the version_number (Section 2.4.4.9 of ISO/IEC 13818-1 [C3]) may be discontinuous. Also, a packet identified by PID 0x0000 (the PAT (program association table) PID) cannot have an adaptation field for any purpose other than for signaling with the discontinuity_indicator that the version_number (Section 2.4.4.5 of ISO/IEC 13818-1 [C3]) may be discontinuous.

[129] One way to solve this conflict with the ATSC standard is to repeal the ATSC constraints on the MPEG-2 standard in view of the substantial benefits provided by the use of SRS which enables a receiver equalizer to mitigate dynamic multi-path interference and other adverse channel conditions and adapt itself to a dynamically changing channel.

[130] Another way to solve this conflict with the ATSC standard is to provide a packet without an adaptation field at a fixed location in a frame, similar to what is done by making the 15th packet in a frame a PCR-carrying packet and the 19th packet in a frame a splice counter-carrying packet.

[131] For example, FIG. 26 shows one slice (52 segments) of a deterministic frame (DF) template for use with SRS according to an aspect of the invention in which a {Null, PAT, PMT} packet without an adaptation field is provided at a fixed location in a

frame. PAT stands for program association table, and PMT stands for program map table. When 10 bytes of SRS pattern data are used, the packet without an adaptation field is provided in the 16th packet. When 20 bytes of SRS pattern data are used, the packet without an adaptation field is provided in the 25th packet. When 26 bytes of SRS pattern data are used, the packet without an adaptation field is provided in the 31st packet. However, it is understood that in other aspects of the invention, a different type of packet without an adaptation field can be provided in the 10th, 25th, 31st, or any other packet, and that two or more packets without an adaptation field can be provided at fixed locations in a frame.

[132] If other pieces of information are to be delivered along with the PCR, they can be assigned to a fixed location in a frame just like is done with the PCR. FIG. 26 shows an example where the 15th packet that carries PCR also carries private data and an adaptation field extension length. These other pieces of information will reduce the number of bytes of SRS pattern data that can be carried in the adaptation field of the 15th packet. However, it is understood that in other aspects of the invention, these other pieces of information can be carried in one or more packets other than the 15th packet, and that one or more different other pieces of information can be carried in the 15th packet and/or in one or more packets other than the 15th packet.

[133] As described above, SRS pattern data is carried in an adaptation field of a transport stream packet. However, the invention is not limited to such an implementation, and similar pattern data for training a receiver equalizer can be carried directly in the payload of a transport stream packet using A/90 data piping which is described in ATSC Data Broadcast Standard A/90 (Including Amendment 1 and Corrigendum 1 and Corrigendum 2), July 26, 2000, the contents of which are incorporated herein by reference in their entirety.

[134] A harmonized single-frequency network (SFN) is another element of the A-VSB system. ATSC A/110A, Synchronization Standard for Distributed Transmission, Revision A, 19 July 2005, describes the following three ATSC 8-VSB elements that must be synchronized in each exciter to produce coherent symbols from multiple ATSC 8-VSB transmitters configured into an SFN.

[135] 1. Frequency Synchronization of the 8-VSB Pilot or Carrier

[136] 2. Data Frame Synchronization

[137] 3. Pre-Coder/Trellis Encoder Synchronization

[138] FIG. 27 shows the emission multiplexer outputting an operational and management packet (OMP) with a reserved PID of 0x1FFA approximately once per second. This special packet is called a VSB frame initialization packet (VFIP), and it has the needed syntax and working in harmony with the A-VSB exciter, the semantic meanings are defined to efficiently and effectively create the extensible functionality needed for an

ATSC SFN.

[139] FIG. 28 depicts the system configuration for a harmonized SFN and A-VSB functionality. However, other configurations can be used for other networks.

[140] The frequency synchronization of the 8-VSB pilot or carrier can be achieved by using a well-known technique?by locking the exciter's carrier frequency to a universally available frequency reference such as the 10 MHz reference from a GPS receiver. This synchronization will regulate the apparent Doppler shift seen by the ATSC receiver from the SFN in overlapping coverage areas and should be controlled to ±0.5 Hz.

[141] Data frame synchronization requires that all exciters in an SFN choose the same TS packet from the incoming TS to start a VSB data frame. Data frame synchronization is implicitly achieved in the A-VSB system by the insertion of a VFIP TS packet. The VFIP always appears as the last (624th) TS packet in a VSB frame). The TS packets in a VSB frame are numbered 0 through 623, so the 624th packet is numbered 623. The semantic meaning is that the A-VSB exciter must insert a data field sync segment with no PN63 inversion directly after the last bit of the VFIP. Then it must continue with normal VSB frame construction starting with next TS packet (0) as the first data segment of the next VSB frame.

[142] This simple, straightforward approach is shown in FIG. 29. The ATSC A/53 VSB frame has 624 payload segments. These 624 payload segments carry data equivalent to 624 TS packets. Although the continuous 52-segment convolutional byte interleaver spreads data from any particular TS packet across VSB frame boundaries, one VSB frame carries data equivalent to 624 TS packets. The emission multiplexer has its data rate locked to a 10 MHz external GPS reference. The emission multiplexer simply starts by selecting a TS packet currently being generated and makes the decision that this TS packet will begin a VSB frame, and then starts counting 624 TS packets (o-623) inclusive of this selected packet. This is the container of data which equals the payload in one VSB frame that will be produced downstream by the ATSC exciter. This count (0-623) becomes the data frame cadence signal of the VSB frame. This count (0-623) will always be maintained by the emission multiplexer and is the essence for all timing and future A-VSB pre-processing. This decision now needs to be signaled to all of the exciters participating in the SFN so they can follow the decision made by the emission multiplexer to achieve initial frame synchronization and to maintain this condition.

[143] This is shown in the diagram as the insertion of a VFIP with the reserved PID 0x1FFA as the last packet (623) of a VSB frame. When inserted, the VFIP will appear only in this packet slot (623) and will be inserted at a periodicity as defined in VFIP syntax (normally approximately once per second).

[144] The pre-coder/trellis encoder synchronization is made simple by using the synergy of the element deterministic trellis reset (DTR) element of the A-VSB system. But to understand this synergy requires an in-depth knowledge of the ATSC 52-segment continuous convolutional byte interleaver. FIG. 30 below shows the byte mapping in the ATSC 52-segment interleaver. The bytes are clocked out in a left-to-right direction and sent to the following stages of the trellis intra-segment interleaver and finally the (12) pre-coder/trellis encoders.

[145] Again, a "deterministic" system is a system in which the output can be predicted with 100% certainty. The complexity of this interleaver process is now well understood and will be leveraged and harnessed. This should become one of the temporal strengths of the ATSC system as was previously mentioned. A brief description of this FIG. 31 shows the insertion of data field sync (no PN63 inversion) in response to a VFIP in a last packet slot (623) of the previous frame. (Field sync is really inserted later in process but is shown here to aid understanding.) The diagonal arrows show the positions assumed by bytes of packet 623 (VFIP) in the interleaver. Some of the VFIP bytes reside in the last 52 segment group before the end of the previous frame (not shown). The remaining bytes are in the first 52 segments of current frame (shown). Notice the (4) bytes 52-55, 104-107, 156-159 marked on each of the three diagonal sections at the top. These bytes are marked with legends identifying the (12) pre-coder/trellis encoders numbered 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C (hex) that will receive these bytes when these bytes exit the interleaver, pass through the trellis intra-segment interleaver, and enter into the corresponding ones of the (12) pre-coder/trellis encoders as shown in FIG. 31.

[146] By knowing this with 100% certainty, a deterministic trellis reset (DTR) is triggered in all of the exciters in the SFN when each one of these (12) bytes first enters its respective pre-coder/trellis encoder. This will occur in a serial fashion over (4) segments and effectively synchronizes all (12) pre-coder/trellis encoders in all exciters in a deterministic fashion.

[147] The byte positions (52-55, 104-107, 156-159) used in the VFIP for DTR are shown in FIG. 32. These map into the (12) byte positions shown previously in the interleaver in FIG. 31. Each byte used for DTR will cause a deterministic (1) byte error in the RS decoder when the VFIP is received.

[148] With a total of 12 bytes being used, it is a fact that every VFIP will have a TS packet error because this will cause 12 byte errors which exceeds the 10 byte error correction limit of the RS decoder. The remaining unused space in the VFIP is used for syntax for the timing and control of the SFN, and will be explained next. It should be well understood that VFIP is an operational and management packet (OMP) that allows a very efficient operation of an ATSC SFN. A packet error will never occur in any

packet other than the VFIP. The timing and control syntax carried in the VFIP is protected by additional RS parity, which serves two purposes. First, protecting against errors in the distribution network link to the transmitters, and second, permitting special automated test and measurement (T&M) equipment in the field to recover the payload of the VFIP for network test and measurement purposes.

[149] The timing syntax to be added in the VFIP will allow each exciter to calculate a delay to compensate for the distribution network and to allow tight temporal control of the emission time of the coherent symbols from the antennas of all transmitters in a SFN. This controls the delay spread seen by receivers.

[150] The efficiency of this new synchronization method is that, just by inserting a VFIP, the data frame synchronization becomes implicit. Also, all pre-coder/trellis encoders are synchronized after the first 4 segments of the VSB data frame. This all happens without any need for any syntax in the VFIP itself. This action will cause coherent symbols just by the insertion of a VFIP. To get tight control on emission timing and auxiliary transmitter control, additional syntax is added.

[151] The following Table 3 shows VFIP syntax according to an aspect of the invention.

[152] Table 3

[Table 3]

[Table]

VSB Frame Initialization Packet (VFIP) Syntax

Syntax	**# bits**	**identifier**
transport_packet_header	32	bslbf
om_type	8	bslbf
section_length	8	uimsbf
sync_time_stamp	24	uimsbf
maximum_delay	24	uimsbf
network_id	12	uimsbf
om_tier_test	4	bslbf
for (i=0; i<4; i++) {		
tier_maximum_delay }	24	uimsbf
}		
field_T&M	40	bslbf
for (i=0; i<20; i++) {		
tx_address	12	uimsbf
reserved	4	'1111'
tx_time_offset	16	uimsbf
tx_power	12	uipfmsbf
tx_id_level	3	uimsbf
tx_data_inhibit	1	uimsbf
}		
crc_32	32	rpchof
for (i=0; i<n; i++) {		
stuffing_byte }	8	uimsbf
VFIP_ECC	160	uimsbf

[153] The identifiers in Table 3 have the following meanings. The identifier "bslbf" means "bit string, left bit first". The identifier "uimsbf" means "unsigned integer, most significant bit first". The identifier "uipfmsbf" means "unsigned integer plus fraction, most significant bit first". The identifier "rpchof" means "remainder polynomial co-

efficients, highest order first". Further details of these identifiers are omitted because they are well known in the art.

[154] The sync_time_stamp and maximum_delay syntax elements are used to compensate all of the transmitters in the SFN for the unequal or time-varying delay in the distribution network. The SFN distribution network is normally by connected by a fiber optic, microwave, or satellite link, or by a piece of coax cable if the transmitter is co-located at the studio. The tx_time_offset syntax element is used to fine tune or adjust the timing of each individual transmitter in the SFN.

[155] The emission multiplexer and all exciters in an SFN have a 1 pulse per second (PPS) reference clock and a simple 24-bit binary counter as shown in FIG. 33. This 1 PPS reference clock is used to reset the 24-bit binary counter to zero on the rising edge of the 1 PPS reference clock. The counter is clocked by a 10 MHz frequency reference and counts from 0 to 9,999,999 (0x000000 to 0x98967F hex) in one second, and then resets. This simple counter forms the basis for all time stamps used in the SFN. Note that both the sync_time_stamp and maximum_delay syntax elements have 24 bits. The emission multiplexer generates time stamps by inserting the current value of its 24-bit counter at a reference point in time. Since all counters at all nodes in the SFN are synchronized to the GPS 1 PPS reference clock, their counts are in sync and this simple time stamp mechanism works thanks to GPS.

[156] The SFN synchronization timelines shown in FIG. 34 show the timing syntax and semantics for an ATSC SFN. The VFIP is shown with the main timing syntax elements (sync_time_stamp (STS), maximum_delay (MD), and tx_time_offset (OD)).

[157] A brief description should add clarity to this process. The sync_time_stamp (STS) syntax element is shown and has 24 bits that carry the value of the 24-bit counter in the emission multiplexer observed at the instant that the VFIP leaves the emission multiplexer and enters the distribution network. The maximum_delay (OD) syntax element has 24 bits and indicates the delay that all transmitters will establish. The value of maximum_delay must be longer than the delay of the longest path in the distribution network. Maximum_delay is a system value entered by the network designer. The tx_time_offset (OD) syntax element gives each transmitter an individual fine tuning of delay, and is used to optimize the network. The emission time for each individual transmitter is given by STS + MD + OD = emission time.

[158] The syntax elements listed in Table 3 above are described below.

[159] transport_packet_header-shall conform to ISO 13818-1 systems. The PID value for VFIP shall be 0x1FFA. VFIP is a form of an operational and management packet (OMP) as defined in ATSC A/110 referred to above and as referenced in the ATSC Code Point Registry (Doc. #TSG-575r34, 18 April 2006, available at www.atsc.org/standards). The payload_unit_start_indicator is not used by the VSB

synchronization function and shall be set to 1. The transport_priority value is not used by the VSB synchronization function and shall be set to 1. The transport_scrambling_control value shall be set to 00 (not scrambled). The adaptation_field_control value shall be set to 01 (payload only). When SRS is carried in the adaptation field, the value shall be set to 11 (adaptation field followed by payload). If the maximum 28 bytes is used for SRS (2 bytes for the adaptation field header and 26 bytes for the SRS pattern data), this limits the maximum number of transmitters addressable with one VFIP to 15 in the worst case.

[160] om_type-value shall be set to 0x20, or shall have a value in a range of 0x20-0x2F and be assigned in sequence starting with 0x20. Each VFIP can address up (20) transmitters. This allows each broadcaster a maximum of 320 (high, medium, low) power transmitters including translator stations that can be addressed with the VFIP syntax.

[161] section_length-The section_length specifies the number of bytes following immediately after the section_length field until, and including, the last byte of the crc_32, but not including any stuffing_bytes or the VFIP_ECC.

[162] sync_time_stamp-The sync_time_stamp of the VFIP contains the time difference, expressed as a number of 100-ns intervals, between the latest pulse of the 1 PPS reference clock (derived, e.g., from GPS) the instant the VFIP is transmitted into the distribution network.

[163] maximum_delay-The maximum_delay value shall be larger than the longest delay path in the distribution network. The unit is 100 ns and the range of the maximum_delay value is 0x000000 to 0x98967F, which equals a maximum delay of 1 s.

[164] network_id-A 12-bit unsigned integer field representing the network in which the transmitter is located that provides a seed value for 12 of the 24 bits used to set the symbol sequence of a unique code assigned to each transmitter. All transmitters within a network shall use the same 12-bit pattern.

[165] om_tier_test-A 4-bit field indicating whether a control channel for automated testing and measurement equipment (a T&M channel) is active, and how many tiers of DTV translators are used in the SFN. The leftmost bit indicates whether the T&M channel is active, with (1) indicating that the T&M channel is active and (1) indicating that the T &M channel is inactive. The last three bits indicate the number of tiers of DTV translators in the SFN, with (000) indicating no DTV translators, (001) indicating one tier of DTV translators, (010) indicating two tiers of DTV translators, (011) indicating three tiers of DTV translators, and (100) indicating four tiers of DTV translators.

[166] tier_maximum_delay-The maximum_delay value shall be larger than the longest delay path in the distribution network. The unit is 100 ns and the range of the

maximum_delay value is 0x000000 to 0x98967F, which equals a maximum delay of 1 s.

[167] field_T&M-signaling channel to be determined (TBD) to control remote field T&M and monitoring equipment that is envisioned for the maintenance and operation of an SFN.

[168] tx_address-A 12-bit unsigned integer field that carries the address of the transmitter to which the following fields are relevant and which shall be used to seed a portion of the RF watermark code sequence generator, can also be transmitter in tier of translator SFN.

[169] tx_time_offset-A 16-bit signed integer field that indicates the time offset value, measured in 100-ns intervals, allows for option to fine adjust emission time of each individual transmitter to optimize network timing.

[170] tx_power-A 12-bit unsigned integer plus fraction that indicates the power level to which the transmitter to which it is addressed should be set. The most significant 8 bits indicate the power in integer dBs relative to 0 dBm, and the least significant 4 bits indicate the power in fractions of a dB. When set to zero, tx_power shall indicate that the transmitter to which the value is addressed is not currently operating in the network.

[171] tx_id_level-A 3-bit unsigned integer field that indicates to which of 8 levels (including off) an RF watermark signal of each transmitter shall be set.

[172] tx_data_inhibit-A 1-bit field that indicates when the tx_data information should not be encoded into the RF watermark signal.

[173] crc_32-A 32-bit field that contains a CRC value that gives a zero output of registers in a 32-bit CRC decoder after processing all of the bytes in the VFIP, excluding the stuffing bytes and VFIP_ECC bytes.

[174] stuffing_byte-Each stuffing_byte has a value of 0xFF.

[175] VFIP_ECC-A 160-bit unsigned integer field that carries 20 bytes worth of Reed-Solomon error correcting code used to protect the remaining 164 payload bytes of the packet

[176] The exciter must have a means of accepting a transmitter and antenna delay (TAD) value, which is a 16-bit value representing a number of 100-ns intervals. The TAD value shall include the total delay from the system point at which the transmitter output timing is measured and controlled to the output of the antenna. The value is entered at commissioning of the transmitter site by an engineer who has calculated the exact delay to allow the most accuracy in control of designed delay spread seen by receivers. TAD compensation shall be performed through a calculation carried out by the transmitter using a fixed value of TAD determined for that transmitter.

[177] Turbo stream is another element of the A-VSB system. The turbo stream according

to an aspect of the invention offers a robust bit stream that is independent of the standard normal stream. The turbo stream is thus operational in a backward compatible manner with the standard normal stream. The turbo stream has to be sufficiently tolerant of severe signal distortion to support other broadcasting applications. The robust performance of the turbo stream is achieved by additional forward error correction and an outer interleaver at the cost of some TS rate loss. Apart from an improvement over the low SNR of the standard normal stream, the turbo stream offers an additional advantage of time diversity that is provided by the outer interleaver.

[178] The ATSC DTV exciter is modified as shown in FIG. 35 to enable the turbo stream. An A-VSB emission multiplexer (MUX) receives a normal stream and another TS stream (a turbo stream). Then the ATSC emission multiplexer assembles deterministic frames (DF) for turbo stream. In a selected DF, the emission multiplexer inserts the required placeholders for turbo data, which serve as containers for redundant bits to be generated by the outer encoder in the turbo post-processor.

[179] In the exciter, packets in the frames are randomized and then encoded in the (207, 187) Reed-Solomon code. After byte interleaving, they are manipulated in the turbo processor. After being processed in the 2/3 rate TCM encoder block, they are then combined with data field sync and segment sync symbols to form a VSB frame.

[180] In the ATSC emission multiplexer, a turbo stream pre-processing is carried out. This is shown in FIG. 36. The emission multiplexer accepts turbo TS packets, which have no sync byte (a packet of 187 bytes). The turbo TS packets are pre-processed before being fed to a service multiplexer that generates deterministic frames. FIG. 37 shows an example of a turbo transport stream according to an aspect of the invention. Since the turbo stream is only visible to an A-VSB receiver, the turbo transport stream can be not only a standard MPEG-2 TS but also an advanced codec stream or other like stream in other aspects of the invention.

[181] The turbo pre-processor block is detailed in FIG. 38. The turbo stream is RS encoded and 20 bytes of (207, 187) RS parity are attached to each turbo TS packet. FIG. 39 shows the outputs of the (207, 187) RS encoder. Then, the placeholder-maker in the turbo pre-processor inserts required placeholders by expanding byte by byte. How to insert placeholders depends on the turbo stream rate. When 1/2 rate encoding is in use, one byte is expanded to 2 bytes as shown in FIG. 40. When 1/4 rate coding is in use, one bye is expanded to 4 bytes as shown in FIG. 41. The outputs of the turbo pre-processor are shown in FIG. 42.

[182] Next, the turbo stream service multiplexer inserts the pre-processed turbo TS packets into stuffing areas in adaptation fields of the deterministic frames. Consequently, a turbo TS packet has to be cut (if necessary, at several places) to fit it into these areas. The outputs of the emission multiplexer are shown in FIG. 43. The number of turbo TS

packets accommodated in one field varies depending on the turbo stream mode.

[183] Similar to the DF for SRS, several pieces of information such as PCR and splice counter have to be delivered in the adaptation field along with the turbo stream to be compatible with the MPEG-2 standard. So PCR and splice counter positions are fixed at the 15th and 19th packets in a slice like the case of SRS DF.

[184] FIG. 50 shows one slice (52 segments) of a deterministic frame (DF) template for use with turbo stream mode 2 or 4 according to an aspect of the invention. Turbo TS packets are carried in every 4th packet. In FIG. 50, PCR and splice counter positions are shown in the 15th and 19th packets of a slice.

[185] There are (7) modes defined by an outer encoder code rate and an adaptation field length. The combination of these two parameters is confined to (2) code rates {1/2, 1/4} and (3) adaptation field lengths {86, 128, 384 bytes} in the A-VSB system. This will result in (6) effective turbo data rates. In mode 0, turbo stream is switched off. This is summarized in the following Table 4.

[186] Table 4

[Table 4]

[Table]

Turbo Stream Modes

Stream Mode	0	1	2	3	4	5	6
Turbo Data Bytes (N-2)Per 4 Segments	0	86	128	86	128	384	384
Turbo Data BytesPer Field	0	6708	9984	6708	9984	29952	29952
Turbo PacketsPer Field	0	8	12	16	24	36	72
Used Turbo DataBytes Per Field	0	6624	9936	6624	9936	29808	29808
Unused Turbo BytesPer Field	0	84	48	84	48	144	144
Code Rate		1/4	1/4	1/2	1/2	1/4	1/2
Normal TS Loss(Mbps)	0	2.19	3.30	2.19	3.30	9.88	9.88
Turbo TS Rate(Mbps)	0	0.5	0.75	0.99	1.49	2.24	4.47
Turbo ProcessingBlock (Bits)	0	8944	13312	8944	13312	{13312,39936}	{13312,39936}

[187] A chunk of a truncated turbo packet is called turbo data. In Table 4, turbo data bytes per field means the space reserved for turbo data in the 312 normal packets (one field).

The starting point of a turbo packet will be synchronized to the first byte in the turbo data area in a field. The number of accommodated turbo packets in a field is turbo packets per field in Table 4. Since the number doesn't fit exactly the entire turbo data area, there are some residual bytes (marked "unused" in FIG. 43) at the end. These unused bytes are filled with stuffing bytes in an aspect of the invention.

[188] For example, in turbo stream mode 2, turbo data per field has 128*312/4=9984 bytes. Since 9984 bytes = 12 packets * (207*4) bytes + 48 residual bytes, this accommodates 12 turbo TS packets. The frame structure in turbo stream mode 2 is shown in FIG. 50.

[189] FIG. 51 shows one slice (52 segments) of a deterministic frame (DF) template for use with turbo stream mode 5 or 6 according to an aspect of the invention. In FIG. 51, PCR and splice counter positions are shown in the 15th and 19th packets of a slice. In turbo stream mode 5 or 6, since turbo data per each set of 4 normal packets is 384 bytes (184 bytes*2+16 bytes), two normal packets are entirely dedicated for carrying turbo data. In that case, a null packet is used instead of a normal packet. By using a null packet, the 2 bytes of AF header space that would be required in a normal packet can also carry turbo data. In this way, 184*2 bytes of turbo data are carried in two null packets and the other 16 bytes of turbo data are carried in the AF of the following normal packet as shown in FIG. 51.

[190] The selected turbo stream mode has to be signaled to the exciter and to the receiver by the signaling scheme described below in the section entitled "A-VSB Mode Signaling Scheme".

[191] A randomized transport stream carrying turbo data is then fed to the RS encoder in FIG. 35. The output of the RS encoder is shown in FIG. 44, which is a just parity-attached version of turbo data-carrying transport stream. The next block, the byte interleaver, spreads this stream byte by byte. The spread transport stream is input to the turbo post-processor.

[192] Basically, the turbo post-processor touches only turbo data bytes. Turbo data is extracted in the turbo data extractor. Placeholders in a turbo data byte are filled with redundancy bits added by the outer encoder and turbo data is interleaved in the outer interleaver bit by bit as shown in FIG. 45. The turbo data stuffer puts the processed turbo data in place.

[193] Since the turbo data placeholders are filled here, the RS parity bytes attached in the previous block are no longer correct. These incorrect parity bytes are corrected in the parity correction block after the turbo data stuffer in FIG. 45.

[194] An example of the turbo data extractor shown in FIG. 45 gets turbo data from byte-interleaved packets. The amount of the extracted turbo data is the turbo post-processing block size. This block size is specified in bits in Table 4. For example, the block size in turbo stream modes 1 and 3 is 8944 bits. Consequently, the outer in-

terleaver length is also 8944 bits. The block size in turbo stream modes 2 and 4 is 13312 bits. Consequently, the outer interleaver length is also 13312 bits. The block size in turbo stream modes 5 and 6 is {13312, 39936} bits, which means that the block size is 39936 bits, and the outer interleaver length can be either 39936 bits, or can be 13312 bits repeated three times, since 39936/13312 = 3. That is, an outer interleaver having an outer interleaver length of 39936 can be implemented by three outer interleavers in sequence each having an outer interleaver length of 13312 bits.

[195] An example of the outer encoder used in the turbo processor is depicted in FIG. 46. The outer encoder receives 1 bit (D) and produces 1 bit (Z) in both the 1/2 rate and 1/4 rate modes. The difference between two modes is the manner in which the input bytes having placeholders are treated to generate output bytes. This is clearly explained in FIGS. 47 and 48. In the 1/2 rate mode, (4) bits (D3, D2, D1, D0) per byte are fed to the outer encoder, while in the 1/4 rate mode, (2) bits (D1, D0) per byte are fed to the outer encoder.

[196] At the beginning of a new block, the outer encoder state is set to 0. No trellis-terminating bits are appended at the end of a block. Since the block size is relatively long, the error-correction capability is not deteriorated very much. Possible residual errors are corrected by the high-layer forward error correction (FEC) (RS code) in the turbo pre-processor.

[197] The outer interleaver scrambles the outer encoder output bits. The bit interleaving rule is defined by a linear congruence expression as follows:

[198] MathFigure 2

[Math.2]

$$\Pi(i) = (P \cdot i + D_{i \bmod 4}) \bmod L$$

[199] For a given interleaving length (L), this interleaving rule has 5 parameters (P, D0, D1, D2, D3) which are defined in the following Table 5.

[200] Table 5

[Table 5]

[Table]

Interleaving Rule Parameters

L	P	D_0	D_1	D_2	D_3
8944	45	0	0	2700	7376
13312	81	0	0	2916	12948

[201] Each turbo stream mode specifies the interleaving length (L) as shown in Table 4, where the interleaving length (L) is equal to the turbo processing block size. For example, and without limitation thereto, the interleaving length L = 13312 is used in

turbo stream mode 2. This length corresponds to turbo data symbols within 52 normal packets. Thus, the turbo data extractor in turbo stream mode 2 collects turbo data in 52 normal packets and the outer encoder fills the placeholders. Finally, the outer interleaver takes turbo data to scramble. The interleaving rule is generated as follows in accordance with Table 5:

[202] $$\Pi(i) = \begin{cases} (81 \cdot i) \bmod 13312 & i \bmod 4 == 0,1 \\ (81 \cdot i + 2916) \bmod 13312 & i \bmod 4 == 2 \\ (81 \cdot i + 12948) \bmod 13312 & i \bmod 4 == 3 \end{cases}$$

[203] An interleaving rule is interpreted as "the -th bit in the block is placed in the i-th bit position after interleaving". FIG. 49 explains an interleaving rule of length 4 by way of example. After bit interleaving, the turbo data are stuffed in the AF of the 52 normal packets by the turbo data stuffer.

[204] SRS and turbo stream can also be used together by inserting SRS pattern bytes into the adaptation field of every normal transport packet, and also inserting turbo data into the adaptation fields of at least some normal transport packets.. Depending on the turbo stream mode being used, a normal transport packet may carry SRS pattern bytes, turbo data, and normal data, or may carry SRS pattern bytes and normal data but no turbo data, or may carry SRS pattern bytes and turbo data but no normal data.

[205] FIG. 52 shows one slice (52 segments) of a deterministic frame template for use with both SRS and turbo stream mode 2 or 4 according to an aspect of the invention that is a combination of the deterministic frame template for use with SRS shown in FIG. 21, and the deterministic frame template for use with turbo stream mode 2 or 4 shown in FIG. 50. In turbo stream mode 2 or 4, turbo data per each set of 4 normal packets is 128 bytes. Thus, the first normal packet in each set of 4 normal packets carries 128 bytes of turbo data and 54-{10, 20, 26} bytes of normal data, and the second, third, and fourth normal packets in each set of 4 normal packets each carry 182-{10, 20, 26} bytes of normal data, where {10, 20, 26} indicates the number of bytes of SRS pattern data that are being used, i.e., 10, 20, or 26 bytes.

[206] Thus, if 10 bytes of SRS pattern data are being used, the first normal packet carries 128 bytes of turbo data and 54-10=44 bytes of normal data, and the second, third, and fourth normal packets each carry 182-10=172 bytes of normal data. If 20 bytes of SRS pattern data are being used, the first normal packet carries 128 bytes of turbo data and 54-20=34 bytes of normal data, and the second, third, and fourth normal packets each carry 182-20=162 bytes of normal data. If 26 bytes of SRS pattern data are being used, the first normal packet carries 128 bytes of turbo data and 54-26=28 bytes of normal data, and the second, third, and fourth normal packets each carry 182-26=156 bytes of normal data.

[207] FIG. 53 shows one slice (52 segments) of a deterministic frame template for use with

both SRS and turbo stream mode 5 or 6 according to an aspect of the invention that is a combination of the deterministic frame template for use with SRS shown in FIG. 21, and the deterministic frame template for use with turbo stream mode 5 or 6 shown in FIG. 51. In turbo stream mode 5 or 6, turbo data per each set of 4 normal packets is 384 bytes. Thus, the first and second normal packets in each set of 4 normal packets each carry 182-{10, 20, 26} bytes of turbo data, the third normal packet in each set of 4 normal packets carries 20+2*{10, 20, 26} bytes of turbo data and 162-3*{10, 20, 26} of normal data, and the fourth normal packet in each set of 4 normal packets carries 182-{10, 20, 26} bytes of normal data, where {10, 20, 26} indicates the number of bytes of SRS pattern data that are being used, i.e., 10, 20, or 26 bytes.

[208] Thus, if 10 bytes of SRS pattern data are being used, the first and second normal packets each carry 182-10=172 bytes of turbo data, the third normal packet carries 20+2*10=40 bytes of turbo data and 162-3*10=132 bytes of normal data, and the fourth normal packet carries 182-10=172 bytes of normal data. If 20 bytes of SRS pattern data are being used, the first and second normal packets each carry 182-20=162 bytes of turbo data, the third normal packet carries 20+2*20=60 bytes of turbo data and 162-3*20=102 bytes of normal data, and the fourth normal packet carries 182-20=162 bytes of normal data. If 26 bytes of SRS pattern data are being used, the first and second normal packets each carry 182-26=156 bytes of turbo data, the third normal packet carries 20+2*26=72 bytes of turbo data and 162-3*26=84 bytes of normal data, and the fourth normal packet carries 182-26=156 bytes of normal data.

[209] A-VSB Mode Signaling Scheme

[210] The SRS and turbo stream features described above assume that each mode is known to an A-VSB receiver. The A-VSB mode signaling scheme fulfils this task.

[211] A mode signaling standard will now be described. Information about the current mode is transmitted in 104 reserved symbols of each data field sync segment. Specifically, as shown in FIG. 54, symbols 1 through 48 of the 104 reserved symbols are allocated for transmitting information about SRS and turbo stream modes, symbols 49 through 82 are reserved, symbols 83 and 84 are reserved, and symbols 85 through 92 are allocated for enhanced data transmission methods. In even data fields, the polarities of symbols 83 through 92 shall be inverted from the polarities of symbols 83 through 92 in odd data fields. Symbols 93 through 102 are allocated for precode. However, it is understood that other allocations can be used in other aspects of the invention.

[212] For more information, refer to "Working Draft Amendment 2 to ATSC Digital Television Standard (A/53C) with Amendment 1 and Corrigendum 1" referred to above which is incorporated herein by reference in its entirety.

[213] An A-VSB mode signaling bit structure will now be described. Walsh codes of (16)

bits are used in the data field sync segment to distinguish different between different SRS and turbo stream modes. The first (16) bit slots specify an SRS mode. The second and third (16) bit slots specify turbo stream modes, where the second (16) bit slots specify a turbo stream data rate and the third (16) bit slots specify a coding rate. The (34) bits are reserved for future use. The A-VSB mode signaling bit structure is summarized in FIG. 54. Examples of the Walsh codes of (16) bits are shown in FIG. 55, wherein the "Modulation Symbol Index" is the Walsh code number (#), and the "Walsh Chip within Symbol" is the individual elements of the Walsh codes. However, it is understood that other A-VSB mode signaling bit structures can be used in other aspects of the invention.

[214] Examples of mappings between Walsh codes and A-VSB modes are as follows.

[215] An example of a mapping between numbers of SRS pattern bytes per packet and Walsh codes of (16) bits is shown in the following Table 6:

[216] Table 6

[Table 6]

[Table]

Mapping of SRS-n

SRS Pattern Bytes Per Packet	Walsh Code # Used
0	1
10	3
20	6
26	14

[217]

[218] The unused Walsh codes of (16) bits are reserved for other numbers of SRS pattern bytes per packet which can be used in other aspects of the invention. However, it is understood that mappings other than that shown in Table 6 can be used in other aspects of the invention.

[219] An example of a mapping between turbo data rates and Walsh codes of (16) bits is shown in the following Table 7:

[220] Table 7

[Table 7]

[Table]

Mapping of Turbo Data Rate

Turbo DataMix Ratio	Turbo Data BytesPer 4 Segments	Turbo Data Rate		Used WalshCode #
		1/2 Coding	1/4 Coding	
0	0			3
10.27%	86	0.99(16 Packet)	0.5(8 Packet)	4
15.46%	128	1.49(24 Packet)	0.75(12 Packet)	9
46.26%	384	4.47(72 Packet)	2.24(36 Packet)	12

[221] The unused Walsh codes of (16) bits are reserved for other turbo data rates which can be used in other aspects of the invention. However, it is understood that mappings other than that shown in Table 7 can be used in other aspects of the invention.

[222] If necessary, the turbo data mix ratio shown in Table 7 can be increased to 100% in the future.

[223] An example of a mapping between coding rates and support of multiple turbo streams and Walsh codes of (16) bits is shown in the following Table 8:

[224] Table 8

[Table 8]

[Table]

Mapping of Other Parameters

Item	Walsh Code # Used
# of Turbo Streams 0	2
# of Turbo Streams 1, Coding Rate 1/2	5
# of Turbo Streams 1, Coding Rate 1/4	7
# of Turbo Streams 2, Coding Rate 1/2	9
# of Turbo Streams 2, Coding Rate 1/4	11

[225] The unused Walsh codes are reserved for other configurations which can be used in other aspects of the invention. However, it is understood that mappings other than that shown in Table 8 can be used in other aspects of the invention.

[226] The last 50 bits shall be reserved space. It is suggested that these bits be filled with a

continuation of inverting values of Walsh codes of (16) bits for SRS modes and turbo data rates.

[227] All data field sync segments transmit the current mode. When the current mode changes to the next mode, the next mode is transmitted in even data field sync segments during the next 16 frames. After the next 16 frames, the next mode becomes valid, the system operates in the next mode, and all data field sync segments transmit the next mode.

[228] ATSC Byte Interleaver Mapping

[229] FIG. 56 shows a diagram of an ATSC 52-segment byte interleaver that is a part of the ATSC 8-VSB system. Since it is crucial to understand the exact mapping of the byte interleaver for A-VSB, a graphical mapping procedure is developed.

[230] FIG. 57 shows a first stage of manipulation of 52 input packets with SRS in the byte interleaver in FIG. 56. FIG. 58 shows a second stage of manipulation of the 52 input packets with SRS in the byte interleaver in FIG. 56. FIG. 59 shows a third stage of manipulation of the 52 input packets with SRS in the byte interleaver in FIG. 56.

[231] FIG. 60 shows a mapping of 52 input packets performed by the byte interleaver in FIG. 56, and FIG. 61 shows a mapping of 104 input packets performed by the byte interleaver in FIG. 56.

[232] FIG. 62 shows a detail of a mapping performed by the byte interleaver in FIG. 56 when 26 bytes are used for SRS.

[233] Although several embodiments of the invention have been shown and described, it would be appreciated by those skilled in the art that changes may be made in these embodiments without departing from the principles and spirit of the invention, the scope of which is defined in the claims and their equivalents.

Claims

[1] A method of processing a digital broadcasting signal, comprising:
generating a transport stream comprising a plurality of transport packets, each of the transport packets having 187 bytes, each of the bytes having 8 bits, the 187 bytes including 3 packet identifier (PID) bytes;
selecting one of the transport packets as a starting packet to be mapped into a first data segment of an encoded data frame; and
constructing deterministic data frames in the transport stream beginning with the starting packet, each of the deterministic data frames having 2 data fields, each of the data fields having 6 slices, each of the slices having 52 transport packets;
wherein at least one of the 52 transport packets does not have an adaptation field and has 187 bytes, each of the bytes having 8 bits, the 187 bytes including 3 PID bytes, followed by 184 data bytes;
wherein all remaining ones of the 52 transport packets each have 187 bytes, each of the bytes having 8 bits, the 187 bytes including 3 PID bytes, followed by 2 adaptation field (AF) header bytes specifying an adaptation field having a length of N bytes, followed by N adaptation field bytes, followed by 182-N data bytes; and
wherein the at least one transport packet that does not have an adaptation field is provided at a fixed location in each of the slices.

[2] The method of claim 1, wherein the at least one transport packet that does not have an adaptation field is a null packet.

[3] The method of claim 2, wherein the null packet is a {Null, PAT, PMT} packet, with PAT being a program association table, and PMT being a program map table.

[4] The method of claim 1, wherein one of the 52 transport packets does not have an adaptation field; and
wherein 51 of the 52 transport packets do have an adaptation field.

[5] The method of claim 1, wherein a number of the transport packets that have an adaptation field is greater than a number of the transport packets that do not have an adaptation field.

[6] The method of claim 1, further comprising inserting a supplementary reference sequence (SRS) in the transport stream by inserting SRS pattern bytes in the adaptation fields of the transport packets that have an adaptation field so that at least some of the N adaptation field bytes are SRS pattern bytes.

[7] The method of claim 6, wherein the fixed location of the at least one transport packet that does not have an adaptation field depends on a number of SRS

pattern bytes in the adaptation field of each of the transport packets that have an adaptation field.

[8] The method of claim 7, wherein there are 10 SRS pattern bytes in the adaptation field of each of the transport packets that have an adaptation field; and
wherein the at least one transport packet that does not have an adaptation field is one transport packet that does not have an adaptation field and is provided in the 16th packet of each of the slices.

[9] The method of claim 7, wherein there are 20 SRS pattern bytes in the adaptation field of each of the transport packets that have an adaptation field; and
wherein the at least one transport packet that does not have an adaptation field is one transport packet that does not have an adaptation field and is provided in the 25th packet of each of the slices.

[10] The method of claim 7, wherein there are 26 SRS pattern bytes in the adaptation field of each of the transport packets that have an adaptation field; and
wherein the at least one transport packet that does not have an adaptation field is one transport packet that does not have an adaptation field and is provided in the 31st packet of each of the slices.

[11] The method of claim 1, wherein the deterministic data frames comply with ATSC (Advanced Television Systems Committee) constraints on an MPEG-2 transport stream.

[12] A method of processing a digital broadcasting signal, comprising:
generating a transport stream comprising a plurality of transport packets, each of the transport packets having 187 bytes, each of the bytes having 8 bits, the 187 bytes including 3 packet identifier (PID) bytes;
selecting one of the transport packets as a starting packet to be mapped into a first data segment of an encoded data frame; and
constructing deterministic data frames in the transport stream beginning with the starting packet, each of the deterministic data frames having 2 data fields, each of the data fields having 6 slices, each of the slices having 52 transport packets;
wherein at least one of the 52 transport packets does not have an adaptation field and has 187 bytes, each of the bytes having 8 bits, the 187 bytes including 3 PID bytes, followed by 184 data bytes;
wherein all remaining ones of the 52 transport packets each have 187 bytes, each of the bytes having 8 bits, the 187 bytes including 3 PID bytes, followed by 2 adaptation field (AF) header bytes specifying an adaptation field having a length of N bytes, followed by N adaptation field bytes, followed by 182-N data bytes; and
wherein the method further comprises inserting a supplementary reference

sequence (SRS) in the transport stream by inserting SRS pattern bytes in the adaptation fields of the transport packets that have an adaptation field so that at least some of the N adaptation field bytes are SRS pattern bytes.

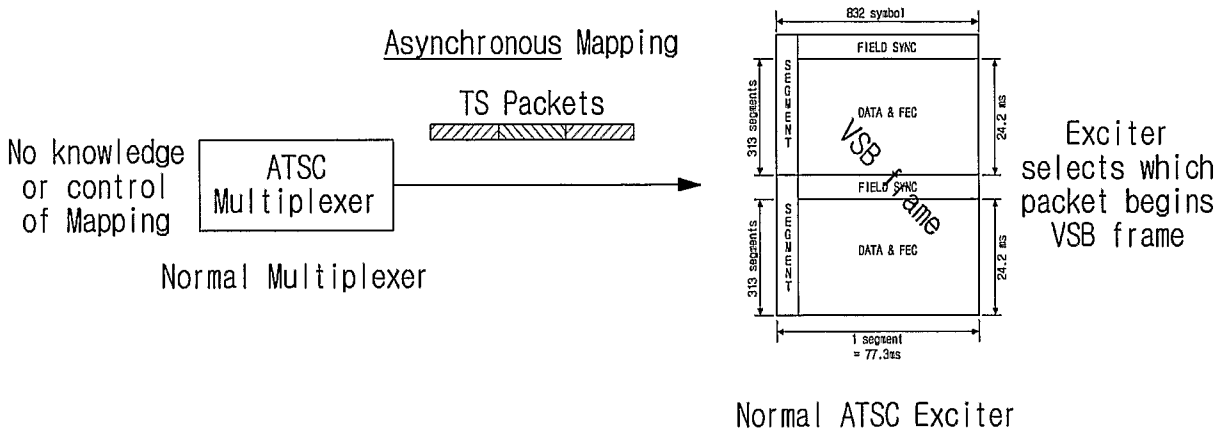
[13] The method of claim 12, wherein the at least one transport packet that does not have an adaptation field is a null packet.

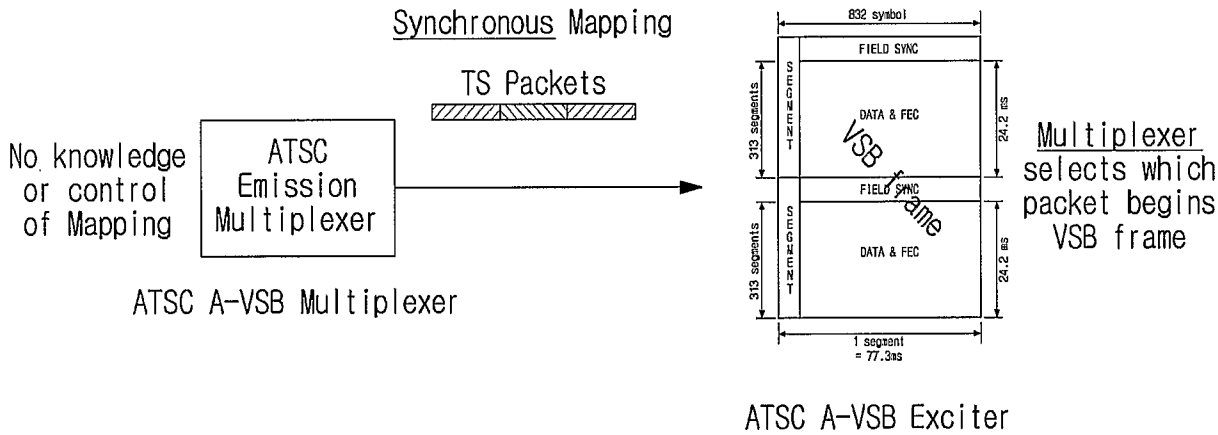
[14] The method of claim 13, wherein the null packet is a {Null, PAT, PMT} packet, with PAT being a program association table, and PMT being a program map table.

[15] The method of claim 12, wherein one of the 52 transport packets does not have an adaptation field; and
wherein 51 of the 52 transport packets do have an adaptation field.

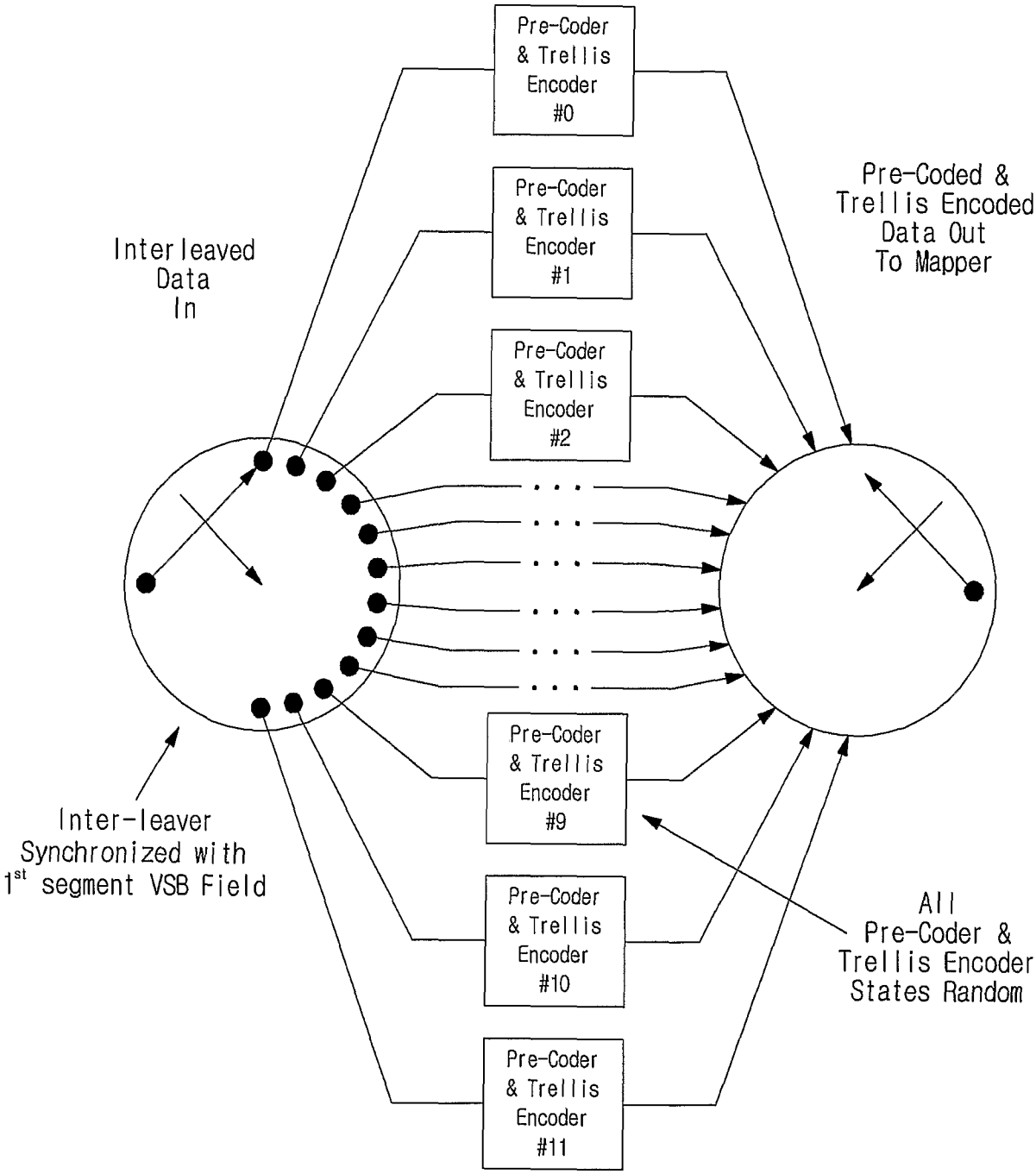
[16] The method of claim 12, wherein a number of the transport packets that have an adaptation field is greater than a number of the transport packets that do not have an adaptation field.

[17] The method of claim 12, wherein the deterministic data frames comply with ATSC (Advanced Television Systems Committee) constraints on an MPEG-2 transport stream.

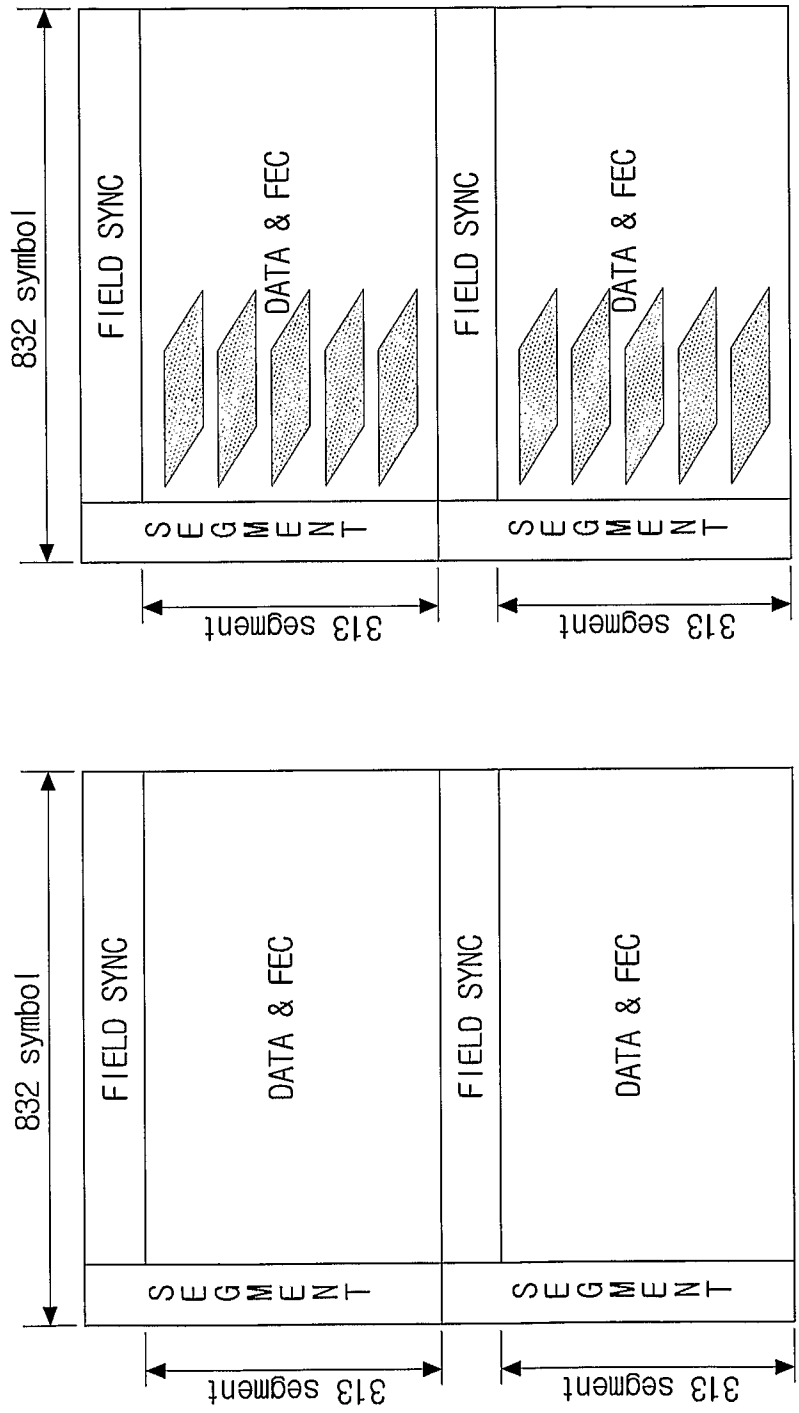

Asynchronous Mapping
TS Packets
No knowledge or control of Mapping
ATSC Multiplexer
Normal Multiplexer
832 symbol
FIELD SYNC
DATA & FEC
VSB frame
313 segments
24.2 ms
1 segment = 77.3ms
Exciter selects which packet begins VSB frame
Normal ATSC Exciter


Synchronous Mapping
TS Packets
No knowledge or control of Mapping
ATSC Emission Multiplexer
ATSC A-VSB Multiplexer
832 symbol
FIELD SYNC
DATA & FEC
VSB frame
313 segments
24.2 ms
1 segment = 77.3ms
Multiplexer selects which packet begins VSB frame
ATSC A-VSB Exciter

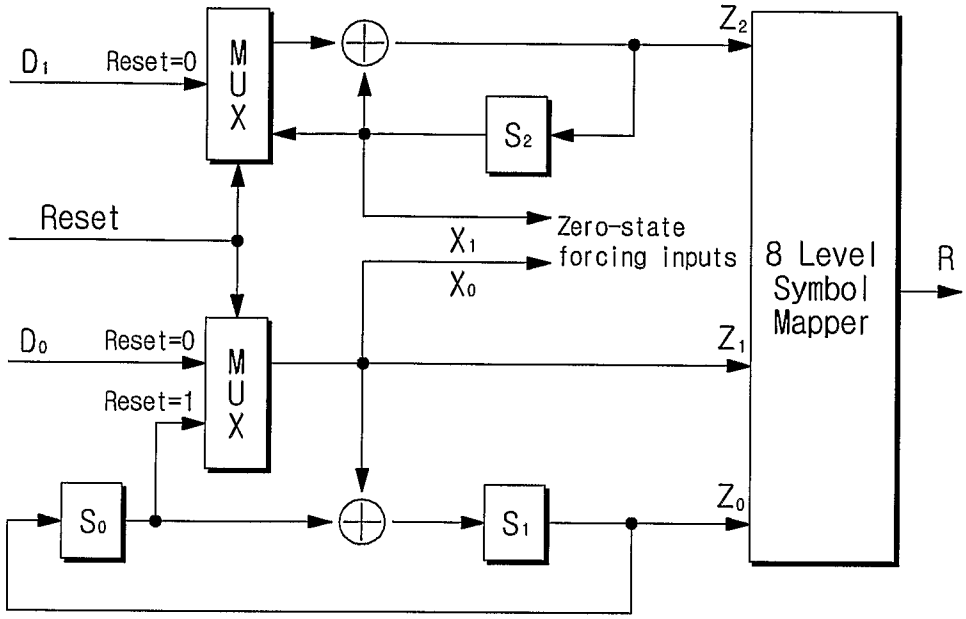
[Fig. 2]


Pre-Coder & Trellis Encoder #0
Pre-Coder & Trellis Encoder #1
Pre-Coder & Trellis Encoder #2
Pre-Coder & Trellis Encoder #9
Pre-Coder & Trellis Encoder #10
Pre-Coder & Trellis Encoder #11
Interleaved Data In
Pre-Coded & Trellis Encoded Data Out To Mapper
Inter-leaver Synchronized with 1st segment VSB Field
All Pre-Coder & Trellis Encoder States Random

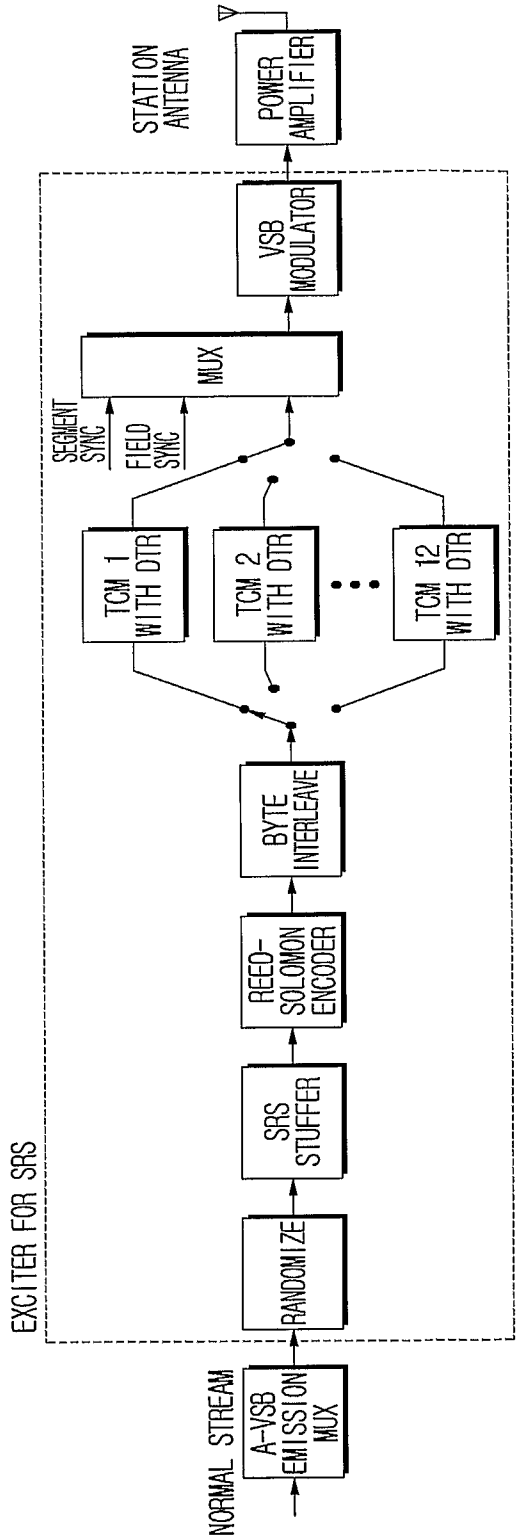
[Fig. 3]


832 symbol
FIELD SYNC
DATA & FEC
FIELD SYNC
DATA & FEC
SEGMENT
SEGMENT
313 segment
313 segment
832 symbol
FIELD SYNC
DATA & FEC
FIELD SYNC
DATA & FEC
SEGMENT
SEGMENT
313 segment
313 segment

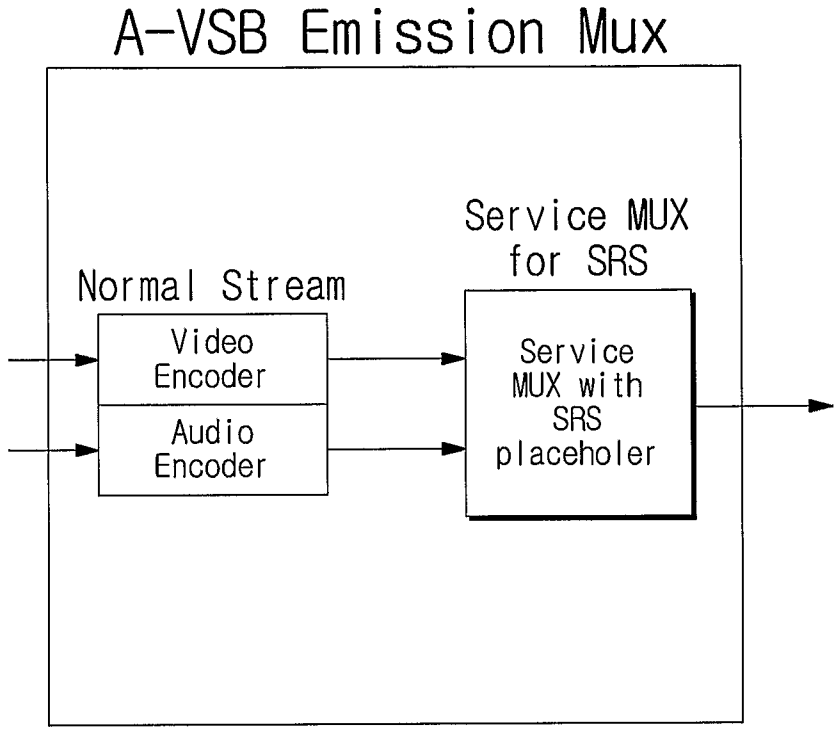
[Fig. 4]


D1
Reset=0
MUX
Z2
S2
Reset
X1
X0
Zero-state
forcing inputs
8 Level
Symbol
Mapper
R
D0
Reset=0
Z1
Reset=1
MUX
S0
S1
Z0

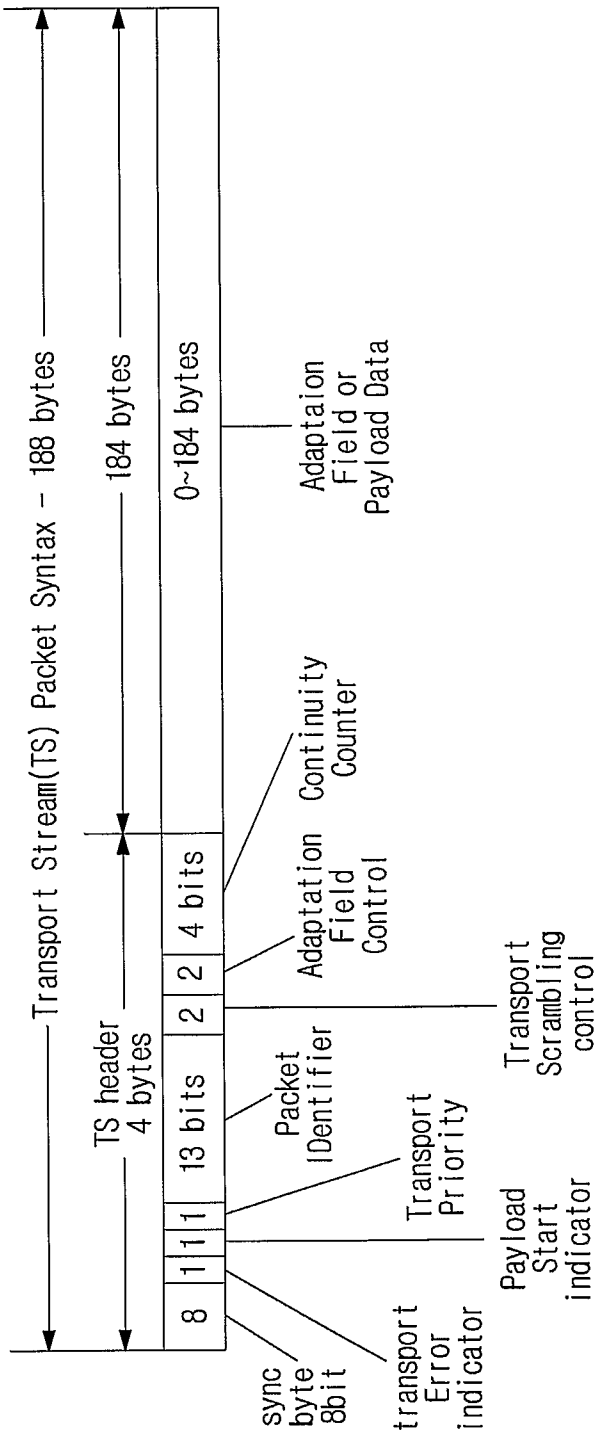
[Fig. 5]


NORMAL STREAM
A-VSB EMISSION MUX
EXCITER FOR SRS
RANDOMIZE
SRS STUFFER
REED-SOLOMON ENCODER
BYTE INTERLEAVE
TCM 1 WITH OTR
TCM 2 WITH OTR
TCM 12 WITH OTR
SEGMENT SYNC
FIELD SYNC
MUX
VSB MODULATOR
POWER AMPLIFIER
STATION ANTENNA

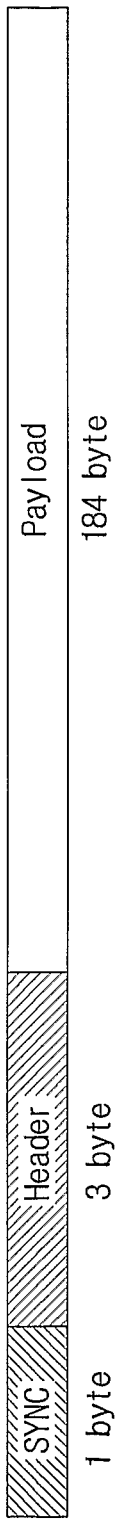
[Fig. 6]


A-VSB Emission Mux
Service MUX for SRS
Normal Stream
Video Encoder
Audio Encoder
Service MUX with SRS placeholer

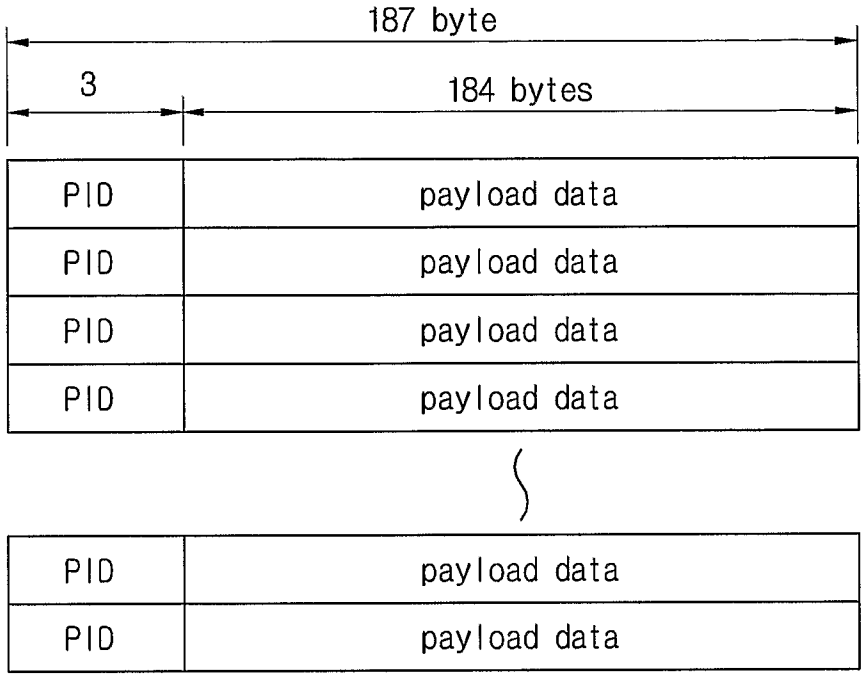
[Fig. 7]


Transport Stream(TS) Packet Syntax - 188 bytes
184 bytes
TS header 4 bytes
8
1
1
1
13 bits
2
2
4 bits
0~184 bytes
sync byte 8bit
transport Error indicator
Payload Start indicator
Transport Priority
Packet IDentifier
Transport Scrambling control
Adaptation Field Control
Continuity Counter
Adaptaion Field or Payload Data

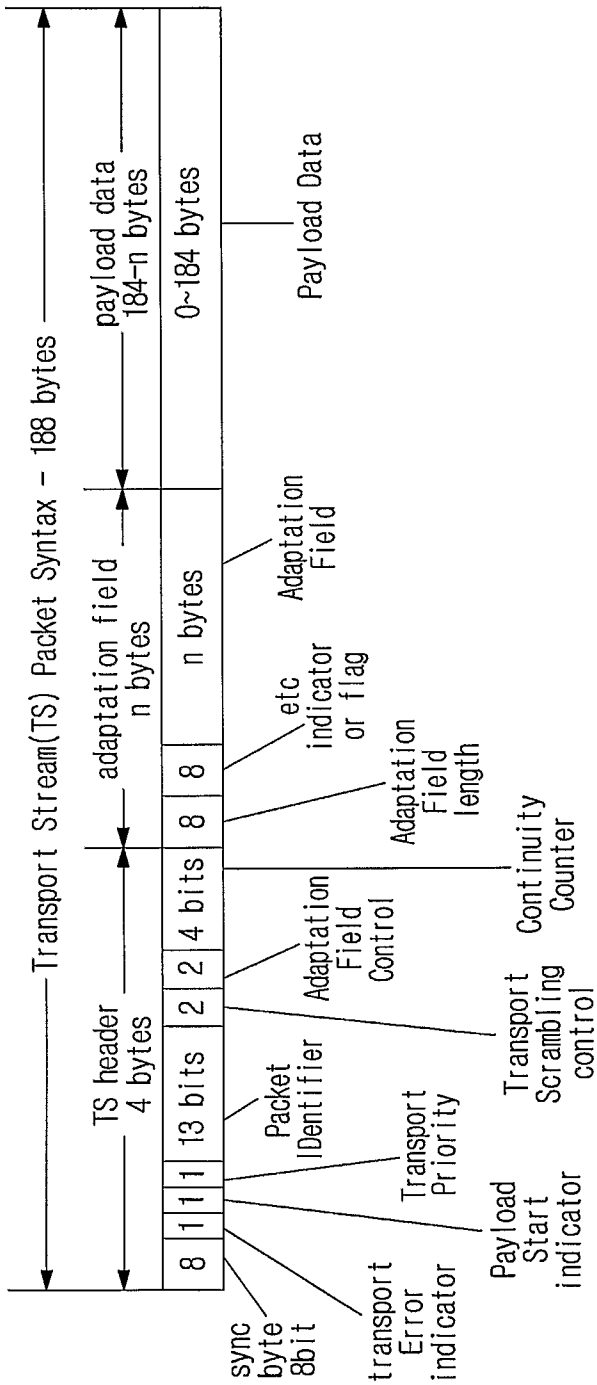
[Fig. 8]



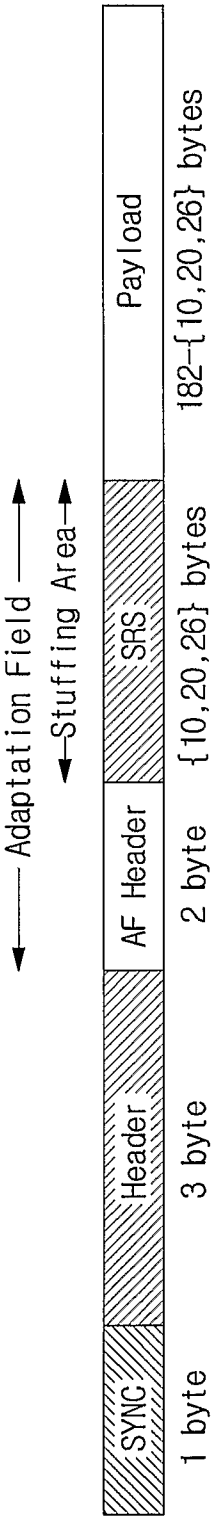
[Fig. 9]


187 byte
3
184 bytes
PID
payload data
PID
payload data
PID
payload data
PID
payload data
PID
payload data
PID
payload data

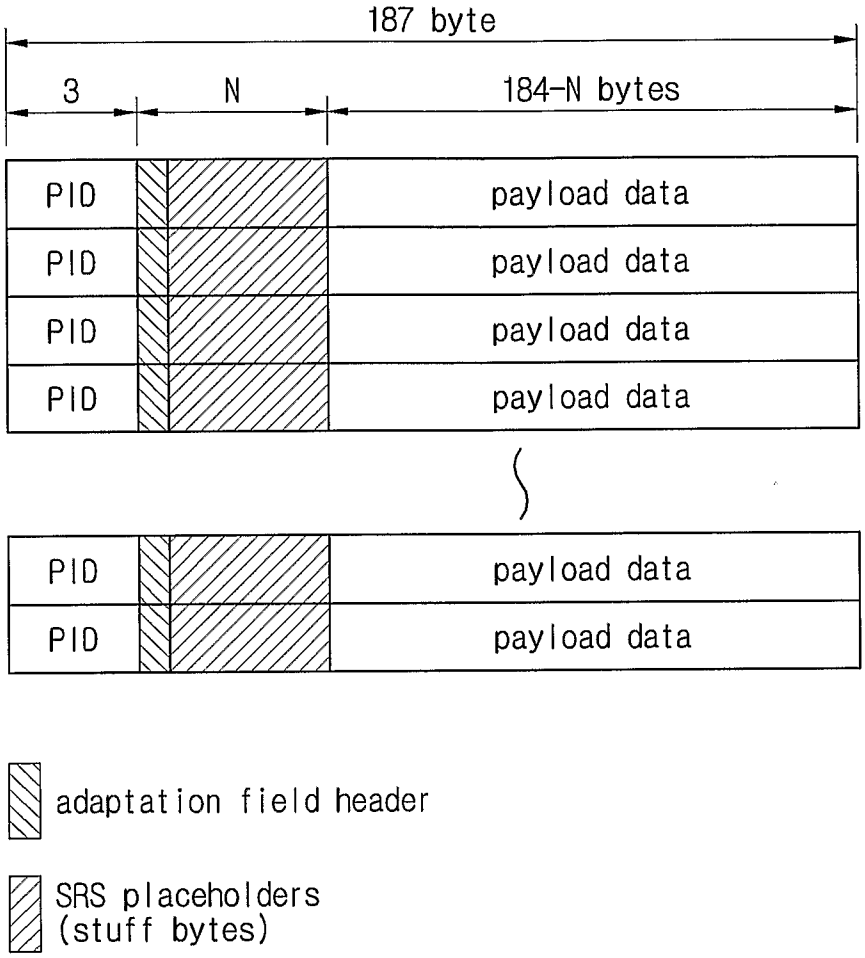
[Fig. 10]


Transport Stream(TS) Packet Syntax - 188 bytes
TS header 4 bytes
adaptation field n bytes
payload data 184-n bytes
8
1
1
1
13 bits
2
2
4 bits
8
8
n bytes
0~184 bytes
sync byte 8bit
transport Error indicator
Payload Start indicator
Transport Priority
Packet IDentifier
Transport Scrambling control
Adaptation Field Control
Continuity Counter
Adaptation Field length
etc indicator or flag
Adaptation Field
Payload Data

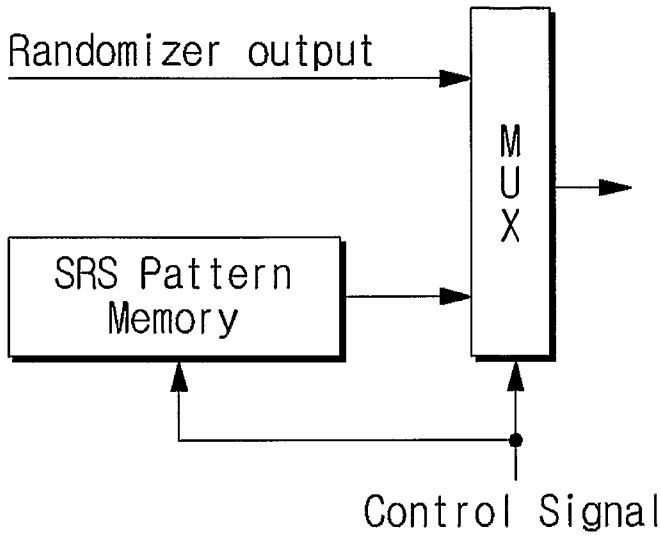
[Fig. 11]


Adaptation Field
Stuffing Area
SYNC
Header
AF Header
SRS
Payload
1 byte
3 byte
2 byte
{10,20,26} bytes
182-{10,20,26} bytes

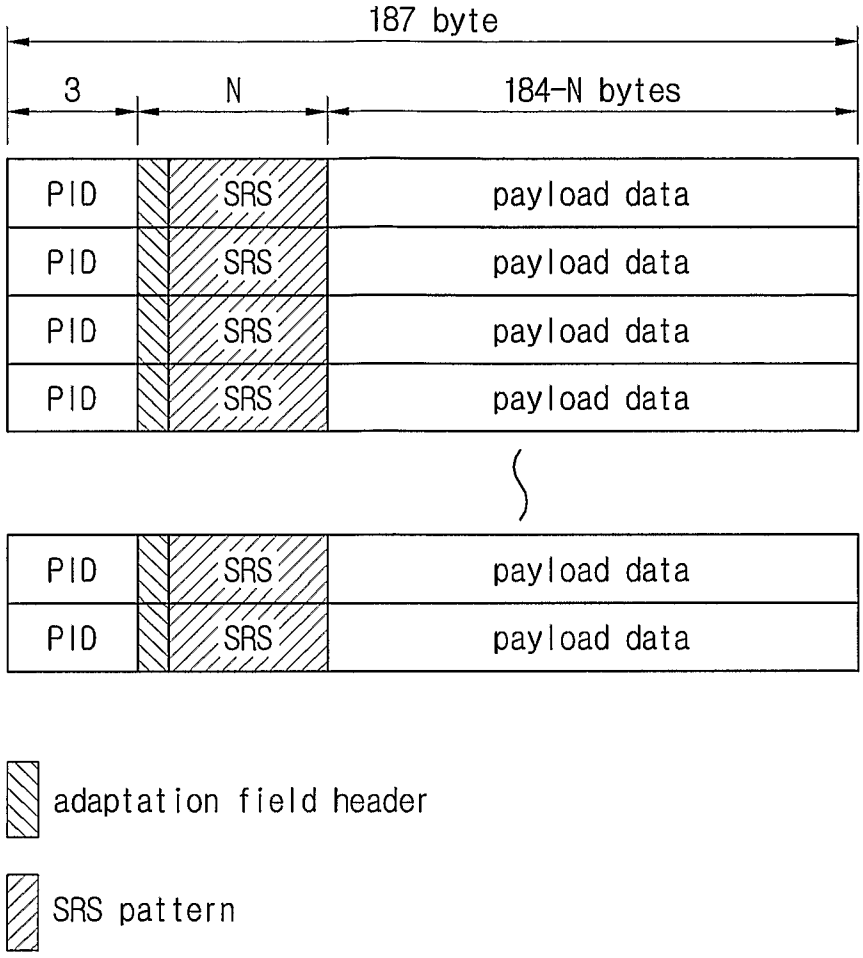
[Fig. 12]


187 byte
3
N
184-N bytes
PID
payload data
PID
payload data
PID
payload data
PID
payload data
PID
payload data
PID
payload data
adaptation field header
SRS placeholders
(stuff bytes)

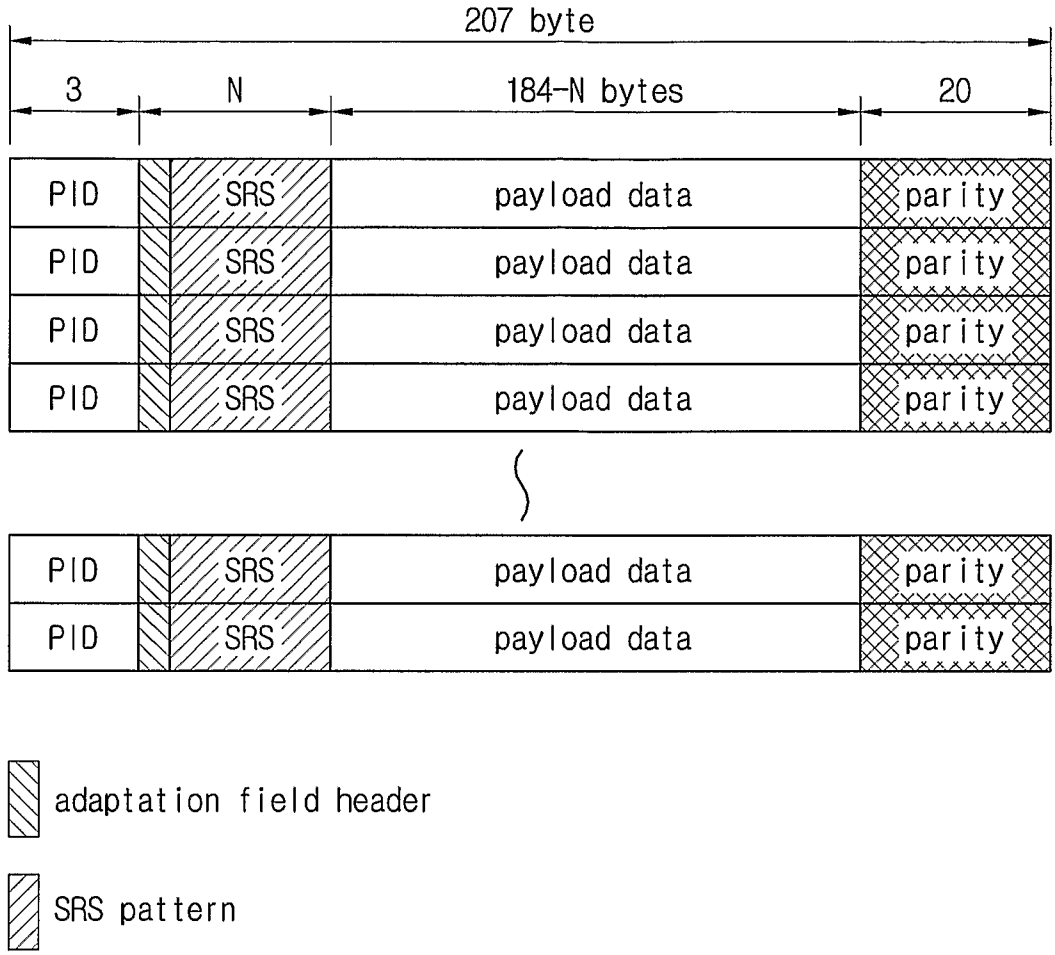
[Fig. 13]



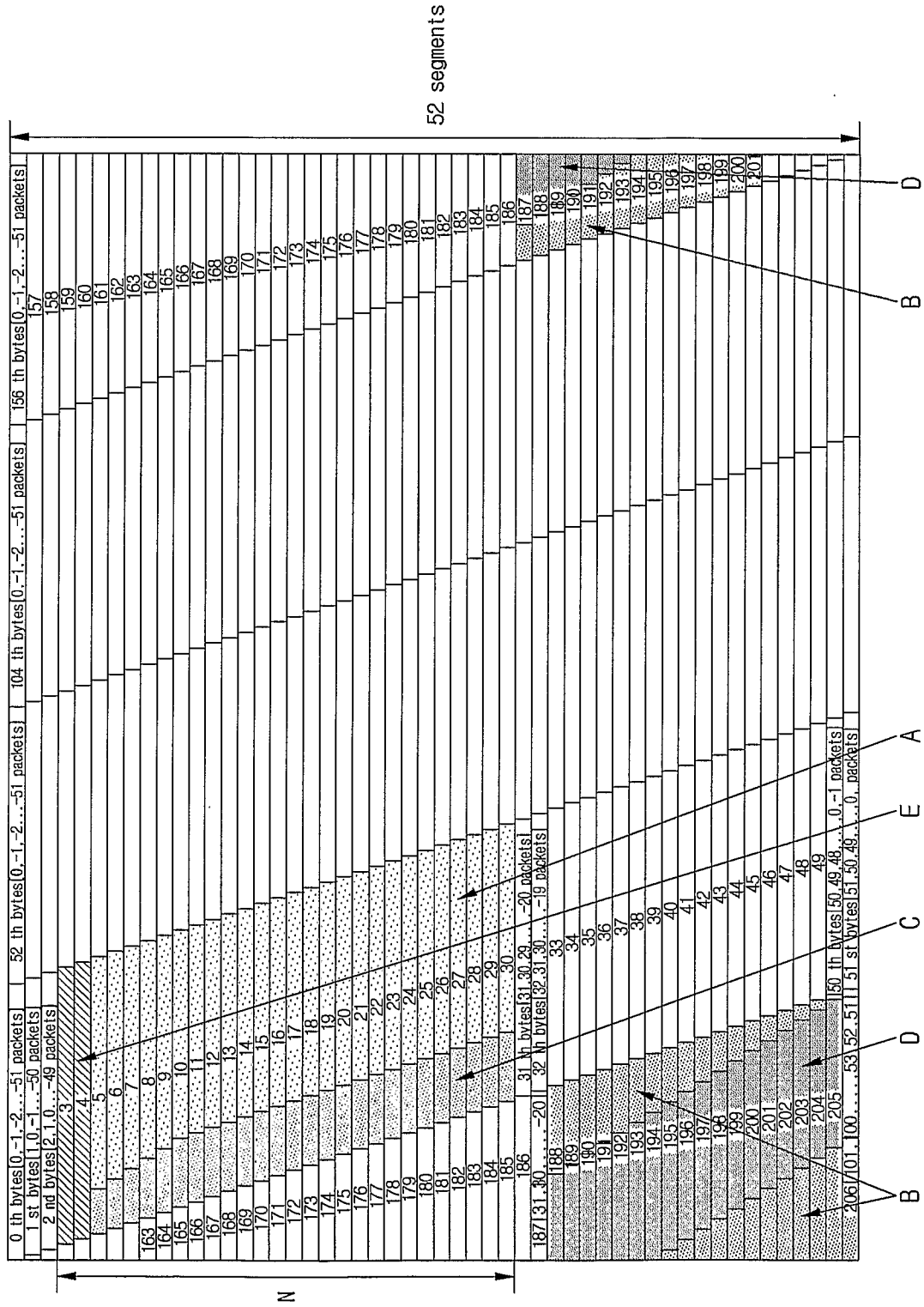
[Fig. 14]


187 byte
3
N
184-N bytes
PID
SRS
payload data
PID
SRS
payload data
PID
SRS
payload data
PID
SRS
payload data
PID
SRS
payload data
PID
SRS
payload data
adaptation field header
SRS pattern

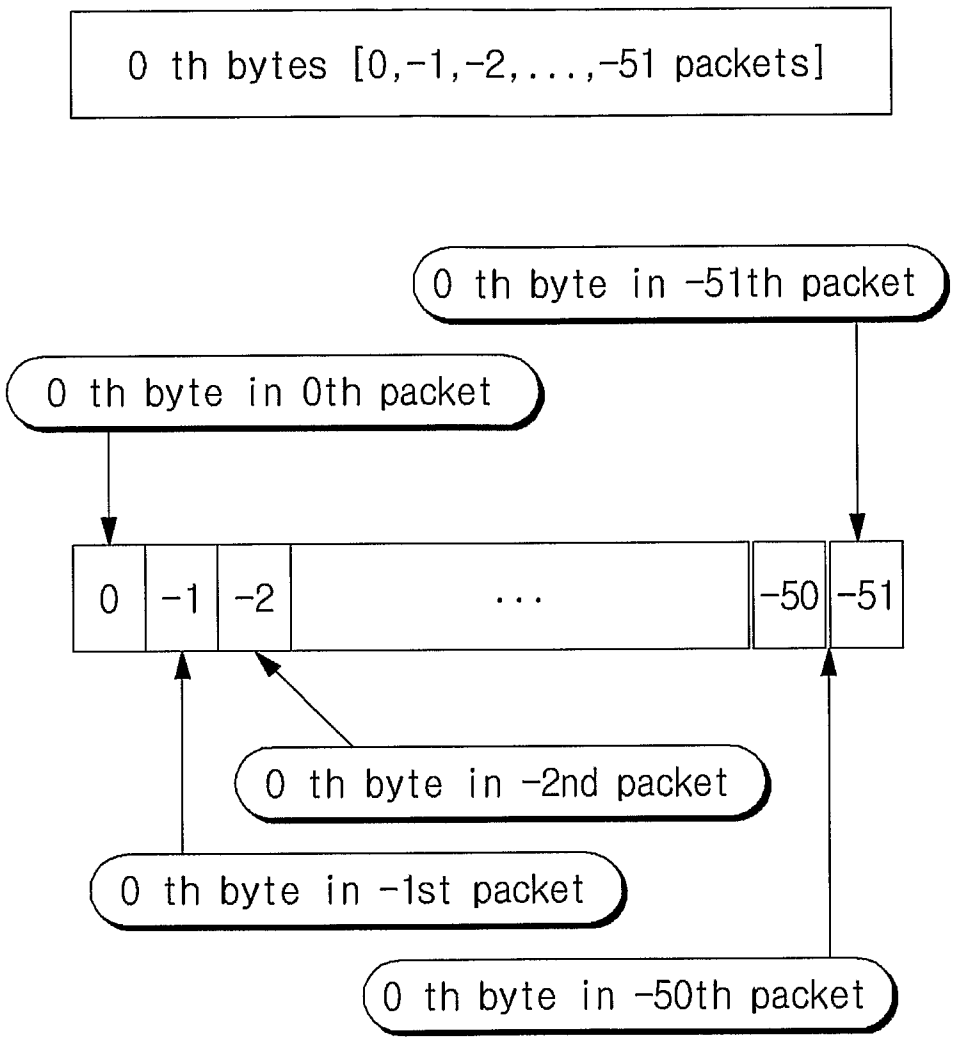
[Fig. 15]


207 byte
3
N
184-N bytes
20
PID
SRS
payload data
parity
adaptation field header
SRS pattern

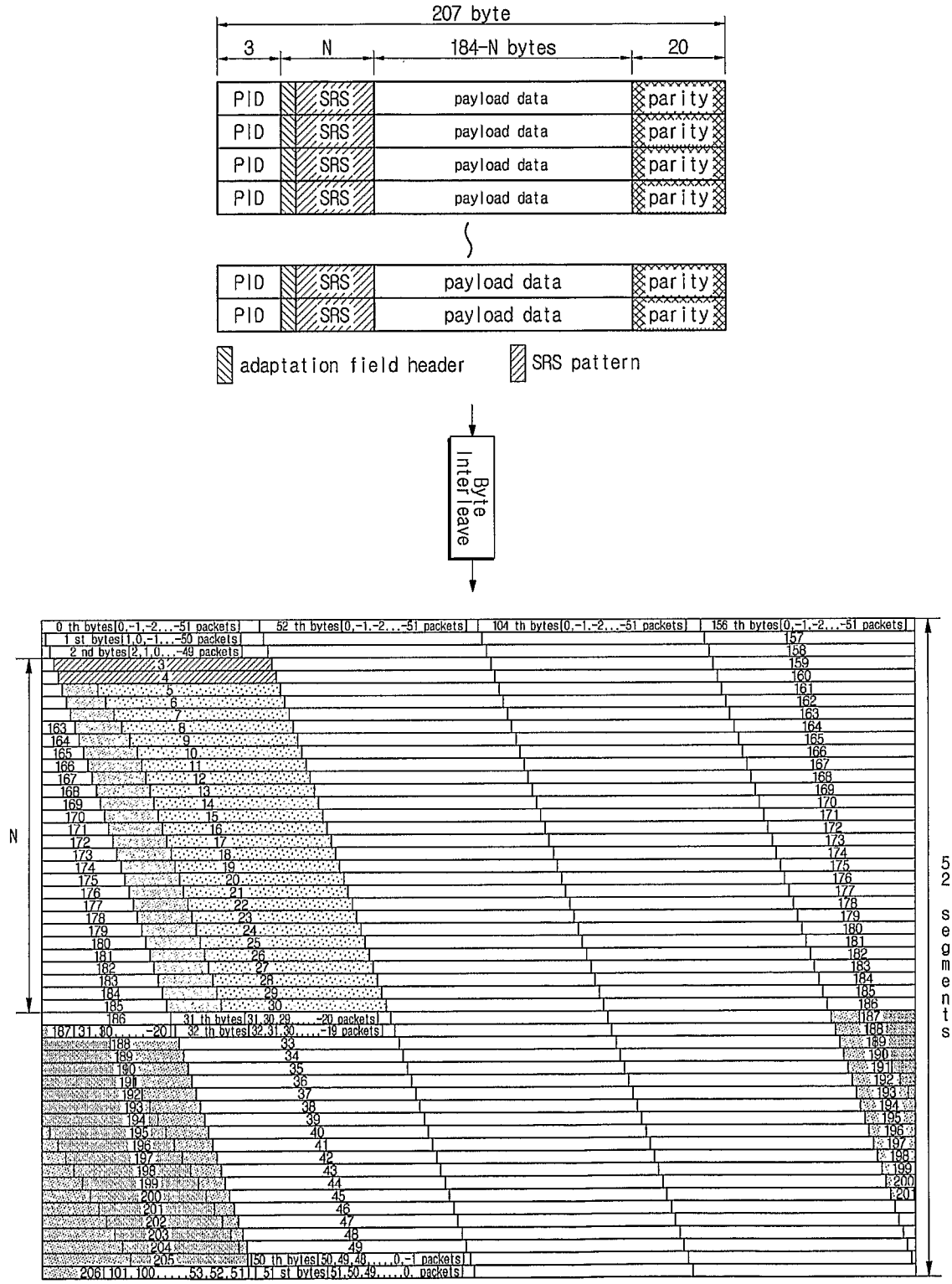
[Fig. 16]



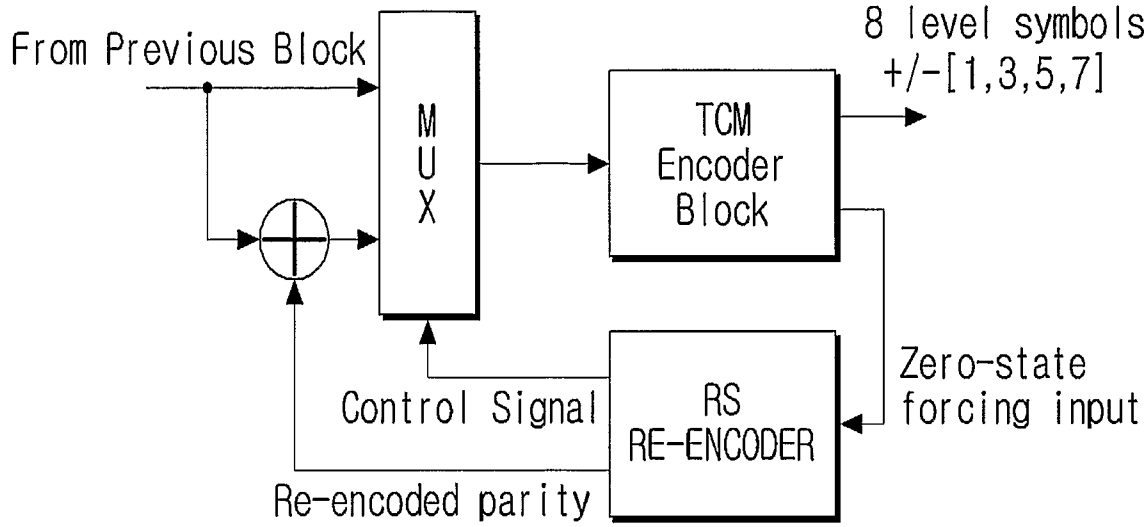
[Fig. 17]


0 th bytes [0,-1,-2,...,-51 packets]
0 th byte in -51th packet
0 th byte in 0th packet
0
-1
-2
...
-50
-51
0 th byte in -2nd packet
0 th byte in -1st packet
0 th byte in -50th packet

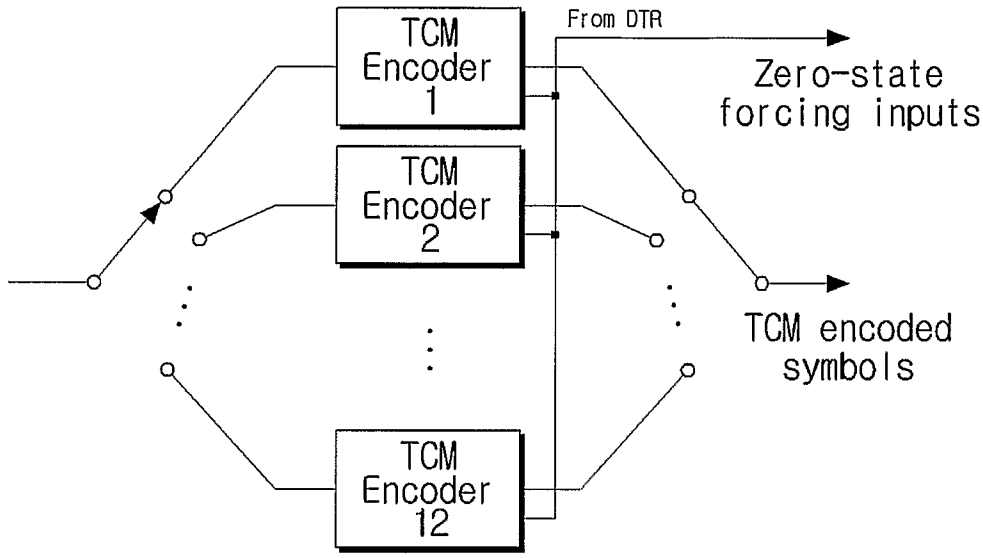
[Fig. 18]


207 byte
3
N
184-N bytes
20
PID
SRS
payload data
parity
adaptation field header
SRS pattern
Byte Interleave
N
52 segments

[Fig. 19]


From Previous Block
M
U
X
TCM
Encoder
Block
8 level symbols
+/-[1,3,5,7]
Zero-state
forcing input
Control Signal
RS
RE-ENCODER
Re-encoded parity

[Fig. 20]


TCM Encoder 1
TCM Encoder 2
TCM Encoder 12
From DTR
Zero-state forcing inputs
TCM encoded symbols

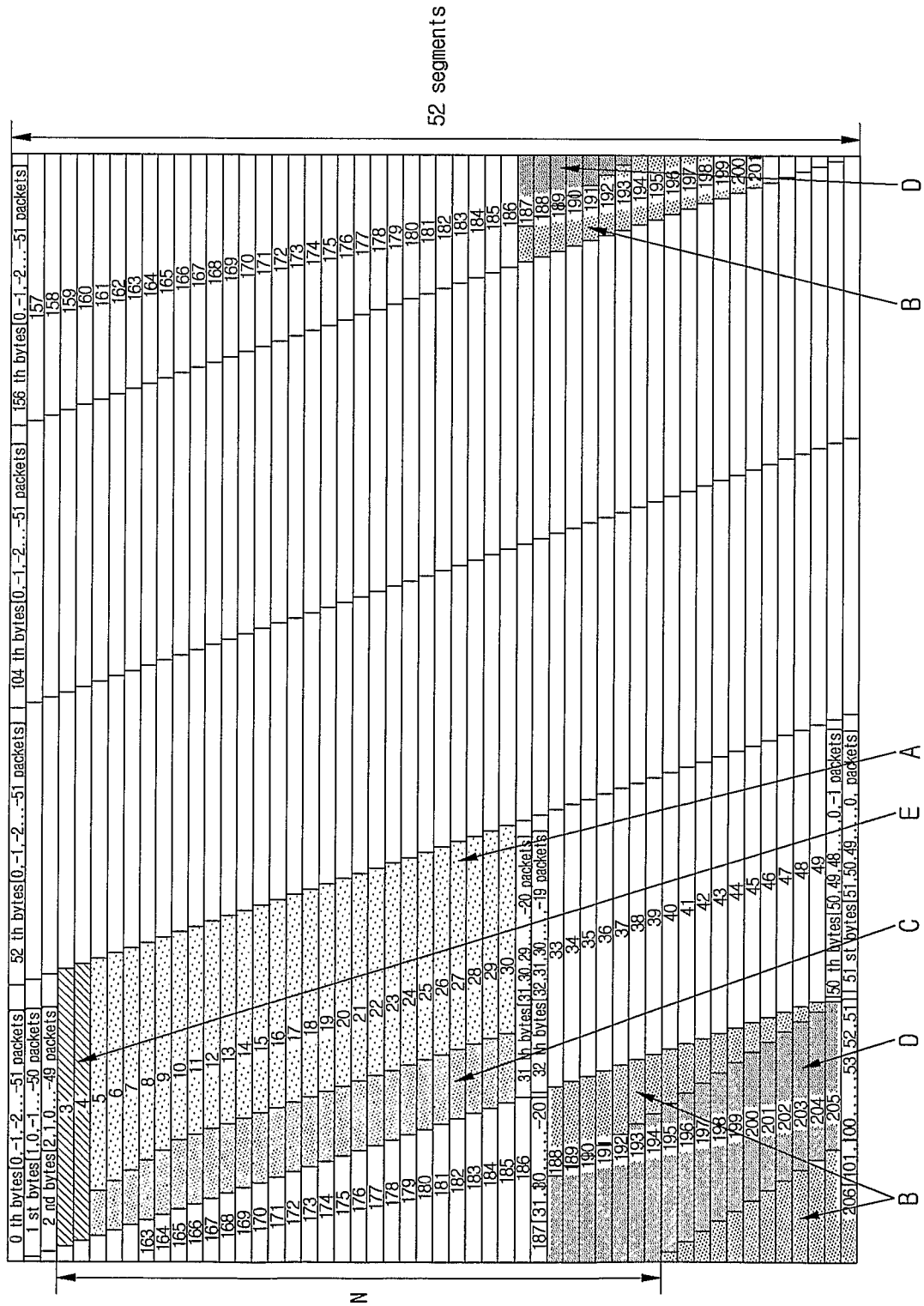
[Fig. 21]

	3 bytes	2 bytes	6 bytes	{4,14,21} bytes	182-{10,20,26} bytes
1	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes
2	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes
3	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes
4	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes
5	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes
6	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes
7	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes
8	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes
9	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes
10	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes
11	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes
12	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes
13	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes
14	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes
15	Header	AF Head	reserved for PCR	4,14,20} bytes SRS	Normal 182-{10,20,26} bytes
16	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes
17	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes
18	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes
19	Header	AF Head	Splice	{9,19,25} bytes of SRS	Normal 182-{10,20,26} bytes
20	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes
21	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes
22	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes
23	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes
24	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes
25	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes
26	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes
27	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes
28	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes
29	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes
30	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes
31	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes
32	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes
33	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes
34	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes
35	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes
36	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes
37	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes
38	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes
39	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes
40	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes
41	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes
42	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes
43	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes
44	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes
45	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes
46	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes
47	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes
48	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes
49	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes
50	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes
51	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes
52	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes

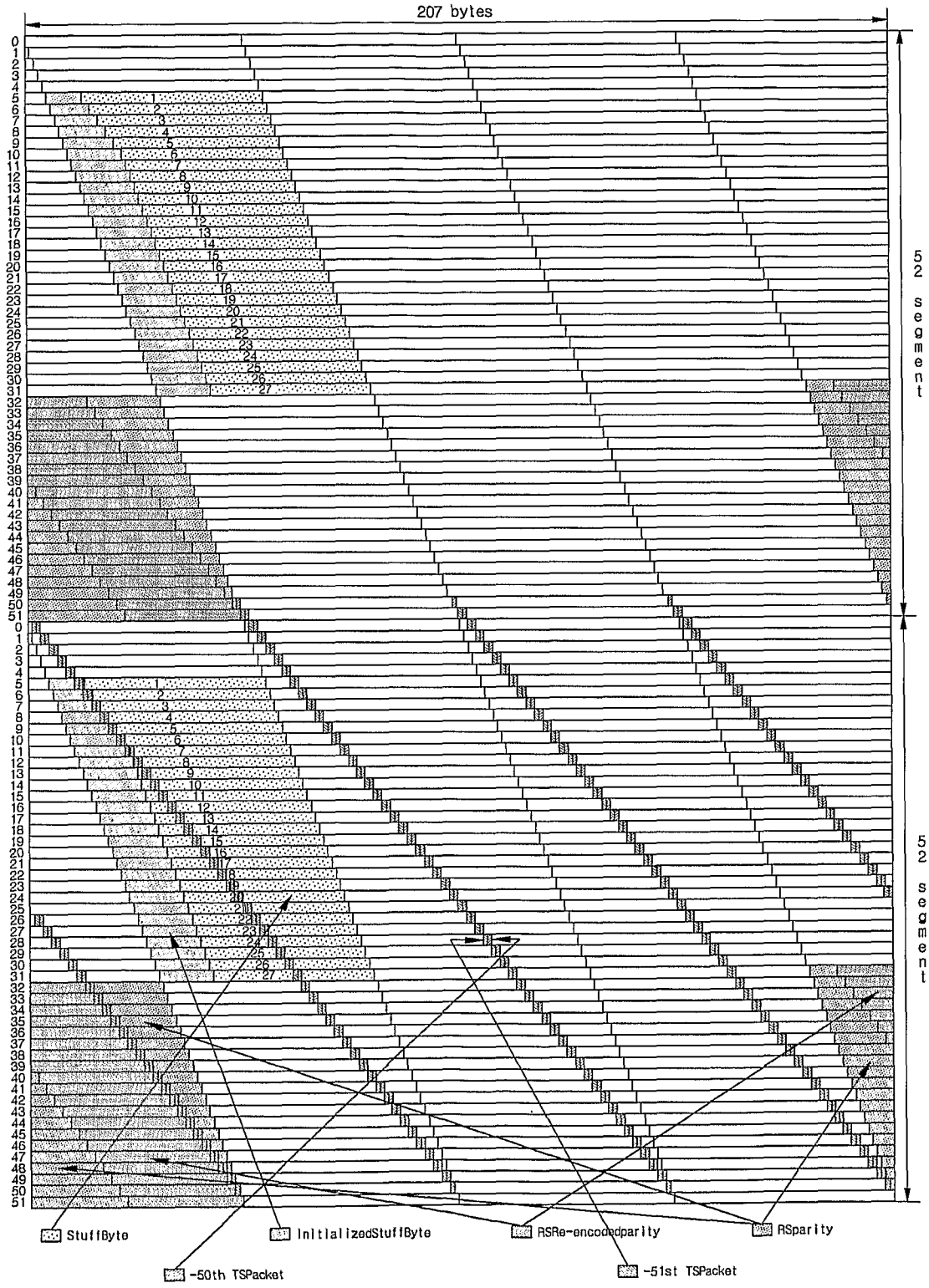
[Fig. 22]

col 1	column 2	column 3	c. 4	c. 5	c. 6	c. 7	c. 8	c. 9	c.10	c.11	c.12	c.13	c.14	c.15	c.16	c.17	c.18	c.19	c.20	c.21	c.22	c.23	c.24	c.25	c.26	c.27	c.28	c.29
	3 byte	2 byte	10 bytes {SRS mode 1}										10 bytes {SRS mode 2}										6 bytes {SRS mode 3}					
1	MPEG Header	AF Header	4	0	7	1	9	11	3	44	3	200	144	17	31	242	131	44	133	0	67	93	144	55	153	223	78	252
2	MPEG Header	AF Header	15	9	15	7	11	9	13	15	1	224	175	181	176	245	226	57	69	94	160	101	33	190	99	19	9	229
3	MPEG Header	AF Header	15	14	3	5	2	8	0	3	1	218	247	241	160	234	194	223	58	157	212	177	5	115	226	5	30	109
4	MPEG Header	AF Header	13	12	5	12	10	0	7	11	13	1	66	235	162	121	101	237	219	212	181	91	130	92	249	120	245	159
5	MPEG Header	AF Header	8	10	4	13	14	13	13	8	8	15	0	182	34	64	144	124	231	83	127	139	239	18	2	41	128	255
6	MPEG Header	AF Header	6	7	1	1	4	14	7	5	16	13	4	9	92	25	34	199	57	177	15	68	121	173	143	142	16	223
7	MPEG Header	AF Header	0	8	9	6	8	12	0	7	5	16	13	14	11	235	46	39	174	173	59	229	163	83	56	253	56	82
8	MPEG Header	AF Header	0	226	0	6	1	11	9	5	0	5	7	11	12	4	215	241	88	247	80	123	214	241	155	34	156	196
9	MPEG Header	AF Header	0	239	22	12	8	8	1	13	9	8	12	15	4	7	4	50	155	205	112	0	61	156	162	218	83	14
10	MPEG Header	AF Header	0	155	84	82	6	13	14	0	9	8	8	2	15	3	14	13	94	139	198	16	95	87	29	62	202	67
11	MPEG Header	AF Header	107	106	52	167	162	15	15	15	1	8	0	16	0	1	10	10	13	193	55	200	10	36	62	253	22	233
12	MPEG Header	AF Header	127	0	220	115	213	150	1	14	5	8	2	8	9	3	2	15	10	14	70	243	71	53	69	44	148	99
13	MPEG Header	AF Header	215	0	0	70	244	196	148	2	3	7	11	15	14	12	8	7	13	2	3	76	102	90	151	203	246	211
14	MPEG Header	AF Header	84	0	0	0	208	161	35	242	15	9	14	5	14	14	0	11	4	11	13	2	135	209	70	227	177	142
15	MPEG Header	AF Header	Reserved for PCR						70	228	23	14	14	8	7	12	3	6	12	5	7	14	1	206	91	245	63	70
16	MPEG Header	AF Header	140	156	207	205	167	85	180	98	227	242	3	6	14	14	14	10	13	13	14	6	3	9	145	150	55	232
17	MPEG Header	AF Header	218	155	42	75	180	57	22	149	249	118	143	10	3	8	3	12	13	12	10	6	15	6	8	154	159	232
18	MPEG Header	AF Header	9	69	81	43	97	228	162	12	216	40	33	154	13	0	5	14	2	5	11	3	15	6	4	0	51	38
19	MPEG Header	AF Header	splice	199	251	6	89	164	78	0	137	252	93	95	123	13	8	1	10	8	8	7	7	3	9	4	12	106
20	MPEG Header	AF Header	0	44	100	113	128	45	11	241	213	122	62	59	146	169	12	15	14	2	14	9	7	3	2	2	6	1
21	MPEG Header	AF Header	0	2	234	151	110	33	36	69	148	110	237	192	177	41	201	9	11	11	5	1	7	1	13	15	6	14
22	MPEG Header	AF Header	0	77	0	134	93	210	158	101	135	212	165	216	108	10	108	17	9	12	0	1	7	13	13	9	5	10
23	MPEG Header	AF Header	45	148	47	106	153	35	130	166	149	105	29	7	26	229	229	166	237	5	10	15	11	3	15	9	13	8
24	MPEG Header	AF Header	145	0	178	29	248	250	216	118	106	35	249	125	171	19	252	118	147	142	13	2	14	12	2	14	12	0
25	MPEG Header	AF Header	136	0	0	116	254	55	232	251	248	173	108	95	127	199	94	47	58	49	204	15	0	6	8	1	5	6
26	MPEG Header	AF Header	136	0	0	0	173	205	244	10	43	203	191	28	123	59	132	190	184	221	62	221	12	10	11	8	7	1
27	MPEG Header	AF Header	0	0	0	0	0	202	222	12	155	120	158	46	64	235	186	250	226	236	148	206	97	4	0	9	4	8
28	MPEG Header	AF Header	124	114	56	226	198	19	98	36	180	94	138	55	113	22	116	16	150	75	217	36	193	55	0	1	4	12
29	MPEG Header	AF Header	168	134	56	195	121	149	65	127	122	247	237	32	207	51	67	81	17	169	208	22	5	225	129	9	4	9
30	MPEG Header	AF Header	53	58	91	190	61	28	132	167	183	59	196	86	54	6	73	215	149	140	183	82	147	55	171	33	2	8
31	MPEG Header	AF Header	0	251	224	155	177	53	7	171	23	96	66	232	106	240	188	245	221	232	253	48	248	195	43	204	48	9
32	MPEG Header	AF Header	0	254	135	77	175	87	236	247	237	142	143	168	210	254	148	8	74	36	56	183	101	137	163	107	125	243
33	MPEG Header	AF Header	0	226	221	167	63	64	58	136	40	227	101	178	182	107	4	251	130	237	245	203	50	181	104	67	75	41
34	MPEG Header	AF Header	0	120	229	181	67	251	233	106	222	221	31	123	208	99	181	143	226	206	204	115	61	245	155	190	237	49
35	MPEG Header	AF Header	126	103	227	229	251	234	149	46	134	10	155	174	113	161	111	44	253	9	79	69	84	217	147	241	196	164
36	MPEG Header	AF Header	131	0	78	105	200	9	135	125	158	4	237	218	58	69	188	156	164	123	238	155	57	244	43	59	141	230
37	MPEG Header	AF Header	186	0	0	128	167	186	45	204	175	142	164	200	204	129	111	235	203	81	223	200	154	121	212	13	125	226
38	MPEG Header	AF Header	79	0	0	0	223	165	28	67	199	67	160	167	108	212	7	131	109	202	144	238	129	42	184	215	204	73
39	MPEG Header	AF Header	0	0	0	0	0	235	100	184	106	31	10	24	75	138	168	192	144	72	13	73	19	228	152	171	166	154
40	MPEG Header	AF Header	58	252	170	63	239	141	171	24	29	29	37	111	93	33	196	204	222	24	104	153	232	58	6	228	141	179
41	MPEG Header	AF Header	123	189	87	165	108	135	209	136	12	207	101	37	212	126	187	109	243	230	23	166	231	92	223	188	81	117
42	MPEG Header	AF Header	33	196	220	156	108	235	142	7	168	93	146	222	197	120	20	112	97	141	207	251	110	99	200	132	243	237
43	MPEG Header	AF Header	0	122	123	21	96	206	89	6	175	190	209	43	171	248	228	105	21	70	4	208	85	34	140	14	187	137
44	MPEG Header	AF Header	0	222	3	109	25	93	40	216	252	63	226	180	219	71	228	226	67	29	44	202	178	115	154	219	129	22
45	MPEG Header	AF Header	0	223	97	71	138	250	246	255	182	34	100	71	84	57	61	139	107	76	160	12	25	130	192	184	233	143
46	MPEG Header	AF Header	0	190	169	242	185	238	137	0	65	205	57	47	39	41	211	220	25	116	49	148	81	228	90	125	83	145
47	MPEG Header	AF Header	242	222	224	209	110	229	133	237	255	0	165	198	29	185	130	208	48	31	55	86	228	72	17	74	52	51
48	MPEG Header	AF Header	184	0	201	165	146	98	201	31	89	156	63	246	235	223	160	135	214	225	203	26	35	61	17	38	168	222
49	MPEG Header	AF Header	196	0	0	147	81	216	7	187	179	82	51	2	71	70	124	240	148	3	10	209	47	37	174	3	162	50
50	MPEG Header	AF Header	86	0	0	0	18	136	169	95	17	104	234	34	72	85	180	23	33	32	172	151	185	195	237	239	190	92
51	MPEG Header	AF Header	0	0	0	0	0	27	69	70	249	227	43	134	68	138	110	251	204	124	160	159	205	185	125	63	74	203
52	MPEG Header	AF Header	15	0	5	16	12	8	254	136	141	8	128	148	189	217	194	3	50	102	125	78	206	55	202	222	124	12

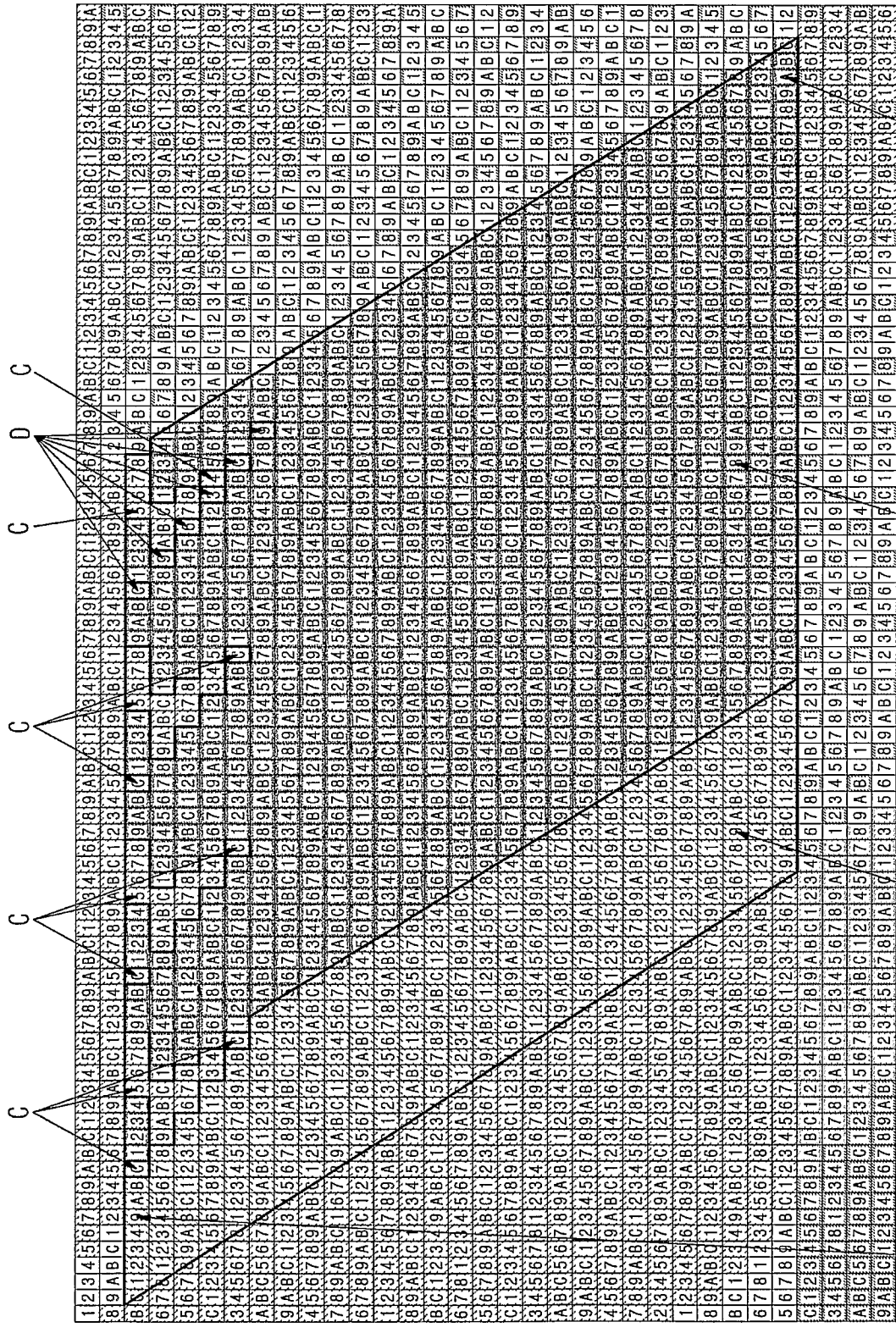
[Fig. 23]



[Fig. 24]


207 bytes
52 segment
52 segment
StuffByte
InitializedStuffByte
RSRe-encodedparity
RSparity
-50th TSPacket
-51st TSPacket

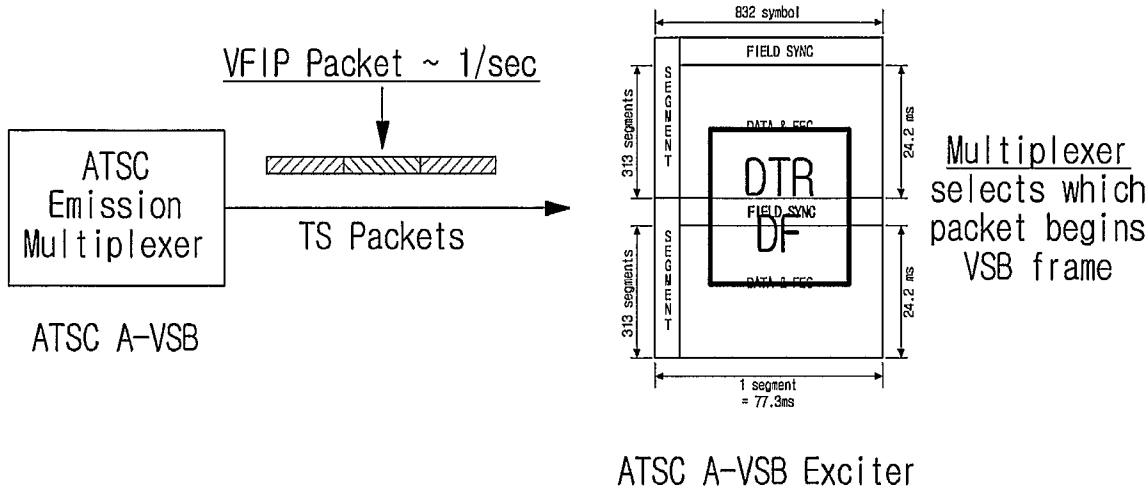
[Fig. 25]



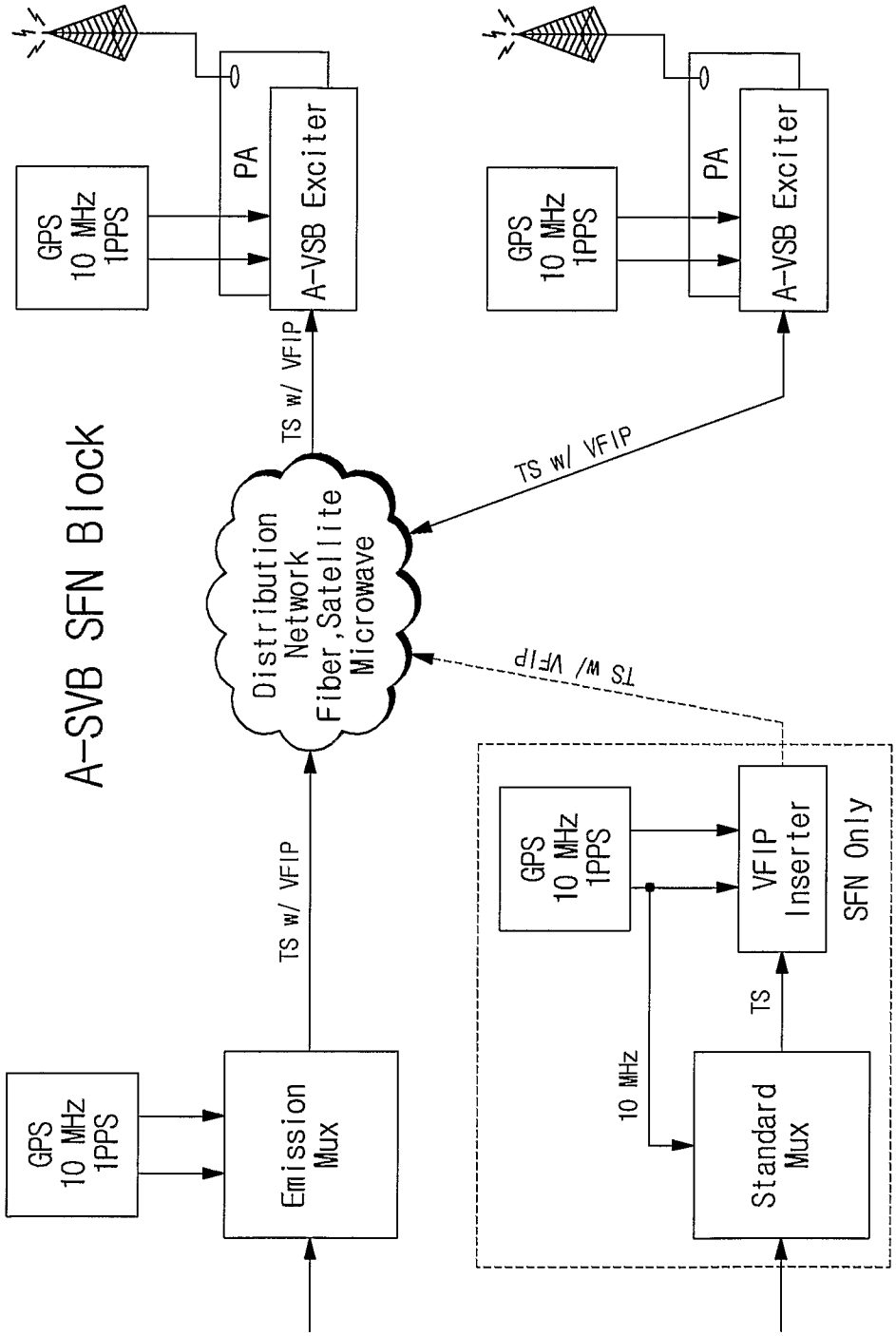
[Fig. 26]

	3 bytes	2 bytes	6 bytes	{4,14,21} bytes	182-{10,20,26} bytes
1	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes
2	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes
3	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes
4	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes
5	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes
6	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes
7	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes
8	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes
9	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes
10	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes
11	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes
12	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes
13	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes
14	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes
15	Header	AF Head	PCR/Private Data/AF Ext	4,14,20} bytes SRS	Normal 182-{10,20,26} bytes
16	Header	{Null,PAT,PMT} packet In SRS-10 bytes			
17	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes
18	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes
19	Header	AF Head	Splice	{9,19,25} bytes of SRS	Normal 182-{10,20,26} bytes
20	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes
21	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes
22	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes
23	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes
24	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes
25	Header	{Null,PAT,PMT} packet In SRS-20 bytes			
26	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes
27	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes
28	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes
29	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes
30	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes
31	Header	{Null,PAT,PMT} packet In SRS-26 bytes			
32	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes
33	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes
34	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes
35	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes
36	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes
37	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes
38	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes
39	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes
40	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes
41	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes
42	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes
43	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes
44	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes
45	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes
46	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes
47	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes
48	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes
49	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes
50	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes
51	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes
52	Header	AF Head		{10,20,26} bytes of SRS	Normal 182-{10,20,26} bytes

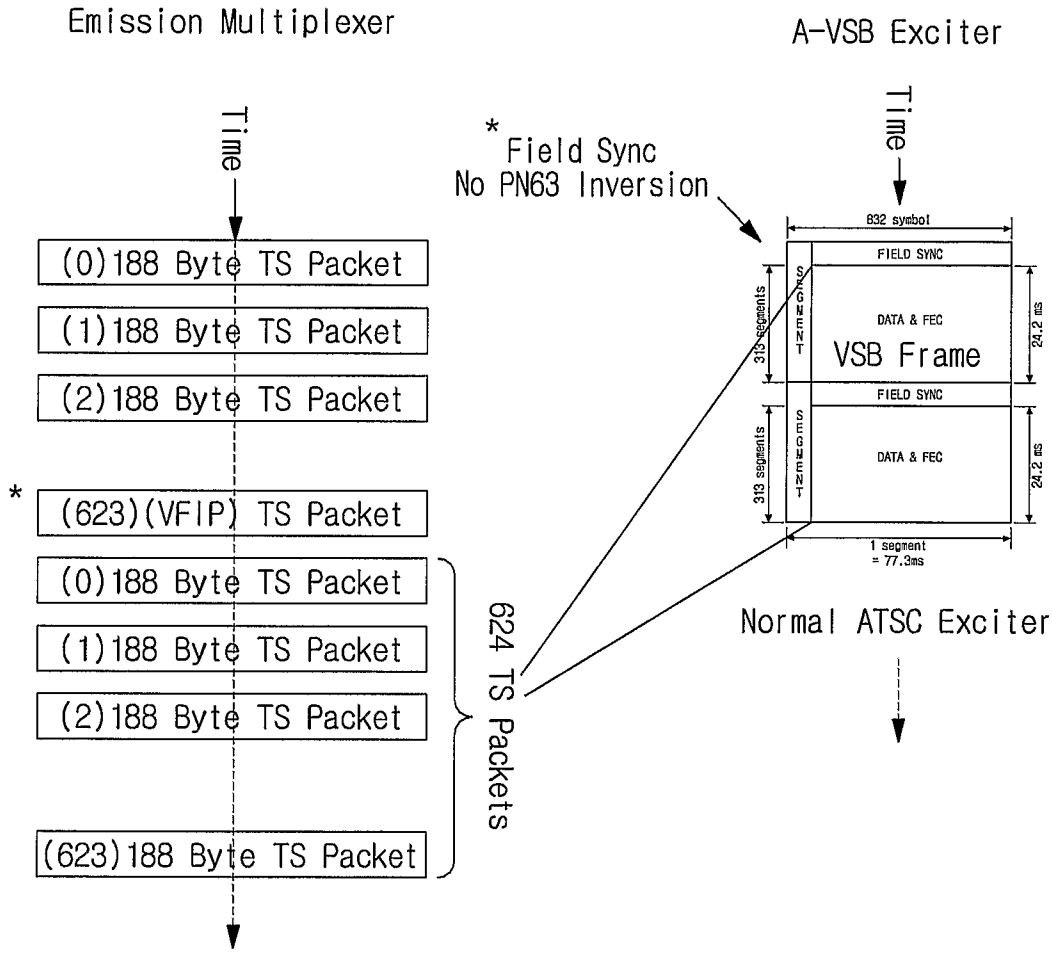
[Fig. 27]


Harmonized ATSC SFN Functionality
VFIP Packet ~ 1/sec
ATSC Emission Multiplexer
TS Packets
ATSC A-VSB
832 symbol
FIELD SYNC
313 segments
SEGMENT
DTR
DF
24.2 ms
1 segment = 77.3ms
Multiplexer selects which packet begins VSB frame
ATSC A-VSB Exciter

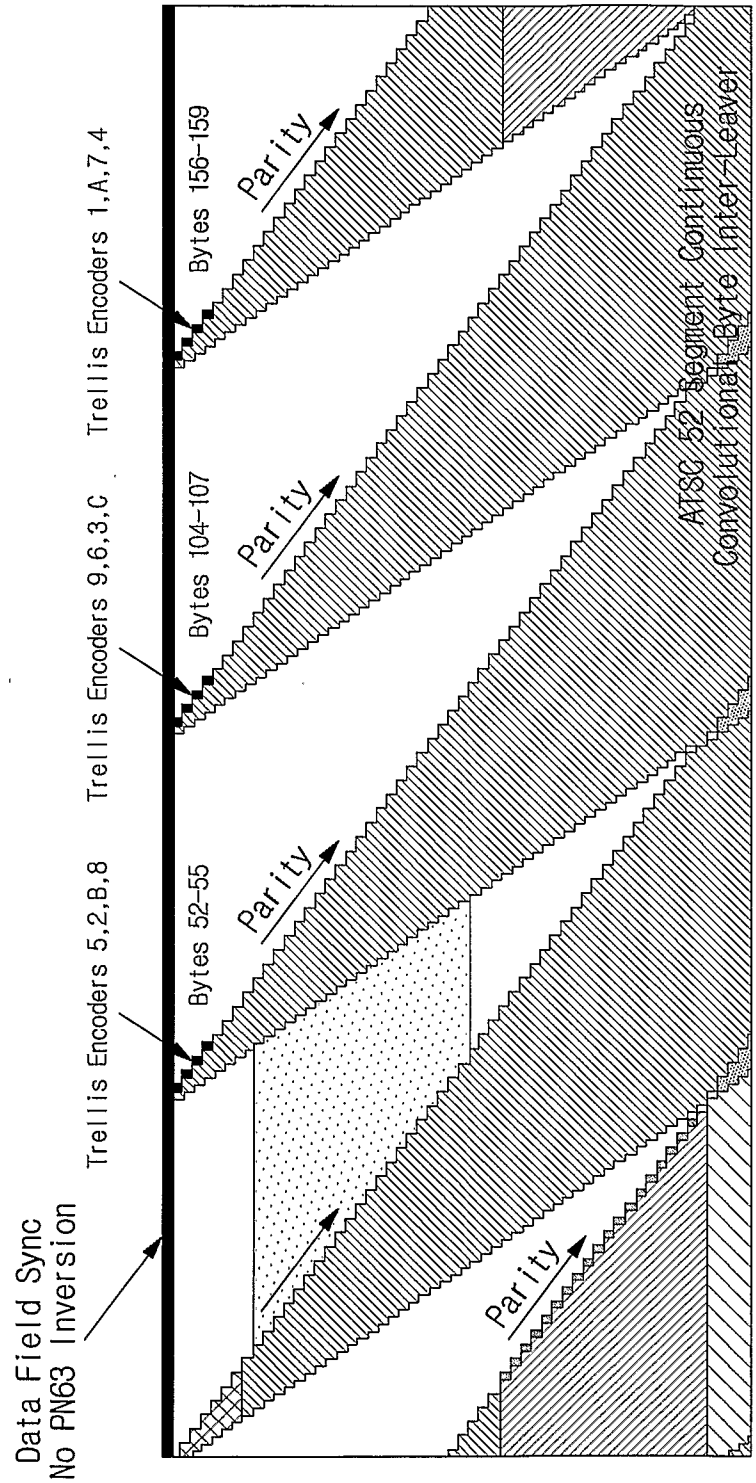
[Fig. 28]


A-SVB SFN Block
GPS 10 MHz 1PPS
PA
A-VSB Exciter
GPS 10 MHz 1PPS
PA
A-VSB Exciter
TS w/ VFIP
TS w/ VFIP
Distribution Network Fiber, Satellite Microwave
TS w/ VFIP
TS w/ VFIP
GPS 10 MHz 1PPS
Emission Mux
GPS 10 MHz 1PPS
VFIP Inserter
SFN Only
TS
10 MHz
Standard Mux

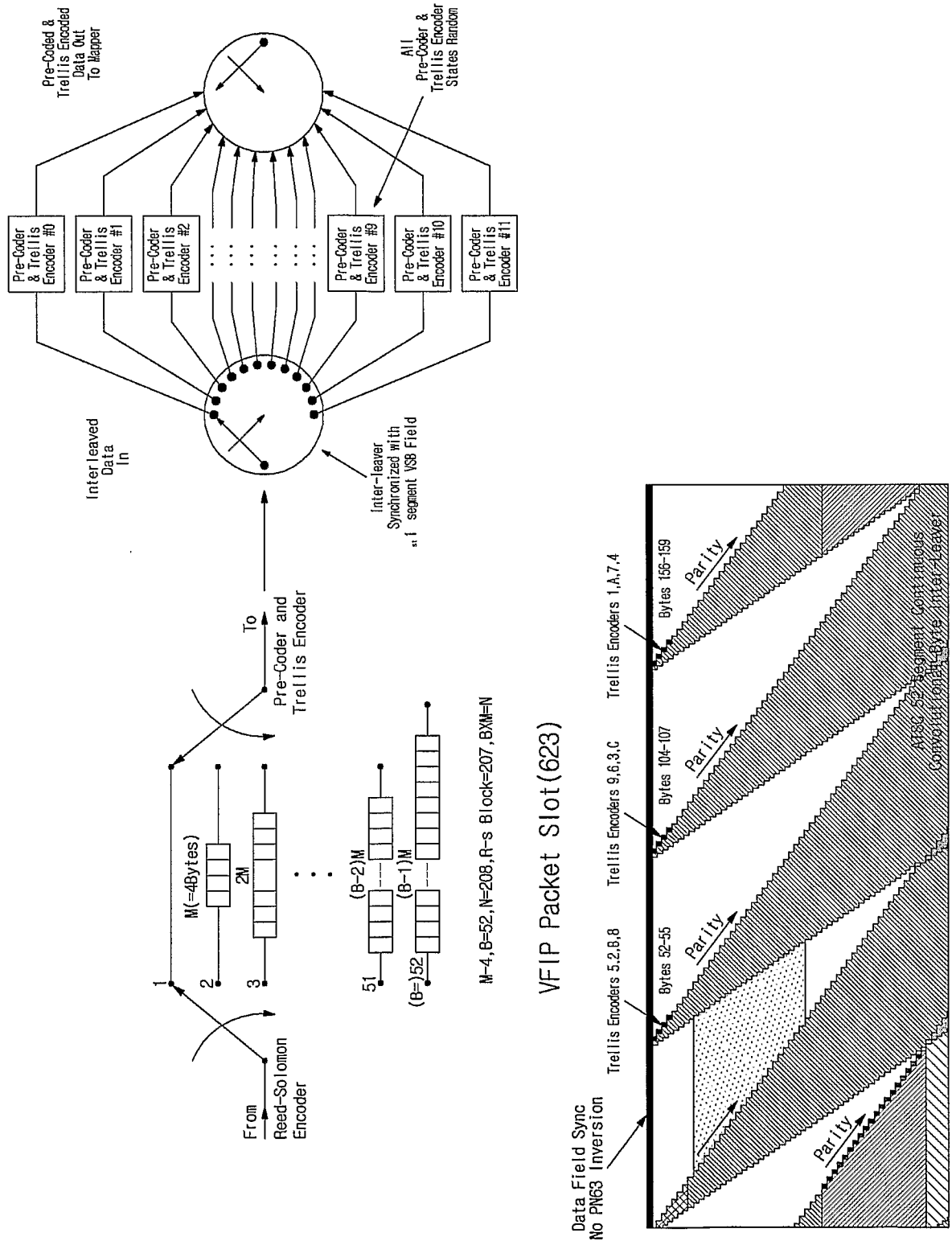
[Fig. 29]


Emission Multiplexer
A-VSB Exciter
Time
Time
* Field Sync
No PN63 Inversion
(0)188 Byte TS Packet
(1)188 Byte TS Packet
(2)188 Byte TS Packet
* (623)(VFIP) TS Packet
(0)188 Byte TS Packet
(1)188 Byte TS Packet
(2)188 Byte TS Packet
(623)188 Byte TS Packet
624 TS Packets
832 symbol
FIELD SYNC
DATA & FEC
VSB Frame
313 segments
24.2 ms
1 segment
= 77.3ms
Normal ATSC Exciter

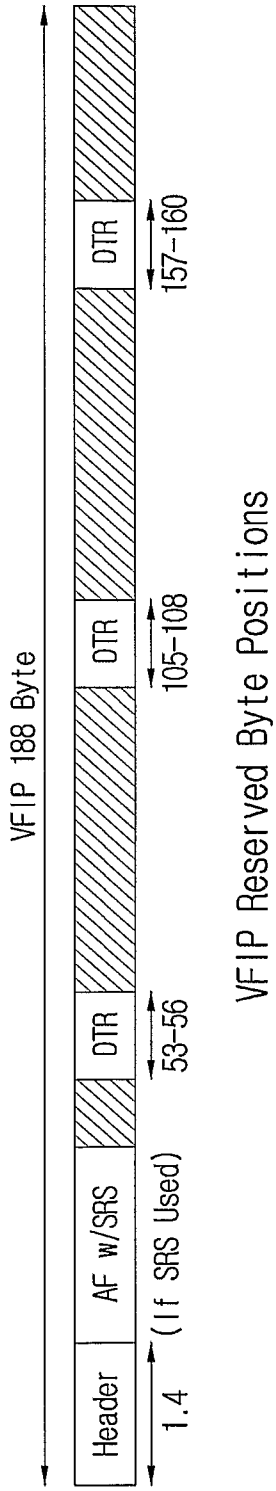
[Fig. 30]


VFIP Packet Slot(623)
Data Field Sync
No PN63 Inversion
Trellis Encoders 5,2,8,8
Trellis Encoders 9,6,3,C
Trellis Encoders 1,A,7,4
Bytes 52-55
Bytes 104-107
Bytes 156-159
Parity
Parity
Parity
Parity
ATSC 52 Segment Continuous
Convolutional Byte Inter-Leaver

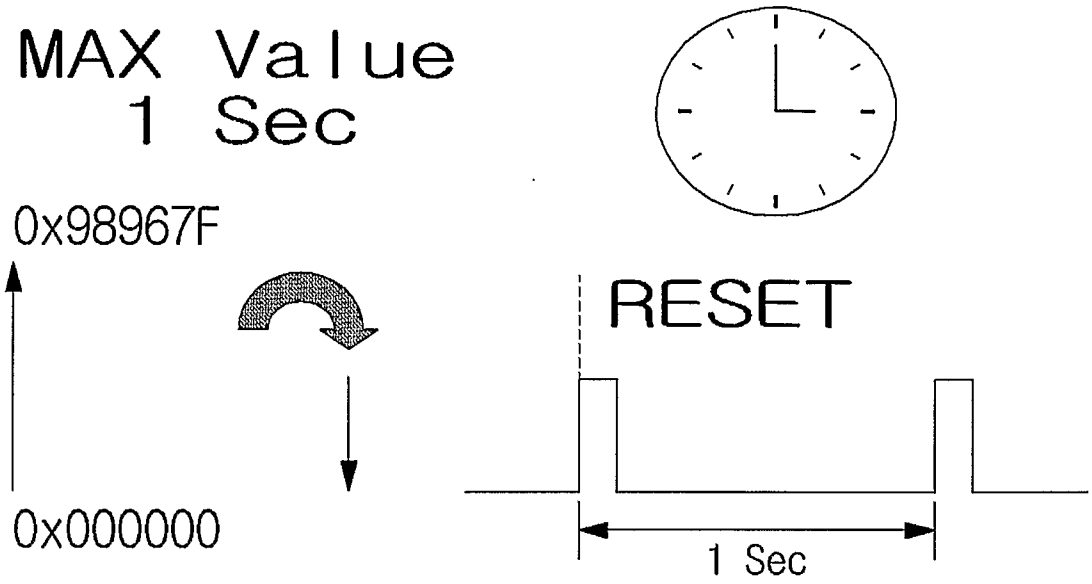
[Fig. 31]


Pre-Coded & Trellis Encoded Data Out To Mapper
All Pre-Coder & Trellis Encoder States Random
Pre-Coder & Trellis Encoder #0
Pre-Coder & Trellis Encoder #1
Pre-Coder & Trellis Encoder #2
Pre-Coder & Trellis Encoder #9
Pre-Coder & Trellis Encoder #10
Pre-Coder & Trellis Encoder #11
Inter leaved Data In
Inter-leaver Synchronized with 1 segment VSB Field
To Pre-Coder and Trellis Encoder
From Reed-Solomon Encoder
M(=4Bytes)
2M
(B-2)M
(B-1)M
(B=)52
M=4,B=52,N=208,R-s Block=207,BXM=N
VFIP Packet Slot(623)
Data Field Sync No PN63 Inversion
Trellis Encoders 5,2,8,8
Trellis Encoders 9,6,3,C
Trellis Encoders 1,A,7,4
Bytes 52-55
Bytes 104-107
Bytes 156-159
Parity
MPEG 2 Segment Continuous Convolutional Byte Inter-Leaver

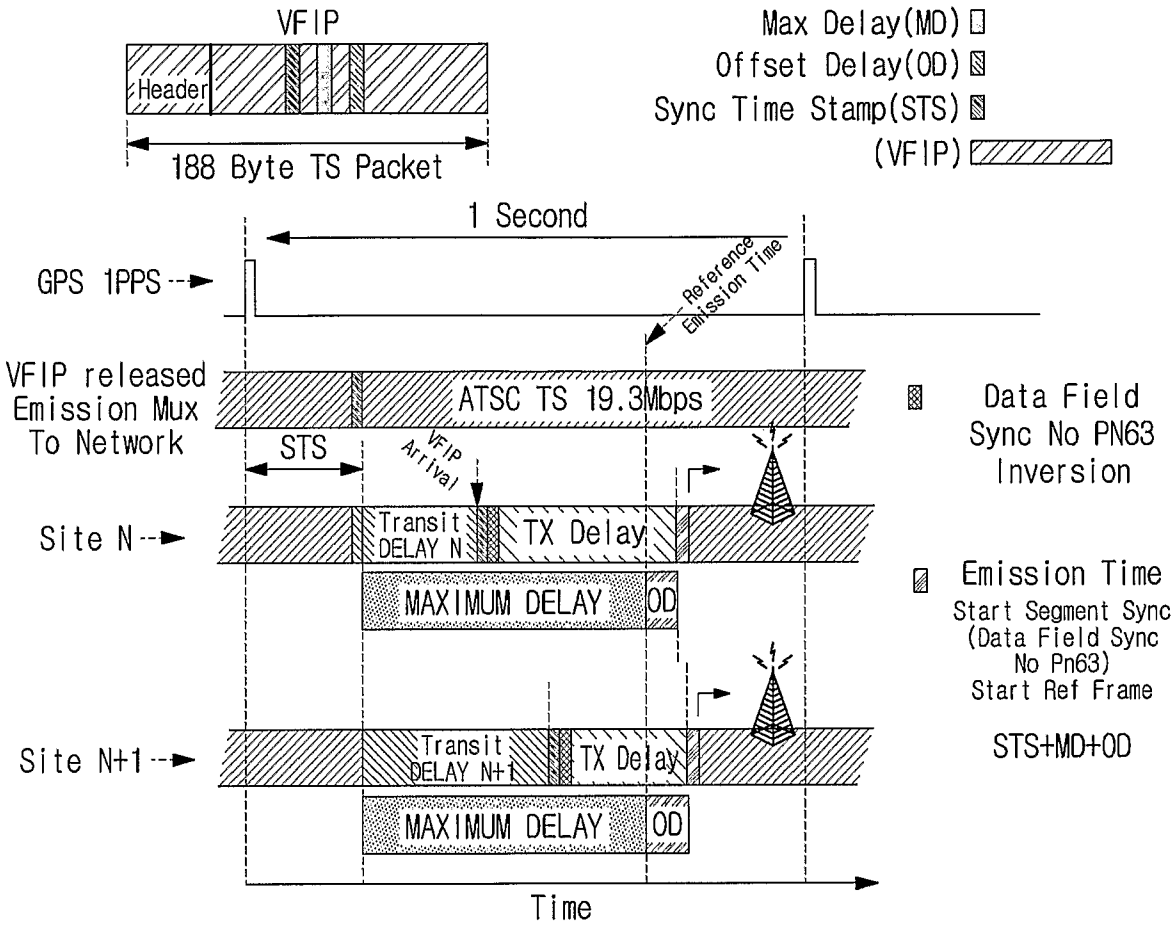
[Fig. 32]


VFIP 188 Byte
Header
AF w/SRS
DTR
DTR
DTR
1.4
(If SRS Used)
53-56
105-108
157-160
VFIP Reserved Byte Positions

[Fig. 33]

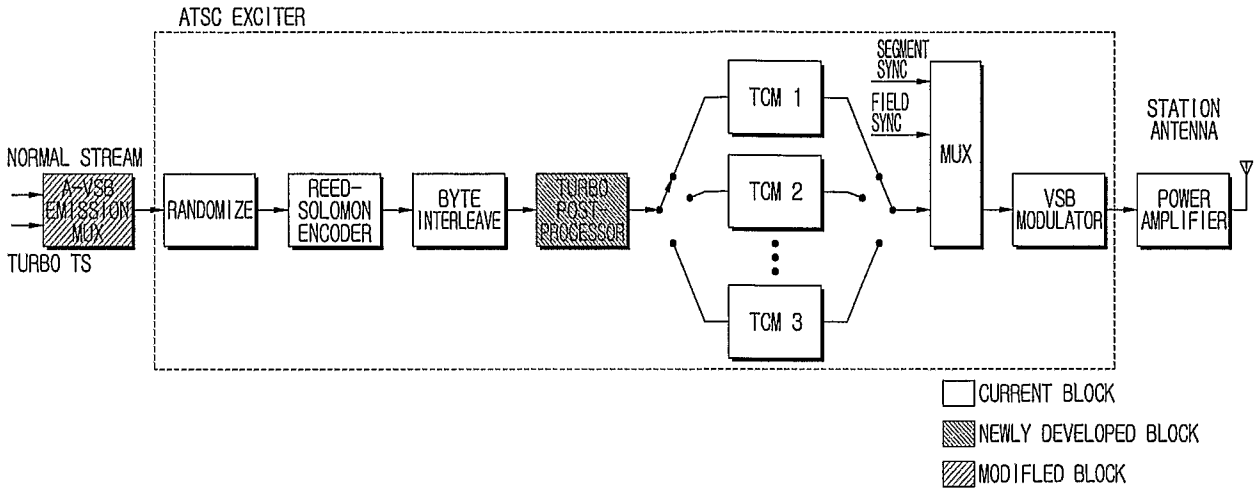


[Fig. 34]

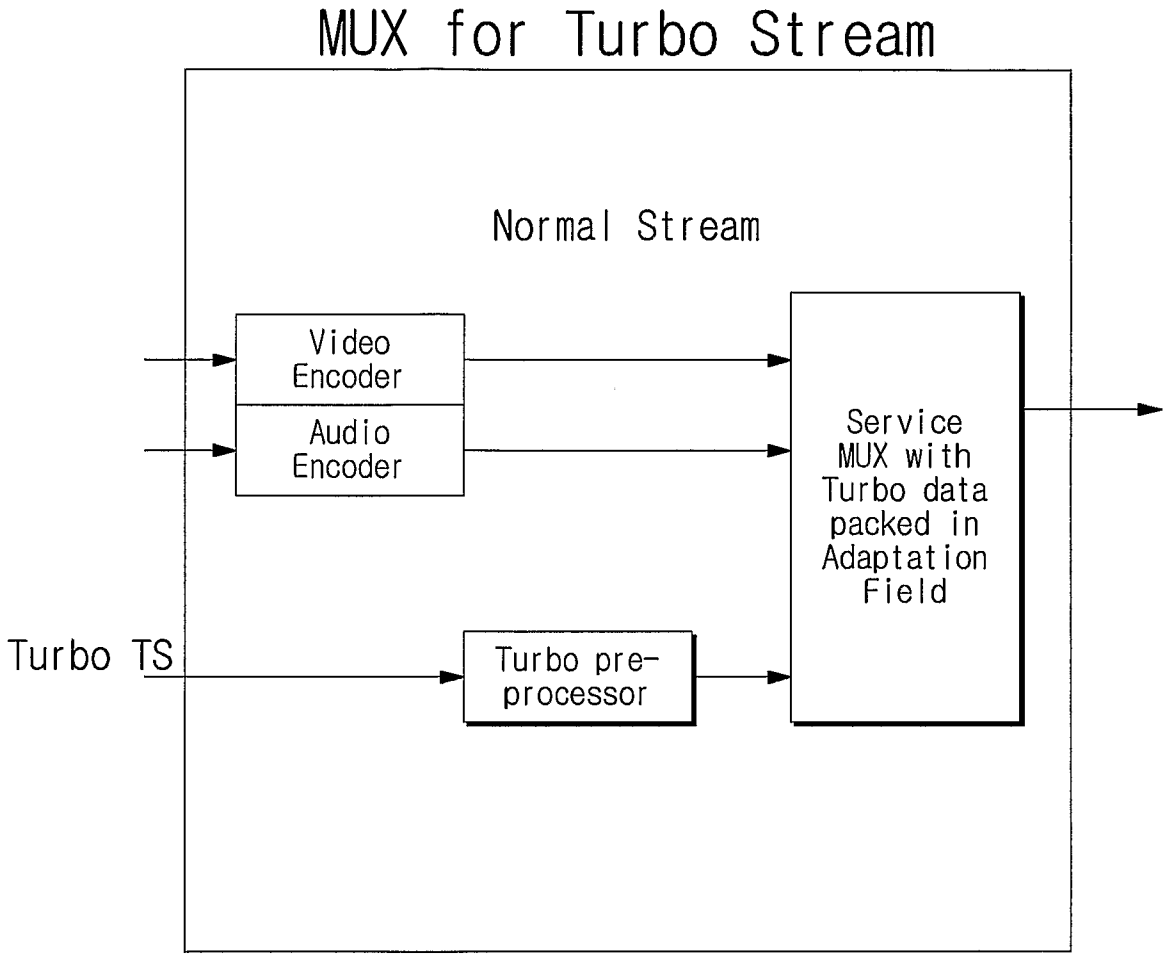


SFN Synchronizaion Timelines

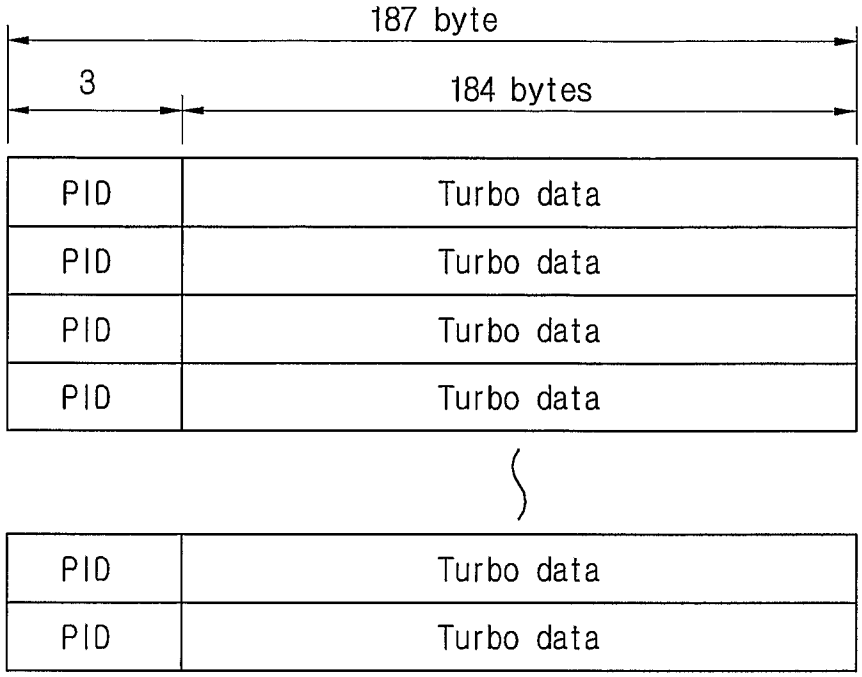
[Fig. 35]


ATSC EXCITER
NORMAL STREAM
A-VSB EMISSION MUX
TURBO TS
RANDOMIZE
REED-SOLOMON ENCODER
BYTE INTERLEAVE
TURBO POST-PROCESSOR
TCM 1
TCM 2
TCM 3
SEGMENT SYNC
FIELD SYNC
MUX
VSB MODULATOR
POWER AMPLIFIER
STATION ANTENNA
CURRENT BLOCK
NEWLY DEVELOPED BLOCK
MODIFLED BLOCK

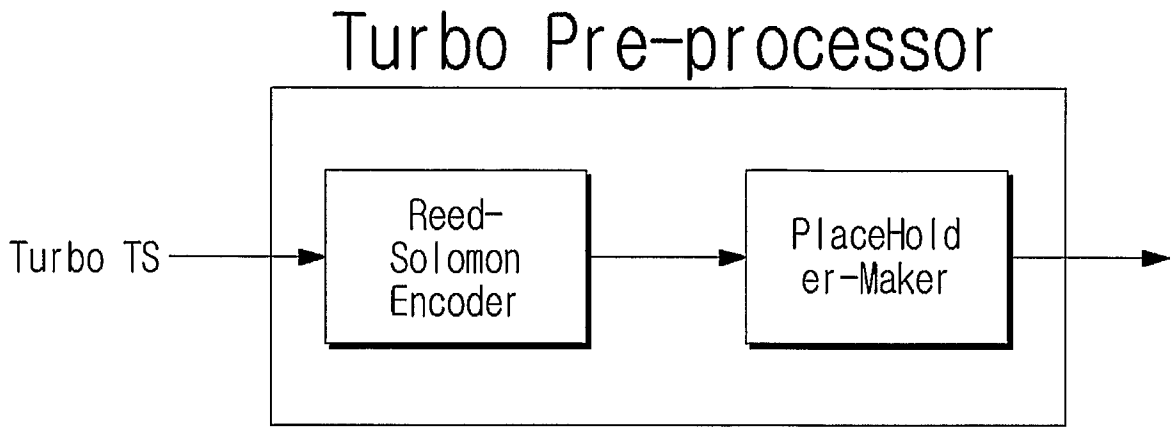
[Fig. 36]


MUX for Turbo Stream
Normal Stream
Video Encoder
Audio Encoder
Service MUX with Turbo data packed in Adaptation Field
Turbo TS
Turbo pre-processor

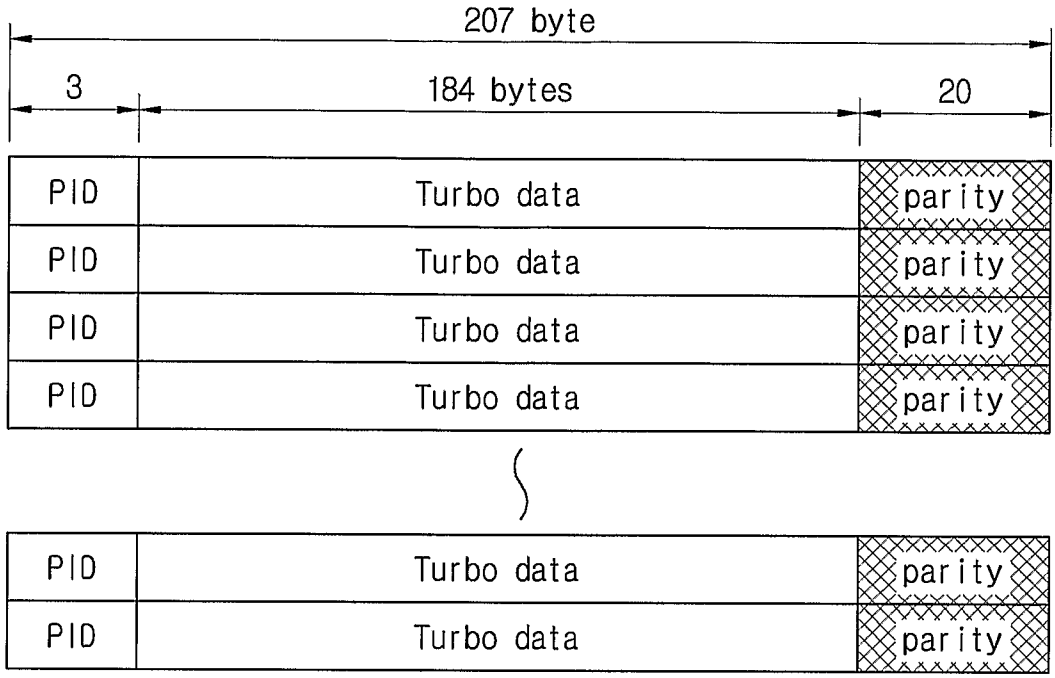
[Fig. 37]


187 byte
3
184 bytes
PID
Turbo data
PID
Turbo data
PID
Turbo data
PID
Turbo data
PID
Turbo data
PID
Turbo data

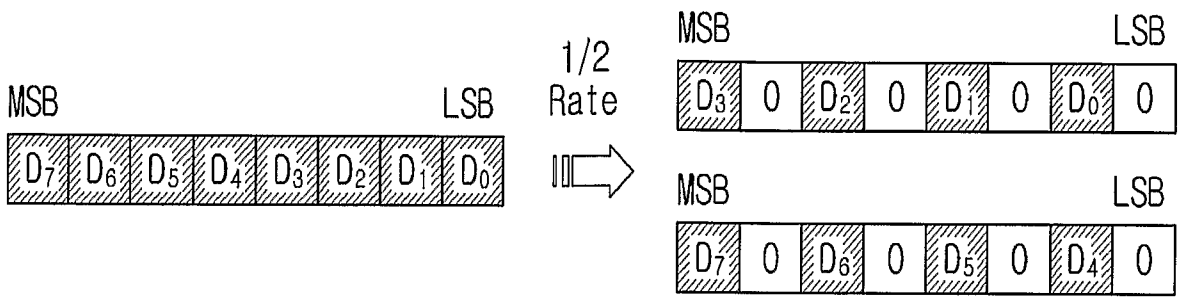
[Fig. 38]


Turbo Pre-processor
Turbo TS
Reed-Solomon Encoder
PlaceHolder-Maker

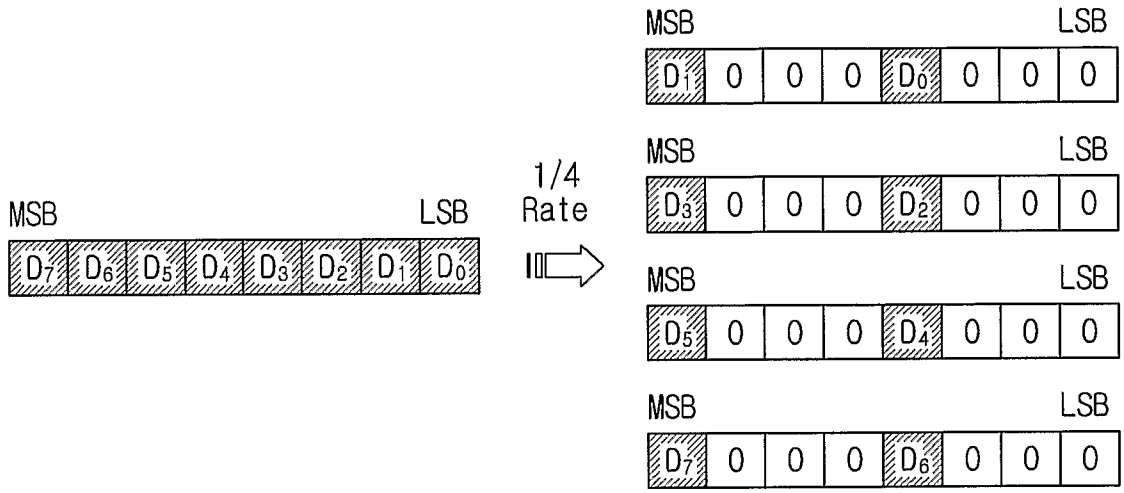
[Fig. 39]


207 byte
3
184 bytes
20
PID
Turbo data
parity
PID
Turbo data
parity
PID
Turbo data
parity
PID
Turbo data
parity
PID
Turbo data
parity
PID
Turbo data
parity

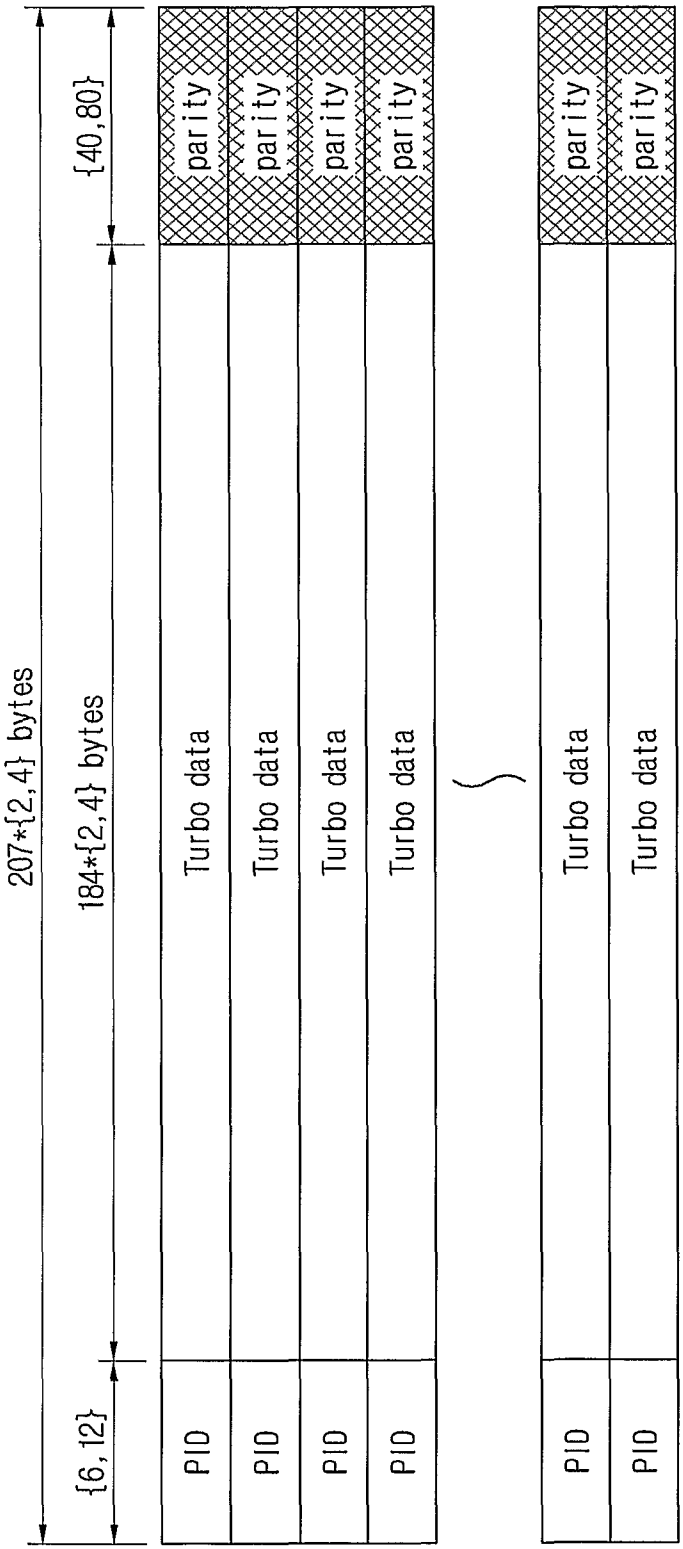
[Fig. 40]


Expansion by 2 [1byte -> 2bytes]
MSB
LSB
D7 D6 D5 D4 D3 D2 D1 D0
1/2
Rate
MSB
LSB
D3 0 D2 0 D1 0 D0 0
MSB
LSB
D7 0 D6 0 D5 0 D4 0

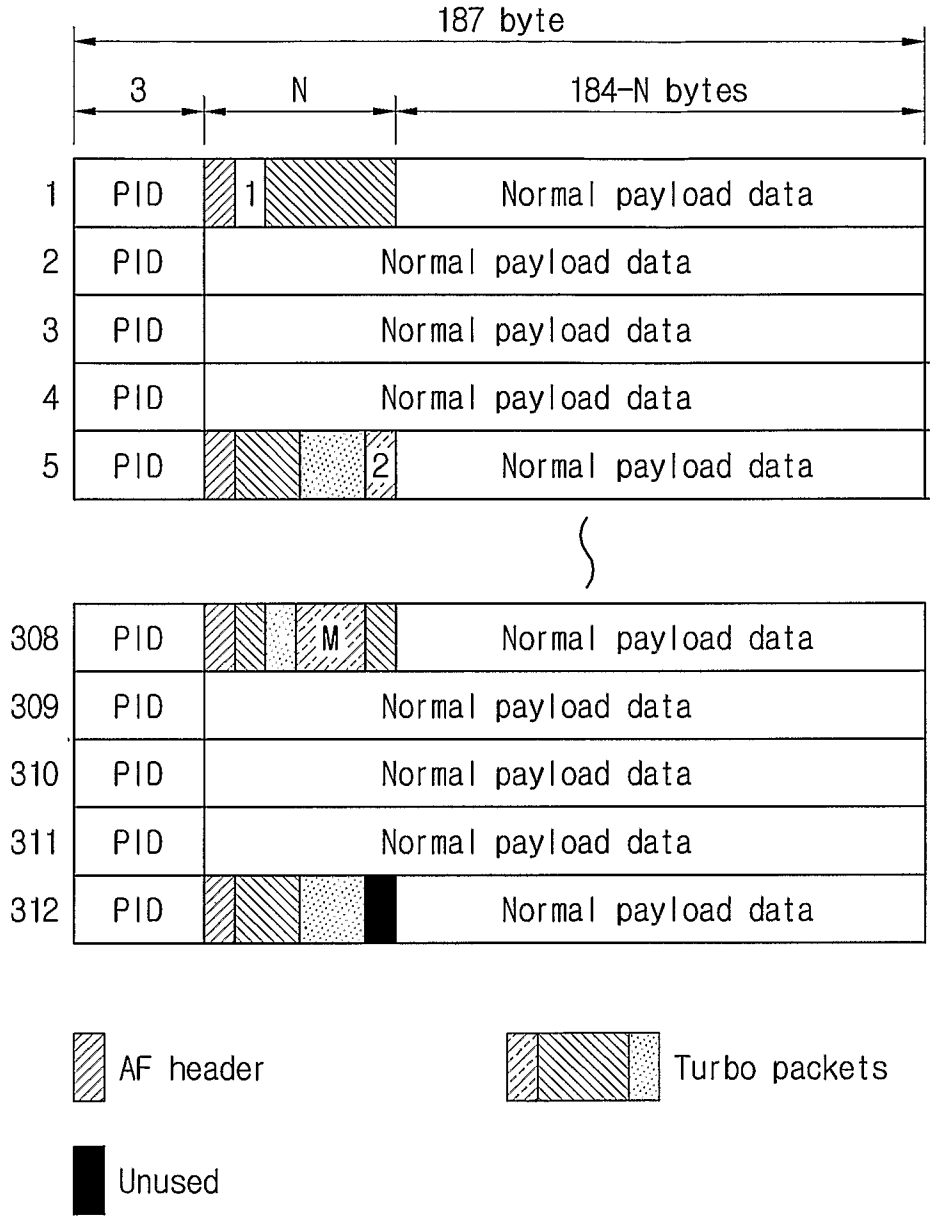
[Fig. 41]


Expansion by 4 [1byte -> 4bytes]
MSB
LSB
D7 D6 D5 D4 D3 D2 D1 D0
1/4
Rate
MSB
LSB
D1 0 0 0 D0 0 0 0
MSB
LSB
D3 0 0 0 D2 0 0 0
MSB
LSB
D5 0 0 0 D4 0 0 0
MSB
LSB
D7 0 0 0 D6 0 0 0

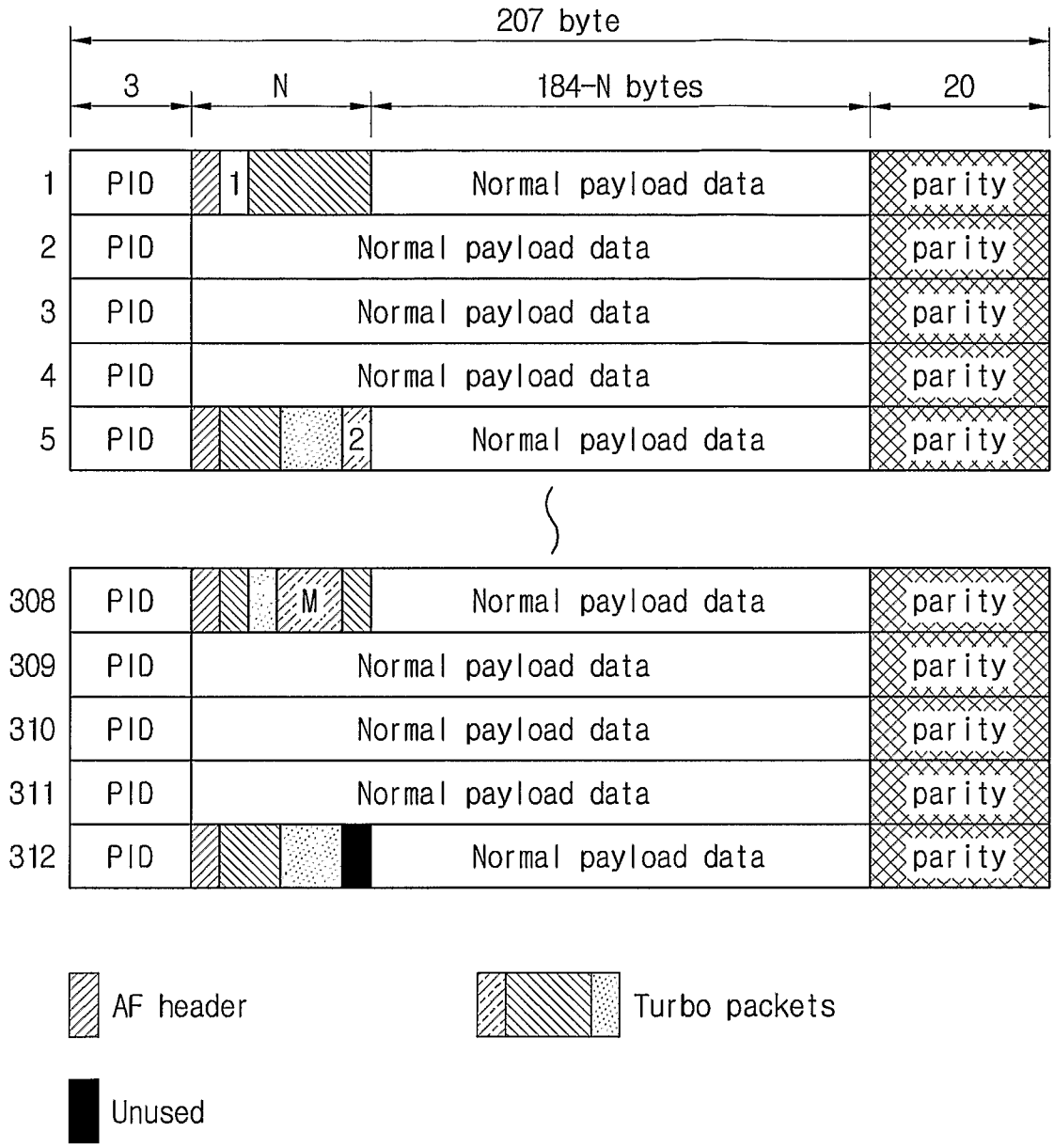
[Fig. 42]



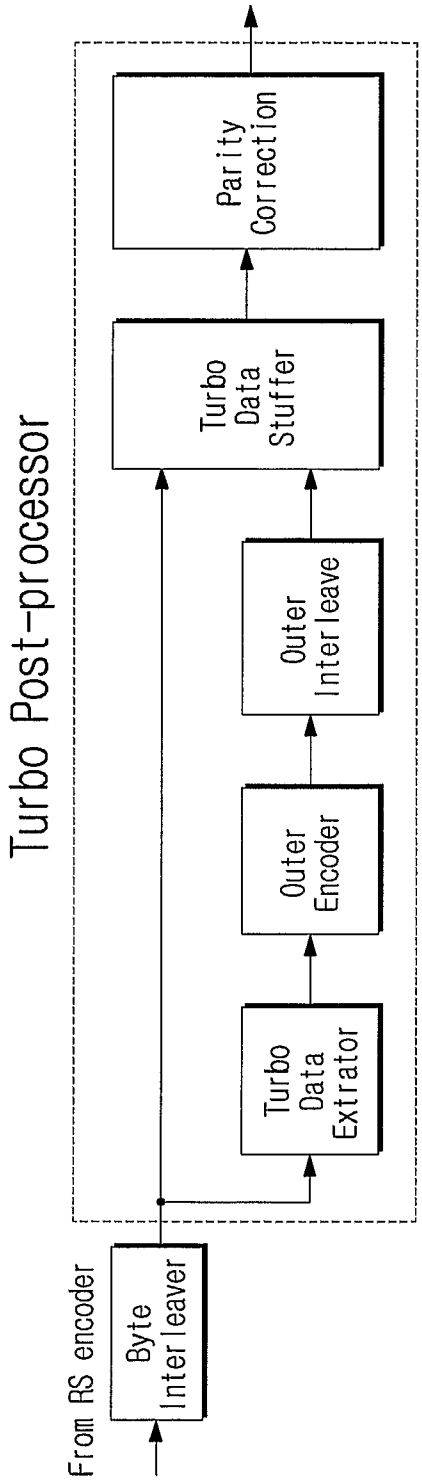
[Fig. 43]


187 byte
3
N
184-N bytes
1 PID 1 Normal payload data
2 PID Normal payload data
3 PID Normal payload data
4 PID Normal payload data
5 PID 2 Normal payload data
308 PID M Normal payload data
309 PID Normal payload data
310 PID Normal payload data
311 PID Normal payload data
312 PID Normal payload data
AF header
Turbo packets
Unused

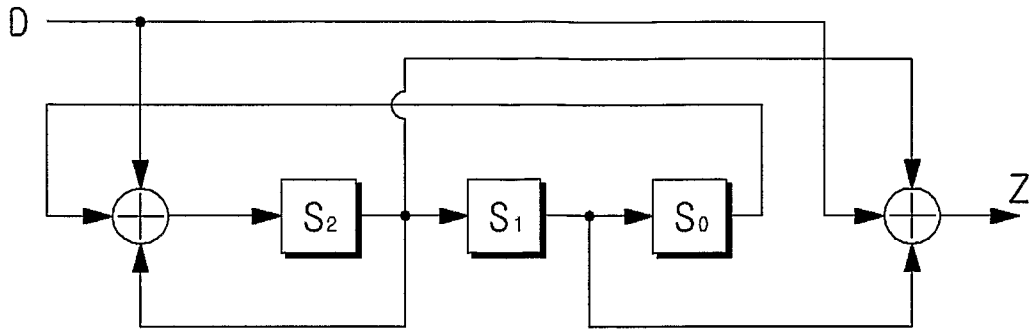
[Fig. 44]


207 byte
3
N
184-N bytes
20
1 PID 1 Normal payload data parity
2 PID Normal payload data parity
3 PID Normal payload data parity
4 PID Normal payload data parity
5 PID 2 Normal payload data parity
308 PID M Normal payload data parity
309 PID Normal payload data parity
310 PID Normal payload data parity
311 PID Normal payload data parity
312 PID Normal payload data parity
AF header
Turbo packets
Unused

[Fig. 45]

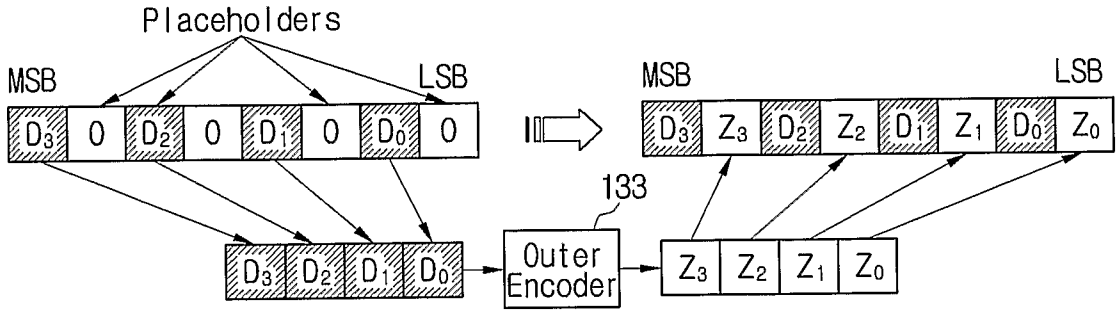

Turbo Post-processor
From RS encoder
Byte Interleaver
Turbo Data Extrator
Outer Encoder
Outer Interleave
Turbo Data Stuffer
Parity Correction

[Fig. 46]

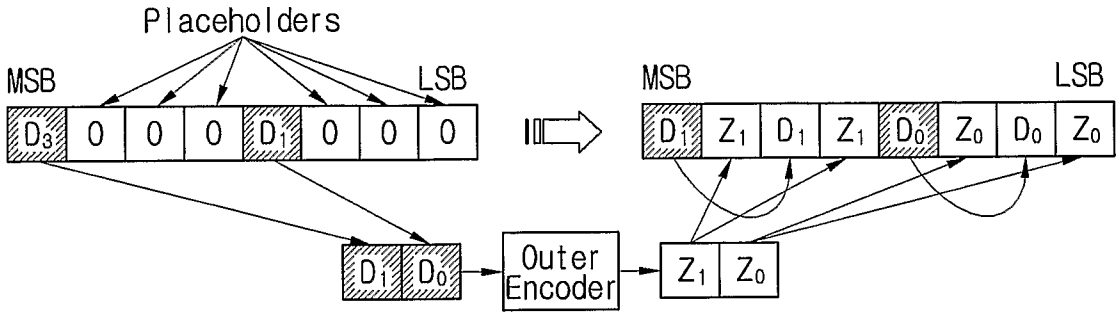


[Fig. 47]

1/2 rate encoding

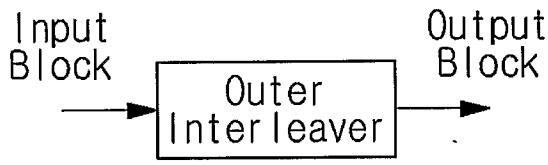


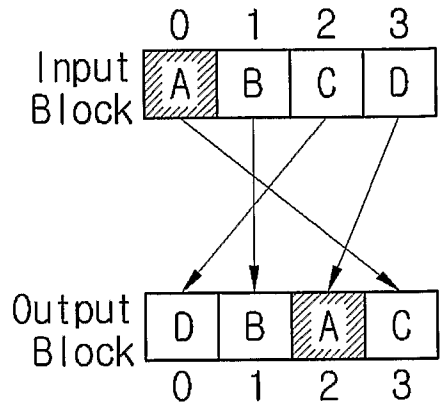
[Fig. 48]


1/2 rate encoding
Placeholders
MSB
LSB
D3 0 0 0 D1 0 0 0
D1 Z1 D1 Z1 D0 Z0 D0 Z0
D1 D0
Outer Encoder
Z1 Z0

[Fig. 49]

Interleaving Rule(L=4) = {n(i)|i=0,1,2,3} = {2,1,3,0}





[Fig. 50]

	3 bytes	2 bytes	128 bytes	54 bytes
1	PID	AF Header	128 bytes of Turbo data	54 bytes of Normal data
2	PID	184 bytes of Normal data		
3	PID	184 bytes of Normal data		
4	PID	184 bytes of Normal data		
5	PID	AF Header	128 bytes of Turbo data	54 bytes of Normal data
6	PID	184 bytes of Normal data		
7	PID	184 bytes of Normal data		
8	PID	184 bytes of Normal data		
9	PID	AF Header	128 bytes of Turbo data	54 bytes of Normal data
10	PID	184 bytes of Normal data		
11	PID	184 bytes of Normal data		
12	PID	184 bytes of Normal data		
13	PID	AF Header	128 bytes of Turbo data	54 bytes of Normal data
14	PID	184 bytes of Normal data		
15	PID	AF Header	reserved for PCR(6 bytes)	176 bytes of Normal data
16	PID	184 bytes of Normal data		
17	PID	AF Header	128 bytes of Turbo data	54 bytes of Normal data
18	PID	184 bytes of Normal data		
19	PID	AF Header	Splice(1 byte)	184 bytes of Normal data
20	PID	184 bytes of Normal data		
21	PID	AF Header	128 bytes of Turbo data	54 bytes of Normal data
22	PID	184 bytes of Normal data		
23	PID	184 bytes of Normal data		
24	PID	184 bytes of Normal data		
25	PID	AF Header	128 bytes of Turbo data	54 bytes of Normal data
26	PID	184 bytes of Normal data		
27	PID	184 bytes of Normal data		
28	PID	184 bytes of Normal data		
29	PID	AF Header	128 bytes of Turbo data	54 bytes of Normal data
30	PID	184 bytes of Normal data		
31	PID	184 bytes of Normal data		
32	PID	184 bytes of Normal data		
33	PID	AF Header	128 bytes of Turbo data	54 bytes of Normal data
34	PID	184 bytes of Normal data		
35	PID	184 bytes of Normal data		
36	PID	184 bytes of Normal data		
37	PID	AF Header	128 bytes of Turbo data	54 bytes of Normal data
38	PID	184 bytes of Normal data		
39	PID	184 bytes of Normal data		
40	PID	184 bytes of Normal data		
41	PID	AF Header	128 bytes of Turbo data	54 bytes of Normal data
42	PID	184 bytes of Normal data		
43	PID	184 bytes of Normal data		
44	PID	184 bytes of Normal data		
45	PID	AF Header	128 bytes of Turbo data	54 bytes of Normal data
46	PID	184 bytes of Normal data		
47	PID	184 bytes of Normal data		
48	PID	184 bytes of Normal data		
49	PID	AF Header	128 bytes of Turbo data	54 bytes of Normal data
50	PID	184 bytes of Normal data		
51	PID	184 bytes of Normal data		
52	PID	184 bytes of Normal data		

[Fig. 51]

	3 bytes	2 bytes	128 bytes	182-128 bytes
1	PID	184 bytes of Normal data		
2	PID	184 bytes of Normal data		
3	PID	AF Header	16 bytes of Turbo data	166 bytes of Normal data
4	PID	184 bytes of Normal data		
5	PID	184 bytes of Normal data		
6	PID	184 bytes of Normal data		
7	PID	AF Header	16 bytes of Turbo data	166 bytes of Normal data
8	PID	184 bytes of Normal data		
9	PID	184 bytes of Normal data		
10	PID	184 bytes of Normal data		
11	PID	AF Header	16 bytes of Turbo data	166 bytes of Normal data
12	PID	184 bytes of Normal data		
13	PID	184 bytes of Normal data		
14	PID	184 bytes of Normal data		
15	PID	AF Header	reserved for PCR(6 bytes)	16 bytes of Turbo D	160 bytes of Normal Data
16	PID	184 bytes of Normal data		
17	PID	184 bytes of Normal data		
18	PID	184 bytes of Normal data		
19	PID	AF Header	Splice(1 byte)	16 bytes of Turbo Data	165 bytes of Normal Data
20	PID	184 bytes of Normal data		
21	PID	184 bytes of Normal data		
22	PID	184 bytes of Normal data		
23	PID	AF Header	16 bytes of Turbo data	166 bytes of Normal data
24	PID	184 bytes of Normal data		
25	PID	184 bytes of Normal data		
26	PID	184 bytes of Normal data		
27	PID	AF Header	16 bytes of Turbo data	166 bytes of Normal data
28	PID	184 bytes of Normal data		
29	PID	184 bytes of Normal data		
30	PID	184 bytes of Normal data		
31	PID	AF Header	16 bytes of Turbo data	166 bytes of Normal data
32	PID	184 bytes of Normal data		
33	PID	184 bytes of Normal data		
34	PID	184 bytes of Normal data		
35	PID	AF Header	16 bytes of Turbo data	166 bytes of Normal data
36	PID	184 bytes of Normal data		
37	PID	184 bytes of Normal data		
38	PID	184 bytes of Normal data		
39	PID	AF Header	16 bytes of Turbo data	166 bytes of Normal data
40	PID	184 bytes of Normal data		
41	PID	184 bytes of Normal data		
42	PID	184 bytes of Normal data		
43	PID	AF Header	16 bytes of Turbo data	166 bytes of Normal data
44	PID	184 bytes of Normal data		
45	PID	184 bytes of Normal data		
46	PID	184 bytes of Normal data		
47	PID	AF Header	16 bytes of Turbo data	166 bytes of Normal data
48	PID	184 bytes of Normal data		
49	PID	184 bytes of Normal data		
50	PID	184 bytes of Normal data		
51	PID	AF Header	16 bytes of Turbo data	166 bytes of Normal data
52	PID	184 bytes of Normal data		

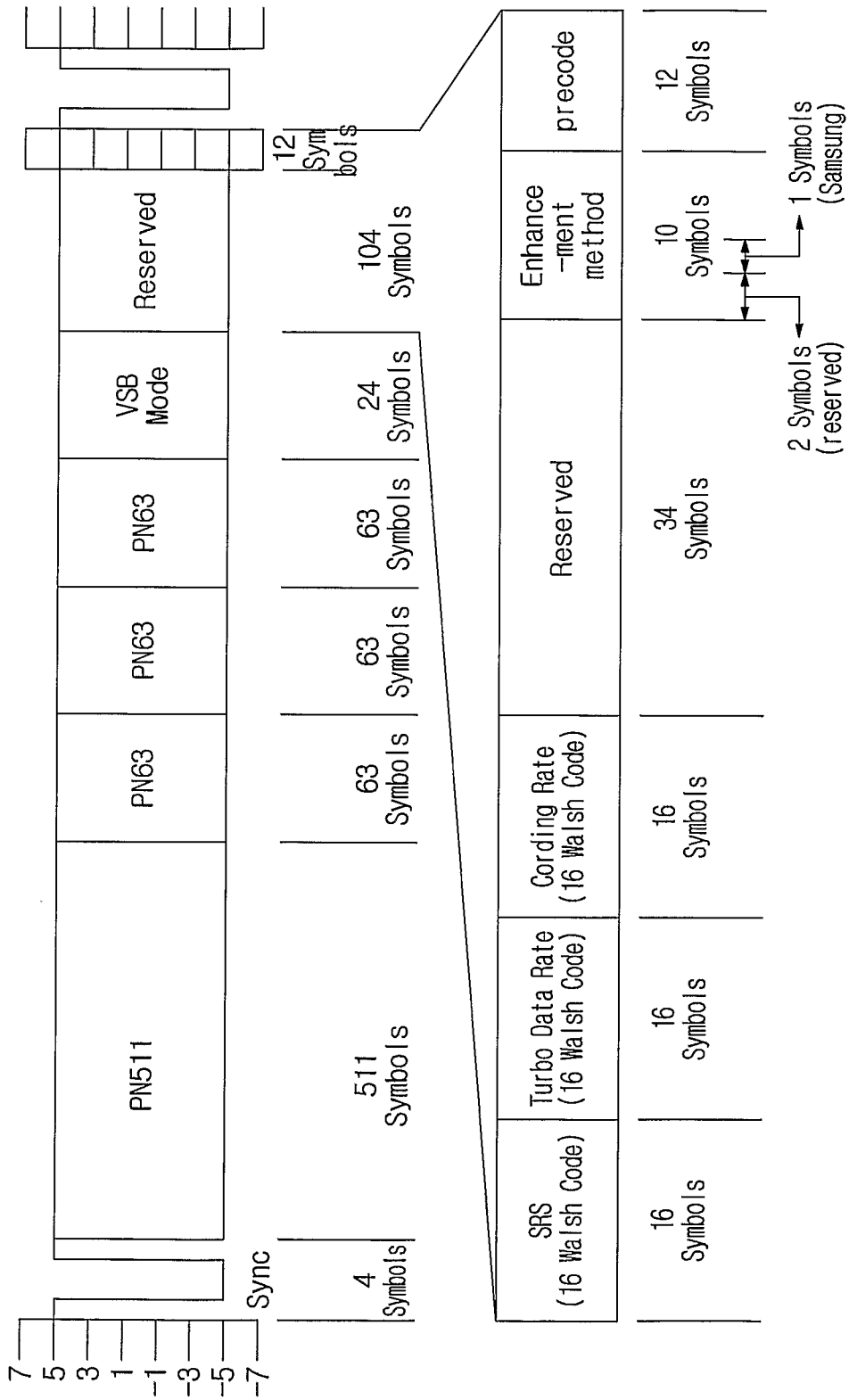
[Fig. 52]

	3 bytes	2 bytes	SRS		Turbo Data	Normal Data
1	Header	AF Header	SRS {10,20,26}		Turbo 128	Normal 54_{10,20,26}
2	Header	AF Header	SRS {10,20,26}		Normal 182-{10,20,26}	
3	Header	AF Header	SRS {10,20,26}		Normal 182-{10,20,26}	
4	Header	AF Header	SRS {10,20,26}		Normal 182-{10,20,26}	
5	Header	AF Header	SRS {10,20,26}		Turbo 128	Normal 54_{10,20,26}
6	Header	AF Header	SRS {10,20,26}		Normal 182-{10,20,26}	
7	Header	AF Header	SRS {10,20,26}		Normal 182-{10,20,26}	
8	Header	AF Header	SRS {10,20,26}		Normal 182-{10,20,26}	
9	Header	AF Header	SRS {10,20,26}		Turbo 128	Normal 54_{10,20,26}
10	Header	AF Header	SRS {10,20,26}		Normal 182-{10,20,26}	
11	Header	AF Header	SRS {10,20,26}		Normal 182-{10,20,26}	
12	Header	AF Header	SRS {10,20,26}		Normal 182-{10,20,26}	
13	Header	AF Header	SRS {10,20,26}		Turbo 128	Normal 54_{10,20,26}
14	Header	AF Header	SRS {10,20,26}		Normal 182-{10,20,26}	
15	Header	AF Header	PCR (6)	SRS {4,14,20}	Normal 182-{10,20,26}	
16	Header	AF Header	SRS {10,20,26}		Normal 182-{10,20,26}	
17	Header	AF Header	SRS {10,20,26}		Turbo 128	Normal 54_{10,20,26}
18	Header	AF Header	SRS {10,20,26}		Normal 182-{10,20,26}	
19	Header	AF Header	Splice (1)	SRS {9,19,25}	Normal 182-{10,20,26}	
20	Header	AF Header	SRS {10,20,26}		Normal 182-{10,20,26}	
21	Header	AF Header	SRS {10,20,26}		Turbo 128	Normal 54_{10,20,26}
22	Header	AF Header	SRS {10,20,26}		Normal 182-{10,20,26}	
23	Header	AF Header	SRS {10,20,26}		Normal 182-{10,20,26}	
24	Header	AF Header	SRS {10,20,26}		Normal 182-{10,20,26}	
25	Header	AF Header	SRS {10,20,26}		Turbo 128	Normal 54_{10,20,26}
26	Header	AF Header	SRS {10,20,26}		Normal 182-{10,20,26}	
27	Header	AF Header	SRS {10,20,26}		Normal 182-{10,20,26}	
28	Header	AF Header	SRS {10,20,26}		Normal 182-{10,20,26}	
29	Header	AF Header	SRS {10,20,26}		Turbo 128	Normal 54_{10,20,26}
30	Header	AF Header	SRS {10,20,26}		Normal 182-{10,20,26}	
31	Header	AF Header	SRS {10,20,26}		Normal 182-{10,20,26}	
32	Header	AF Header	SRS {10,20,26}		Normal 182-{10,20,26}	
33	Header	AF Header	SRS {10,20,26}		Turbo 128	Normal 54_{10,20,26}
34	Header	AF Header	SRS {10,20,26}		Normal 182-{10,20,26}	
35	Header	AF Header	SRS {10,20,26}		Normal 182-{10,20,26}	
36	Header	AF Header	SRS {10,20,26}		Normal 182-{10,20,26}	
37	Header	AF Header	SRS {10,20,26}		Turbo 128	Normal 54_{10,20,26}
38	Header	AF Header	SRS {10,20,26}		Normal 182-{10,20,26}	
39	Header	AF Header	SRS {10,20,26}		Normal 182-{10,20,26}	
40	Header	AF Header	SRS {10,20,26}		Normal 182-{10,20,26}	
41	Header	AF Header	SRS {10,20,26}		Turbo 128	Normal 54_{10,20,26}
42	Header	AF Header	SRS {10,20,26}		Normal 182-{10,20,26}	
43	Header	AF Header	SRS {10,20,26}		Normal 182-{10,20,26}	
44	Header	AF Header	SRS {10,20,26}		Normal 182-{10,20,26}	
45	Header	AF Header	SRS {10,20,26}		Turbo 128	Normal 54_{10,20,26}
46	Header	AF Header	SRS {10,20,26}		Normal 182-{10,20,26}	
47	Header	AF Header	SRS {10,20,26}		Normal 182-{10,20,26}	
48	Header	AF Header	SRS {10,20,26}		Normal 182-{10,20,26}	
49	Header	AF Header	SRS {10,20,26}		Turbo 128	Normal 54_{10,20,26}
50	Header	AF Header	SRS {10,20,26}		Normal 182-{10,20,26}	
51	Header	AF Header	SRS {10,20,26}		Normal 182-{10,20,26}	
52	Header	AF Header	SRS {10,20,26}		Normal 182-{10,20,26}	

[Fig. 53]

	3 bytes	2 bytes	SRS		Turbo Data	Normal Data
1	Header	AF Header	SRS {10,20,26}		Turbo 182-{10,20,26}	
2	Header	AF Header	SRS {10,20,26}		Turbo 182-{10,20,26}	
3	Header	AF Header	SRS {10,20,26}		Turbo 20+2*{10,20,26}	Normal 162-3*{10,20,26}
4	Header	AF Header	SRS {10,20,26}		Normal 182-{10,20,26}	
5	Header	AF Header	SRS {10,20,26}		Turbo 182-{10,20,26}	
6	Header	AF Header	SRS {10,20,26}		Turbo 182-{10,20,26}	
7	Header	AF Header	SRS {10,20,26}		Turbo 20+2*{10,20,26}	Normal 162-3*{10,20,26}
8	Header	AF Header	SRS {10,20,26}		Normal 182-{10,20,26}	
9	Header	AF Header	SRS {10,20,26}		Turbo 182-{10,20,26}	
10	Header	AF Header	SRS {10,20,26}		Turbo 182-{10,20,26}	
11	Header	AF Header	SRS {10,20,26}		Turbo 20+2*{10,20,26}	Normal 162-3*{10,20,26}
12	Header	AF Header	SRS {10,20,26}		Normal 182-{10,20,26}	
13	Header	AF Header	SRS {10,20,26}		Turbo 182-{10,20,26}	
14	Header	AF Header	SRS {10,20,26}		Turbo 182-{10,20,26}	
15	Header	AF Header	PCR (6)	SRS {4,14,20}	Turbo 20+2*{10,20,26}	Normal 162-3*{10,20,26}
16	Header	AF Header	SRS {10,20,26}		Normal 182-{10,20,26}	
17	Header	AF Header	SRS {10,20,26}		Turbo 182-{10,20,26}	
18	Header	AF Header	SRS {10,20,26}		Turbo 182-{10,20,26}	
19	Header	AF Header	Splice (1)	SRS {9,19,25}	Turbo 20+2*{10,20,26}	Normal 162-3*{10,20,26}
20	Header	AF Header	SRS {10,20,26}		Normal 182-{10,20,26}	
21	Header	AF Header	SRS {10,20,26}		Turbo 182-{10,20,26}	
22	Header	AF Header	SRS {10,20,26}		Turbo 182-{10,20,26}	
23	Header	AF Header	SRS {10,20,26}		Turbo 20+2*{10,20,26}	Normal 162-3*{10,20,26}
24	Header	AF Header	SRS {10,20,26}		Normal 182-{10,20,26}	
25	Header	AF Header	SRS {10,20,26}		Turbo 182-{10,20,26}	
26	Header	AF Header	SRS {10,20,26}		Turbo 182-{10,20,26}	
27	Header	AF Header	SRS {10,20,26}		Turbo 20+2*{10,20,26}	Normal 162-3*{10,20,26}
28	Header	AF Header	SRS {10,20,26}		Normal 182-{10,20,26}	
29	Header	AF Header	SRS {10,20,26}		Turbo 182-{10,20,26}	
30	Header	AF Header	SRS {10,20,26}		Turbo 182-{10,20,26}	
31	Header	AF Header	SRS {10,20,26}		Turbo 20+2*{10,20,26}	Normal 162-3*{10,20,26}
32	Header	AF Header	SRS {10,20,26}		Normal 182-{10,20,26}	
33	Header	AF Header	SRS {10,20,26}		Turbo 182-{10,20,26}	
34	Header	AF Header	SRS {10,20,26}		Turbo 182-{10,20,26}	
35	Header	AF Header	SRS {10,20,26}		Turbo 20+2*{10,20,26}	Normal 162-3*{10,20,26}
36	Header	AF Header	SRS {10,20,26}		Normal 182-{10,20,26}	
37	Header	AF Header	SRS {10,20,26}		Turbo 182-{10,20,26}	
38	Header	AF Header	SRS {10,20,26}		Turbo 182-{10,20,26}	
39	Header	AF Header	SRS {10,20,26}		Turbo 20+2*{10,20,26}	Normal 162-3*{10,20,26}
40	Header	AF Header	SRS {10,20,26}		Normal 182-{10,20,26}	
41	Header	AF Header	SRS {10,20,26}		Turbo 182-{10,20,26}	
42	Header	AF Header	SRS {10,20,26}		Turbo 182-{10,20,26}	
43	Header	AF Header	SRS {10,20,26}		Turbo 20+2*{10,20,26}	Normal 162-3*{10,20,26}
44	Header	AF Header	SRS {10,20,26}		Normal 182-{10,20,26}	
45	Header	AF Header	SRS {10,20,26}		Turbo 182-{10,20,26}	
46	Header	AF Header	SRS {10,20,26}		Turbo 182-{10,20,26}	
47	Header	AF Header	SRS {10,20,26}		Turbo 20+2*{10,20,26}	Normal 162-3*{10,20,26}
48	Header	AF Header	SRS {10,20,26}		Normal 182-{10,20,26}	
49	Header	AF Header	SRS {10,20,26}		Turbo 182-{10,20,26}	
50	Header	AF Header	SRS {10,20,26}		Turbo 182-{10,20,26}	
51	Header	AF Header	SRS {10,20,26}		Turbo 20+2*{10,20,26}	Normal 162-3*{10,20,26}
52	Header	AF Header	SRS {10,20,26}		Normal 182-{10,20,26}	

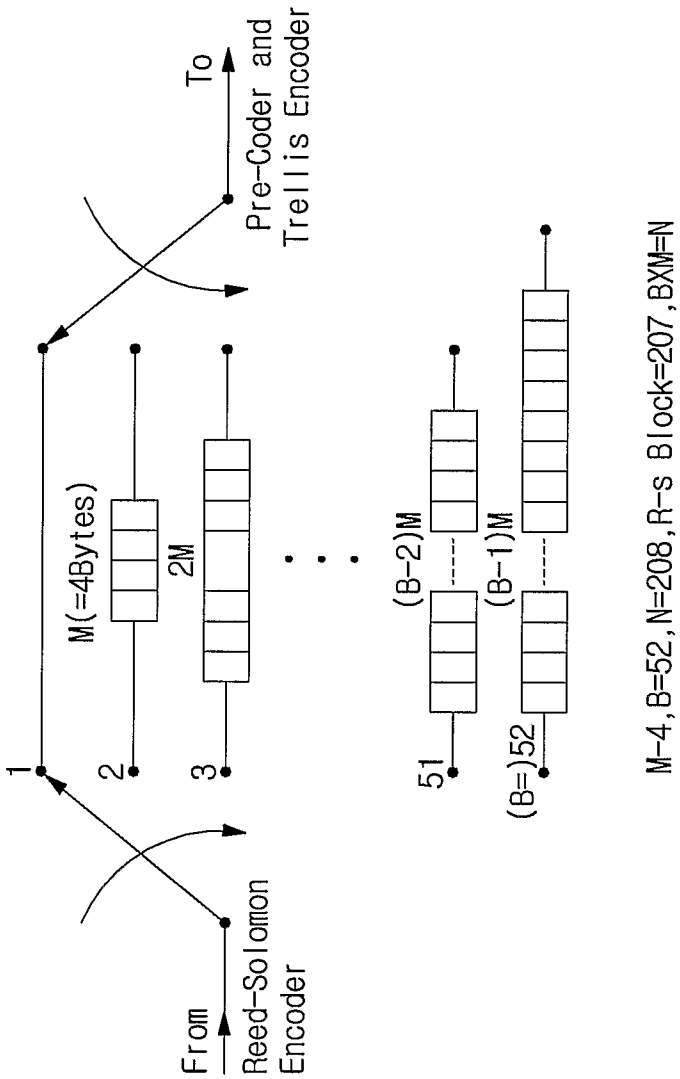
[Fig. 54]


7
5
3
1
-1
-3
-5
-7
Sync
4 Symbols
PN511
PN63
PN63
PN63
VSB Mode
Reserved
12 Symbols
511 Symbols
63 Symbols
63 Symbols
63 Symbols
24 Symbols
104 Symbols
SRS (16 Walsh Code)
Turbo Data Rate (16 Walsh Code)
Cording Rate (16 Walsh Code)
Reserved
Enhance-ment method
precode
16 Symbols
16 Symbols
16 Symbols
34 Symbols
10 Symbols
12 Symbols
1 Symbols (Samsung)
2 Symbols (reserved)

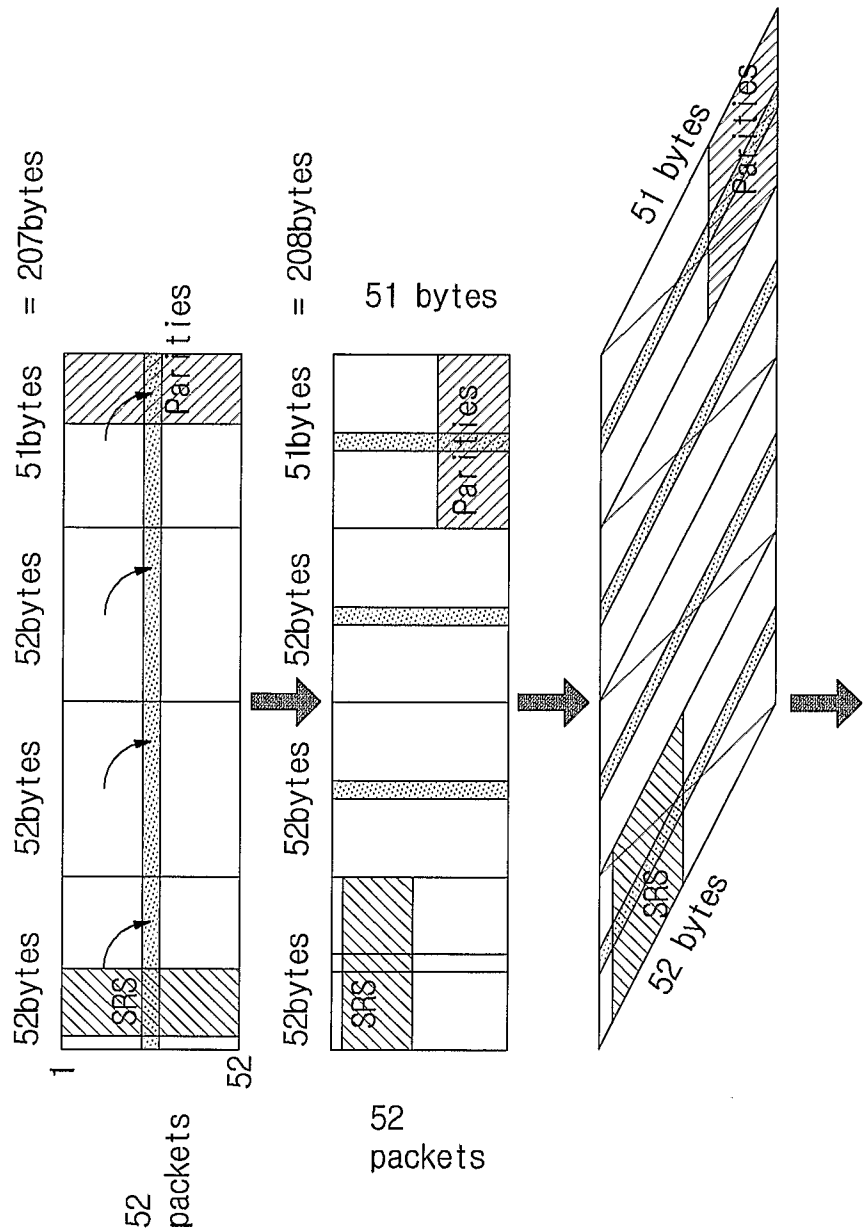
[Fig. 55]

		Walch Chip within Symbol															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Modulation Symbol Index	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
	2	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
	3	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0
	4	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
	5	0	1	0	1	1	0	1	0	0	1	0	1	1	0	1	0
	6	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0
	7	0	1	1	0	1	0	0	1	0	1	1	0	1	0	0	1
	8	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	9	0	1	0	1	0	1	0	1	1	0	1	0	1	0	1	0
	10	0	0	1	1	0	0	1	1	1	1	0	0	1	1	0	0
	11	0	1	1	0	0	1	1	0	1	0	0	1	1	0	0	1
	12	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0
	13	0	1	0	1	1	0	1	0	1	0	1	0	0	1	0	1
	14	0	0	1	1	1	1	0	0	1	1	0	0	0	0	1	1
	15	0	1	1	0	1	0	0	1	1	0	0	1	0	1	1	0

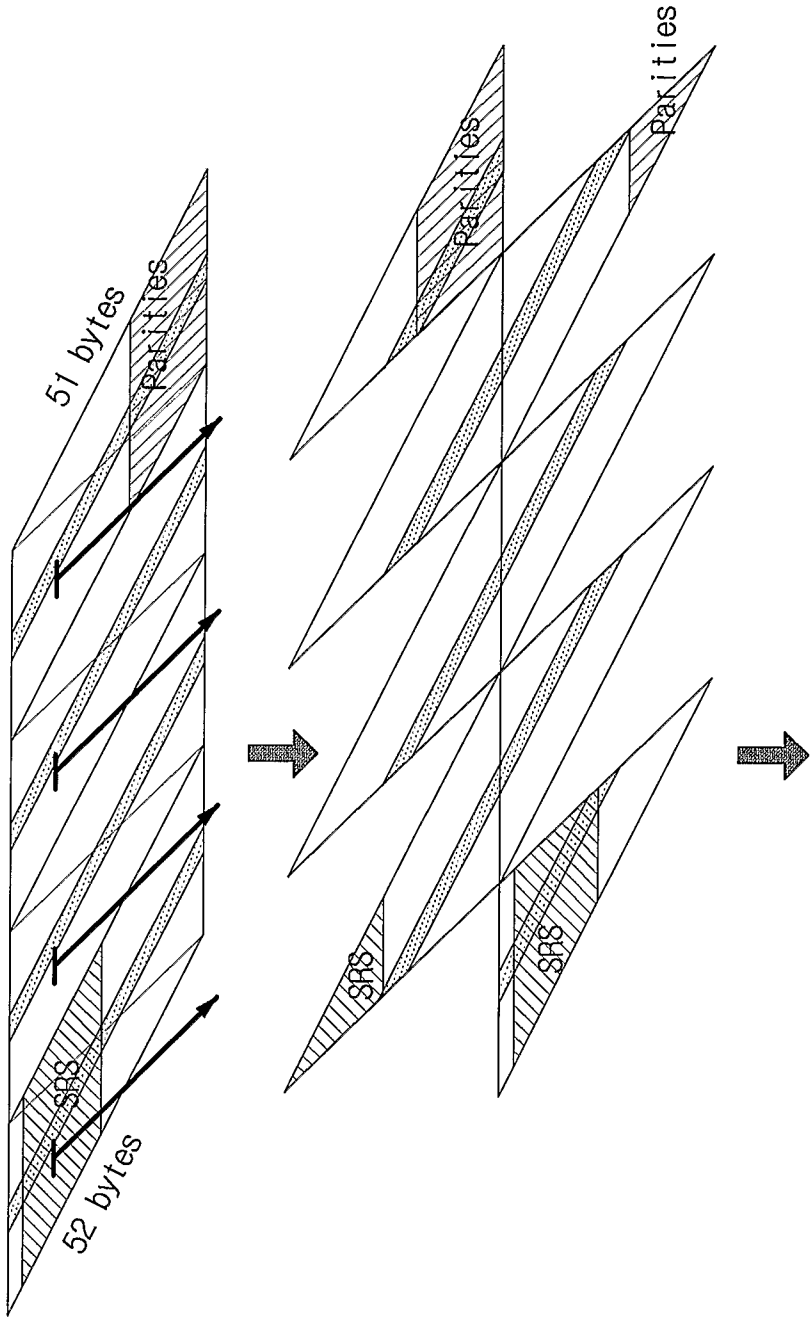
[Fig. 56]


From
Reed-Solomon Encoder
To
Pre-Coder and Trellis Encoder
1
2
3
51
(B=)52
M(=4Bytes)
2M
(B-2)M
(B-1)M
M=4, B=52, N=208, R-s Block=207, BXM=N

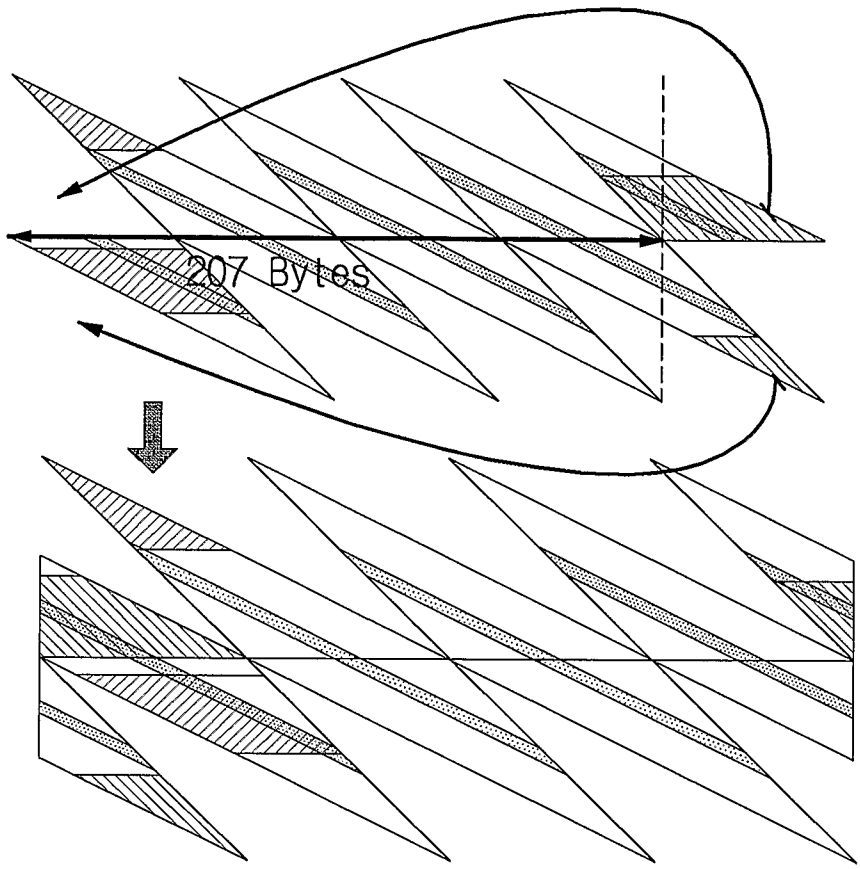
[Fig. 57]


= 207bytes
51bytes
52bytes
52bytes
52bytes
Parities
SRS
1
52
52 packets
= 208bytes
51 bytes
51bytes
52bytes
52bytes
52bytes
Parities
SRS
52 packets
51 bytes
Parities
SRS
52 bytes

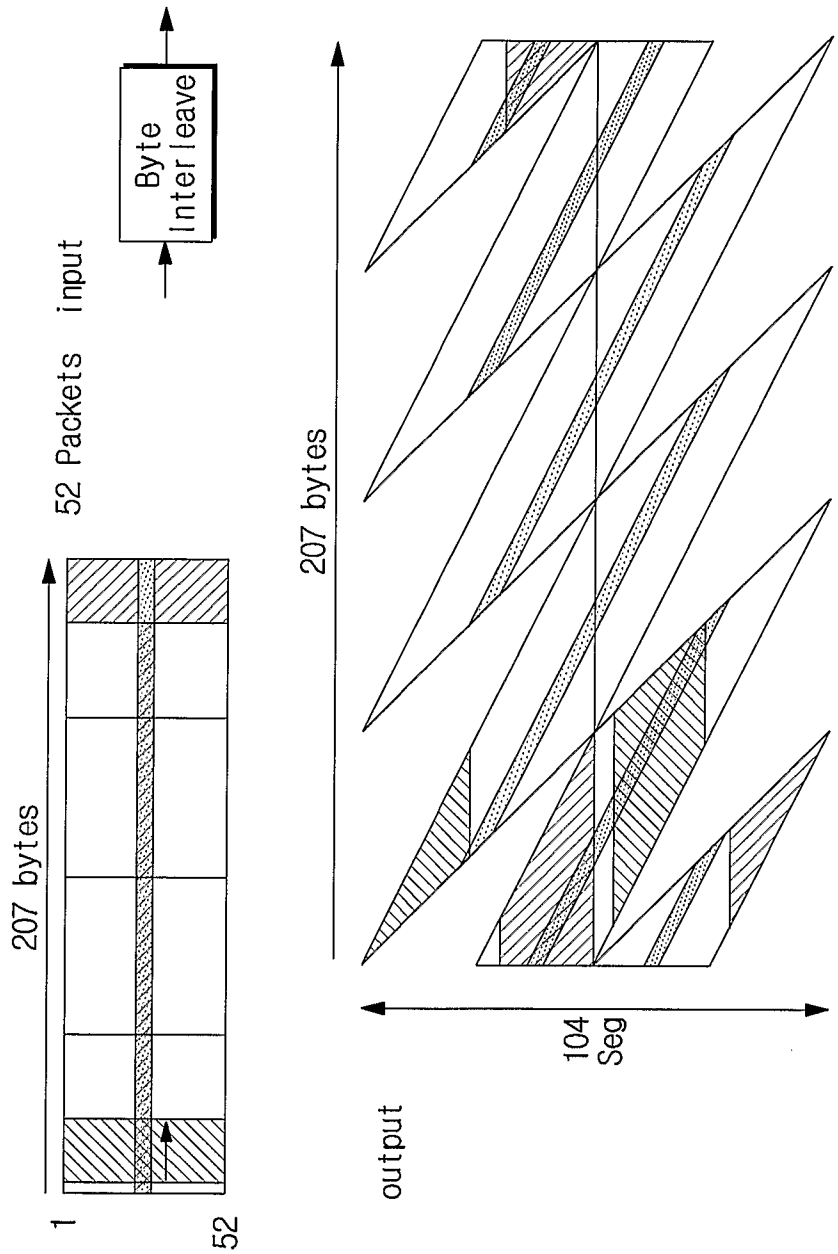
[Fig. 58]



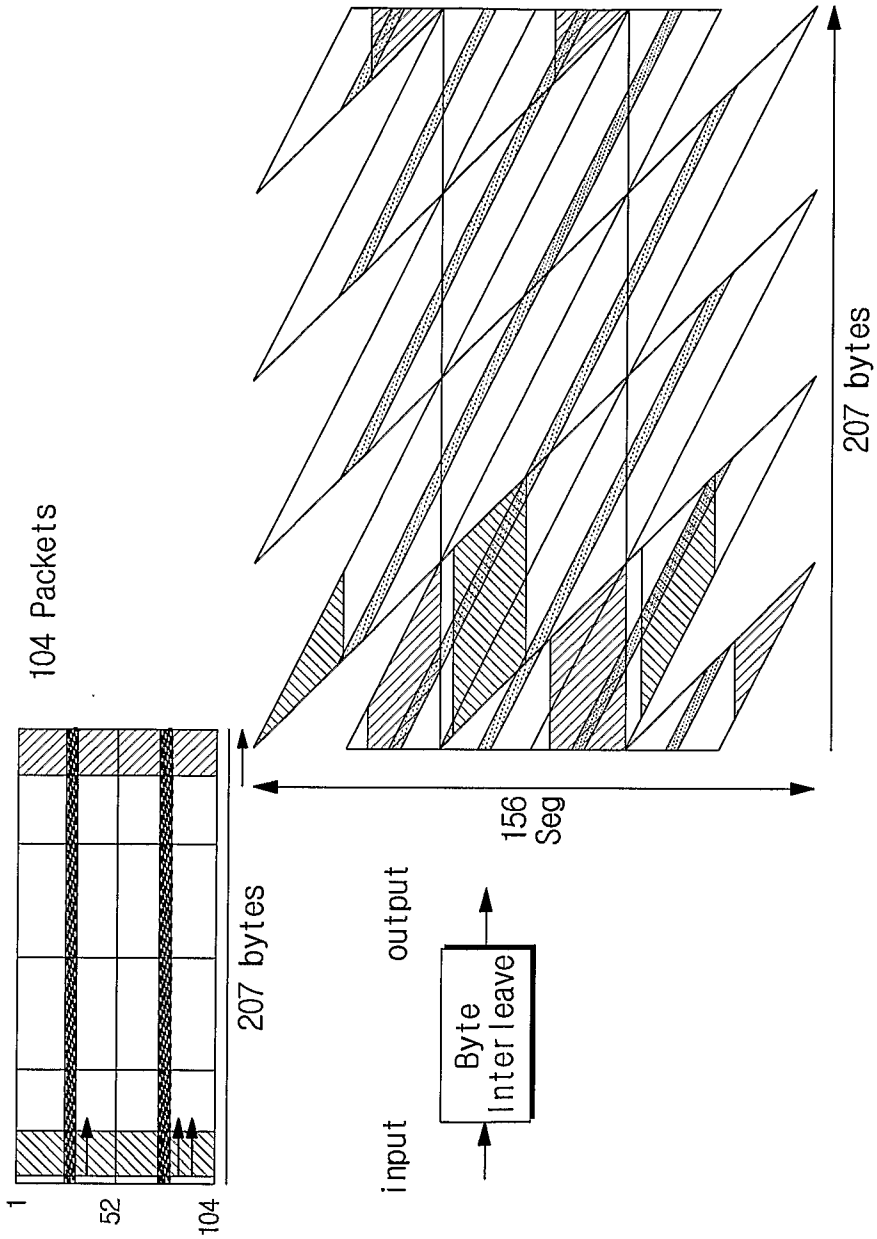
[Fig. 59]



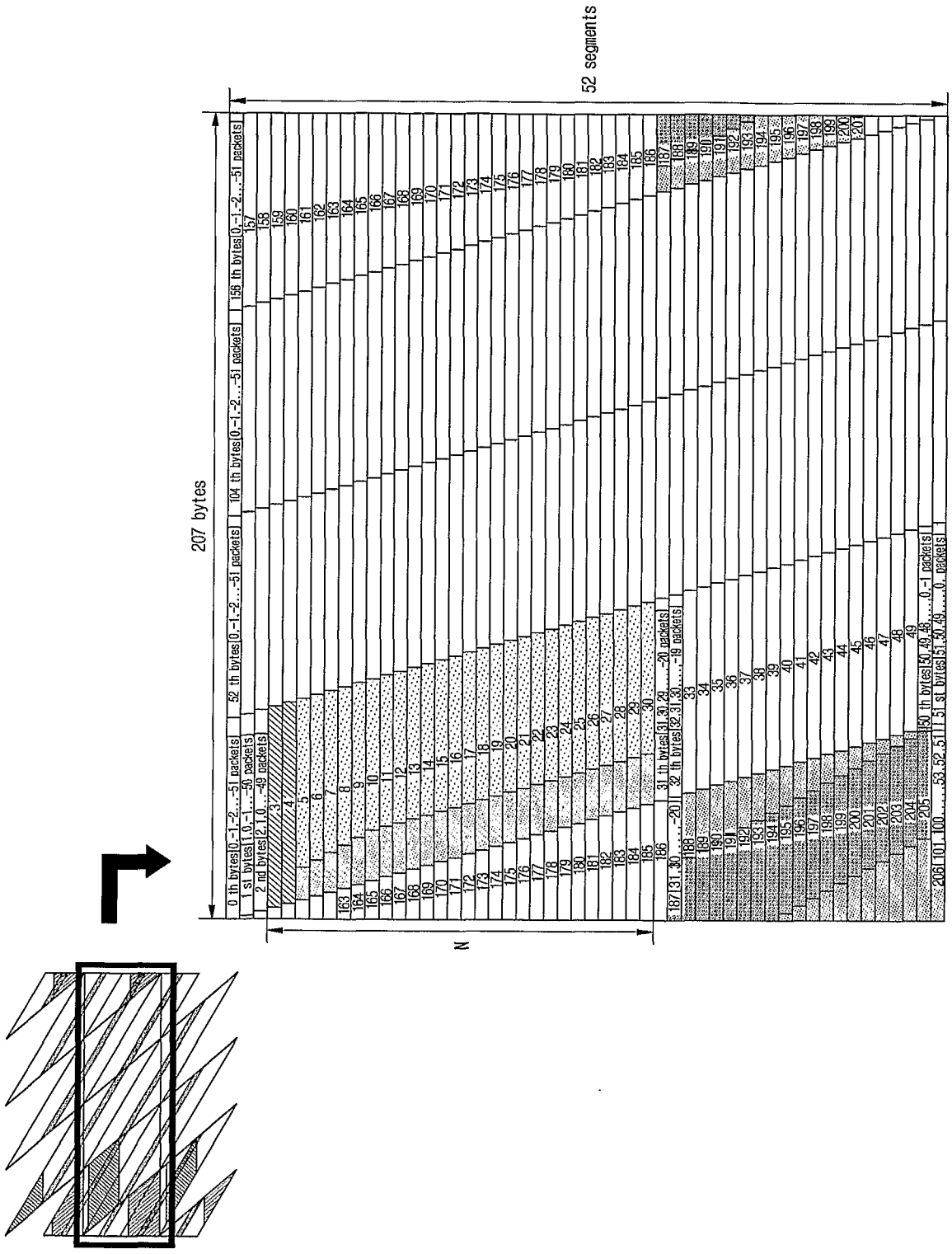
[Fig. 60]


Byte Interleave
52 Packets input
207 bytes
1
52
207 bytes
104 Seg
output

[Fig. 61]


104 Packets
207 bytes
156 Seg
207 bytes
output
Byte Interleave
input
1
52
104

[Fig. 62]



INTERNATIONAL SEARCH REPORT

International application No.
PCT/KR2007/001667

A. CLASSIFICATION OF SUBJECT MATTER

H04N 7/24(2006.01)i, H04N 7/64(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 8 H04N

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean Utility models and applications for Utility models : IPC as above

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKIPASS (KIPO internal) : "ATSC, Digital Television, A-VSB, MPEG-2 Transport Stream"

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 6738102 B1 (JONG SEOK PARK ET AL) 18 May. 2004 See abstract.	1-17
A	WO 2004/06283 A1 (KIM SUNG HOON ET AL) 22 July. 2004 See abstract.	1-17

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
12 JULY 2007 (12.07.2007)	**13 JULY 2007 (13.07.2007)**
Name and mailing address of the ISA/KR Korean Intellectual Property Office 920 Dunsan-dong, Seo-gu, Daejeon 302-701, Republic of Korea Facsimile No. 82-42-472-7140	Authorized officer KU, Dae Sung Telephone No. 82-42-481-8192

Form PCT/ISA/210 (second sheet) (April 2007)

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/KR2007/001667

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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WO2004/062283	22.07.2004	AU2003288781A1	29.07.2004
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		MXPA05007353A	30.03.2006
		US20060269012A1	30.11.2006
		WO2004062283A1	22.07.2004