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Zegarski et al.

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[54] **SHOCK FALSING INHIBITOR CIRCUIT FOR A PLURAL TONE RECEIVER**

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[52] **U.S. Cl.** ..... **340/167 R,** 340/171 R, 340/164 R

[51] **Int. Cl.** **H04g 5/00**

[58] **Field of Search** ..... 340/167 R, 171 R

[56] **References Cited**

UNITED STATES PATENTS

3,465,294 9/1969 Carsello ..... 340/167 RV

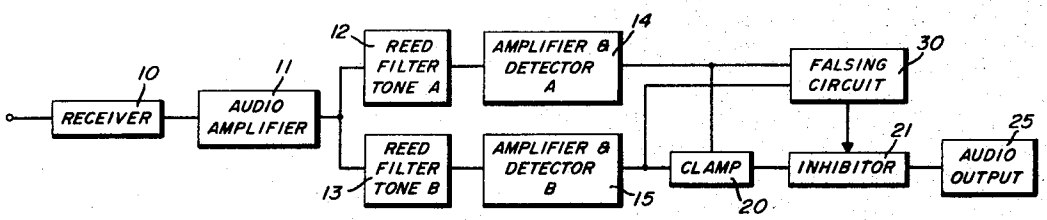
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[57] **ABSTRACT**

In a sequential plural tone receiver, the first tone is detected and differentiated to produce a pulse which begins when the tone is received and continues for a predetermined duration. The differentiated pulse and the detected second tone are applied to an AND gate which, if both signals are simultaneously applied, provides an output that inhibits the operation of the receiver and is applied through a latch to the input of the AND gate to maintain the AND gate in operation until the second tone stops. If the second tone appears at any time after the differentiated pulse is removed the receiver operates in a normal fashion.

8 Claims, 3 Drawing Figures



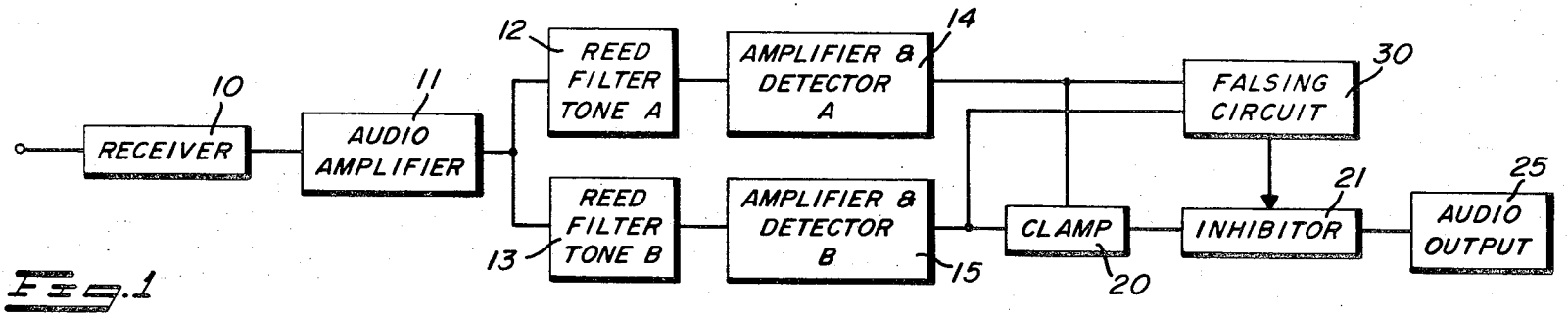


Fig. 1

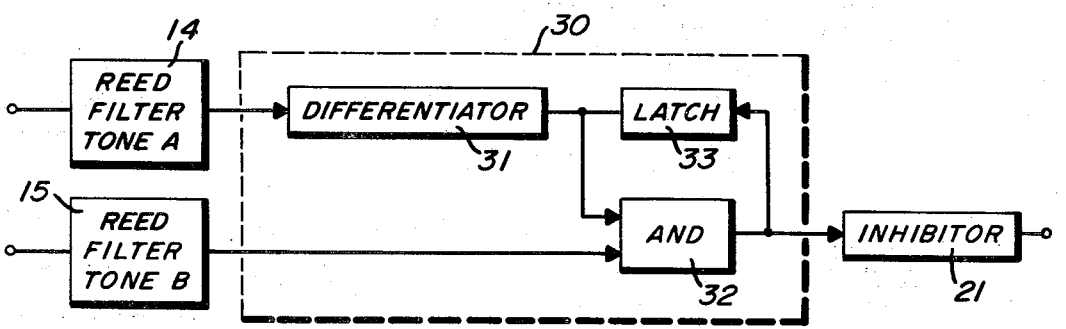


Fig. 2

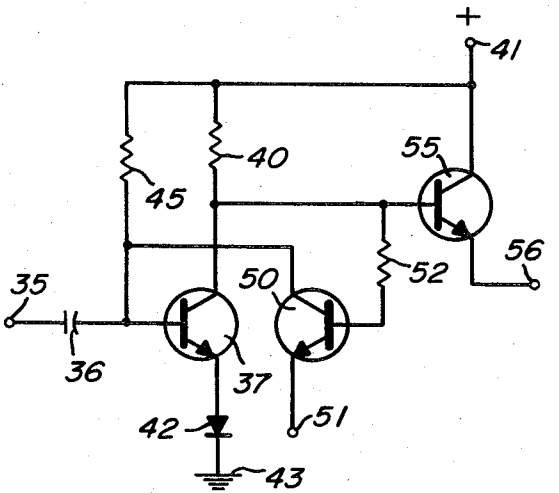


Fig. 3

SHOCK FALSING INHIBITOR CIRCUIT FOR A PLURAL TONE RECEIVER

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present device pertains to plural tone receivers wherein at least two tones are transmitted in a predetermined sequence and a specific receiver responds to these tones. It has become quite common to use frequency selective reed devices in tone decoders because such devices provide a very sharp response to select signals of one frequency from signals of closely adjacent frequencies. Miniature reed devices have been provided for small portable units, such as paging units, wherein selective alarms are provided. However, such portable units may be dropped or otherwise subjected to shock which can cause vibratory movement of the reeds to provide false alarm signals. Another problem is that the received signal may include simultaneously a large number of frequencies including the frequencies to which the tone selective devices respond to cause false operation.

2. Description of the Prior Art

In U.S. Pat. No 3,355,709, issued to G. M. Hanus on Nov. 28, 1967 and assigned to the same assignee, a sequential tone receiver is utilized wherein the first tone, if correct, blanks the second channel until after termination thereof whereupon the output of the first channel opens the second channel to allow passage of a correct second tone. Thus, as long as the second tone is present after the first tone terminates the receiver will respond.

U.S. Pat. No. 3,477,133, issued to W. J. Cole et al. on May 27, 1969 and assigned to the same assignee, describes a tone inhibitor circuit for plural tone receivers wherein a timing circuit is connected between two channels and a first tone received in the first channel enables the second channel to receive a second tone only within a particular time duration after the termination of the first tone.

U.S. Pat. No. 3,465,294, issued to R. D. Carsello et al. on Sept. 2, 1969 and assigned to the same assignee, discloses a third type of inhibitor circuit for plural tone receivers wherein a proper tone applied to the first channel enables the second channel only a predetermined time after the first tone terminates.

In each of the above-described inhibitor circuits an exceptionally long second tone, produced by shocking, jarring, or some other external interference, may cause falsing of the receiver. In addition, the above-described inhibiting circuits may be susceptible to multiple shocks, shocks of varying severity, shocks during partly correct paging sequences, etc. While each of the above-described circuits prevents falsing under normal conditions and substantially reduces the falsing under most of the above-described conditions, some falsing may still occur and this falsing may be especially predominant in particular geographic locations (high electrical interference areas) or in particular jobs (where the person carrying the receiver is highly active).

SUMMARY OF THE INVENTION

The present invention pertains to a shock falsing inhibitor circuit for a plural tone receiver including first and second detector means adapted to receive first and second tone signals and provide square pulses equal in duration to the tone signals in response to the tone signals, differentiating means coupled to the first detector for differentiating the first square pulse and providing a pulse of predetermined duration in response thereto, AND gate means connected to receive the pulse from the differentiating means and the square pulse from the second detector for providing an inhibiting signal therefrom in response to the simultaneous application of the two pulses, and latching means connected from the output of the gate means to the input thereof for maintaining operation of the gate means for the duration of the second pulse whenever the second pulse and the differentiated pulse are applied simultaneously. Thus, whenever the first tone signal is received a window is provided from the leading edge thereof for a predetermined duration, during which time the reception of the second tone signal will produce an inhibit signal for the duration of the second tone signal.

It is an object of the present invention to provide a new shock falsing inhibitor circuit for a plural tone receiver which provides a window, in response to a first tone signal, from the leading edge of the first tone signal for a predetermined duration and which, upon the reception of a second tone signal during the predetermined duration, provides an inhibit signal to prevent the operation of the receiver.

It is a further object of the present invention to provide a shock falsing inhibitor circuit for a plural tone receiver which has fewer components and positive protection from simultaneous tones.

these and other objects of this invention will become apparent to those skilled in the art upon consideration of the accompanying specification, claims and drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Referring to the drawings, wherein like characters indicate like parts throughout the figures:

FIG. 1 is a block diagram of a plural tone receiver incorporating the present shock falsing inhibitor circuit;

FIG. 2 is a block diagram of the present shock falsing inhibitor circuit; and

FIG. 3 is a schematic diagram of the shock falsing inhibitor circuit illustrated in block form in FIG. 2.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring to FIG. 1 there is shown a block diagram of a plural tone receiver incorporating an embodiment of a shock falsing inhibitor circuit. A carrier modulated by tone signals is received by receiver **10** and detected to develop audio signals. The tones are amplified in audio amplifier **11** and coupled to two reed filters **12** and **13.** Reed filters **12** and **13** are activated by tones of the proper frequency and develop output signals which are applied to amplifier and detector circuits **14** and **15,** respectively. The outputs from the amplifier and detector circuits **14** and **15** are negative going square pulses having a duration approximately equal to the duration of the output signals from the reed filters **12** and **13.** While the present shock falsing inhibitor circuit is designed to operate on a variety of combinations of timing between tones A and B (first and second tones), the signal transmitted in the present embodiment constitutes a tone A signal having approximately a one second duration followed immediately by a tone

B signal having approximately a three second duration.

A clamping circuit **20**, which operates as a normally closed gate, is connected to the output of the amplifier and detector circuit **14** for operation in response to and output signal therefrom. The clamping circuit **20** is also connected to the output of the amplifier and detector circuit **15** for passing an output signal therefrom, during operation of the clamping circuit **20**, to an inhibiting circuit **21** and, from the inhibiting circuit **21**, to an audio output circuit **25**. Upon receipt of the correct tone A the amplifier and detector circuit **14** provides a signal which opens the clamping circuit **20**. If a correct tone B follows the tone A the amplifier and detector circuit **15** provides an output signal which passes through the clamping circuit **20** and the inhibiting circuit **21** (as will be described presently) to the audio output circuit **25**. While a relatively simple plural tone receiver is illustrated in block form, which receiver is only for providing a paging signal, it should be understood that this receiver is illustrated and disclosed only for exemplary purposes and a great variety of different types of receivers might be utilized with the present shock falsing inhibitor circuit.

The outputs of the amplifier and detector circuits **14** and **15** are also applied to a falsing circuit **30**, the output of which is applied to the inhibitor circuit **21**. The inhibitor circuit **21** is constructed to normally pass the output from the clamping circuit **20** to the audio output **25** unless the falsing circuit **30** provides an output. Neither the clamping circuit **20** nor the inhibiting circuit **21** are illustrated in detail herein since any of a variety of circuits can be utilized by those skilled in the art.

Referring to FIG. **2**, the falsing circuit **30** is illustrated in block form. The output of the amplifier and detector circuit **14** is applied to a differentiator **31**, the output of which is applied to one input of an AND gate **32**. The output of the amplifier and detector circuit **15** is applied to a second input of the AND gate and the output of the AND gate **32** is applied to the inhibitor circuit **21**. The output of the AND gate **32** is also applied to a latching circuit **33**, the output of which is applied to the first input of the AND gate **32**. The operation of the catching circuit **33** is such that whenever the AND circuit **32** provides an output the latching circuit **33** operates to maintain a signal at the first input of the AND gate **32** so that the AND gate **32** continues to provide an output signal to the inhibitor **21** as long as the amplifier and detector circuit **15** provides an output.

Referring to FIG. **3**, a schematic diagram of the falsing circuit **30** is illustrated. Output signals from the amplifier and detector circuit **14** are applied to a terminal **35** which is connected through a relatively large capacitor **36** to the control or base electrode of an NPN type transistor **37**. The first or collector electrode of the transistor **37** is connected through a resistor **40** to a terminal **41** adapted to have a suitable source of positive voltage applied thereto. The second or emitter electrode of the transistor **37** is connected to the anode of a diode **42**, the cathode of which is connected to the negative terminal of the voltage source or ground **43**. The base of the transistor **37** is connected through a resistor **45** to the terminal **41** and is also connected to the first or collector electrode of a second NPN type transistor **50**. The second or emitter electrode of the transistor **50** is connected to a terminal **51** which is connected to receive output signals from the amplifier and detector circuit **15**. The base or control electrode of the transistor **50** is connected through a resistor **52** to the collector of the transistor **37** and to the base or control electrode of a third NPN type transistor **55**. The first or collector electrode of the transistor **55** is connected to the positive terminal **41** and the second or emitter electrode is connected to the inhibiting circuit **21** by way of an output terminal **56**.

In the operation of the falsing circuit **30**, when a negative going square pulse, provided by the reception of a correct tone A, is applied to the terminal **35**, the capacitor **36** and resistor **45** operate to differentiate the circuit to produce a negative going pulse at the base of the transistor **37**. The duration of the negative going pulse is determined by the size of the capacitor **36** and resistor **45** and should be of sufficient duration to insure that tone A and tone B are not produced by a common mechanical or electrical shock on reed filters **12** and **13**. The resistor **45** also serves to bias the transistor **37** normally into conduction and, it should be noted, that the positive portion of the differentiated square wave has substantially no effect on the circuit and may be ignored. With no signal applied to the terminal **35** and the transistor **37** conducting in or near saturation, the transistors **50** and **55** are both non-conductive.

When the negative going square pulse from the amplifier and detector **14** is applied to the terminal **35**, the negative going leading edge thereof coincides with the negative going leading edge of the pulse applied to the base of the transistor **37**. When the base of the transistor **37** drops sharply in a negative direction, conduction in the transistor **37** is sharply reduced and the potential on the collector moves sharply in a positive direction. This positive going potential is applied to the base of the transistor **55** and, through the resistor **52**, to the base of the transistor **50**. However, the circuit is designed so that the positive going potential on the collector of the transistor **37** due to tone A being received is insufficient to produce conduction in transistor **50**.

If, while the negative pulse is present on the base of the transistor **37**, a negative going square pulse from the amplifier and detector circuit **15** is applied to the terminal **51**, the potential of the emitter of transistor **50** drops to near ground potential so that the transistor **50** is biased into conduction. With transistor **50** conducting, the potential on the base of the transistor **37**, which was held at appproximately **2** diode drops by the diode **42** and base to emitter junction of the transistor **37** is clamped near ground potential thereby keeping transistor **37** in the cutoff state. With transistor **50** at or near saturation and transistor **37** at or near cutoff the potential on the base of the transistor **55** is sufficient to produce conduction therein and provide an output at the terminal **56** to operate the inhibiting circuit **21** and prevent an audio output from the circuit **25**.

It should be noted that once the negative square pulse is applied to the terminal **51** when the negative pulse from the differentiator is present on the base of the transistor **37**, the transistors **50** and **37** form a closed loop which maintains the transistor **55** in conduction until the negative square pulse is removed from the terminal **51**, regardless of the signal at the terminal **35**. Once the negative pulse or window produced by the differentiator is removed from the base of the transistor **37** the negative square pulse from the amplifier and detector **15** can be applied to the terminal **51** with substantially no effect. Thus, either of the negative square

pulses from the amplifier and detector circuits **14** and **15** can be applied to the terminals **35** and **51,** respectively, individually without causing conduction of the transistor **55** and the consequent output of a signal. However, whenever the negative pulse or window, which extends from the leading edge of tone A a predetermined duration, is present on the base of the transistor **37** the application of a negative going signal to the terminal **51** triggers the AND gate and the latch to prevent the output of an audio signal from the circuit **25** for the duration of the negative signal applied to the terminal **51.** In the present circuit utilized with the length of tones A and B previously described, the size of the capacitor **36** is approximately 1 microfarad and the size of the resistor **45** is approximately 1 megohm. The size of the resistors **40** and **52** are approximately 47 K-ohms and 270 K-ohms, respectively. For components of this size the window or duration of negative pulse supplied by the differentiator **31** is approximately 200 milliseconds.

Thus, a shock falsing inhibitor circuit is described which has substantially fewer components than any of the prior art circuits and which positively inhibits operation of the receiver upon reception of simultaneous tones. Further, while the falsing circuit inhibits operation of the receiver whenever simultaneous or near simultaneous pulses are produced in reed filters **12** and **13,** by electrical or mechanical shocks or the like, the circuit is designed to operate for a variety of combinations of tones, i.e., slightly overlapping, sequential, slightly separated, etc.

While we have shown and described a specific embodiment of this invention, further modifications and improvements will occur to those skilled in the art. We desire it to be understood, therefore, that this invention is not limited to the particular form shown and we intend in the appended claims to cover all modifications which do not depart from the spirit and scope of this invention.

We claim:

1. A shock falsing inhibitor circuit for a plural tone receiver comprising:

a. first detector means adapted to receive a first tone signal and providing a first square pulse approximately equal in duration to the first tone signal in response to the first tone signal;

b. second detector means adapted to receive a second tone signal and providing a second square pulse approximately equal in duration to the second tone signal in response to the second tone signal;

c. differentiating means coupled to said first detector means for providing a pulse having a predetermined duration in response to the first square pulse;

d. gate means coupled to said means means and said second detector mens and providing an output signal in response to the simultaneous application of the pulse from the differentiating means and the second square pulse; and

e. means coupled to said gate means and responsive to the output signal therefrom to inhibit the operation of the pural tone receiver.

2. A shock falsing inhibitor circuit as claimed in claim **1** including in addition latch means coupled to the gate means for applying an input signal to said gate means in response to an output signal from said gate means for the duration of the second square pulse.

3. A shock falsing inhibitor circuit as claimed in claim **2** wherein the gate means includes an AND gate.

4. A shock falsing inhibitor circuit for a plural tone receiver comprising:

a. first, second and third transistors each having first, second and control electrodes;

b. means coupling the first and second terminals of said first transistor between first and second junction points adapted to have opposite terminals of a power supply connected thereto;

c. a resistor-capacitor network connected to the control electrode of said first transistor for biasing said first transistor normally into conduction and adapted to receive a square pulse generated by a first tone and supply a pulse of predetermined duration to the control electrode of said first transistor to reduce the conduction for said predetermined duration in response to the square pulse;

d. the first terminal of said second transistor being coupled to the control electrode of said first transistor and the second terminal of said second tansistor adapted to receive a second square pulse generated by a second tone;

e. means coupling the control electrode of said second transistor to the first electrode of said first transistor and to the control electrode of said third transistor; and

f. the first electrode of said third transistor being coupled to the first junction point and the second electrode of said third transistor being adapted to supply an inhibit signal in response to the second square pulse applied to the second terminal of said second transistor during the application of the pulse of predetermined duration to the control electrode of said first transistor.

5. A shock falsing inhibitor circuit as set forth in claim **4** wherein the means coupling the first and second terminals of said first transistor between first and second junction points include a resistor coupled between the first terminal and the first junction point and a semiconductor diode coupled between the second terminal and the second junction point.

6. A shock falsing inhibitor circuit as set forth in claim **4** wherein the resistor-capacitor network includes a series capacitor coupled to the control electrode of said first transistor and a resistor coupled between the control electrode of said first transistor and the first junction point.

7. A shock falsing inhibitor circuit as set forth in claim **4** wherein the means coupling the control electrode of said second transistor to the first electrode of said first transistor and to the control electrode of said third transistor includes a resistor.

8. A shock falsing inhibitor circuit as set forth in claim **4** wherein the first, second and third transistors are each the NPN conduction type with the first electrodes being the collectors and the second electrodes the emitters and the first junction point is adapted to have a positive voltage supply connected thereto.

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