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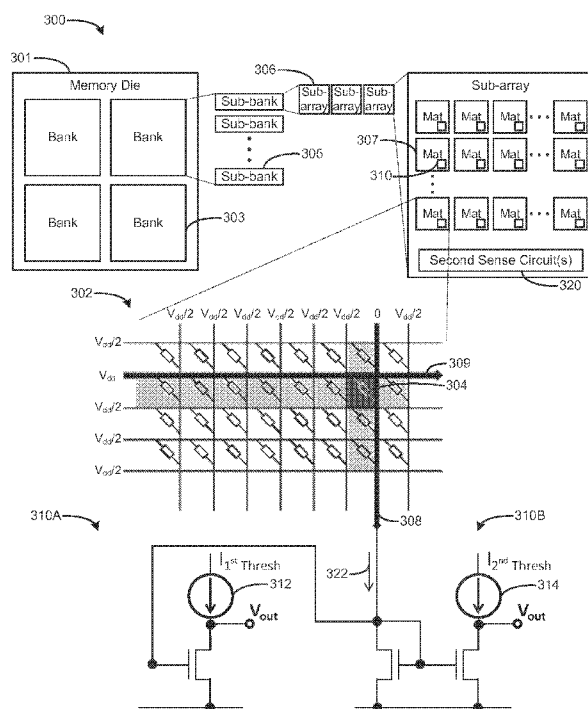
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[Continued on next page]

(54) Title: MULTI-LEVEL SENSING CIRCUITS FOR CROSSBAR MEMORY ARRAYS

**FIG. 3**

(57) Abstract: An example device in accordance with an aspect of the present disclosure includes a plurality of first sense circuits of a first type and at least one second sense circuit of a second type. The first sense circuits are to perform first-level sensing of memory elements of a crossbar memory array based on reads that are high-confidence. The second sense circuit is to perform second-level sensing.



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MULTI-LEVEL SENSING CIRCUITS FOR CROSSBAR MEMORY ARRAYS

BACKGROUND

[0001] Crossbar arrays of memory elements can include read circuits, such as sensing circuits based on sample-and-hold functionality. The read circuits can be significantly complicated, which can manifest in the form of lower memory density and higher latency for the memory array.

BRIEF DESCRIPTION OF THE DRAWINGS/FIGURES

[0002] FIG. 1 is a block diagram of a multi-level sensing circuit for a crossbar memory array including a first sense circuit and a second sense circuit according to an example.

[0003] FIG. 2 is a block diagram of a multi-level sensing circuit including a first sense circuit and a second sense circuit according to an example.

[0004] FIG. 3 is a block diagram of a multi-level sensing circuit for a crossbar memory array illustrating an example plurality of first sense circuits according to an example.

[0005] FIG. 4 is a block diagram of a second sense circuit according to an example.

[0006] FIG. 5 is a flow chart based on performing first-level and second-level sensing according to an example.

[0007] FIG. 6 is a flow chart based on identifying whether a read is high-confidence according to an example.

DETAILED DESCRIPTION

[0008] In a crossbar memory array architecture, wordlines and bitlines of the crossbar can be used to select memory elements to perform reads and obtain read currents. However, for a given read of a selected memory element, in addition to the read current, the selected bitline will also carry sneak/leakage current from half-selected and un-selected cells, which makes it difficult to reliably sense on or off current of the selected memory element. As a result, there will be a non-trivial overlap in the histogram of the on and off current of the crossbar memory array, even for reasonable half-select or sneak/leakage currents, leading to high bit error rates (BERs). The overlap and high BER can be affected by process variation in the memory elements, their associated selectors, the distributions of logic 1s and 0s across the memory array, and other such factors. Additionally, applied voltages can gradually degrade due to current-resistance (IR) drop due to wire resistance, such that an applied V_{dd} value may come across differently at the cell to which it is applied (associated with some delta that can vary). Crossbar arrays can mitigate such issues using a complex sensing mechanism. For example, the selected row can be read by first using a half-select voltage, whereby the resulting current in the bitline defines the present state of sneak/leakage currents in the bitline. Next, the complex sensing mechanism can perform the actual reading of the cell/memory element. To determine the state of the memory element, the complex sensing mechanism can then sense the difference between the read current and the background/leakage/sneak current. Although this process is relatively more robust than simple sensing, it incurs a need for relatively more energy and increased access latency.

[0009] To address such issues, examples described herein include a multi-level sensing circuit for a crossbar memory array. Examples can achieve hierarchical two-level sensing of reads, based on a plurality of first sense circuits of a first type, and at least one second sense circuit of a second type. The plurality of first sense circuits can perform first-level sensing of memory elements of the crossbar memory array, based on reads that are high-confidence. The at least one second sense circuit can perform second-level sensing of memory elements

of the crossbar memory array, based on reads that are not high-confidence (although, the second sense circuit is capable of also performing high-confidence reads). In this manner, examples described herein may reduce the access latency and the access energy of crossbar arrays, achieving relatively faster sensing based on the plurality of first sense circuits that operate faster than the second sense circuit(s). These different types of sensing circuits (e.g., sense-amps) can be used within the same bank of resistive memory technology, enabling multi-level sensing to improve speed and efficiency of reads.

[0010] FIG. 1 is a block diagram of a multi-level sensing circuit 100 for a crossbar memory array 102 including a first sense circuit 110 and a second sense circuit 120 according to an example. The plurality of first sense circuits 110 perform first-level sensing of reads that are high-confidence, and the at least one second sense circuit 120 is to perform second-level sensing of reads that are not high-confidence. The second sense circuit 120 can accommodate a higher noise margin and lower bit error rate (BER) compared to the first sense circuits 110.

[0011] The memory element 104 can be based on memristor memory technology, used in a crossbar memory array 102. The memory element 104 may include other types of memory elements, such as resistive random access memory (RRAM), phase change random-access memory (PCRAM), magnetoresistive random-access memory (MRAM), or other storage cells that are readable with a controllable voltage and/or current. A memory element 104 of a memristor cell can be associated with a selector (not shown) to provide non-linearity to the cell.

[0012] The crossbar memory array 102 may include a plurality of memory elements 104, arranged in rows and columns. However, when applying a voltage between the select row (wordline) and the select column (bitline) for a memory element 104, some of the applied voltage also may appear across other cells in the crossbar memory array 102, which may lead to sneak/leakage current.

[0013] The plurality of first sense circuits 110 can provide one level of sensing very quickly, but if the sensing is not resolvable with a desired level of definiteness and/or within a desired timeframe, the second sense circuit(s) 120 can provide a second level of sensing at a slower speed. As for which reads can be resolved

by the first level of sensing, a non-trivial fraction of reads can be read with high confidence using basic sense-amps that require very low silicon real-estate, i.e., the first sense circuits 110. Thus, the multi-level sensing circuit 100 can provide multi-level sensing for crossbar memory arrays 102 by leveraging basic sense-amps (first sense circuits 110) that are fast and area-efficient to complete high confidence sensing, and fall back on more complex, slower second sense circuit(s) 120 for low-margin, lower-confidence reads. Regarding whether a read is high confidence or not, the sense circuits can identify the magnitude of a sensed current and check it against one or more thresholds, as described in further detail below with respect to FIG. 2.

[0014] The speed/latency benefits provided by the first sense circuits, in contrast to the slower second sense circuit(s), arise not only from the basic structure of the first sense circuits, but also from their closer proximity (e.g., electrical coupling path length/fan-out) to the crossbar memory array 102 compared to the second sense circuit(s) 120. For example, an electrical bus delay can be a contributor to the overall sensing delay/latency, e.g., due to sharing the second sense circuit(s) 120 among multiple mats/tiles of memory elements 104. A mat/tile can have signal fanout paths, thereby adding layers of loads and signal travel across the plurality of mats, resulting in non-trivial additional latency (e.g., wire delay can exhibit quadratic increases in length and sharing delays).

[0015] In contrast to the use of few or a single one of the relatively more complex second sense circuit(s) 120, the example multi-level sensing circuits 100 can use many of the first sense circuits 110 to provide high bandwidth and low latency. For example, the multi-level sensing circuit 100 can attempt to perform sensing using the first sense circuits 110, and fall back to using the more complex second sense circuit 120 if the sensing by the first sense circuits 110 is unresolved (e.g., after a given timeframe). In alternate examples, the multi-level hierarchy provided by the first and second sense circuits 110, 120 can be altered, by bypassing (e.g., temporarily ignoring or disabling) the first sense circuits 110. The first sense circuits 110 also can provide an overall power reduction (compared to relying on second sense circuit(s) 120 for all reads), because the

first sense circuits 110 are more basic in structure, resulting in net power savings compared to the relatively more complex and time-consuming operation of the second sense circuit(s) 120.

[0016] FIG. 2 is a block diagram of a multi-level sensing circuit 200 including a first sense circuit 210 and a second sense circuit 220 according to an example. The first and second sense circuits 210, 220 are coupled to the crossbar memory array 202, which can be formed as a collection of multiple memory elements 204 arranged in mats (see FIG. 3 for more details). The first and second sense circuits 210, 220 are to sense the read current 222 based on a hierarchical approach, indicated by the dashed line whereby the first sense circuit 210 has priority to sense high confidence reads based on at least one of the first threshold 212 and the second threshold 214, and/or within a timeframe 216. For example, a given first sensing circuit can identify whether a given read is high-confidence based on identifying the read current 222 as being less than the first threshold 212 associated with a low resistance state (LRS) of the memory element 204, or identifying the read current 222 as being greater than a second threshold 214 associated with a high resistance state (HRS) of the memory element 204.

[0017] The high speed/low latency basic structure of the small-sized first sense circuits 210 (e.g., sense amps) may encounter a read current 222 that is not in satisfaction of the first or second thresholds 212, 214, and/or whether the read current 222 can be identified within the timeframe 216. For example, the first sense circuits 210 can identify with high confidence that they themselves cannot reliably sense the signal if the current range is between a first threshold and a second threshold. In an alternate example, the first sense circuits 210 can identify whether a sensed current is high-confidence or not based on one threshold (high or low), e.g., without a need for the use to both thresholds 212, 214 (although both thresholds 212, 214 are shown in FIG. 2 for clarity, both are not needed in alternate examples). Thus, various approaches are possible in identifying whether a current is not high-confidence. In such situations, the second sense circuit 220 can be used to sense the read current 222 using more complex/slower circuitry. Thus, the second sense circuit 220 can identify whether a given read current 222 is not high-confidence based on passage of the

timeframe 216 without the first sense circuit 210 identifying the read current 222. The second sense circuit 220 thus can perform second-level sensing of memory elements 204 of the crossbar memory array 202 based on reads not satisfying the first threshold 212 or the second threshold 214. For example, the second sense circuit 220 can perform the medium- and low-confidence reads by sensing a difference between sensed currents 222 and background currents 224, thereby subtracting the background currents 224 (e.g., "sneak" currents) for the selected bitline, from the sensed currents 222, to obtain the current through the selected memory element 204 of the selected wordline and bitline.

[0018] FIG. 3 is a block diagram of a multi-level sensing circuit 300 for a crossbar memory array 302 illustrating an example plurality of first sense circuits 310, 310A, 310B according to an example. A memory die 301 includes a plurality of banks 303. A bank 303 includes a plurality of sub-banks 305. A sub-bank 305 includes a plurality of sub-arrays 306. A sub-array includes a plurality of mats/tiles 307, first sense circuits 310, and one or more second sense circuit(s) 320. The mat/tile 307 is shown expanded to illustrate a portion as the crossbar memory array 302 of memory elements 304, showing one or more bit line(s) coupled to a pair of first sense circuits 310A, 310B to read the sensed current 322 and compare against first and second thresholds 312, 314. Two first sense circuits 310A, 310B and associated thresholds 312, 314 are shown. However, in alternate examples, one first sense circuit (or more than two) and its associated threshold may be used (as explained above regarding FIG. 2), e.g., to identify whether or not a sensed current 322 is high-confidence based on a comparison to a single, or more, threshold(s).

[0019] The mats 307 can represent an array of various dimensions, such as an array of 64x64 memory elements 304. The crossbar memory array 302 of the mats 307 can be other dimensions, such as 32x32, 128x128, 256x256, etc., and can include asymmetric array dimensions such as 128x64, 64x32, or 128x32, and so on. For asymmetric (rectangular) arrays, the biasing of the wordlines and bitlines, as well as other pertinent characteristics, can be varied accordingly, to accommodate the differing length and width dimensions. The sub-array 306 is shown with a plurality of mats, where a first sense circuit 310 is associated with a

corresponding one of the plurality of mats. However, in alternate examples, a first sense circuit 310 may be shared among a larger number of mats 307 (e.g., sharing one first sense circuit 310 among four mats 307). Alternatively, a larger number of first sense circuits 310 may be used at a given mat 307 (e.g., using a first sense circuit 310 per bitline 308 of the mat 307). Similarly, a single second sense circuit 320 is illustrated in the sub-array 306 of FIG. 3. In alternate examples, a greater or fewer number of second sense circuits 320 may be assigned to or shared among a given number of mats 307/crossbar memory arrays 302.

[0020] The crossbar memory array 302 arranges a plurality of cells/memory elements 304 (which can be associated with selectors, not shown) to improve density and reduce cost. For efficiency, it is preferable that the sub-threshold leakage current of a selector for a given cell (i.e., the current through the selector for any voltage drop across a cell less than V_{th} , where V_{th} is the threshold voltage of a selector) is close to zero. However, a small amount of sneak or leakage current will flow through cells, even if they are not selected and the potential across them is less than V_{th} .

[0021] In resistive memory elements 304 such as memristors, the value stored in a cell is read by applying a small voltage across the selected cell, and detecting the resulting current flowing through its bitline. When selecting a wordline 309 and a bitline 308 of the crossbar memory array 302 to perform a read or write operation, it would be preferred that the entire current flowed through the cell at the intersection of the selected wordline 309 and bitline 308. However, other cells/memory elements 304 in the selected wordline 309 and bitline 308 will be half selected as shown in FIG. 3, and will leak current with the sensed currents 322. As shown, the crossbar memory array 302 biases unselected rows and columns with the value $V_{dd}/2$, but the selected wordline 309 receives a voltage of V_{dd} , and the selected bitline receives a voltage of zero. Accordingly, unselected cells that share a row or column with the selected cell will contribute half-selected leakage current (e.g., the difference between the $V_{dd}/2$ applied as bias, and the other values applied to the selected wordline 309 and bitline 308). Accordingly, to identify whether a read is high-confidence despite such

leakage/sneak current, the first sense circuits 310, 310A, 310B can use the first threshold 312 and/or the second threshold 314 to check whether a sum of the current is below the first threshold 312 or above the second threshold 314. The sum of the current can arise from the selected memory element 304 and the half-selected leakage/sneak currents for a given high-confidence read.

[0022] More specifically, cells sharing the selected wordline 309 and selected bitline 308 with the selected memory element 304 are half selected, such that the potential across them is $V_{dd}/2$, based on the use of the illustrated biasing scheme where unselected rows/columns are half-selected ($V_{dd}/2$). Those half-selected cells conduct current because of the voltage drop across them, where those unselected cells in row 309 see $V_{dd} - (V_{dd}/2) = V_{dd}/2$, and those unselected cells in column 308 see $(V_{dd}/2) - 0 = V_{dd}/2$. Such low-power read/sensing operations result in potential ambiguity in the selected bitline 308. The examples described herein are particularly suited for identifying high-confidence reads in these types of low-power biasing schemes, where unselected rows/columns are partially biased such that fully unselected cells experience roughly zero voltage (the difference of $V_{dd}/2 - V_{dd}/2$). The example biasing scheme uses $V_{dd}/2$ for biasing unselected wordlines and bitlines, but other biasing values may be used (such as $V_{dd}/3$ etc.), for example, on arrays having non-square width x height dimensions.

[0023] The potential ambiguity when interpreting the value read at a selected bitline 308 can arise because of the lack of certainty as to what proportion of the sensed current 322 is due to background/leakage current, and what proportion is due to the contribution of the memory element 304 (either in its LRS or HRS). The first sense circuits 310, 310A, 310B can resolve the ambiguity for high-confidence reads based on the first and second thresholds 312, 314, and the second sense circuit 320 can resolve all reads using a two-step operation to 1) read a background current for a given bitline, 2) read the total cell current for the selected bitline, then 3) subtract the background current from the total cell current to provide the current corresponding to the state of the selected memory element 304.

[0024] Illustrated examples include two thresholds, consistent with identifying high confidence logic 0 and logic 1 states (e.g., corresponding to a memory element 304 having two set states). In alternate examples, the first sense circuits can use multiple thresholds, to identify a plurality of logic states (e.g., corresponding to a memory element 304 having multiple set states).

[0025] In one example, for a given read voltage and/or biasing scheme, a memristor cell memory element 304 can be targeted to conduct approximately 4 microamps (uA) in its off state (logic "0"), and approximately 20 uA in its on state (logic "1"), resulting in a difference of a factor of five between the on-state current and the off-state current. While a 5x on/off ratio offers an excellent read margin, ambiguity can still arise when such memory element cells are connected in a crossbar fashion. For example, a selected bitline can carry a sneak current of approximately 65-95 uA, in addition to the current of the selected cell (for an example 128x128 array; different amounts of selected bitline sneak currents would correspond to different dimensions of arrays). The variation in the sneak current corresponds at least in part due to the distribution of logic 1s and 0s across the array for a given time. The lowest leakage/sneak current can arise when every cell of the selected bitline is in the HRS, and the highest can arise when every cell is in the LRS. However, given a random distribution of logic 1s and 0s across the crossbar memory array, the odds of having all cells in the same state is low. Thus, an acceptable probability arises for ranges of logic distribution for a given data set, and a corresponding range of sneak current within which the sneak current will be for a given state of the memory array with a very high likelihood and probability. Accordingly, a first sense circuit 310 can sense a bitline of the crossbar memory array and determine whether the selected memory cell 304 is within an upper range and a lower range of leakage current for that bitline. The first threshold can correspond to a read current of the lower range of sneak currents, plus a value less than an "on" state for a given memory element. Accordingly, if the sneak current happens to be on the low end of probability, and the memory element expresses a low value, the first sense circuit can safely identify that the system is in a high-confidence range for concluding that the memory element is off. Similarly, the first sense circuit 310 can use the second

threshold, corresponding to a read current of the upper range plus a value greater than an "off" state for a given memory element, to conclude that the memory element is on, based on such high-confidence sensing.

[0026] In another example, during a read operation, the sensed current 322 may be 94 μ A (using the typical memory cell values and memory array sizes set forth above). This value is somewhat ambiguous (i.e., not satisfying either the first or second high-confidence thresholds) because it possibly could satisfy two interpretations absent further sensing: a selected cell 304 in an off-state conducting 4 μ A + a background current of 90 μ A; or a cell in an on-state conducting 20 μ A + a background current of 74 μ A. Because of this ambiguity, the first sense circuit 310 could recognize that the sensed current 322 is outside of the range for the thresholds 312, 314, and the two-step sensing of the second sense circuit 320 with its high noise margin and low bit error rate can be used to bypass the first sense circuit 310 and resolve the ambiguity at the second sense circuit 320.

[0027] More specifically, for an example crossbar memory array 302 having a random distribution of logic 1s and 0s, a non-trivial number of reads to low resistance state can have a current less than or equal to approximately 75 μ A, which could be used as a first threshold 312. The number 75 corresponds to a lower value of the range 70-90, plus a margin of five μ A (e.g., plus a value that is less than the full 20 μ A of the on state). Similarly, reads to high resistance state can have a current greater than approximately 96 μ A, which could be used as a second threshold 314. The number 96 corresponds to an upper value of the range 70-90, plus a margin of six μ A (e.g., plus a value that greater than the 4 μ A of the off state). Such values can arise based on the cell characteristics and array size described above, although other values are possible with different cell and array characteristics/sizes. For these reads that satisfy the first or second thresholds, the cell state can be predicted with high confidence, without resorting to the two-step sensing of the second sense circuit 320. Furthermore, the first sensing circuits 310, 310A, 310B are shown as basic in structure, for these high confidence reads (one to two transistors and a current source, without a need for a capacitor or other physically large component). Such basic structure does not

need much circuit area/silicon real estate. As a result, the first sense circuits 310 can be placed in large numbers in close proximity right next to the crossbar, incurring low wire delay due to avoiding a longer electrical path from the crossbar to the first sense circuit(s) 310.

[0028] Because of the multiple steps involved in the second sense circuit(s) 320 to perform reads/sensing, both the area and the latency of the second sense circuits/amps 320 for the crossbar memory array 302 are relatively high compared to the first sense circuits 310, 310A, 310B. As a result, for a given bank 303, a relatively limited number of second sense circuits 320 are shared among the mats 310, to minimize cost/size/complexity at the cost of speed. For example, a memristor sub-array 306 can use a single second sense circuit/amp 320 shared across 32 mats/crossbars 307. With each mat/crossbar 307 having 128-256 bitlines 308, this corresponds to one second sense-amp for 4096 to 8192 bitlines. Furthermore, a shared second sense-amp 320 is located relatively farther from the actual crossbar compared to the first sense-amp 310, and thus incurs relatively much higher wire delay, increasing the read latency for the second sense-amp 320. In contrast, the small size of the first sense circuits 310 enable a far greater number of them to be used, with the benefit of increased speed and throughput (e.g., employing a single first sense-amp 310 per mat 307 or even per bitline 308, far closer in proximity to the crossbar).

[0029] As illustrated in the example of FIG. 3, two first sense circuits 310A, 310B are used to provide the first and second thresholds 312, 314 for a given bitline 308. In alternate examples, a single first sense circuit 310 can include both thresholds 312, 314. A first sense circuit can operate as an enhanced latch, for example, to compare reference currents. In the illustrated example, the pair of first sense circuits 310A, 310B corresponds to the selected bitline 308 of the crossbar memory array 302, to compare a given read 322 of the bitline 308 against the first threshold 312 using one of the pair of first sense circuits 310A, 310B, and to compare against the second threshold 314 using a remaining one of the pair of first sense circuits 310A, 310B.

[0030] FIG. 4 is a block diagram of a second sense circuit 420 according to an example. The second sense circuit 420 is to receive a sensed current from

memory element 404. In addition to the latch-based structure including multiple transistors contained in the black box labeled "Sensing Circuit," the second sense circuit 420 also includes a plurality of capacitors, switches, and additional transistors. Accordingly, the second sensing circuit 420 is based on a sample-and-hold design, using a relatively more complex sensing scheme compared to the first sense circuits, to achieve sufficient read margin and low bit error rate (BER) in order to resolve potentially ambiguous sensed currents (e.g., using a two-step approach) that are not high-confidence. The multiple additional components, such as the illustrated capacitors, add area and latency, e.g., resistor-capacitor (RC) delay, to the second sense amp/circuit 420, resulting in relatively much slower performance compared to the basic and fast structure/operation of the example first sense circuits of FIGS. 3 and 4.

[0031] Referring to Figures 5 and 6, flow diagrams are illustrated in accordance with various examples of the present disclosure. The flow diagrams represent processes that may be utilized in conjunction with various systems and devices as discussed with reference to the preceding figures. While illustrated in a particular order, the disclosure is not intended to be so limited. Rather, it is expressly contemplated that various processes may occur in different orders and/or simultaneously with other processes than those illustrated.

[0032] FIG. 5 is a flow chart 500 based on performing first-level and second-level sensing according to an example. In block 510, a plurality of first sense circuits of a first type perform first-level sensing of memory elements of the crossbar memory array based on reads that are high-confidence. For example, the first sense circuit can compare whether the sensed currents/reads fall below a first threshold, or fall above a second threshold, to identify whether the selected memory element is on or off (i.e., logic "1" or "0"). In block 520, at least one second sense circuit of a second type is to perform second-level sensing of memory elements of the crossbar memory array based on reads that are not high-confidence. The at least one second sense circuit is associated with a higher noise margin and lower bit error rate than the first sense circuits. For example, the second sense circuit can apply a two-step approach, using a capacitor-based sense-and-hold design, to identify a background/leakage current for a bitline,

identify the total current for a selected bitline, and subtract the former from the latter to isolate the current of the selected memory element.

[0033] FIG. 6 is a flow chart 600 based on identifying whether a read is high-confidence according to an example. In block 610, a plurality of first sense circuits of a first type are to perform first-level sensing of memory elements of the crossbar memory array based on reads that are high-confidence. For example, the first sense circuit can perform fast determination of the reads based on a direct comparison(s), without a need to rely on a slower second sense circuit of a second type that stores and/or subtracts multiple values. In block 620, a given first sensing circuit is to identify whether a given read is high-confidence based on identifying a read current satisfying at least one of i) being less than a first threshold associated with a low resistance state, and ii) being greater than a second threshold associated with a high resistance state. For example, the first sense circuit can directly evaluate whether the sensed current corresponds to a LRS or HRS for the selected memory element according to whether the sensed current falls below the first low threshold, or exceeds the second high threshold. Such comparisons can be performed directly using basic circuit structures not associated with an RC time delay or other complexities that might slow down circuit operation.

WHAT IS CLAIMED IS:

1. A multi-level sensing circuit for a crossbar memory array, comprising:

a plurality of first sense circuits of a first type to perform first-level sensing of memory elements of the crossbar memory array based on reads that are high-confidence; and

at least one second sense circuit of a second type to perform second-level sensing of memory elements of the crossbar memory array based on reads that are not high-confidence, wherein the at least one second sense circuit is associated with a higher noise margin and lower bit error rate than the first sense circuits.

2. The circuit of claim 1, wherein a given first sensing circuit is to identify whether a given read is high-confidence based on identifying a read current satisfying at least one of i) being less than a first threshold associated with a low resistance state, and ii) being greater than a second threshold associated with a high resistance state.

3. The circuit of claim 2, wherein the given first sensing circuit is to identify whether the given read is high-confidence based on identifying the read current within a timeframe.

4. The circuit of claim 3, wherein a given second sense circuit is to identify whether a given read is not high-confidence based on passage of the timeframe without the first sensing circuit identifying the read current.

5. The circuit of claim 2, wherein the circuit is to bias unselected rows and columns such that unselected cells that share a row or column with a selected cell contribute half-selected leakage current to the reads, and wherein the first threshold is chosen such that a sum of the half-selected leakage current for a given high-confidence read is below the first threshold.

6. The circuit of claim 2, wherein the circuit includes at least one first sense circuit per bitline of the crossbar memory array, to compare a given read of the bitline against the first threshold and the second threshold.

7. The circuit of claim 2, wherein the circuit includes at least a pair of first sense circuits per bitline of the crossbar memory array, to compare a given read of the bitline against the first threshold using one of the pair of first sense circuits, and to compare against the second threshold using a remaining one of the pair of first sense circuits.

8. The circuit of claim 1, wherein the crossbar memory array includes a plurality of mats including a plurality of memory cells, and wherein a given one of the plurality of first sense circuits is associated with a corresponding one of the plurality of mats.

9. The circuit of claim 1, wherein a given first sense circuit associated with a given memory cell is disposed at the crossbar memory array at a closer proximity to the memory cell than the second sense circuit associated with that memory cell.

10. The circuit of claim 1, wherein a given first sense circuit is faster in operation and smaller in silicon real-estate than a given second sense circuit.

11. The computing system of claim 1, wherein the crossbar memory array is based on memristor memory technology.

12. A multi-level sensing circuit for a crossbar memory array, comprising:

a plurality of first sense circuits of a first type to perform first-level sensing of memory elements of the crossbar memory array based on reads satisfying at least one of i) being less than a first threshold associated with a low resistance

state, and ii) being greater than a second threshold associated with a high resistance state; and

at least one second sense circuit of a second type to perform second-level sensing of memory elements of the crossbar memory array based on reads not satisfying the first threshold or the second threshold, wherein the at least one second sense circuit is to perform the reads by sensing a difference between sensed currents and background currents.

13. The circuit of claim 12, wherein a given one of the plurality of first sense circuits is to sense a bitline of the crossbar memory array associated with an upper range and a lower range of leakage current for that bitline, wherein the first threshold corresponds to a read current of the lower range plus a value less than an on state for a given memory element, and wherein the second threshold corresponds to a read current of the upper range plus a value greater than an off state for a given memory element.

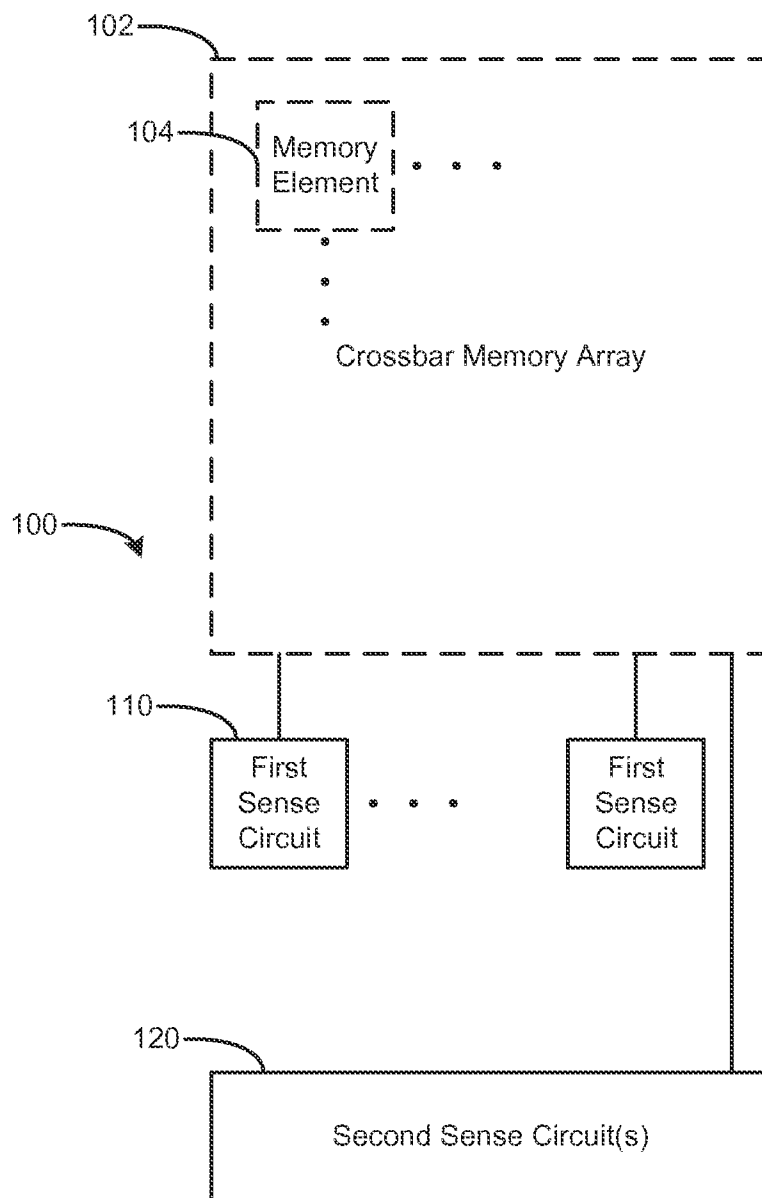
14. A method of sensing by a multi-level sensing circuit for a crossbar memory array, comprising:

performing first-level sensing, by a plurality of first sense circuits of a first type, of memory elements of the crossbar memory array based on reads that are high-confidence; and

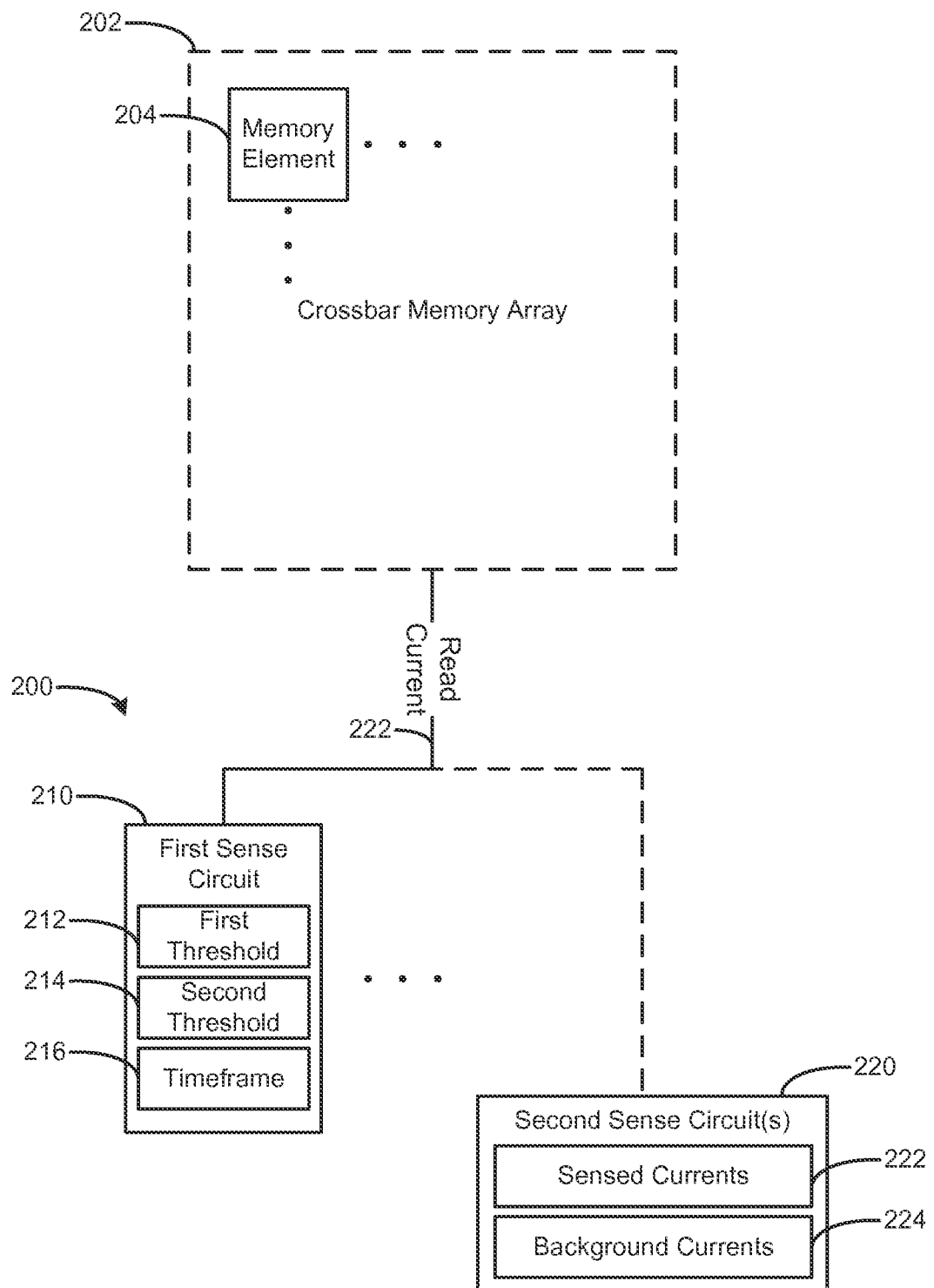
performing second-level sensing, by at least one second sense circuit of a second type, of memory elements of the crossbar memory array based on reads that are not high-confidence, wherein the at least one second sense circuit is associated with a higher noise margin and lower bit error rate than the first sense circuits.

15. The method of claim 14, further comprising identifying, by a given first sensing circuit, whether a given read is high-confidence based on identifying a read current satisfying at least one of i) being less than a first threshold associated with a low resistance state, and ii) being greater than a second threshold associated with a high resistance state.

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**FIG. 1**

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**FIG. 2**

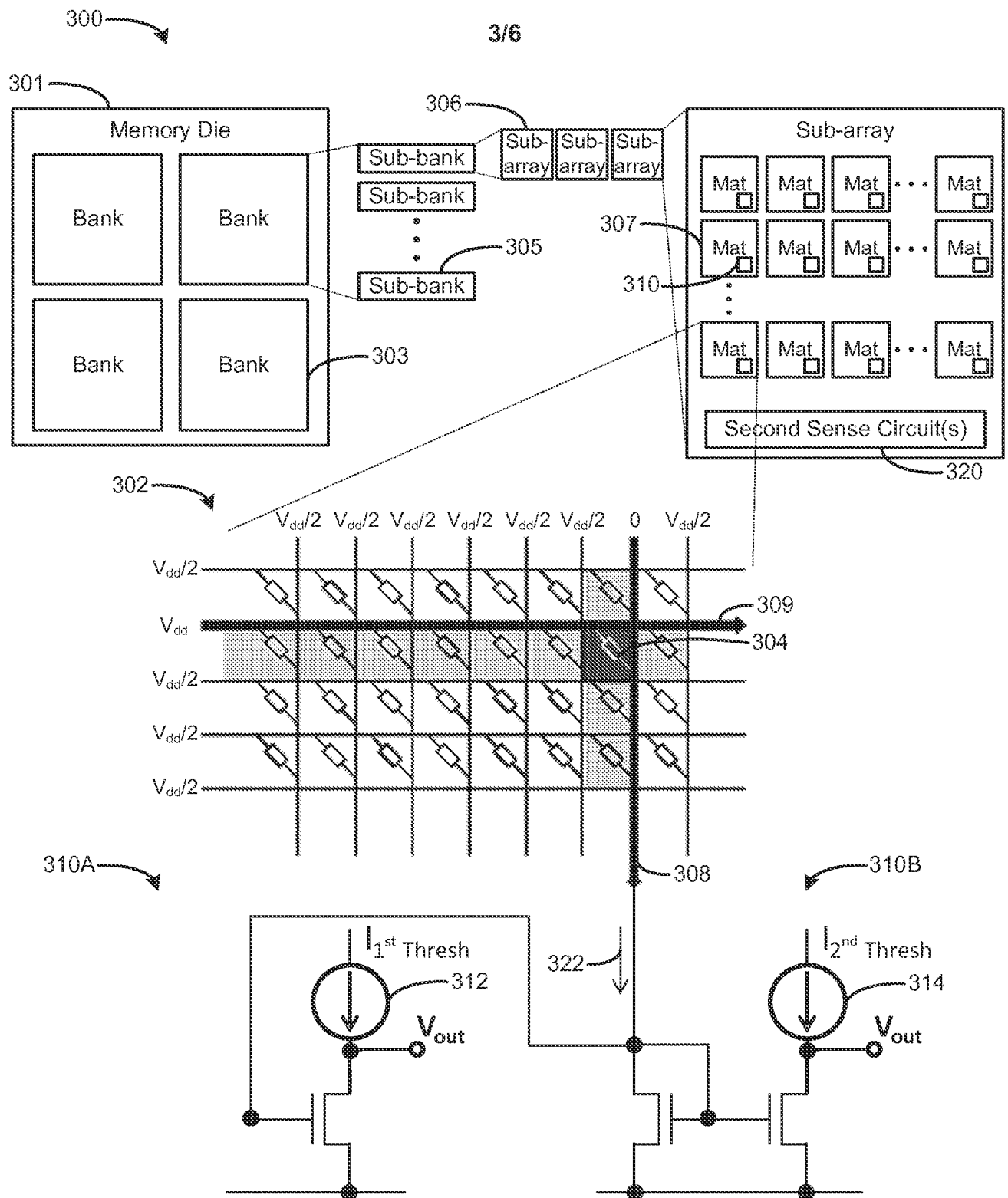


FIG. 3

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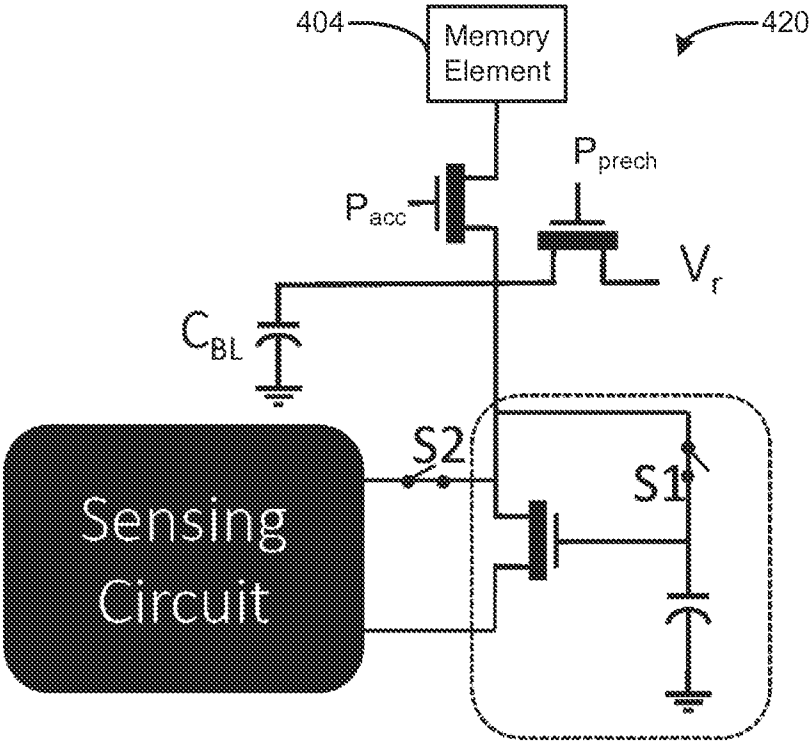
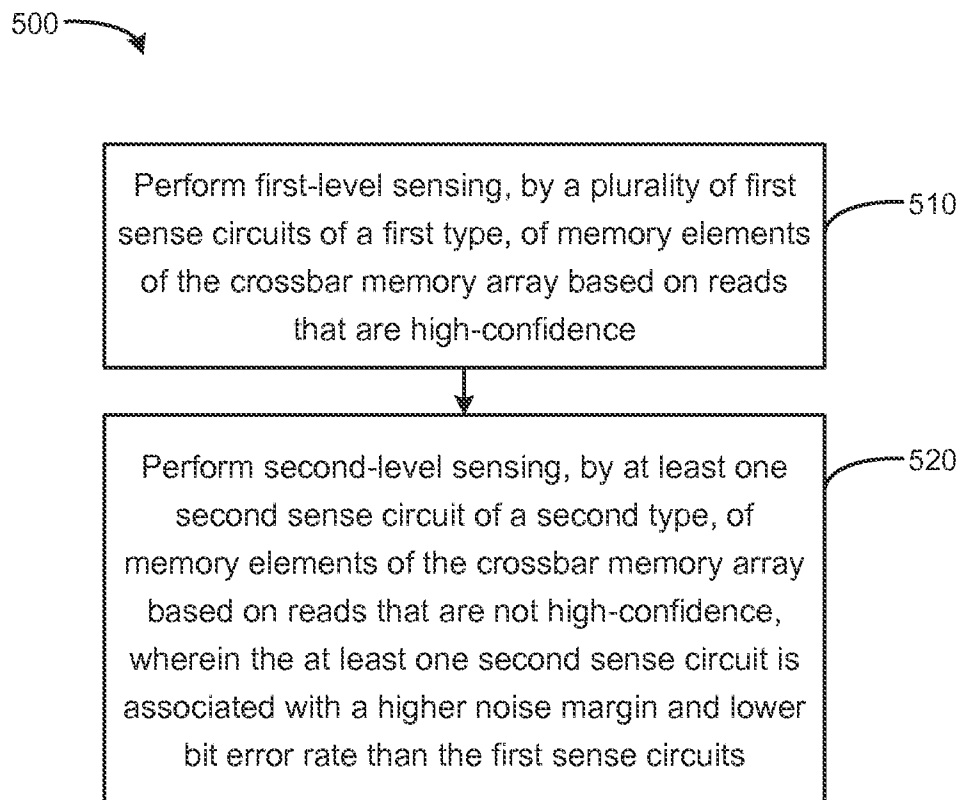
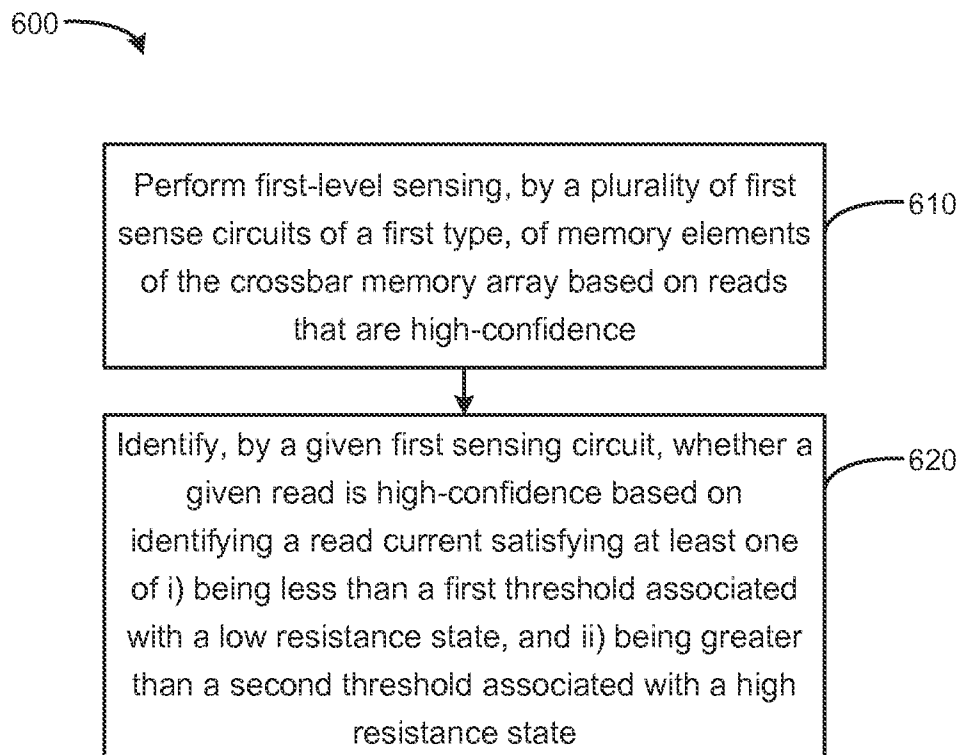


FIG. 4

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**FIG. 5**

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**FIG. 6**

A. CLASSIFICATION OF SUBJECT MATTER**G11C 13/00(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G11C 13/00; G11C 11/02; G11C 16/26; G11C 16/28; G11C 7/02; G11C 7/12

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: multi-level, sensing, circuit, crossbar, memory, array, read, error, rate, threshold, memristor

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2014-0133211 A1 (HAGOP NAZARIAN et al.) 15 May 2014 See paragraphs [0026], [0030], [0037], [0050], [0052], [0064]–[0065]; and figures 1–4, 7.	1–3, 5–11, 14–15
A		4, 12–13
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A	US 2013-0235674 A1 (CHUN-HSIUNG HUNG et al.) 12 September 2013 See paragraph [0082]; and figure 6.	1–15
A	US 2010-0290301 A1 (ROY E. SCHEUERLEIN) 18 November 2010 See paragraphs [0054]–[0055]; and figure 10.	1–15
A	US 2007-0070753 A1 (HIEU VAN TRAN) 29 March 2007 See paragraphs [0048]–[0050]; and figure 5.	1–15



Further documents are listed in the continuation of Box C.



See patent family annex.

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