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ELECTRONIC COMBINATION LOCK

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2 Sheets-Sheet 1

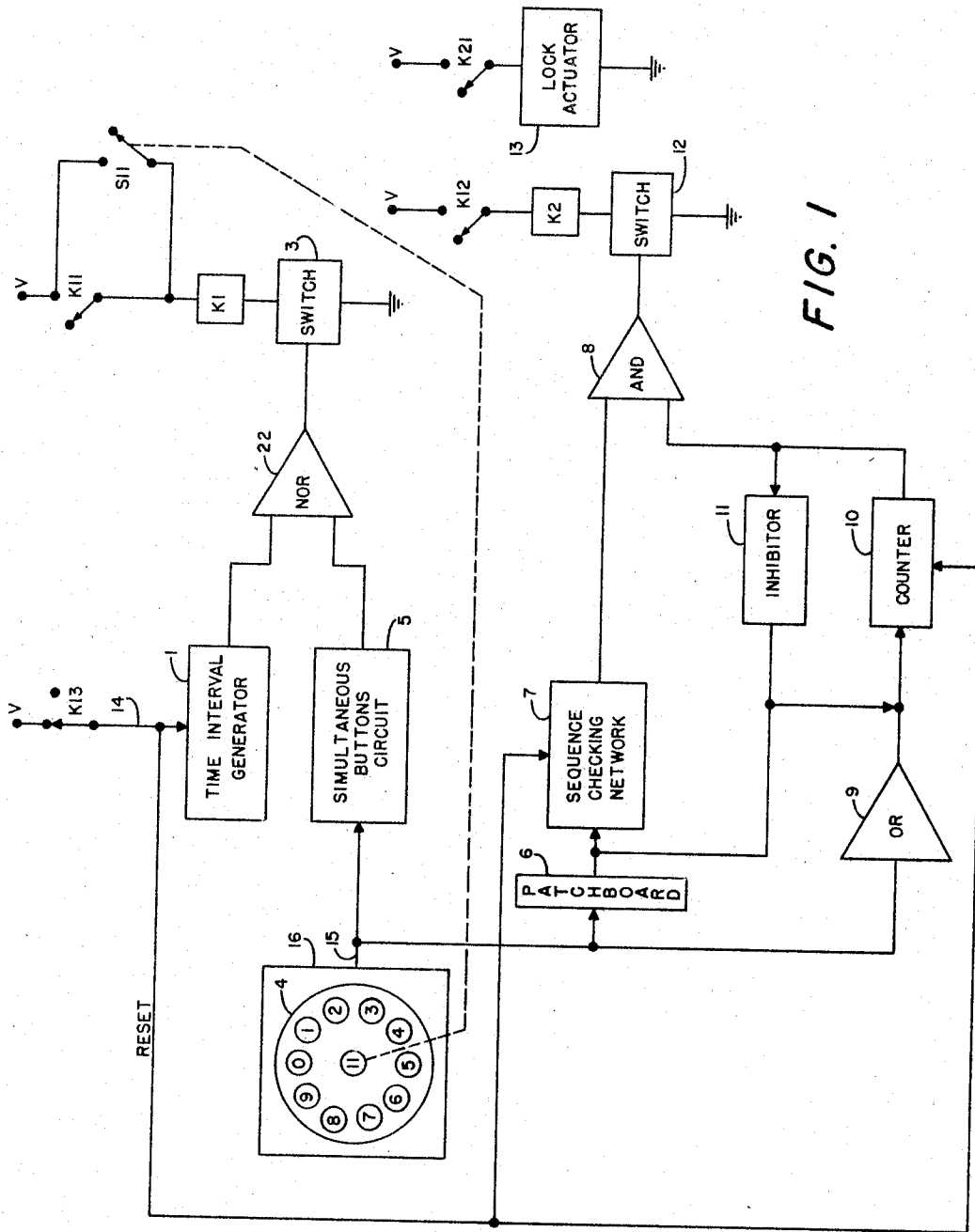


FIG. 1

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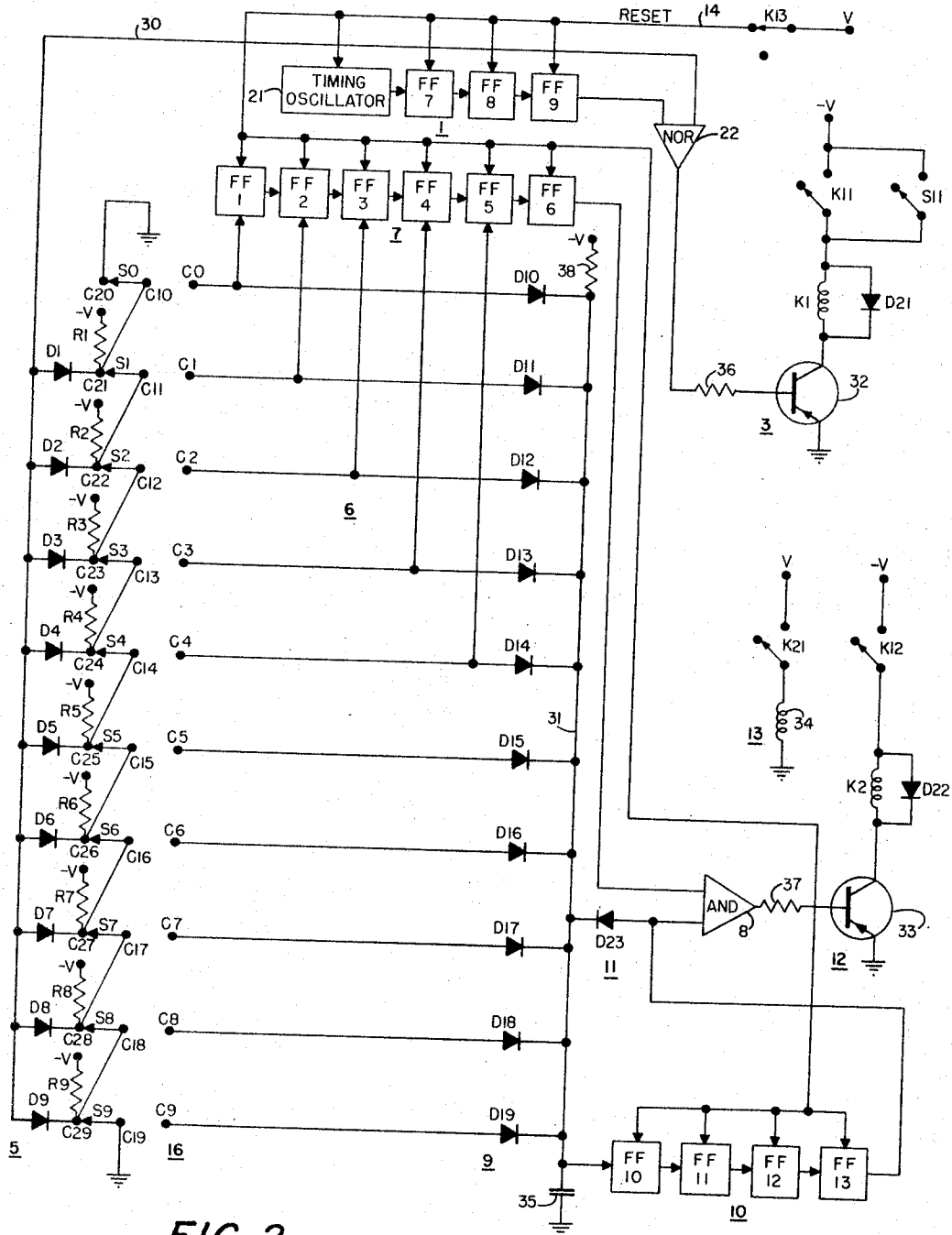


FIG. 2

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3,320,490

ELECTRONIC COMBINATION LOCK

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 Filed Sept. 15, 1964, Ser. No. 396,781
 17 Claims. (Cl. 317-134)

The invention described herein may be manufactured and used by or for the Government of the United States of America for governmental purposes without the payment of any royalties thereon or therefor.

The present invention relates to locks and more particularly to an improvement in electrically controlled combination locks.

Those concerned with the development of electronic combination locks have long recognized the need for a solid-state, single-dial, push-button combination lock which is acceptable where great security is important. Prior devices employ stepping switches, relays and other mechanical means for controlling a door latch. These devices are often cumbersome and unsatisfactory where great security is paramount. These devices also require considerable maintenance. In the prior devices the combination cannot be quickly changed and the locks can sometimes be opened by continually pressing the input buttons or turning keys simultaneously in an attempt to foil the system.

According to this invention, the foregoing and other disadvantages of prior devices are overcome by providing a solid-state, low signal-level, single dial, push-button electronic combination system for operating a lock or electromechanical lock release quickly and reliably. The combination may be altered very quickly by changing plug-in connections on a matrix patchboard. The solid-state circuitry features a start circuit, an automatic reset circuit, an elapsed-time counter for allowing the combination to be entered only during a predetermined time interval, a circuit for inhibiting or resetting the system whenever two or more push-buttons are pressed simultaneously, and a circuit for counting the total number of buttons pressed. If too many buttons are pressed, the system accepts no further button information.

An object of the present invention is to provide an improved combination lock.

Another object is to provide a single-dial, solid-state system for operating a lock or lock release.

A further object is to provide an electronic combination lock which is operated by sequentially entering digits in accordance with a preselected combination and wherein the combination can be quickly and easily changed.

Still another object is to provide an electronic combination lock actuating system which is reset when two or more buttons are pressed simultaneously.

A still further object of the present invention is to provide a solid-state electronic lock control system which is reset when a preset time interval elapses and which is inhibited when too many buttons are pressed.

A still further object of the present invention is to provide a solid-state electronic lock control system which will open the lock only when the preset combination is entered in the proper order and only the preset number of digits have been entered.

Other objects and many of the attendant advantages of this invention will be readily appreciated as the same becomes better understood by reference to the following detailed description when considered in connection with the accompanying drawings in which like reference numerals designate like parts throughout the figures thereof and wherein:

FIG. 1 is a functional block diagram of the invention; and

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FIG. 2 is a circuit diagram of an embodiment of the invention.

Referring now to the drawings, there is shown in FIG. 1 a block diagram of the electronic combination lock wherein ten push-buttons 0-9 are located about the periphery of dial 4 and a push-button 11 is located at the center of the dial. Push-buttons 0-9 and 11 will be referred to as P0-P9 and P11 throughout this specification. Line 15, shown as a single line, is representative of the ten lines from P0-P9.

The combination to the lock is entered into the system by means of push-buttons P0-P9. P11 must be pressed to start the system before the digits can be entered by P0-P9. Each of the push-buttons closes its respective contact when pressed and the contact remains closed until the push-button is released. The push-button contacts S0-S9 are illustrated in FIG. 2.

When P1 is pressed its respective contact S11 is held closed thereby by-passing relay contact K11 which is normally open. Relay K1 is normally deenergized. Switch 3 is normally ON or closed so that when S11 is closed relay K1 is energized and contact K11 of relay K1 is closed thereby maintaining relay K1 energized when P11 is released and S11 is opened.

A reset line 14 is shown connected to circuits which must be reset or turned OFF. The reset line is normally active and holds all the circuits in the reset or OFF condition since relay contact K13 of relay K1 is normally closed. However when P11 is pressed relay K1 energizes, K13 opens and the reset line is thereby inactivated allowing the circuits to accept the digit information and turning on time interval generator 1.

In the block diagram of FIG. 1, time interval generator 1 is turned ON when P11 is pressed and produces at its output a signal whose duration can be varied depending upon the desired length of time for allowing the digit information to be accepted. The output of time interval generator 1 is fed to an input of NOR gate 22. Another input of NOR gate 22 receives a signal from simultaneous buttons circuit 5, which circuit receives the digit information entered by means of the push-buttons and produces an output whenever two or more push-buttons are pressed simultaneously. NOR gate 22 will therefore produce an output to the start circuit comprising switch 3, relay coil K1, relay contact K11, and switch S11 whenever two or more buttons have been pressed simultaneously, or whenever the preselected time interval has elapsed. When either of these conditions are met, switch 3, which is normally ON, is inhibited or turned OFF thereby breaking the circuit to relay K1 and closing contact K13. When K13 closes, the entire system is reset and no further information will be received until P11 is pressed again.

The digit information from dial 4 is also received by sequence checking network 7 through matrix patchboard 6. The sequence checking network produces an output only if the correct combination is entered on the dial in the correct order. In general, the matrix patchboard 6 is an $n \times m$ matrix where n is the number of digits in the combination and m is the number of push-button switches. The matrix patchboard 6 can be wired to connect any preselected combination to the sequence checking network in the correct order. By means of the matrix patchboard 6 the combination can be quickly and easily changed. Only the proper push-button switches are wired to the sequence checking network in a preselected sequence in accordance with the combination. Network 7, which may be a conventional address counter, will produce an output only if the lines from the patchboard are activated in the proper sequence.

OR gate 9, which is also connected to receive the

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dial input information from dial input circuit 16, produces an output whenever any of the buttons P0-P9 is pressed. Counter 10 receives the signals from OR gate 9 and has an output which corresponds to a count which is the number of digits in the combination. For example, if there are five digits in the preselected combination, the counter will be wired so that its output indicates a count of five. It therefore produces an output only when the count corresponding to the number of digits in the combination has been reached. When that count has been reached inhibitor 11 is activated and the inputs to counter 10 and the sequence checking network 7 are inhibited so that no further digit information is received by the system. The output of counter 10 is received by one input of AND gate 8. The other input of AND gate 8 receives the signal from sequence checking network 7.

AND gate 8 produces an output only when the correct push-buttons are pressed in the proper sequence and when the correct number of push-buttons is pressed. If the combination has five digits, for example, AND gate 8 will produce an output only when the correct five push-buttons have been pressed in the proper sequence. When these conditions are both met, switch 12 is turned ON and completes the circuit to relay K2. Contact K12 of relay K1 is already closed since K1 has been previously energized. When switch 12 is turned ON, relay K2 is energized and contact K21 of relay K2 is closed thereby closing the circuit path to lock actuator 13 which will open or disengage the latch (not shown). Lock actuator 13 and relay contact K21 comprise the lock release circuit, and switch 12, the coil of relay K2, and relay contact K12, together with the lock release circuit, comprise the lock control circuit.

NOR gate 22 and AND gate 8 have been shown with two inputs, however, these gates may have any number of inputs depending on the conditions to be imposed upon the system. NOR gate 22 insures that the digit information is entered within a given time interval and/or that two or more buttons have not been pushed simultaneously in an attempt to foil the system. AND gate 8 insures that the proper number of digits have been entered in the proper sequence. Other conditions may be added and the number of inputs to the gates may be easily changed. Any logically equivalent circuit may be substituted for the NOR, OR, or AND gates. For example, a NOR gate may be used in place of AND gate 8.

As an additional feature, an alarm circuit can be implemented to activate a bell and/or indicator whenever P11 is pressed to start the system. This would apprise those in the locked area that someone is attempting to enter.

Referring now to FIG. 2, there is shown a circuit diagram of the invention. The push-button switches are shown as single-pole, double-throw switches S0-S9 in their normal or inactive position so that the lines going to diodes D10-D19 and to flip-flops FF1 through FF5 are all open. For purposes of illustration, the matrix patchboard unit has been set so that the push-button must be operated to close only switches S0-S4 sequentially. Transistor 32, resistor 36, the coil of relay K1, diode D21, relay contact K11 and push-button switch S11 comprise the start circuit.

In the circuit diagram of FIG. 2, the time interval generator is composed of timing oscillator 21, circuits FF7, FF8 and FF9. Circuits FF7-FF9 are bistable devices such as conventional flip-flops. FF7 and FF8 comprise a two-stage binary counter for counting the cycles from timing oscillator 21, and FF9 is a set-reset circuit which is turned ON when a preselected count is reached by the counter FF7-FF8. The counter may have any number of stages depending on the desired total count which represents the length of time for allowing digit information to be accepted by the system. The time interval is also dependent upon the frequency of the timing oscillator. For example, if the desired time interval is 12 seconds and

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the counter has two stages and is allowed to count to 4, then the oscillator frequency should be one cycle every three seconds, or approximately 0.33 cycle per second. If a count of four is desired then the appropriate line from the counter is connected to set-reset circuit FF9 which is set when the desired count (four) has been reached. The output signal of FF9 would therefore indicate that the time interval has expired. When the time interval has elapsed the output of NOR gate 22 provides a signal which will turn OFF transistor 32 which acts as a switch to open the circuit to relay K1. Between the output of NOR gate 22 and transistor 32 is resistor 36, which together with transistor 32 comprises switch 3. Transistor 32 is normally turned ON and will stay ON as long as the time interval has not elapsed.

In addition to an input for receiving the signal from FF9, NOR gate 22 also has an input for receiving a signal from the simultaneous buttons circuit which comprises a set of diodes D1-D9 having their anodes connected in parallel and a set of biasing resistors R1-R9 having a voltage V connected at one end and the other end connected to contacts C20-C29. Contacts C20-C29 are all interconnected when the switches S0-S9 are in their normal position which is as shown in FIG. 2. The contacts are interconnected by means of the wires between C10 and C21, C11 and C22, C12 and C23, etc. Contacts C20 and C19 are grounded so that the cathodes of all the diodes D1-D9 are connected together to ground potential when the switches S0-S9 are in their normal position. When only one button is pressed at a time no negative signal will be present on line 30 since all of the contacts C20-C29 will still be at ground potential. When a button is pressed it will make contact with its respective line in the matrix network and when it is released it will return immediately to its normal position. However when two or more buttons are pressed simultaneously at least one contact C21-C29 will be separated from ground and a negative signal will be present on line 30. The negative signal will produce a positive signal at the output of NOR gate 22 and through resistor 36 at the base of transistor 32 to turn off transistor 32. NOR gate 22 will therefore produce a positive output when neither of its inputs are positive, that is, when the time interval has elapsed, and/or when two or more buttons have been pressed simultaneously.

Transistor 32 is shown in the common emitter configuration. The coil of relay K1 in the collector circuit of transistor 32 is energized when transistor 32 is in its normally ON condition and contact K11 of relay K1 is closed when K1 is energized. Relay K1 is energized when push-button P11 is initially pressed to close contact S11. A diode D21 is connected across the relay coil to suppress transients resulting from the back E.M.F. of the coil. When a positive signal is present at the output of NOR gate 22, transistor 32 is turned OFF, relay K1 is deenergized, thereby insuring that relay K2 cannot be energized to close contact K21 of relay K2 which allows lock solenoid 34 to be activated.

The digit information is also received by a sequence checking network which comprises circuits FF1-FF6 which are bistable devices such as conventional flip-flops. Circuits FF1-FF5 comprise a five stage circuit, commonly known as an address counter, which transfers a signal to its output only if each stage is sequentially activated. If the circuits are sequentially activated a signal will be sent to activate set-reset circuit FF6. When FF6 is set it will produce an output signal indicating that the proper digits in the combination have been entered and that they have been entered in the proper sequence.

Circuits FF1-FF5 receive their input signals from switches S0-S9 through the patchboard matrix network which comprises the lines connecting contacts C0-C9 to diodes D10-D19 and the lines connecting a selected number of those lines to bistable circuits FF1-FF5. As is seen from the circuit diagram of the patchboard matrix

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network, not all of the lines from the switches are connected to the sequence checking network. Only those lines are connected which correspond to the proper push-buttons which in turn correspond to the proper digits of the combination. In the network shown, the proper digits are 0, 1, 2, 3 and 4, in that sequence. Any other of the ten digits can be made a part of the combination by merely changing patchboard connections. If more than five digits are employed in the combination additional bistable circuits are added. The total number of bistable circuits in the sequence checking network will equal the number of digits in the combination plus a set-reset circuit. The patchboard is also used to program the proper connections to the sequence checking network in the proper order. The push-button switches are connected to the bistable circuits with the switch corresponding to the first digit of the combination connected to FF1, the switch corresponding to the second digit of the combination connected to FF2, and so on. FF2 cannot be activated before FF1 since FF1 must first produce an output signal which will enable FF2 before FF2 can be activated by a button signal. The line from contact C1 to FF2 is connected to the reset side of FF2 and the output of FF1 is connected to the set side of FF2. FF2 will not change state when push-button P1 is pressed first, since FF2 is already in the reset state when the system is turned on. However, when push-button P0 is pressed first, it will cause FF1 to be set. At that time FF1 produces an output signal which will set FF2. Since FF2 is now in the set condition, or enabled, a pulse received at its reset side when P2 is pressed will cause FF2 to be changed to its reset state. FF2 in turn sets or enables FF3 which will be reset when P2 is pressed, and so on. When the push-button representing the last digit of the combination is pressed (P4 in accordance with the combination wired in FIG. 2) bistable circuit FF6 will be set thereby indicating that the correct buttons have been pressed in the proper sequence and that one condition for turning ON AND gate 8 has been satisfied. The output of FF6 is connected to an input of AND gate 8. Circuits FF1-FF5 are connected to the matrix so that they will be activated only by positive or ground signals from switches S0-S9 and will not be activated by negative voltage levels such as received from source -V through diodes D10-D19.

Whenever any of the push-buttons are pressed, a signal is fed through one of the diodes D10-D19 to the binary counter circuit 10 comprising flip-flops FF10-FF12. This counter will count the total number of buttons pressed. It will have as many stages as are necessary to count the total number of digits in the combination. In the circuit of FIG. 2, the combination has five digits so that a three stage binary counter is required. The output of the counter representing a count of five is connected to set-reset circuit FF13 which is set when the count of five is reached. The signal produced by FF13 is received by an input of AND gate 8 and also by diode D23 which inhibits or clamps line 31 so that no additional button information will be transmitted to counter FF10-FF12 and sequence checking network FF1-FF6. The system will accept no further button information after the count of five has been reached. Capacitor 35 is placed between line 31 and ground for suppressing transients.

In the circuit diagram of FIG. 2, if the count of five is not reached AND gate 8 will be inhibited. However when the output of FF13 indicates that all the digits of the combination have been counted AND gate 8 will produce an output which will trigger and turn ON switch 12 comprising transistor 33 and resistor 37 provided that the other input to AND gate 8 has received a signal from FF6 indicating that the proper buttons have been pressed in the proper sequence. Transistor 33 is shown in the common emitter configuration and has the coil of relay K2 in its collector circuit. A diode is connected across the relay coil for suppressing transients due to the back E.M.F. produced by the coil. Relay contact K12 of relay

K1 is serially connected between voltage source -V and the relay coil of relay K2. When transistor 33 is turned ON relay K2 is energized since contact K12 is closed when K1 is energized at the beginning of system operation when P11 is pressed. When relay K2 is energized, contact K21 of relay K2 is closed thereby closing the circuit path from voltage source V to lock solenoid 34. Lock solenoid 34 will thereby disengage or unlock the latch (not shown). Lock solenoid 34 and relay contact K21 comprise the lock release circuit. Transistor 33, resistor 37, the relay coil of K2, diode D22, and relay contact K12, together with the lock release circuit, comprise the lock control circuit.

NOR gate 22 and AND gate 8 have been shown with two inputs. However these gates may have any number of inputs depending upon the conditions imposed on the system. Any other circuit which will perform the logic function can be used in place of the gates illustrated. OR gate 9 will have as many inputs as there are buttons for entering digits of a combination.

A reset line 14 is connected to all of the bistable circuits to provide a reset voltage so that all the circuits are held in the reset or OFF condition. When push-button P11 is pressed and relay K1 is energized, contact K13 of relay K1 will open and the flip-flops will be capable of being set or turned ON. As soon as the predetermined time interval for entering the combination information has elapsed or whenever two or more buttons are pressed simultaneously, NOR gate 22 will produce an output which will turn OFF transistor 32 thereby deenergizing relay K1 and closing contact K13 which allows all circuits to be immediately reset. Deenergization of relay K1 also opens the circuit to relay K2 thus further insuring that lock solenoid 34 will not be energized.

Though the invention has been described and illustrated to accommodate a given combination composed of five digits, it is to be understood that any other combination of five or less digits may be used with the present device. The present device operates with ten push-buttons with a five-digit combination, giving 100,000 combinations from which to choose. However a device can be built to use fewer or more buttons with a shorter or longer code to give almost any number of combinations. This would be accomplished by employing a larger patchboard, adding bistable elements in the sequence checking network and counter 10, and adding the appropriate number of push-buttons if needed.

What is claimed and desired to be secured by Letters Patent of the United States is:

1. A combination-operated electrical lock system which opens a lock when digits of a combination are sequentially entered into the system, comprising,
 - input means having a plurality of digit inputs for entering the digits of the combination,
 - first means coupled to said input means for resetting said system when the digits are entered after a preset time interval has elapsed, or when two or more digits of the combination have been entered simultaneously,
 - lock control means, and
 - second means coupled between said input means and said lock control means for energizing said lock control means if the preselected digits are entered in a preselected order and the total number of digits in the combination has been entered.
2. The combination-controlled electrical lock system of claim 1 wherein said first means includes:
 - a reset circuit,
 - means coupled to said reset circuit for starting said system,
 - a first gate having at least two inputs and an output wherein said output is coupled to said means for starting said system,
 - a time interval generator for producing an output signal having a predetermined duration coupled to one input of said first gate, and
 - means for producing an output whenever two or more

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digits are simultaneously entered into the system coupled between said input means and another input of said first gate,

whereby said first gate produces an output when either the time interval has elapsed, or two or more digits have been entered simultaneously for turning off said means for starting.

3. The combination-controlled electrical lock system of claim 1 wherein said second means comprises:

a second gate having at least two inputs and an output wherein said output is coupled to said lock release means,

sequence checking means coupled between said input means and an input of said second gate for producing an output only when the proper digits have been entered in accordance with a preselected sequence, means coupled between said input means and another input of said second gate for producing an output when the proper number of digits has been entered, whereby said second gate produces an output signal when the proper digits have been entered in the preselected sequence and the proper number of digits has been entered.

4. The system of claim 3 wherein said sequence checking means is coupled to said input means by patchboard means for allowing the combination to be changed.

5. The system of claim 3, wherein the sequence checking means comprises an address counter.

6. The system of claim 3 in which the means for producing an output when the proper number of digits has been entered includes:

a binary counter having an input and an output, an OR gate having an output coupled to the input of said binary counter and having a plurality of inputs corresponding in number to the number of digit inputs of said input means and with each of the OR gate inputs coupled to a single digit input, and inhibitor means coupled from the output of said binary counter to the input of said binary counter and to said sequence checking means for inhibiting the system when the proper number of digits has been entered.

7. A combination-controlled lock system which opens a lock when digits of a combination are entered into the system, comprising:

input means having a plurality of digit inputs for entering the digits of the combination, a reset circuit coupled to the system, starting means coupled to said reset circuit for starting said system by deactivating said reset circuit, a first gate having at least two inputs and an output wherein said output is coupled to said starting means, a time interval generator for producing an output signal having a predetermined duration coupled to one input of said first gate,

means for producing an output whenever two or more digits are simultaneously entered into the system coupled between said input means and another input of said first gate,

lock control means,

a second gate having at least two inputs and an output wherein said output is coupled to said lock control means,

a sequence checking means coupled between said input means and an input of said second gate for producing an output only when the proper digits have been entered in accordance with a preselected sequence, means coupled between said input means and another input of said second gate for producing an output when the proper number of digits has been entered, whereby said first gate produces an output for resetting the system and for inhibiting said lock control means when either the time interval has elapsed, or two or more digits have been entered simultaneously, and whereby said second gate produces an output signal for triggering said lock release means when the proper

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digits have been entered in the preselected sequence and the proper number of digits has been entered.

8. The system of claim 7 in which the sequence checking means is coupled to said input means by means of a patchboard matrix for allowing the combination to be changed.

9. The system of claim 7 in which the means for producing an output when the proper number of digits has been entered includes:

a binary counter having an input and an output, an OR gate having an output coupled to the input of said binary counter and a plurality of inputs corresponding in number to the number of digit inputs of said input means and with each of the OR gate inputs coupled to a single digit input, and inhibitor means coupled from the output of said binary counter to the input of said binary counter and to said sequence checking means for inhibiting the system when the proper number of digits has been entered.

10. The system of claim 9 in which the inhibitor means is a diode.

11. The system of claim 7 in which the sequence checking means is an address counter.

12. The system of claim 7 in which the time interval generator includes a timing oscillator coupled to binary circuit means which produces an output only when a given count is reached.

13. The system of claim 7 in which the input means further includes a start input coupled to said starting means for energizing said starting means.

14. The system of claim 13 in which said starting means comprises:

a first switch, a first relay, a relay coil of said first relay serially connected to said switch, a first relay contact of said first relay serially connected with said first relay coil, and a second switch responsive to said start input coupled across said first relay contact of said first relay, whereby said relay coil of said first relay is energized to close said first relay contact when said second switch is closed.

15. The system of claim 14 in which said lock control means comprises:

a third switch, a second relay, a relay coil of said second relay serially connected to said third switch, a second relay contact of said first relay serially connected to said relay coil of said second relay, and a lock release circuit having a lock actuator serially connected with a first relay contact of said second relay.

16. The system of claim 15 in which said first and third switches are transistors.

17. A solid-state combination-operated electrical lock system which opens a lock when digits of a combination are entered into the system by a number of manually operated push-buttons in accordance with preselected conditions, and push-button switches corresponding to each push-button, which push-button switches are closed only when the corresponding push-button is in the pressed condition, comprising:

input means comprising a plurality of push-button switches which are closed while said push-buttons are pressed and including an output for each of said push-buttons for producing an output signal when the respective push-button is pressed, a time interval generator for producing an output signal having a predetermined duration, circuit means connected to said input means for generating an output signal whenever two or more push-buttons are pressed simultaneously.

- a first NOR gate having at least two inputs and an output with one of its inputs coupled to said time interval generator and another of its inputs coupled to said circuit means, said NOR gate producing a signal at its output whenever the preselected time interval has elapsed or whenever two or more push-buttons have been pressed simultaneously, 5
- a start circuit comprising a first switch, first relay coil, and first relay contact serially connected to receive a bias voltage, and a push-button start switch connected in parallel with said first relay contact, said first switch being connected to the output of said NOR gate for opening the circuit connection to said relay coil whenever a signal is received by said first control switch from said NOR gate, 10
- a sequence checking network for producing an output only when the proper push-buttons have been pressed in the proper sequence, 15
- a matrix patchboard connected between said sequence checking network and said input means for programming only preselected outputs of said input means to said sequence checking network in the proper order, 20
- an OR gate connected to said input circuit for producing an output signal when any of the push-buttons are pressed, 25
- a counter connected to said OR gate for producing an output signal when the number of push-buttons pressed corresponds to the number of digits in the combination, 30
- an inhibitor circuit coupled from the output of said counter to its input and to said sequence checking network for inhibiting the input of said counter and the input to said sequence checking network whenever the proper number of push-buttons have been pressed so that no further digits will be accepted by the system, 35
- an AND gate having at least two inputs and an output, with one of said inputs connected to the output of said sequence checking network and another of said inputs connected to the output of said counter, said AND gate producing an output signal whenever 40

- the proper push-buttons have been pressed in the proper sequence and when the proper number of pushbuttons have been pressed,
- a lock control circuit comprising a second switch in series with a second relay coil and a second contact operated by said first relay coil, said second contact being closed when said start circuit is energized, and said switch connected to the output of said AND gate for receiving the output signal of said AND gate, so that said second switch is closed when the signal from said AND gate is received thereby causing the relay coil to be energized,
- a lock release circuit comprising a lock actuator for opening a lock and a fourth relay contact energized by said second relay coil serially connected to a voltage, with said fourth relay contact closing to allow said lock actuator to be activated when all preselected conditions are met, and
- a reset circuit comprising a third contact of said first relay coil which is connected between a voltage source and said system which is closed to reset the system whenever the preselected conditions are not met.

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