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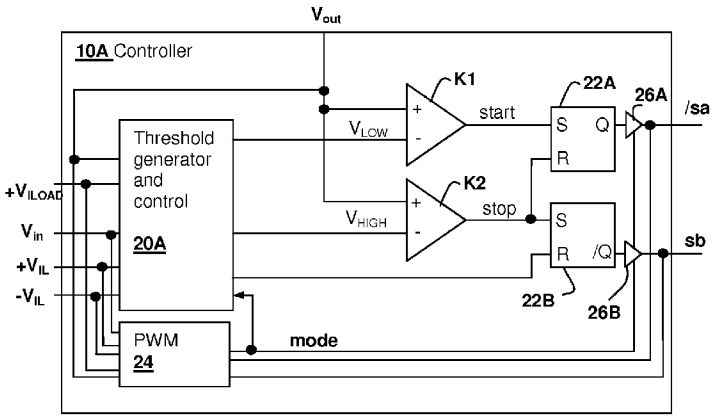

Fig. 2A

(57) Abstract: A hysteretic buck converter provides improved regulation control, in particular for buck converter standby operation. A comparison circuit (K1, K2) compares the output voltage (Vout) of the buck converter to a waveform (V_{Low}) that is generated from an indication ($+V_{ILOAD}$) of the output current of the converter, so that the turn-on time of the converter is advanced as the output current demand increases. The resulting action anticipates a reduction in output voltage (V_{out}) due to the increased current, preventing an excursion of the output voltage (V_{out}) below the ripple voltage minimum. The turn-off time of the converter is controlled by an upper threshold (V_{HIGH}) that limits the ripple voltage maximum. The output current indication may be a measurement of output current, or may be a dynamic value calculated from the input voltage (V_{in}) and the output voltage (V_{out}) waveform.

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HYSTERETIC BUCK CONVERTER HAVING DYNAMIC THRESHOLDS

FIELD OF THE INVENTION

[0001] The present invention relates generally to hysteretic buck converter control schemes, and more specifically, to a buck converter control circuit in which an indication of output current is used to adjust turn-on timing dynamically.

BACKGROUND OF THE INVENTION

[0002] At low output current levels, pulse width modulator (PWM) controllers and other types of switching power regulators that deliver high current levels under high load conditions are inefficient. Since the pulse width becomes very narrow for low output current levels, the power used to operate the switching circuits and control/sensing circuits, which does not typically change with load current demand, predominates converter power consumption, making the converter very inefficient during low demand conditions. Alternative controller modes are frequently implemented to operate the converter in a standby low power mode, in which the full converter dynamic performance is not available, but a minimum output voltage is maintained to provide required power supply voltage(s) when the load current demand is low. Pulse-

frequency modulator (PFM) circuits are frequently used in low power operating modes, as the pulse frequency can be arbitrarily reduced based upon load demand. Hysteretic control circuits, in which the output voltage is maintained between two predetermined set points, have been applied to provide such low-power operating modes. Hysteretic converters have a wide dynamic range and potentially low power consumption, due to their activation only when the output voltage falls below an acceptable limit.

[0003] Also, in low power applications in which either the complexity or the power required for PWM operation is undesirable, hysteretic controllers are sometimes used to provide the power supply control algorithm for all levels of output current, since the control circuit itself can be placed entirely in standby mode, with the low-limit voltage sensing circuit being the only circuit required to operate. The output of the low-limit voltage sensing circuit can then activate the remainder of the converter when the output voltage must be raised. Further, in any application in which the transient response of a PWM converter is not sufficiently fast for responding to load transients, hysteretic converters are also used to provide a fast response to changing load conditions.

[0004] In typical hysteretic converters, a constant-width pulse is provided when the output voltage falls below a low-

limit threshold, injecting a charge into the output capacitor that raises the output voltage by a predetermined amount. However, if the output current or input voltage conditions are changing, such a converter can produce an undesirable level of ripple, as the constant-width pulse is not responsive to different levels of load current or input voltage. In other types of hysteretic converters, the input voltage and other power supply conditions are monitored and the width of the output pulse is controlled so that the level of ripple is controlled to a greater degree than the constant-width controllers can provide.

[0005] However, each of the above hysteretic controllers, load transients or input voltage droop can cause undershoot of the low-limit threshold due to time required for the converter to respond. In the constant-width converter, several pulses may be required for the output voltage to recover and in the width-controlled hysteretic converter, an initial undershoot is present, which is corrected by the pulse that has been triggered.

[0006] Therefore, it would be desirable to provide a power supply circuit and control method that reduce ripple in a hysteretic converter by controlling undershoot.

DISCLOSURE OF THE INVENTION

[0007] The above stated objective of controlling undershoot in a hysteretic converter is provided in a buck switching voltage regulator circuit and a method of operation of the buck switching voltage regulator circuit.

[0008] The buck switching voltage regulator circuit provides improved ripple control by anticipating the magnitude of the ripple due to load current changes. The circuit may be a control circuit active in a standby mode of a switching regulator, such as a PWM regulator that uses a PWM control mode during higher current output demand and enters standby mode during lower current output demand conditions. A comparison circuit compares the output voltage of the converter to a waveform that is generated from an indication of the output current of the converter, so that the turn-on time of the converter is advanced as the output current demand increases and the lower voltage limit is adjusted to prevent undershoot below a specified lower ripple voltage limit. The turn-off time of the converter is controlled by an upper threshold that limits the ripple voltage maximum. The output current indication may be a measurement of output current, or may be a value calculated from the input voltage and the output voltage waveform.

[0009] The foregoing and other objectives, features, and advantages of the invention will be apparent from the following, more particular, description of the preferred embodiment of the invention, as illustrated in the accompanying drawings.

DESCRIPTION OF THE DRAWINGS

[00010] **Figures 1A-1B** are block diagrams depicting power switching circuits in accordance with embodiments of the present invention.

[0011] **Figure 2A** is a simplified schematic diagram of control circuit **10A** of **Figure 1A.**

[0012] **Figure 2B** is a simplified schematic diagram of control circuit **10B** of **Figure 1B.**

[0013] **Figure 3A** is a signal waveform diagram illustrating calculations performed within threshold generator and control circuit **20A** of **Figure 2A** and threshold generator and control circuit **20B** of **Figure 2B,** in discontinuous conduction mode (DCM).

[0014] **Figure 3B** is a signal waveform diagram illustrating calculations performed within threshold generator and control circuit **20A** of **Figure 2A** and threshold generator and control circuit **20B** of **Figure 2B,** in continuous conduction mode (CCM).

[0015] **Figures 4A-4B** are signal waveform diagrams depicting signals within the circuits depicted in **Figures 1A-1B** and **Figures 2A-2B.**

BEST MODE FOR CARRYING OUT THE INVENTION

[0016] The present invention encompasses circuits and methods for providing control of a buck switching voltage regulator, in which ripple undershoot is prevented by controlling the turn-on threshold in conformity with an indication of the output current drawn by a load. The output current indication can be provided by measuring the output current directly, or as will be shown in the following description, can be calculated from the output voltage waveform and the value of the input voltage.

[0017] Referring now to **Figure 1A**, a buck switching voltage regulator circuit in conformity with an embodiment of the invention is shown. A control circuit, controller **10A** provides gate drive signals to a switching circuit **SWA** that couples an inductor **L1** in series between an input voltage source V_{IN} and output terminal V_{OUT}, when transistor **P1** is activated by control signal **/sa**. Switching circuit **SWA** couples inductor **L1** in shunt between output terminal V_{OUT} and a common return path (ground) associated with input voltage source V_{IN} and output terminal V_{OUT}, when transistor **N1** is activated by control signal **sb**. Output capacitor **C1** filters the output of the buck switching voltage regulator circuit, so that the voltage generated at output terminal V_{OUT} is held substantially constant, except for

a ripple voltage. At low demand, i.e., for low load current I_L supplied to a load Z_L, controller **10A** operates in discontinuous conduction mode (DCM), first activating transistor **P1** to charge output capacitor **C1** through inductor **L1**, then deactivating transistor **P1** and activating transistor **N1** to discharge energy stored in inductor **L1** onto capacitor, and then finally deactivating transistor **N1** until the voltage of output terminal V_{OUT} falls below a threshold magnitude. At higher levels of load current I_L, controller **10A** may operate in continuous conduction mode (CCM) as a hysteretic converter, or may transition directly to another CCM control algorithm, such as pulse-width modulation (PWM). Even if CCM operation is implemented for the hysteretic operation of the converter, PWM or other operation modes may be initiated after a range of load current I_L is exceeded for which hysteretic CCM operation is used.

[0018] In the buck switching voltage regulator of the present invention, the threshold magnitude used to determine the turn-on time of transistor **P1** is a time-varying waveform generated from an indication of the output current provided from output terminal V_{OUT} to a load and from the magnitude of the input voltage provided from voltage source V_{IN}, so that as the output current increases or the input voltage decreases, the time at which transistor **P1** is activated occurs earlier in

time and as the output current decreases or the input voltage decreases, the time at which transistor **P1** is activated occurs later in time. The threshold magnitude is computed from an indication of the output current, which may be a measurement of the output current generated by a sense resistor R_S, which provides a voltage $+V_{ILOAD}$ that differs from the output terminal V_{OUT} voltage in proportion to load current I_0. (For illustrative purposes V_{OUT} is also designated as $-V_{ILOAD}$.) Controller **10A** computes the turn-off time of transistor **P1**, which is also the turn-on time of transistor **N1**, from the input voltage provided by voltage source V_{IN} and the voltage of output terminal V_{OUT}, so that the ripple voltage at output terminal V_{OUT} does not exceed a specified maximum. Finally the turn-off time for transistor **N1** can be controlled by the current I_L provided through inductor **L** to capacitor **C1** as measured by the voltage ($+/-V_{IL}$) across resistor R_L reaching a zero or a slightly negative value, to ensure there is no residual energy stored in inductor **L.**

[0019] Referring now to **Figure 1B**, a buck switching voltage regulator in accordance with another embodiment of the invention is shown. The buck switching voltage regulator of **Figure 1B** is similar to that of the buck switching voltage regulator of **Figure 1A**, so only differences between them will be described below. Further, various features in buck

switching voltage regulator of **Figure 1B** can be used as alternatives for features illustrated in the buck switching voltage regulator of **Figure 1A**, and vice-versa. Switching circuit **SWB** uses two N-type transistors **N2** and **N1** and receives corresponding gate control signals **sa** and **sb** from a controller **10B**. An N-channel pair can also be used in the buck switching voltage regulator of Figure 1A, with appropriate change in the polarity of gate control signal **/sa**. Controller **10B** receives only two control input values: the voltage of input source $\mathbf{V_{IN}}$, and the voltage of output terminal $\mathbf{V_{OUT}}$. Controller **10B** performs all switch control in conformity with the two control input signal values ($\mathbf{V_{out}}$,$\mathbf{V_{in}}$), provided by respective input source $\mathbf{V_{IN}}$ and from output terminal $\mathbf{V_{OUT}}$, to generate gate control signals **sa** and **sb**. A P-N switching stage such as switching circuit **SWA** as illustrated in Figure 1A can be used with appropriate change to the polarity of gate control signal **sa**. Since the output current is related to the voltage waveform of output terminal $\mathbf{V_{OUT}}$ and the voltage of voltage source $\mathbf{V_{IN}}$, the turn-on time of transistor **N1** can be determined from the two input control signal values ($\mathbf{V_{out}}$,$\mathbf{V_{in}}$) as will be described in further detail below.

[0020] Referring now to **Figure 2A**, details of controller **10A** of Figure 1A are shown. A pair of tri-state buffers, **26A** and **26B**

are activated by a control signal **mode** provided by PWM controller **24**, when load current I_O falls below a threshold, or alternatively when PWM controller **24** is placed in standby mode via an external control signal. When control signal **mode** is active, the gate control outputs of PWM **24** are placed in a high-impedance state, so that the hysteretic controller implemented by the balance of circuits within controller **10A** provides gate control output signals **/sa** and **sb**. A threshold generator and control circuit **20A** provides a threshold voltage to a comparator **K1**, which sets a threshold magnitude (voltage signal V_{low}) below which input control signal V_{out} activates a **start** signal, which triggers the beginning edge of gate control signal **/sa** by activating the set input of flip-flop **22A**. When the magnitude of input control signal V_{out} rises above another threshold voltage V_{HIGH}, another comparator **K2** activates the reset input of flip-flop **22A** and the set input of a flip-flop **22B**, which triggers the trailing edge of gate control signal **/sa** and the leading edge of gate control signal **sb**. Threshold generator and control circuit **20A** also provides a control signal to the reset input of flip-flop **22B**, to trigger the trailing edge of gate control signal **sb**, when inductor current I_L falls below a zero or slightly negative value.

[0021] Referring now to **Figure 2B**, details of controller **10B** of Figure 1B are shown. Controller **10B** is similar to controller **10A** of Figure 2A, so only differences between them will be described below. Controller **10B** is provided as an example of a minimum-input controller, and also exemplifies a controller that provides all control in hysteretic mode. However, it is understood that the minimum-input configuration can be used in standby modes with another controller type, such as PWM controller **24**, illustrated in Figure 2A. Threshold generator and control circuit **20B** receives control input signals ($\mathbf{V_{out}}$,$\mathbf{V_{in}}$) and generates threshold voltages $\mathbf{V_{LOW}}$ and $\mathbf{V_{HIGH}}$ by calculating them from control input signals ($\mathbf{V_{out}}$,$\mathbf{V_{in}}$) as will be described in further detail below. A timer **28** is provided, which will generally be a counter chain operated from a clock signal, to time the duration of gate control signal **sa**, for use in calculating an appropriate width of gate control signal **sb**, since controller **20B** does not directly measure inductor current $\mathbf{I_L}$.

[0022] With reference now to **Figure 3A**, calculations within threshold generator and control circuit **20A** of Figure 2A and threshold generator and control circuit **20B** of Figure 2B are illustrated for discontinuous conduction mode (DCM). The value of threshold voltage magnitude V_{LOW} required to ensure that the ripple on output terminal $\mathbf{V_{OUT}}$ does not fall below a specified

minimum V_{MIN} can be determined either using a measured value for output current $\mathbf{I_o}$ as illustrated in control circuit **20A** of Figure 2A or by using an indication of output current $\mathbf{I_o}$ calculated from control signal values ($\mathbf{V_{in}}$, $\mathbf{V_{out}}$) as illustrated in control circuit **20B** of Figure 2B. Assuming that output terminal voltage $\mathbf{V_{OUT}}$ is constant, while gate control signal **sa** is active, inductor current $\mathbf{I_L}$ can be approximated as

$$I_L(t) = (V_{in} - V_{out})(t - t_0)/L$$

, where L is the inductance of inductor **L1**, and therefore at time t_1,

$$I_L(t_1) = I_0 = (V_{in} - V_{out})(t_1 - t_0)/L$$

Therefore,

$$t_1 - t_0 = I_0L/(V_{in} - V_{out})$$

The actual voltage droop on output terminal $\mathbf{V_{OUT}}$ from time t_0 to time t_1, assuming a linear inductor current $\mathbf{I_L}$, is given by

$$\Delta V = I_L\Delta t/2C$$

, where C is the total output capacitance at output terminal $\mathbf{V_{OUT}}$. To maintain the voltage at output terminal V_{OUT} above minimum voltage V_{MIN}, gate control signal **sa** should be activated no later than the time at which control signal V_{out} falls to a threshold level

$$V_{LOW} = V_{MIN} + \Delta V = V_{MIN} + I_0(t_1 - t_0)/2C$$

Since

$$t_1 - t_0 = I_0L/(V_{in} - V_{out})$$

in the above approximation for constant inductor current I_L,

threshold magnitude V_{LOW} can be calculated as

$$V_{LOW} = I_0^2 L/2C(V_{in} - V_{out})$$

Therefore, once the values of the inductor and capacitor are known, a waveform for threshold voltage V_{LOW} can be determined from the input voltage signal V_{in} and control signal V_{out} and the load current I_L, since at the time threshold magnitude V_{LOW} is crossed, $I_L(t_1) = I_0$.

[0023] To determine the load current used to calculate threshold magnitude V_{LOW} from $V_{LOW} = I_0^2 L/2C(V_{in} - V_{out})$, the load current can be measured directly, or by estimation. Since the voltage change across capacitor **C1** from time t_0 to time t_2 is $V_{HIGH} - V_{LOW}$, the charge added to the capacitor can be expressed as

$$C(V_{HIGH} - V_{LOW}) = [(V_{in} - V_{out})(t_2 - t_0)^2]/2L - I_0(t_2 - t_0)$$

and current I_0 can therefore be expressed as

$$I_0 = [(V_{in} - V_{out})(t_2 - t_0)]/2L - C(V_{HIGH} - V_{LOW})/(t_2 - t_0)$$

By measuring the time (e.g., counting clock periods) between the time that the charging switch (e.g., transistor **P1** of Figure 1A or transistor **N2** of Figure 1B) is on, I_0 can be calculated and used as an estimate of inductor current I_L, since the difference between them is generally small except under very light load conditions. Alternatively, I_0 can be calculated from the time period extending from time t_2 to time t_5 according to:

$$C(V_{HIGH} - V_{LOW}) = (V_{in} - V_{out})(t_4 - t_2)^2/2L - I_0(t_5 - t_2)$$

which leads to:

$$I_0 = V_{out}(t_4 - t_2)^2/2L(t_5 - t_2) - C(V_{HIGH} - V_{LOW})/(t_5 - t_2)$$

[0024] To determine the magnitude V_{HIGH} of the voltage on output terminal $\mathbf{V_{OUT}}$ at which gate control signal **sa** should be de-asserted and gate control signal **sb** asserted, another calculation is performed. The voltage at output terminal $\mathbf{V_{OUT}}$ at time t_2, at which $V_{OUT} = V_{HIGH}$ is $V_{MAX} - Q(t_3 - t_2)/C$, where $Q(t_3 - t_2)$ is the total charge added to capacitor **C1** after gate control signal **sa** is de-asserted and gate control signal **sb** is asserted, which is equal to $V_{MAX} - (I_{MAX} - I_0)(t_3 - t_2)/2C$, where maximum current I_{MAX} is the peak inductor current. Therefore, setting

$$V_{HIGH} = V_{MAX} - (I_{MAX} - I_0)(t_3 - t_2)/2C$$

will provide the desired switching time. Threshold magnitude V_{HIGH} can also be expressed in terms of V_{MIN}:

$$V_{HIGH} = V_{MIN} + (I_{MAX} - I_0)(t_2 - t_1)/2C$$

The peak current, I_{MAX}, can be determined from

$$I_{MAX} = I_0 + (V_{in} - V_{out})(t_2 - t_1)/L$$

and

$$I_{MAX} = I_0 + V_{out}(t_3 - t_2)/L$$

, which assume that the output voltage is not changing substantially, and that the inductor current is constant during the charging and discharging. Therefore,

$$(V_{in} - V_{out})(t_2 - t_1)/L = V_{out}(t_3 - t_2)/L$$

, which leads to:

$$t_3 - t_2 = (t_2 - t_1)(V_{in} - V_{out})/V_{out}$$

The above expression for $t_3 - t_2$ can be substituted in the above expression for V_{HIGH}, yielding:

$$V_{HIGH} = V_{MAX} - [(I_{MAX} - I_0)(t_2 - t_1)(V_{in} - V_{out})]/2CV_{out}$$

$I_{MAX} - I_0$ can be determined from the expression for threshold magnitude V_{HIGH} in terms of minimum voltage V_{MIN} to yield:

$$I_{MAX} - I_0 = 2C(V_{HIGH} - V_{MIN})/(t_2 - t_1)$$

Finally, combining the last two equations yields:

$$V_{HIGH} = V_{MAX} - (V_{HIGH} - V_{MIN})(V_{in} - V_{out})/V_{out}$$

and therefore

$$V_{HIGH} = V_{MIN} + (V_{MAX} - V_{MIN})V_{out}/V_{in}$$

The above expression can be used to produce or calculate a value for threshold magnitude V_{HIGH} as a discrete value based on previous values of control signals V_{in} and V_{out} or to generate a continuous waveform to control the upper threshold magnitude.

[0025] In each of the above calculations, it was assumed that the circuit is operating in DCM, i.e., operating such that all of the energy stored in inductor **L1** is discharged at times t_0 and t_5. However, under higher load conditions, the circuit of the present invention can operate in continuous conduction mode (CCM) and for optimum operation, the

computation of the lower threshold magnitude V_{LOW} is changed. However, the computation of the upper threshold magnitude V_{HIGH} is the same as in the above description.

Referring now to **Figure 3B**, such operation is illustrated. In the signal diagram of **Figure 3B** time t_4 is absent, because there is no significant period of time for which both switching transistors (charging and discharging) are off. In continuous conduction mode, assuming that output voltage V_0 is constant,

$$dI_L/dt = (V_{in} - V_{out})/L$$

after the charging transistor (e.g., transistor **P1** of Figure 1A or transistor **N2** of Figure 1B) is turned on, given a lower current I_{MIN}, which is the initial non-zero current value at the turn-on time, then

$$I_L(t) = (V_{in} - V_{out})(t - t_0)/L + I_{MIN}$$

which according to the above definition of $I_0 = I_L(t)$ for discontinuous conduction mode, leads to:

$$t - t_0 = (I_0 - I_{MIN})L/(V_{in} - V_{out})$$

Therefore, in order to ensure that the voltage of output terminal V_{OUT} does not fall below minimum voltage V_{MIN}, threshold magnitude V_{LOW} should be set to:

$$V_{LOW} = V_{MIN} + L(I_0 - I_{MIN})^2/2C(V_{in} - V_{out})$$

[0026] To determine the load current in CCM, as described

above for DCM, the load current can be measured directly, or by estimation. Since the voltage change across capacitor **C1** from time t_0 to time t_2 is $V_{HIGH} - V_{LOW}$, the charge added to the capacitor can be expressed as

$$C(V_{HIGH} - V_{LOW}) = (V_{in} - V_{out})(t_2 - t_0)^2/2L - (I_0 - I_{MIN})(t_2 - t_0)$$

and $I_0 - I_{MIN}$ can be expressed as

$$I_0 - I_{MIN} = (V_{in} - V_{out})(t_2 - t_0)/2L - C(V_{HIGH} - V_{LOW})/(t_2 - t_0)$$

which is the same as the expression for I_0 in DCM. Since the required quantity for determining V_{LOW} above is $I_0 - I_{MIN}$, the same computation can be used for estimating the value of $I_0 - I_{MIN}$ in CCM that was used to estimate I_0 in DCM. The alternative expression based upon the time period from time t_2 to time t_4 may also alternatively be used, as follows:

$$I_0 - I_{MIN} = V_{out}(t_4 - t_2)^2/2L(t_3 - t_2) - C(V_{HIGH} - V_{LOW})/(t_5 - t_2)$$

[0027] In CCM, it is possible to further optimize the control of threshold magnitude V_{LOW}. Since, for the time period between time t_5 and time t_6, the total charge lost from capacitor **C1** is given by:

$$(I_0 - I_{MIN})(t_6 - t_5)/2$$

Lower threshold magnitude V_{LOW} is therefore given by:

$$V_{LOW} = V_{MIN} + (I_0 - I_{MIN})(t_6 - t_5)/2$$

Lower threshold magnitude V_{LOW} can also be expressed as:

$$V_{LOW} = V_{MAX} - (I_0 - I_{MIN})(t_5 - t_3)/2$$

The inductor current $I_L = I_{MIN}$ at time t_5, which occurs when V_O

= V_{LOW}, can be expressed as:

$$I_{MIN} = I_O - (V_{in} - V_{out})(t_6 - t_5)/L = I_O - V_{out}(t_5 - t_3)/L$$

and therefore

$$(V_{in} - V_{out})(t_6 - t_5) = V_{out}(t_5 - t_3)$$

The above relations can be combined to yield:

$$V_{LOW} = V_{MIN} + V_{out}(I_0 - I_{MIN})(t_5 - t_3)/2(V_{in} - V_{out})$$

$$= V_{MAX} - (I_0 - I_{MIN})(t_5 - t_3)/2$$

and then,

$$V_{LOW} = V_{MIN} + (V_{MAX} - V_{MIN})V_{out}/V_{in}$$

which is the same as the expression for V_{HIGH} in both CCM and DCM. Therefore, for CCM, $V_{LOW} = V_{HIGH}$.

[0028] With reference now to **Figure 4A** and **Figure 4B**, operation of the buck switching voltage regulator circuits of Figure 1A and Figure 1B, controller **10A** of Figure 2A and controller **10B** of Figure 1B is illustrated and the calculations used in controllers **10A** and **10B** to determine switching times as described above are described in further detail below. Only DCM is shown, but the illustration is applicable to CCM operation, as well. **Figure 4A** shows operation of the hysteretic converter circuits of the present invention in response to a change in load current I_O. As load current I_O increases, threshold voltage V_{LOW} is increased according to the formulas above, causing the charging transistor to turn on progressively earlier. Similarly, **Figure**

4B shows operation of the hysteretic converter in response to a decreasing voltage at input source V_{IN}, such as operation from a battery that is discharging. The discharge rate is exaggerated to illustrate the effect of the decreasing input voltage on threshold voltage V_{LOW}, which is increased to cause the charging transistor to turn on earlier, compensating for the decrease in the voltage of input source V_{IN}.

[0029] While the invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that the foregoing and other changes in form, and details may be made therein without departing from the spirit and scope of the invention.

CLAIMS

WHAT IS CLAIMED IS:

1. A buck switching voltage regulator circuit, comprising:

a comparison circuit for providing a first indication when a voltage of an output of the buck switching voltage regulator circuit does not exceed a first threshold magnitude and providing a second indication when the voltage of the output of the buck switching regulator circuit exceeds a second threshold magnitude, wherein the second threshold magnitude is greater than the first threshold magnitude;

an inductive storage element;

a switching circuit for coupling the inductive storage element between an input of the buck switching voltage regulator circuit and the output of the buck switching voltage regulator circuit in response to the first indication, and coupling the inductive storage element between the output of the buck switching voltage regulator circuit and a return path of the output of the buck switching voltage regulator circuit in response to the second indication; and

a control circuit for generating the first threshold magnitude and the second threshold magnitude, such that the first threshold magnitude increases with increases in an output current provided by the output of the buck switching voltage regulator circuit to a load and decreases with decreases in the output current, and wherein the control circuit calculates an indication of the output current and

sets the first threshold magnitude in conformity therewith.

2. The buck switching voltage regulator circuit of Claim 1, wherein the control circuit further sets the second threshold magnitude in conformity with a value of the output current.

3. The buck switching voltage regulator circuit of Claim 1, wherein the control circuit calculates the indication of the output current from a voltage of the output of the buck switching voltage regulator circuit and a time period extending from a beginning of the second indication in a given cycle of the switching circuit and a beginning of the first indication in a next cycle of the switching circuit.

4. The buck switching voltage regulator circuit of Claim 3, wherein the control circuit calculates the indication of the output current according to the formula:

$$(V_{in} - V_{out})(t_2 - t_0)/2L - C(V_{HIGH} - V_{LOW})/(t_2 - t_0)$$

where V_{in} is a voltage of the input of the buck switching regulator circuit, V_{out} is the voltage of the output of the buck switching regulator circuit, C is a capacitance at the output of the buck switching regulator circuit. L is the inductance of the inductive storage element, t_2 is a time of the beginning of the second indication in the given cycle, t_0 is a time of the beginning of the first indication in the given cycle, V_{HIGH} is a maximum ripple voltage value, and V_{LOW} is

a minimum ripple voltage value.

5. The buck switching voltage regulator circuit of Claim 3, wherein the control circuit calculates the indication of the output current according to the formula:

$$V_{out}(t_4 - t_2)^2/2L(t_5 - t_2) - C(V_{HIGH} - V_{LOW})/(t_5 - t_2),$$

where V_{out} is the voltage of the output of the buck switching regulator circuit, C is a capacitance at the output of the buck switching regulator circuit. L is the inductance of the inductive storage element, t_2 is a time of the beginning of the second indication in the given cycle, t_5 is a time of the beginning of the first indication in the next cycle, V_{HIGH} is a maximum ripple voltage value, V_{LOW} is a minimum ripple voltage value, and t_4 is a time of the end of the second indication in the given cycle.

6. The buck switching voltage regulator circuit of Claim 1, wherein the control circuit measures the output current to provide the indication of the output current.

7. The buck switching voltage regulator circuit of Claim 1, wherein the control circuit calculates the first threshold magnitude further in conformity with a difference between a voltage of the input of the buck switching voltage regulator circuit and the voltage of the output of the buck switching voltage regulator circuit.

8. The buck switching voltage regulator circuit of Claim 7, wherein the control circuit calculates the first threshold magnitude according to the formula:

$$I_0^2 L/2C(V_{in} - V_{out}),$$

where V_{in} is a voltage of the input of the buck switching regulator circuit, V_{out} is the voltage of the output of the buck switching regulator circuit, C is a capacitance at the output of the buck switching regulator circuit, L is the inductance of the inductive storage element, and I_0 is the indication of the output current.

9. The buck switching voltage regulator circuit of Claim 1, wherein the control circuit is operating in a continuous conduction mode and the indication of output current is a difference between a current delivered to the output of the buck switching voltage regulator circuit and a minimum current in the inductive storage element.

10. The buck switching voltage regulator circuit of Claim 1, wherein the control circuit calculates the second threshold magnitude from the voltage of the output of the buck switching voltage regulator circuit and a voltage of the input of the buck switching voltage regulator circuit.

11. The buck switching voltage regulator circuit of Claim 10, wherein the control circuit calculates the second threshold magnitude according to the formula:

$$V_{HIGH} = V_{MIN} + (V_{MAX} - V_{MIN})V_{out}/V_{in},$$

where V_{in} is a voltage of the input of the buck switching regulator circuit, V_{out} is the voltage of the output of the buck switching regulator circuit, V_{HIGH} is a maximum ripple voltage value, and V_{LOW} is a minimum ripple voltage value.

12. A buck switching voltage regulator circuit, comprising:

a comparison circuit for providing a first indication when a voltage of an output of the buck switching voltage regulator circuit does not exceed a first threshold magnitude and providing a second indication when the voltage of the output of the buck switching regulator circuit exceeds a second threshold magnitude, wherein the second threshold magnitude is greater than the first threshold magnitude;

an inductive storage element;

a switching circuit for coupling the inductive storage element between an input of the buck switching voltage regulator circuit and the output of the buck switching voltage regulator circuit in response to the first indication, and coupling the inductive storage element between the output of the buck switching voltage regulator circuit and a return path of the output of the buck switching voltage regulator circuit in response to the second indication; and

a control circuit for generating the first threshold magnitude as a waveform at a rate greater than or equal to a switching period of the switching circuit, wherein the first indication is generated repetitively to control a start of the switching period, and wherein the waveform is generated such that the first indication occurs earlier in time within the switching period as an output current provided by the output of the buck switching voltage regulator circuit to a load increases and occurs later in time within the switching period as the output current decreases.

13. A method for regulating the output voltage of a buck switching voltage regulator circuit, comprising:

first comparing a voltage of an output of the buck switching voltage regulator circuit to a first threshold magnitude;

second comparing the voltage of the output of the buck switching voltage regulator circuit to a second threshold magnitude, wherein the second threshold magnitude is greater than the first threshold magnitude;

coupling an inductive storage element between an input of the buck switching voltage regulator circuit and the output of the buck switching voltage regulator circuit when the first comparing indicates that the voltage of the output of the buck switching voltage regulator circuit does not exceed the first threshold magnitude;

coupling the inductive storage element between the output of the buck switching voltage regulator circuit and a return path of the output of the switching voltage regulator circuit when the second comparing indicates that the voltage of the output of the buck switching voltage regulator circuit exceeds the second threshold magnitude; and

controlling values of the first threshold magnitude and the second threshold magnitude, such that the first threshold magnitude increases with increases in output current provided by the output of the buck switching voltage regulator circuit to a load and decreases with decreases in the output current, by calculating an indication of an output current provided by the output of the buck switching voltage regulator circuit to a load and setting the first threshold magnitude in conformity therewith.

14. The method of Claim 13, wherein the controlling further comprises setting the second threshold magnitude in conformity with a value of the output current.

15. The method of Claim 13, wherein the controlling calculates the indication of the output current from a voltage of the output of the buck switching voltage regulator circuit and a time period extending from a beginning of the second indication in a given cycle of the buck switching voltage regulator circuit and a beginning of the first indication in a

next cycle of the buck switching voltage regulator circuit.

16. The method of Claim 15, wherein the controlling calculates the indication of the output current according to the formula:

$$(V_{in} - V_{out})(t_2 - t_0)/2L - C(V_{HIGH} - V_{LOW})/(t_2 - t_0)$$

where V_{in} is a voltage of the input of the buck switching regulator circuit, V_{out} is the voltage of the output of the buck switching regulator circuit, C is a capacitance at the output of the buck switching regulator circuit, L is the inductance of the inductive storage element, t_2 is a time of the beginning of the second indication in the given cycle, t_0 is a time of the beginning of the first indication in the given cycle, V_{HIGH} is a maximum ripple voltage value, and V_{LOW} is a minimum ripple voltage value.

17. The method of Claim 15, wherein the controlling calculates the indication of the output current according to the formula:

$$V_{out}(t_4 - t_2)^2/2L(t_5 - t_2) - C(V_{HIGH} - V_{LOW})/(t_5 - t_2),$$

where V_{out} is the voltage of the output of the buck switching regulator circuit, C is a capacitance at the output of the buck switching regulator circuit, L is the inductance of the inductive storage element, t_2 is a time of the beginning of the second indication in the given cycle, t_5 is a time of the beginning of the first indication in the next cycle, V_{HIGH} is a maximum ripple voltage value, V_{LOW} is a minimum ripple voltage value, and t_4 is a time of the end of the second indication in

the given cycle.

18. The method of Claim 13, further comprising measuring the output current to provide the indication of the output current.

19. The method of Claim 13, wherein the controlling calculates the first threshold magnitude further in conformity with a difference between a voltage of the input of the buck switching voltage regulator circuit and the voltage of the output of the buck switching voltage regulator circuit.

20. The method of Claim 19, wherein the controlling calculates the first threshold magnitude according to the formula:

$$I_0^2 L/2C(V_{in} - V_{out}),$$

where V_{in} is a voltage of the input of the buck switching regulator circuit, V_{out} is the voltage of the output of the buck switching regulator circuit, C is a capacitance at the output of the buck switching regulator circuit, L is the inductance of the inductive storage element, and I_0 is the indication of the output current.

21. The method of Claim 13, wherein the buck switching voltage regulator circuit is operating in a continuous conduction mode and the indication of output current is a difference between a current delivered to the output of the buck switching voltage

regulator circuit and a minimum current in the inductive storage element.

22. The method of Claim 13, wherein the controlling calculates the second threshold magnitude from the voltage of the output of the buck switching voltage regulator circuit and a voltage of the input of the buck switching voltage regulator circuit.

23. The method of Claim 22, wherein the controlling calculates the second threshold magnitude according to the formula:

$$V_{HIGH} = V_{MIN} + (V_{MAX} - V_{MIN})V_{out}/V_{in},$$

where V_{in} is a voltage of the input of the buck switching regulator circuit, V_{out} is the voltage of the output of the buck switching regulator circuit, V_{HIGH} is a maximum ripple voltage value, and V_{LOW} is a minimum ripple voltage value.

24. A method for regulating the output voltage of a buck switching voltage regulator circuit, comprising:

first comparing a voltage of an output of the buck switching voltage regulator circuit to a first threshold magnitude;

second comparing the voltage of the output of the buck switching voltage regulator circuit to a second threshold magnitude, wherein the second threshold magnitude is greater than the first threshold magnitude;

coupling an inductive storage element between an input of

the buck switching voltage regulator circuit and the output of the buck switching voltage regulator circuit when the first comparing indicates that the voltage of the output of the buck switching voltage regulator circuit does not exceed the first threshold magnitude;

coupling the inductive storage element and between the output of the buck switching voltage regulator circuit and a return path of the output of the switching voltage regulator circuit when the second comparing indicates that the voltage of the output of the buck switching voltage regulator circuit exceeds the second threshold magnitude; and

generating the first threshold magnitude as a waveform at a rate greater than or equal to a switching period of the switching circuit, wherein the first indication is generated repetitively to control a start of the switching period, and wherein the waveform is generated such that the first indication occurs earlier in time within the switching period as an output current provided by the output of the buck switching voltage regulator circuit to a load increases and occurs later in time within the switching period as the output current decreases.

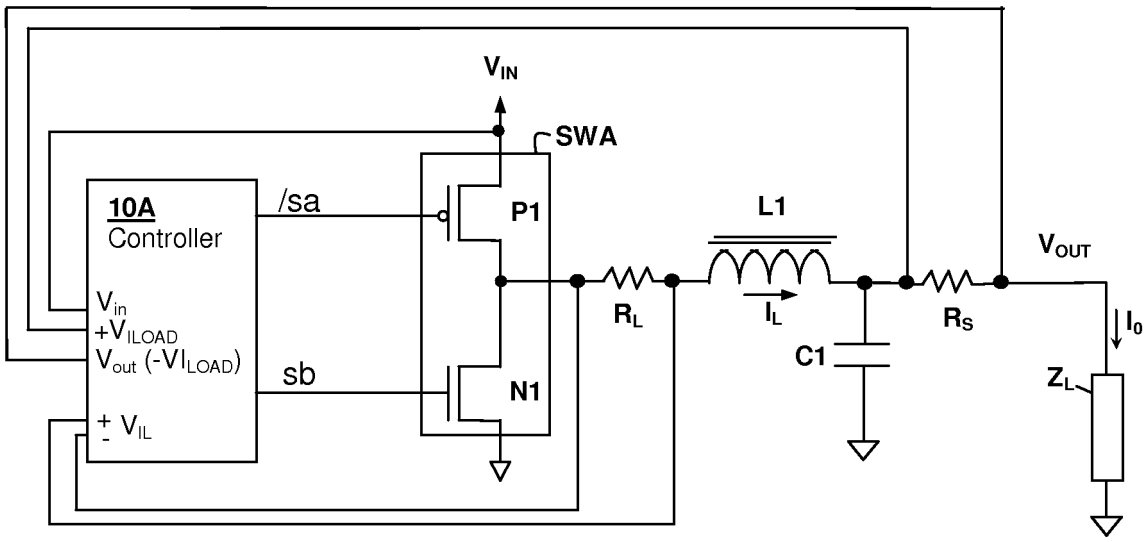
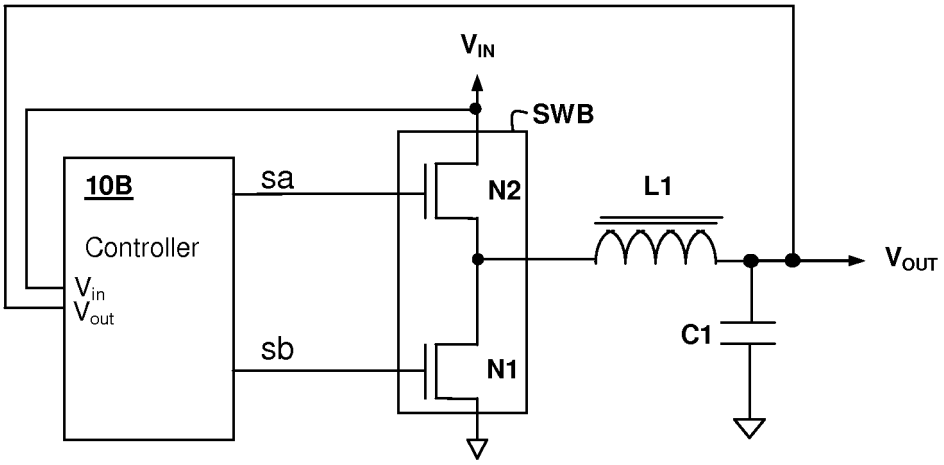

V_{IN}
SWA
10A
Controller
V_{in}
$+V_{ILOAD}$
V_{out} ($-VI_{LOAD}$)
$\pm$ V_{IL}
/sa
sb
P1
N1
L1
R_L
I_L
C1
R_S
V_{OUT}
I_0
Z_L

Fig. 1A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V_{in}
V_{out}
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L1
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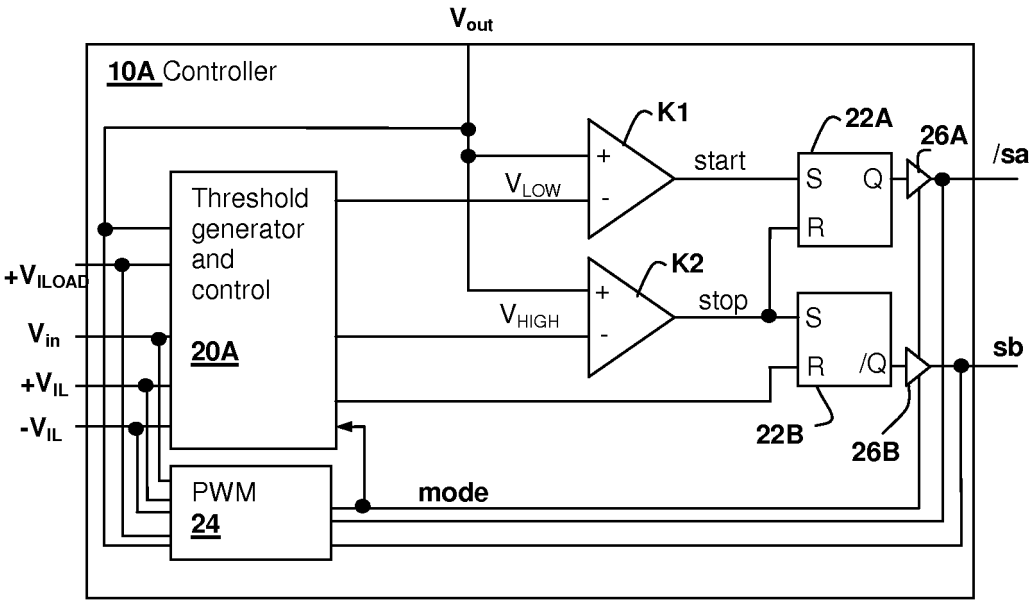
Fig. 1B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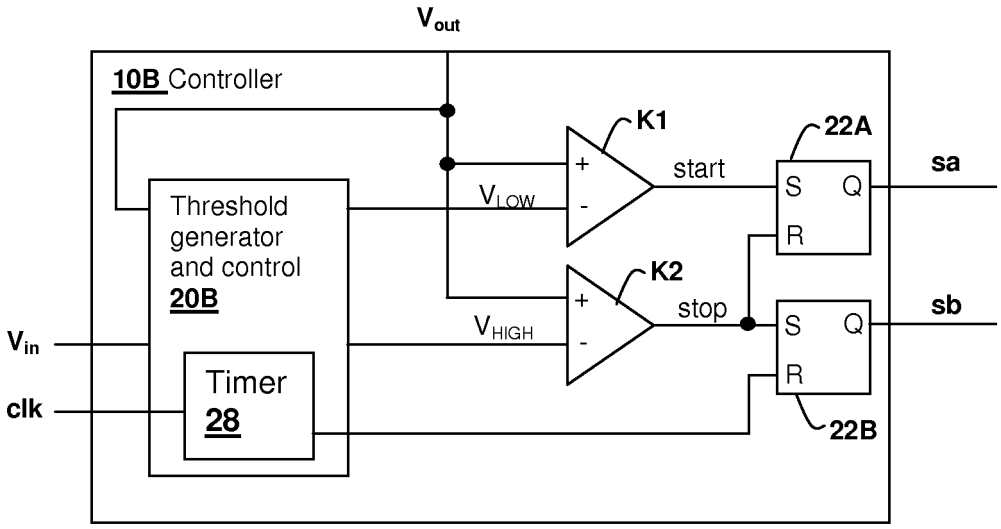
10A Controller
K1
22A
26A
/sa
start
S
Q
R
VLOW
+
-
Threshold generator and control
20A
+VILOAD
Vin
+VIL
-VIL
K2
stop
VHIGH
S
R
/Q
sb
22B
26B
PWM
24
mode

Fig. 2A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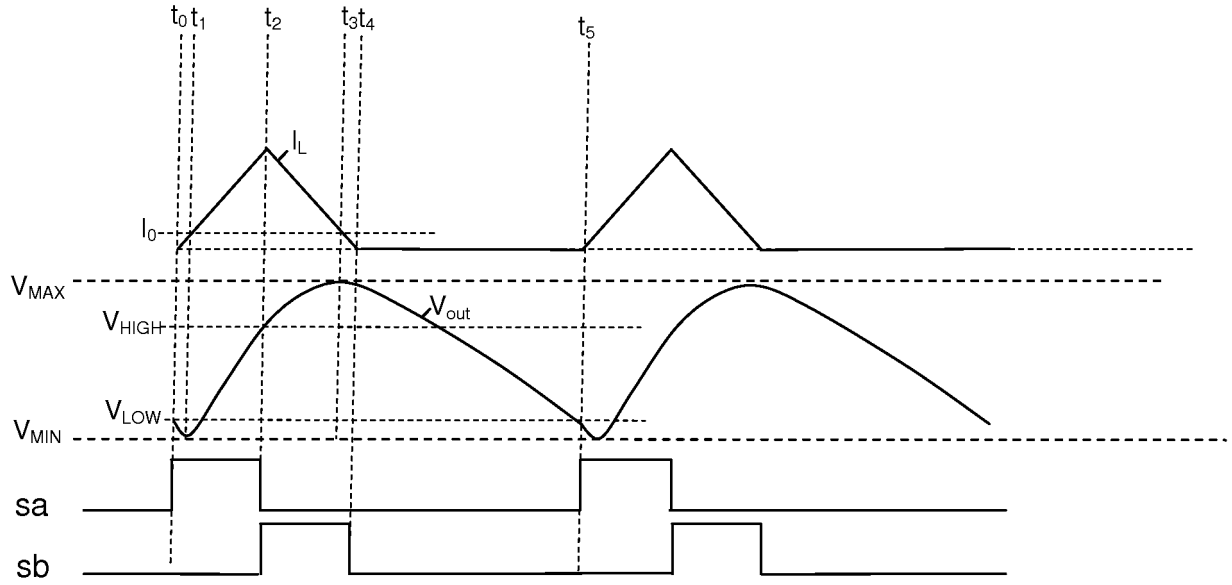
10B Controller
K1
22A
sa
start
S
Q
R
VLOW
+
-
Threshold generator and control
20B
K2
stop
sb
VHIGH
Vin
clk
Timer
28
22B

Fig. 2B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t2
t3 t4
t5
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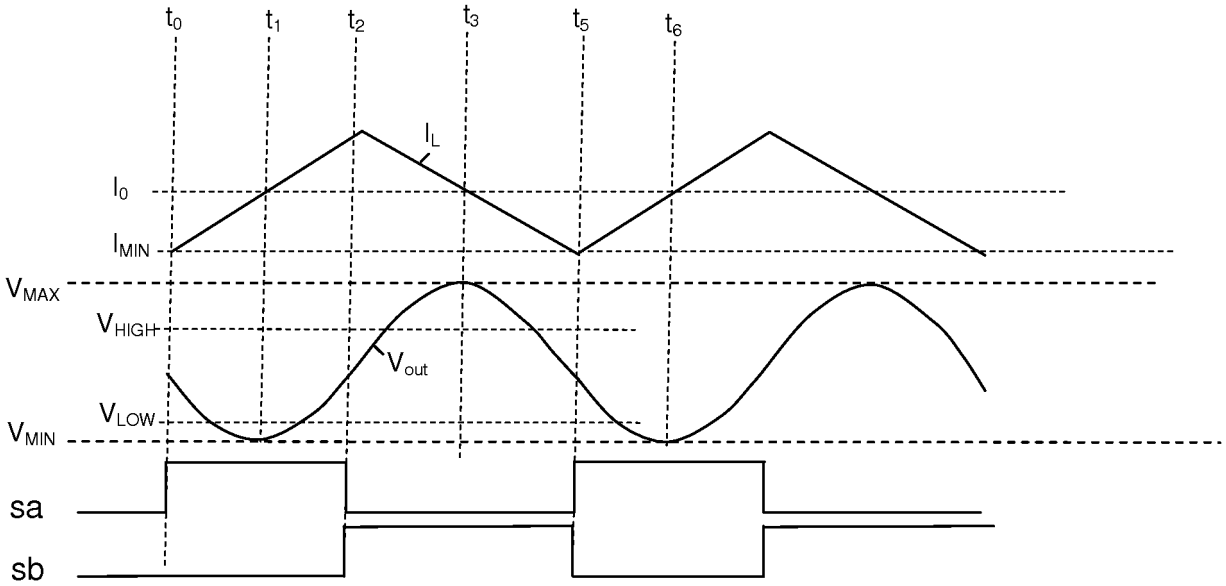
I0
VMAX
VHIGH
Vout
VLOW
VMIN
sa
sb

Fig. 3A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t1
t2
t3
t5
t6
IL
I0
IMIN
VMAX
VHIGH
Vout
VLOW
VMIN
sa
sb

Fig. 3B

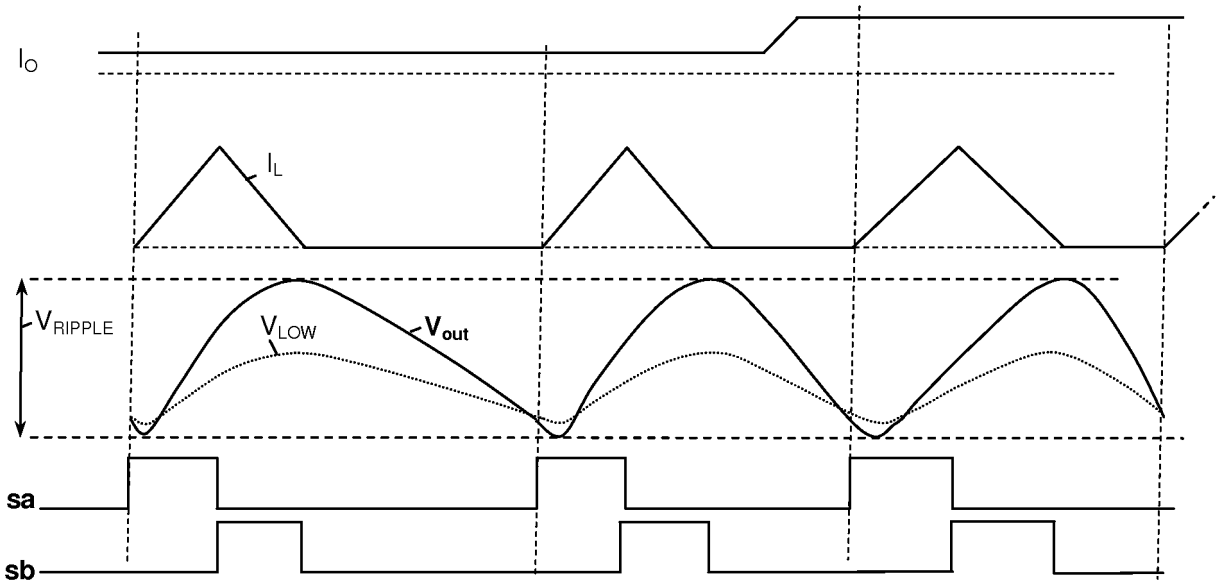

Fig. 4A

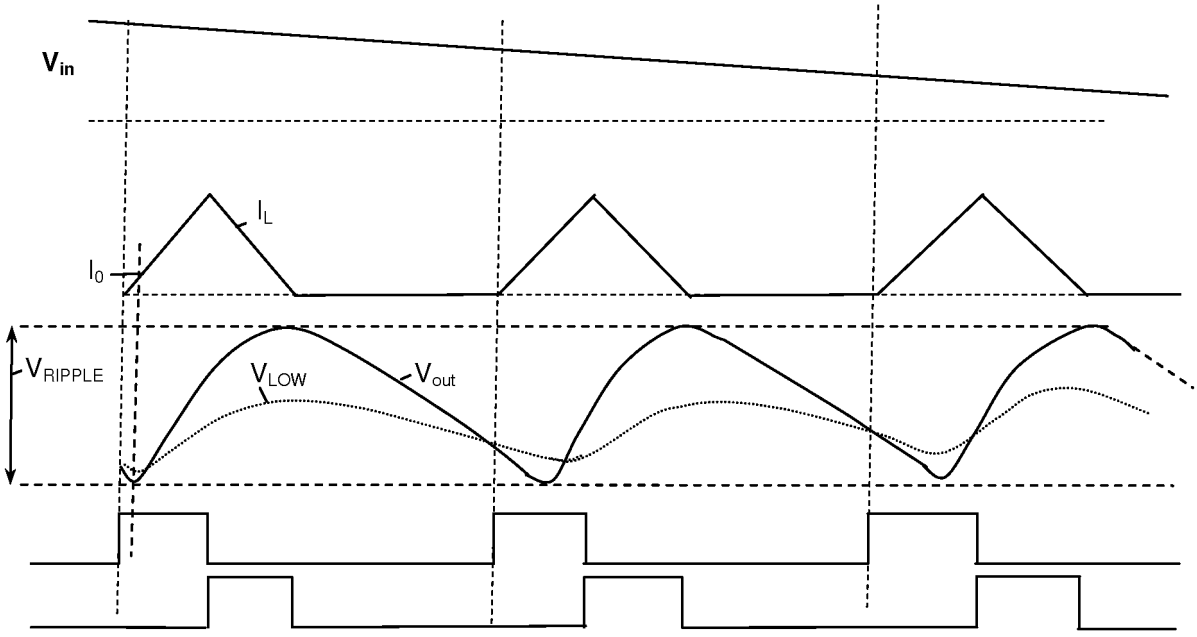

Fig. 4B

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2009/048016

A. CLASSIFICATION OF SUBJECT MATTER
INV. H02M3/156

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H02M G05F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, COMPENDEX, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	ZHAO J ET AL: "Steady-state and dynamic analysis of a buck converter using a hysteretic PWM control" POWER ELECTRONICS SPECIALISTS CONFERENCE, 2004. PESC 04. 2004 IEEE 35T H ANNUAL AACHEN, GERMANY 20-25 JUNE 2004, PISCATAWAY, NJ, USA,IEEE, US, 20 June 2004 (2004-06-20), pages 3654-3658Vol.5, XP010738297 ISBN: 978-0-7803-8399-9 page 3654 - page 3656 ----- -/--	1-24

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
10 August 2009	25/08/2009

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Braccini, Roberto

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2009/048016

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	FENG SU ET AL: "Ultra Fast Fixed-Frequency Hysteretic Buck Converter With Maximum Charging Current Control and Adaptive Delay Compensation for DVS Applications" IEEE JOURNAL OF SOLID-STATE CIRCUITS, IEEE SERVICE CENTER, PISCATAWAY, NJ, US, vol. 43, no. 4, 1 April 2008 (2008-04-01), pages 815-822, XP011206705 ISSN: 0018-9200 page 816 - page 818	1-24
A	WO 01/84697 A (INTERSIL CORP [US]; MURATOV VOLODYMYR [US]; HODGINS ROBERT [US]; JOCHU) 8 November 2001 (2001-11-08) page 4, line 32 - page 7, line 3; figures 1a-4	1-24
P,A	WONG L K ET AL: "Steady state analysis of hysteretic control buck converters" POWER ELECTRONICS AND MOTION CONTROL CONFERENCE, 2008. EPE-PEMC 2008. 13TH, IEEE, PISCATAWAY, NJ, USA, 1 September 2008 (2008-09-01), pages 400-404, XP031343605 ISBN: 978-1-4244-1741-4 the whole document	1-24

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2009/048016

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
WO 0184697 A	08-11-2001	AU 6112601 A	12-11-2001
		CN 1430806 A	16-07-2003
		CN 101277062 A	01-10-2008
		DE 10196149 T0	22-05-2003
		TW 533660 B	21-05-2003