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(54) **Title**: UNDERSHOOT REDUCTION

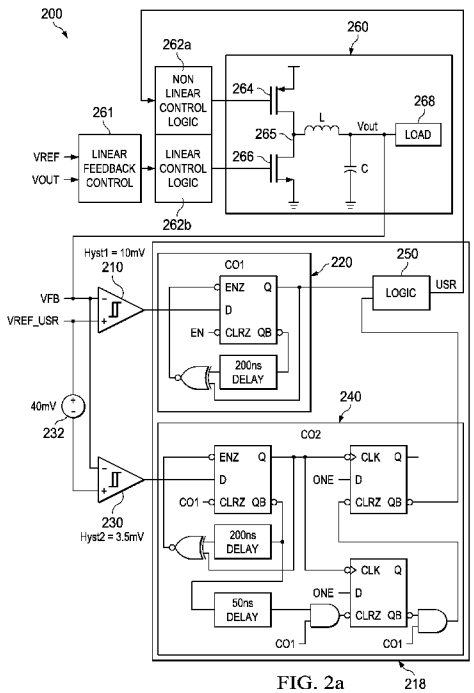

FIG. 2a

(57) **Abstract**: In described examples, undershoot reduction circuitry includes a first comparator (210), a second comparator (230), and a controller (218). The first comparator (210) is operable for comparing an indication of a power supply voltage output against a first threshold. The second comparator (230) is operable for comparing an indication of the power supply voltage output against a second threshold. The controller (218) is operable for generating a first power control signal USR to raise the power supply voltage output when the indication of the power supply voltage output has a first slope and crosses the first threshold and to lower the power supply voltage output when the indication of the power supply voltage output has an opposite slope and crosses the second threshold.

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UNDERSHOOT REDUCTION

BACKGROUND

[0001] Many applications include integrated circuits that are powered by power supplies having voltage regulation. Some regulators (such as direct-current-to-direct-current regulators) include undershoot reduction circuitry to achieve regulation of power supply outputs. For example, when the voltage of a power supply output falls below a certain reference voltage, the undershoot reduction circuitry turns on a nonlinear control fast control loop for applying power to raise the voltage of a power supply output. The nonlinear fast control loop is turned off by the undershoot reduction circuitry after the output voltage rises above the reference voltage plus a hysteresis value of the comparator used. This approach often results in an overshoot of the output voltage due to hysteresis and extra energy dissipated in the inductor that is part of the power supply output LC filter. The overshoot problem is compounded in multiphase regulators where more than one such regulated phase is turned on in response to increased load demands.

SUMMARY

[0002] In described examples, undershoot reduction circuitry includes a first comparator, a second comparator, and a controller. The first comparator is operable for comparing an indication of an output (e.g. a, regulated power supply voltage output) against a first threshold. The second comparator is operable for comparing an indication of the regulated power supply voltage output against a second threshold. The controller is operable for generating a first power control signal to raise the power supply voltage output when the indication of the power supply voltage output has a first slope and crosses the first threshold and to lower the power supply voltage output when the indication of the power supply voltage output has an opposite slope and crosses the second threshold.

BRIEF DESCRIPTION OF THE DRAWINGS

[0003] FIG. 1 shows an illustrative electronic device of example embodiments.

[0004] FIG. 2a is a schematic of an independent threshold undershoot reducer of example embodiments.

[0005] FIG. 2b is a schematic of an independent threshold undershoot reducer-controlled

multiphase buck converter of example embodiments.

[0006] FIG. 3 is a timing diagram of independent thresholds of the independent threshold undershoot reducer of FIG. 2a.

[0007] FIG. 4 is a timing diagram of a simulation of independent thresholds of the independent threshold undershoot reducer of FIG. 2a using "negative" hysteresis of example embodiments.

[0008] FIG. 5 is a timing diagram of a simulation of independent thresholds of the independent threshold undershoot reducer of FIG. 2a using a single comparator of example embodiments.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0009] A system can be a sub-system of yet another system. If a first device couples to a second device, that connection can be made through a direct electrical connection, or through an indirect electrical connection via other devices and connections. The term "calibration" can include the meaning of the word "test." The term "input" can mean either a source or a drain (or even a control input such as a gate where context indicates) of a PMOS (positive-type metal oxide semiconductor) or NMOS (negative-type metal oxide semiconductor) transistor. The term "pulse" can mean a portion of waveforms, such as "squarewave" or "sawtooth" waveforms.

[0010] FIG. 1 shows an illustrative computing device 100 of example embodiments. For example, the computing device 100 is, or is incorporated into, or is coupled (e.g., connected) to an electronic system 129, such as a computer, electronics control "box" or display, communications equipment (including transmitters or receivers), or any type of electronic system operable to process information.

[0011] In some embodiments, the computing device 100 includes a megacell or a system-on-chip (SoC) which includes control logic such as a CPU 112 (central processing unit), a storage 114 (e.g., random access memory (RAM)) and a power supply 110. For example, the CPU 112 can be a CISC-type (complex instruction set computer) CPU, RISC-type CPU (reduced instruction set computer), MCU-type (microcontroller unit), or a digital signal processor (DSP). The storage 114 (which can be memory such as on-processor cache, off-processor cache, RAM, flash memory, or disk storage) stores one or more software applications 130 (e.g., embedded applications) that, when executed by the CPU 112, perform any suitable function associated with the computing device 100.

[0012] The CPU 112 includes memory and logic that store information frequently accessed from the storage 114. The computing device 100 is often controlled by a user using a UI (user

interface) 116, which provides output to and receives input from the user during the execution the software application 130. The output is provided using the display 118, indicator lights, a speaker and vibrations. The input is received using audio and/or video inputs (such as using voice or image recognition), and electrical and/or mechanical devices, such as keypads, switches, proximity detectors, gyros and accelerometers.

[0013] The CPU 112 and power supply 110 are coupled to I/O (input-output) port 128, which provides an interface that is configured to receive input from (and/or provide output to) networked devices 131. The networked devices 131 can include any device (including test equipment) capable of point-to-point and/or networked communications with the computing device 100. The computing device 100 is coupled to peripherals and/or computing devices, including tangible, non-transitory media (such as flash memory) and/or cabled or wireless media. These and other input and output devices are selectively coupled to the computing device 100 by external devices using wireless or cabled connections. For example, the storage 114 is accessible by the networked devices 131. The CPU 112, storage 114 and power supply 110 are also optionally coupled to an external power supply (not shown), which is configured to receive power from a power source (such as a battery, solar cell, "live" power cord, inductive field, fuel cell and capacitor).

[0014] The computing device 100 includes a power module 138. The power module 138 includes at least one regulator 110. The regulator 110 is operable for generating at least one voltage output that is protected by undershoot reducer 140. In the embodiment discussed below with respect to FIG. 2, the undershoot reducer 140 includes two comparators, in which each comparator has a separate voltage reference. The first comparator compares a regulated voltage (such as an indication of a power supply voltage output) against a first voltage reference when the regulated voltage has a negative-going slope. The second comparator compares a regulated voltage against a second voltage reference when the regulated voltage has a positive-going slope.

[0015] For example, the independent thresholding of the undershoot reducer 140 is used for avoiding potential problems associated with the fixed hysteresis of a single comparator. The degree of hysteresis of a given comparator is determined at the time of design and/or manufacture. In contrast, the independent thresholding permits designs having (e.g., virtual) negative hysteresis. For example, the negative hysteresis (e.g., provided by independent thresholds of two comparators) helps reduce wasted energy. Energy is conserved, such as by

reducing output overshoot voltages (where the corrected voltage exceeds a target voltage) and the undershoot voltages (where the overshot voltage drops substantially below the target voltage as the feedback control mechanism of the output voltage attempts to "zero in" on the target voltage) of the power module 138.

[0016] FIG. 2a is a schematic of an independent threshold undershoot reducer system of example embodiments. The independent threshold undershoot reducer system 200 is undershoot reduction circuitry such as the independent threshold undershoot reducer 140. The independent threshold undershoot reducer system 200 includes a first comparator 210, a first comparator latch 220, a second comparator 230, a second comparator latch 240, a state machine 218, and a power converter 260. Such included components are usually formed on a common substrate.

[0017] The first comparator 210 is coupled to voltage feedback (VFB) signal at the inverting input and is coupled to the undershoot reduction voltage reference (VREF_USR) at the non-inverting input. For example, the first comparator 210 has a hysteresis of 10 millivolts, which affects when the output of the first comparator 210 toggles in response to comparisons of the VFB and the VREF_USR the input signals. The comparator 210 is arranged to maintain any active high output for a selected delay (e.g., around 200 nanoseconds as shown in the example). The selected delay helps ensure that the signal USR is asserted for a duration at least as long as the selected delay.

[0018] The output of the first comparator 210 is coupled to an input of the first comparator latch 220 of the state machine 218. The first comparator latch 220 produces the first comparator output (CO1) signal in response to the output of the first comparator 210 as described below with reference to FIG. 3. The state of the first comparator latch 220 is initially set in response to an assertion of the Enable signal at a "clear-negative" pin of an internal latch of the first comparator latch 220.

[0019] The second comparator 230 is coupled to voltage feedback (VFB) signal at the inverting input and is coupled to the offset undershoot reduction voltage reference (offset VREF_USR) signal at the non-inverting input. The VREF_USR-OFFSET is offset downwards by 40 millivolts (or other such selected value) by the voltage source 232. For example, the second comparator 230 has a hysteresis of 3.5 millivolts, which affects when the output of the second comparator 230 toggles in response to comparisons of the VFB and the offset VREF_USR the input signals.

[0020] The second comparator can have a hysteresis that is the same as or is different from the hysteresis of the first comparator. In other example embodiments, the hysteresis of the first comparator 210 and the hysteresis of the second comparator 230 are both 10 millivolts. The comparator 230 is arranged to maintain minimum active high or low of signal C02 for selected delay (e.g., for at least 200 nanoseconds), which helps ensure that the signal USR is asserted for at least for selected delay time span.

[0021] The output of the second comparator 230 is coupled to an input of the second comparator latch 240 of the state machine 218. The second comparator latch 240 produces the second comparator output (CO2) signal in response to the output of the second comparator 230 as described below with reference to FIG. 3. Accordingly, state of the second comparator latch 240 is initially set in response the current state of the first comparator latch 220 (e.g., via signal CO1). The CO1 and CO2 signals are input to the logic 250 of the state machine 218, which generates the the undershoot reduction (USR) signal in accordance with the waveforms described below with reference to FIG. 3.

[0022] The USR signal is received by the non-linear control logic 262a, whereas a linear feedback control 261 circuit is responsive to the received voltage reference signal (Vref) and the power supply voltage output (Vout) to drive the linear control logic 262b. The non-linear control logic 262a and the linear control logic 262b are operable to drive power transistors 264 and 266 of power converter 260 in accordance of the values of the inductor L and the capacitor C and the respective signals received by the non-linear control logic 262a and the linear control logic 262b. The power transistor 264 is a "high-side" field-effect transistor (FET), whereas the power transistor 266 is a "low-side" FET. A first terminal of an inductor L is coupled between the power transistor 264 and the power transistor 266 at node 265. The logic 262 is operable for applying power to the inductor L or shunting power from the inductor L. A second terminal of the inductor L is coupled to the high side of capacitor C and to the output voltage node Vout. In operation, extra power is usually applied to the inductors L in response to the assertion of the signal USR by the non-linear control logic 262a.

[0023] A load (the amount of which usually varies during operation) is optionally coupled to the output voltage node Vout. The output voltage node of the power converter 260 is coupled to the respective inverting inputs of the first comparator 210 and the second comparator 230 as signal VFB.

[0024] The second comparator latch 240 is responsive to the CO1 signal output by the first comparator latch 220. Accordingly, the first comparator 210 is operable for performing a first comparison when the signal VFB has a first (e.g., negative) slope and the second converter 230 is operable for performing a second comparison when the signal VFB has a second (e.g., positive) slope. For example, the two comparisons (each using a separate, predetermined threshold) allow the timing of the undershoot reduction circuitry for the output voltage to be determined independently of the timing of the command to increase the output voltage.

[0025] FIG. 2b is a schematic of an independent threshold undershoot reducer-controlled multiphase buck converter of example embodiments. The independent threshold undershoot reducer-controlled multiphase buck converter 270 includes a logic 272 block that is similar to the non-linear control logic 262a discussed above with respect to FIG. 2a.

[0026] The independent threshold undershoot reducer system logic 272 block is coupled to a number "n" of multiphase generators such as phase generator 274, phase generator 276, and phase generator 278. Phase generator 274 includes a high-side/low-side power transistor stack and an inductor L1, phase generator 276 includes a high-side/low-side power transistor stack, and phase generator 278 includes a high-side/low-side power transistor stack and an inductor Ln. In various embodiments, a multiphase buck converter includes two or more phase generators. The logic 272 block is operable to provide non-linear control separately to each of the phase generators 274, 276, and 278. The output of each phase generator is coupled (e.g., wire-ORed together) to the load 280.

[0027] FIG. 3 is a timing diagram of independent thresholds of the independent threshold undershoot reducer of FIG. 2a. Timing diagram 300 includes the signals VFB 310, first reference voltage (VREF1) 320, second reference voltage (VREF2) 330, CO1 (first comparator output) 340, CO2 (second comparator output) 350, and USR 360. The signals VFB 310, CO1 340, CO2 350, and USR 360 are similar to the respective signals as discussed above with respect to FIG. 2. The signal VREF1 320 is similar to the VREF_USR (described above with reference to FIG. 2), whereas the signal VREF2 330 is similar to the offset VREF_USR (also described above with reference to FIG. 2).

[0028] Signal VFB 310 is illustrated as having a negative slope portion 310a, an inflexion point 312, and a positive slope portion 310b. The first comparator 210 is operable for comparing the VFB 310 signal with the VREF1 320 signal. At time 342, the (falling) level of the signal

VFB 310 falls below the level of the VREF1 320 signal. In response, the CO1 340 signal, and the USR 360 signal in turn, is asserted at (e.g., around) time 342. The assertion of the USR 360 signal causes the power converter 260 to apply power to the inductor such that, after a period of latency, the falling voltage of signal VFB eventually recovers at inflection point 312 and starts to rise again (as shown by a positive slope portion 310b of signal VFB 310).

[0029] At time 352, the (falling) level of the signal VFB 310 falls below the level of the VREF2 330 signal. The value of VREF2 330 is equal to the value of VREF1 320 minus the offset voltage (e.g., which provides a virtual "negative hysteresis") such as provided by voltage source 232. In response to the level of the signal VFB 310 falling below the level of the VREF2 330 signal and the asserted state of the CO1 340 signal, the CO2 350 signal is asserted at (e.g., around) time 342.

[0030] In the event that the VFB 310 signal does not fall below the level of VREF2 330 signal , the USR signal 360 is asserted and then de-asserted (e.g., by the state machine 218) when the VFB 310 signal rises above the VREF1 320 signal plus the hysteresis 312. The latch 220 ensures a selected minimum active duration (such as 200ns) for the USR 360 signal.

[0031] At time 354, the (rising) level of the signal VFB 310 rises above the level of the VREF2 330 signal plus the hysteresis value 322 of the second comparator (which can be the same as or different from the hysteresis value 312 of the first comparator). In response to the level of the signal VFB 310 rising above the level of the VREF2 330 signal plus the hysteresis value 322, the CO2 350 signal is deasserted (e.g., driven low) at time 354. Also at time 354, the signal USR 360 is deasserted. Deasserting the signal USR 360 in response to the VREF2 signal (e.g., in place of deasserting the signal USR in response to the VREF1 signal) allows the USR 360 signal to be deasserted at an earlier time (e.g., time 354 as compared with time 344). Deasserting the signal USR 360 at an earlier time helps to avoid potential overshoot of the regulated output voltage (as discussed below with respect to FIG. 4 and FIG. 5), which saves power.

[0032] At time 344, the (rising) level of the signal VFB 310 rises above the level of the VREF1 320 signal plus the hysteresis value 312 of the first comparator. In response to the level of the signal VFB 310 rising above the level of the VREF1 320 signal plus the hysteresis value 312, the CO1 340 signal is deasserted (e.g., driven low) at time 354. For example, the deassertion of the CO1 340 signal affects the control signals of internal latches of the second

comparator latch 240, such that the cycle of the assertion and deassertion of the signal USR 360 is repeated cyclically, as discussed below with respect to FIG. 4 and FIG. 5.

[0033] FIG. 4 is a timing diagram of a simulation of a first set of independent thresholds of the independent threshold undershoot reducer of FIG. 2a. Timing diagram 400 includes the regulated target voltage (RTV) signal 410, first reference voltage (VREF1) 420, second reference voltage (VREF2) 430, VFB 440, and USR 450. The RTV signal 410 is a target voltage of undershoot reducer circuitry, such as undershoot reducer 140. The signals VREF1 420, VREF2 430, VFB 440, and USR 450 are similar to the respective signals as discussed above with respect to FIG. 3. Simulation 400 generally illustrates the operation of undershoot reduction circuitry such as described above with respect to FIG. 2.

[0034] The simulation 400 operates using an undershoot reduction system 200 having a USR couple-power (e.g., "turn on" power) threshold 472 that is higher than the USR decouple-power (e.g., "turn off" power) threshold 474. The couple-power threshold 472 being higher than the USR decouple-power threshold 474 provides virtual (e.g., mimics the effects of) "negative hysteresis" that would apparently occur if a single comparator was being used by the undershoot reduction system 200.

[0035] The signal RTV 410 is a target voltage of undershoot reducer circuitry, which regulates the signal VFB 440. The signal VFB 440 is regulated such that the level of signal VFB 440 is maintained at a level relatively close to, but not exceeding, the level of RTV 410 (which here is substantially constant, but can vary in various applications).

[0036] Initially, the signal VFB 440 has a negative slope. At time 450, the signal VFB 440 crosses (e.g., falls below) the signal VREF1 420 (at couple-power threshold 472). When the signal VFB 440 falls below the signal VREF1 420, the signal USR 450 is asserted, which causes the power converter (e.g., that generates the signal VFB 440) to apply power to the inductor L. Due to the nature of the power converter (e.g., a buck converter), the application of power to the inductor does not immediately cause a rise in the voltage the signal VFB 440. Accordingly, the signal VFB 440 falls below the signal VREF2 430 and subsequently the signal VFB 440 starts to rise (now having a positive slope) due to the application of power applied in response to the assertion of the signal USR 450.

[0037] At time 452, the signal VFB 440 crosses (e.g., rises above) the signal VREF2 430 (at decouple-power threshold 474). When the signal VFB 440 rises above the signal VREF2 430,

the signal USR 450 is deasserted, which causes the power converter to decouple the applied power from the inductor L. Due to the nature of the power converter, the decoupling of the applied power to the inductor does not immediately cause a reduction in the voltage the signal VFB 440. Accordingly, the signal VFB 440 continues to rise, rising above the signal VREF1 420, and approaches the signal RTV 410. Because of the decoupling of applied power from the energy elements of the power converter at time 452, the signal VFB 440 starts to fall as the voltage level of the signal VFB 440 reaches a voltage level approximately equal to the voltage level of RTV 410.

[0038] At time 454, the signal VFB 440 falls below the signal VREF1 420. When the signal VFB 440 falls below the signal VREF1 420, the signal USR 450 is asserted, which again causes the power converter to apply power to the inductor L. Due to the nature of the power converter, the application of power to the inductor does not immediately cause a rise in the voltage the signal VFB 440. Accordingly, the signal VFB 440 falls below the signal VREF2 430 and subsequently the signal VFB 440 starts to rise (now having a positive slope) due to the application of power applied in response to the assertion of the signal USR 450.

[0039] At time 456, the signal VFB 440 rises above the signal VREF2 430. When the signal VFB 440 rises above the signal VREF2 430, the signal USR 450 is deasserted, which causes the power converter to decouple the applied power from the inductor L.

[0040] At time 458, the signal VFB 440 falls below the signal VREF2 430 (without first rising above the signal VREF1 420) The signal VFB 440 can fall below the signal VREF2 420 (e.g., without first rising above the signal VREF1 420), such as due to an instantaneous increase in load (and no coupled power to the inductor L). When the signal VFB 440 falls below the signal VREF2 430 (at time 458), the signal USR 450 is asserted, which again causes the power converter to apply power to the inductor L. Due to the nature of the power converter, the application of power to the inductor does not immediately cause a rise in the voltage the signal VFB 440. Accordingly, the signal VFB 440 falls below the signal VREF2 430 and subsequently the signal VFB 440 starts to rise (now having a positive slope) due to the application of power applied in response to the assertion of the signal USR 450.

[0041] At time 460, the signal VFB 440 rises above the signal VREF2 430. When the signal VFB 440 rises above the signal VREF2 430, the signal USR 450 is again deasserted, which causes the power converter to decouple the applied power from the inductor L. The signal VFB

440 continues to rise, rising above the signal VREF1 420, and approaches the signal RTV 410. Because of the decoupling of applied power from the energy elements of the power converter at time 452, the signal VFB 440 starts to fall as the voltage level of the signal VFB 440 reaches a voltage level approximately equal to the voltage level of RTV 410.

[0042] At time 462, the signal VFB 440 falls below the signal VREF1 420 and in response the signal USR 450 is asserted, which again causes the power converter to apply power to the inductor L. The signal VFB 440 falls below the signal VREF2 430 and subsequently the signal VFB 440 starts to rise.

[0043] At time 464, the signal VFB 440 rises above the signal VREF2 430 and in response the signal USR 450 is deasserted, which causes the power converter to decouple the applied power from the inductor L. The signal VFB 440 continues to rise, rising above the signal VREF1 420, and approaches the level of the signal RTV 410 where the signal VFB 440 again starts to fall.

[0044] At time 466, the signal VFB 440 falls below the signal VREF1 420 and in response the signal USR 450 is asserted, which again causes the power converter to apply power to the inductor L. The signal VFB 440 falls below the signal VREF2 430 and subsequently the signal VFB 440 starts to rise.

[0045] At time 468, the signal VFB 440 rises above the signal VREF2 430 and in response the signal USR 450 is deasserted, which causes the power converter to decouple the applied power from the inductor L. Again, due to changing load factors for example, the signal VFB 440 starts to fall without having reached the voltage level of the signal VREF1 420.

~~[0046]~~ At time 470, signal VFB 440 falls below the signal VREF2 430 (without having risen above the level of the signal VREF1 420), and in response the signal USR 450 is asserted, which again causes the power converter to apply power to the inductor L. Subsequently, the signal VFB 440 continues to fall and then starts to rise (now having a positive slope) due to the application of power applied in response to the assertion of the signal USR 450.

[0047] Accordingly, the logic of the state machine 218 is responsive to assert the signal USR 450 in response to the signal VFB 440 falling below the signal VREF1 420. The logic of the undershoot voltage reducer is also responsive to assert the signal USR 450 in response to signal VFB 440 falling below the signal VREF2 430 without first having risen above the level of the signal VREF1 420.

[0048] FIG. 5 is a timing diagram of a simulation of independent thresholds of the independent

threshold undershoot reducer of FIG. 2a using a single comparator of example embodiments. Timing diagram 500 includes the signals maximum voltage (RTV) 510, first reference voltage (VREF1) 520, second reference voltage (VREF2) 530, VFB 540, and USR 550. The signal RTV 510 is a target voltage of undershoot reducer circuitry, such as undershoot reducer 140. The signals VREF1 520, VREF2 530, VFB 540, and USR 550 are similar to the respective signals as discussed above with respect to FIG. 3. Simulation 500 generally illustrates the operation of undershoot reduction circuitry such as described above with respect to FIG. 2.

[0049] In contrast to the simulation 400 using the undershoot reduction system 200, the simulation 500 operates using an undershoot reduction system having a USR decouple-power threshold 574 that is higher than the USR couple-power threshold 572. The decouple-power threshold 574 being higher than the USR couple-power threshold 572 provides virtual (e.g., mimics the effects of) additional "positive hysteresis" that would appear to occur if (e.g., only) a single comparator were used by the undershoot reduction system.

[0050] The signal RTV 510 is a target voltage of undershoot reducer circuitry. The signal VFB 540 is regulated such that the level of signal VFB 540 is maintained at a level relatively close to the level of RTV 510 (which here is substantially constant, but can vary in various embodiments).

[0051] Initially, the signal VFB 540 has a negative slope. At time 550, the signal VFB 540 falls below the signal VREF2 530 (at couple-power threshold 572). When the signal VFB 540 falls below the signal VREF2 530, the signal USR 550 is asserted, which causes the power converter (e.g., that generates the signal VFB 540) to apply power to the inductor L. Due to the nature of the power converter (e.g., a buck converter), the application of power to the inductor does not immediately cause a rise in the voltage the signal VFB 540. Accordingly, the signal VFB 540 continues to fall but recovers (now having a positive slope) due to the application of power applied in response to the assertion of the signal USR 550.

[0052] At time 552, the signal VFB 540 rises above the signal VREF1 520 (at decouple-power threshold 574). When the signal VFB 540 rises above the signal VREF2 5200, the signal USR 550 is deasserted, which causes the power converter to decouple the applied power from the inductor L. Due to the nature of the power converter, the decoupling of the applied power to the inductor does not immediately cause a reduction in the voltage the signal VFB 540. Accordingly, the signal VFB 540 continues to rise and approaches the signal RTV 510. Because

of the decoupling of applied power from the energy elements of the power converter at time 552, the signal VFB 540 starts to fall as the voltage level of the signal VFB 540 reaches a voltage level approximately equal to the voltage level of RTV 510.

[0053] At time 554, the signal VFB 540 falls below the signal VREF1 520 firstly, and then the signal VREF2 530 secondly. When the signal VFB 540 falls below the signal VREF2 530, the signal USR 550 is asserted, which again causes the power converter to apply power to the inductor L. Accordingly, the signal VFB 540 continues to fall but then recovers (now having a positive slope) due to the application of power applied in response to the assertion of the signal USR 550. Again, due to changing load factors for example, the signal VFB 540 starts to fall again without having reached the voltage level of the signal VREF2 530. As the application of power applied in response to the assertion of the signal USR 550 continues, the signal VFB 540 (after some latency) recovers and begins to rise again. The signal USR 550 remains asserted during this time (e.g., from time 554 to time 556).

[0054] At time 556, the signal VFB 540 rises above the signal VREF1 520. When the signal VFB 540 rises above the signal VREF1 520, the signal USR 550 is deasserted, which causes the power converter to decouple the applied power from the inductor L. Accordingly, the signal VFB 540 approaches the level of the signal RTV 510 and subsequently starts to fall.

[0055] At time 558, the signal VFB 540 falls below the signal VREF2 530. When the signal VFB 540 falls below the signal VREF2 520, the signal USR 550 is asserted, which again causes the power converter to apply power to the inductor L. Accordingly, the signal VFB 540 falls below the signal VREF2 530 and subsequently the signal VFB 540 starts to rise (now having a positive slope) due to the application of power applied in response to the assertion of the signal USR 550.

[0056] At time 560, the signal VFB 540 rises above the signal VREF1 520. When the signal VFB 540 rises above the signal VREF1 520, the signal USR 550 is deasserted, which causes the power converter to decouple the applied power from the inductor L. Accordingly, the signal VFB 540 approaches the level of the signal RTV 510 and subsequently starts to fall.

[0057] At time 562, the signal VFB 540 falls below the signal VREF2 530. When the signal VFB 540 falls below the signal VREF2 520, the signal USR 550 is asserted, which again causes the power converter to apply power to the inductor L. Accordingly, the signal VFB 540 falls below the signal VREF2 530 and subsequently the signal VFB 540 starts to rise (now having a

positive slope) due to the application of power applied in response to the assertion of the signal USR 550. Again, due to changing load factors for example, the signal VFB 540 starts to fall without having reached the voltage level of the signal VREF2 530. As the application of power applied in response to the assertion of the signal USR 550 continues, the signal VFB 540 (after some latency) recovers and begins to rise again. The signal USR 550 remains asserted during this time (e.g., from time 562 to time 564).

[0058] Accordingly, the state machine of the undershoot voltage reducer (e.g., state machine 250) is responsive to assert the signal USR 550 in response to the signal VFB 540 falling below the signal VREF1 520 and to assert the signal USR 550 in response to signal VFB 540 falling below the signal VREF2 530 without having risen above the level of the signal VREF1 520.

[0059] In an embodiment, a controller (e.g., such as a microcontroller or a digital signal processor) is used to control one or more attributes of the undershoot reduction circuitry. Some of the variables are software programmable, which allows more flexibility for implementing the disclosed control techniques and provides an enhanced ability to adaptively adjust to dynamically changing conditions for optimized system performance. Other variables can be programmed during the manufacturing process (e.g., to compensate for lot characteristics) by trimming trim-able resistors to increase operational stability and accuracy.

[0060] In various embodiments, the above described components can be implemented in hardware or software, internally or externally, and share functionality with other modules and components as illustrated herein. For example, the switching portions of the power converter can be implemented outside of a device and/or substrate upon which the undershoot reduction circuitry is formed.

[0061] Modifications are possible in the described embodiments, and other embodiments are possible, within the scope of the claims.

CLAIMS

What is claimed is:

1. A circuit for voltage undershoot control, comprising:

a first comparator operable for comparing an indication of a power supply voltage output against a first threshold;

a second comparator operable for comparing an indication of the power supply voltage output against a second threshold; and

a controller operable for generating a first power control signal to raise the power supply voltage output when the indication of the power supply voltage output crosses the first threshold when the power supply voltage output has a first slope and to lower the power supply voltage output when the indication of the power supply voltage output crosses the second threshold when the power supply voltage output has a second slope opposite in direction to the first slope.

2. The circuit of claim 1, wherein the first threshold is higher than the second threshold.

3. The circuit of claim 2, wherein the controller is operable for generating a second power control signal to raise the power supply voltage when the indication of the power supply voltage output crosses the second threshold when the power supply voltage output has the first slope and when no signal to raise to raise the power supply voltage has been asserted.

4. The circuit of claim 3, wherein the first power control signal and the second power control signal are the same power control signal.

5. The circuit of claim 1, wherein the first slope is a negative slope and the second slope is a positive slope.

6. The circuit of claim 1, wherein the second threshold is lower than the first threshold.

7. The circuit of claim 6, wherein the first power control signal is generated to raise the power supply voltage output for at least a selected period of time.

8. The circuit of claim 1, wherein the first power control signal is responsive to a first comparator latch for latching an output of the first comparator and is responsive to a second comparator latch for latching an output of the second comparator.

9. The circuit of claim 8, wherein the controller includes a state machine responsive to signals of the first and second comparator latches.

10. The circuit of claim 1, wherein the first threshold is higher than the second threshold, wherein the first threshold is equal to a first voltage reference signal, and wherein the second

threshold is equal to the sum of a second voltage reference signal and a hysteresis voltage of the second comparator.

11. A voltage regulation system, comprising:

a power supply operable for generating a power supply voltage output;

a first comparator operable for comparing an indication of the power supply voltage output against a first threshold;

a second comparator operable for comparing an indication of the power supply voltage output against a second threshold; and

a controller operable for signaling the power supply to raise the power supply voltage output when the indication of the power supply voltage output crosses the first threshold when the power supply voltage output has a first slope and to lower the power supply voltage output when the indication of the power supply voltage output crosses the second threshold when the power supply voltage output has a second slope opposite in direction to the first slope.

12. The system of claim 11, wherein the power supply includes a multiphase buck converter.

13. The system of claim 11, wherein the power supply is operable for raising the power supply voltage output by coupling power to an inductor and for lowering the power supply voltage output by decoupling power from the inductor.

14. The system of claim 13, wherein power is coupled to the inductors by closing a respective FET (field-effect transistor) transistor and power is decoupled from the inductor by opening the respective FET transistor.

15. The system of claim wherein the first threshold is a undershoot reference voltage and wherein the second threshold is equal to the first threshold voltage minus a voltage offset plus a hysteresis value of the second comparator.

16. A method, comprising:

comparing an indication of a power supply voltage output against a first threshold;

comparing an indication of the power supply voltage output against a second threshold; and

generating a power control signal to raise the power supply voltage output when the indication of the power supply voltage output crosses the first threshold when the power supply voltage output has a first slope and to lower the power supply voltage output when the indication of the power supply voltage output crosses the second threshold when the power supply voltage

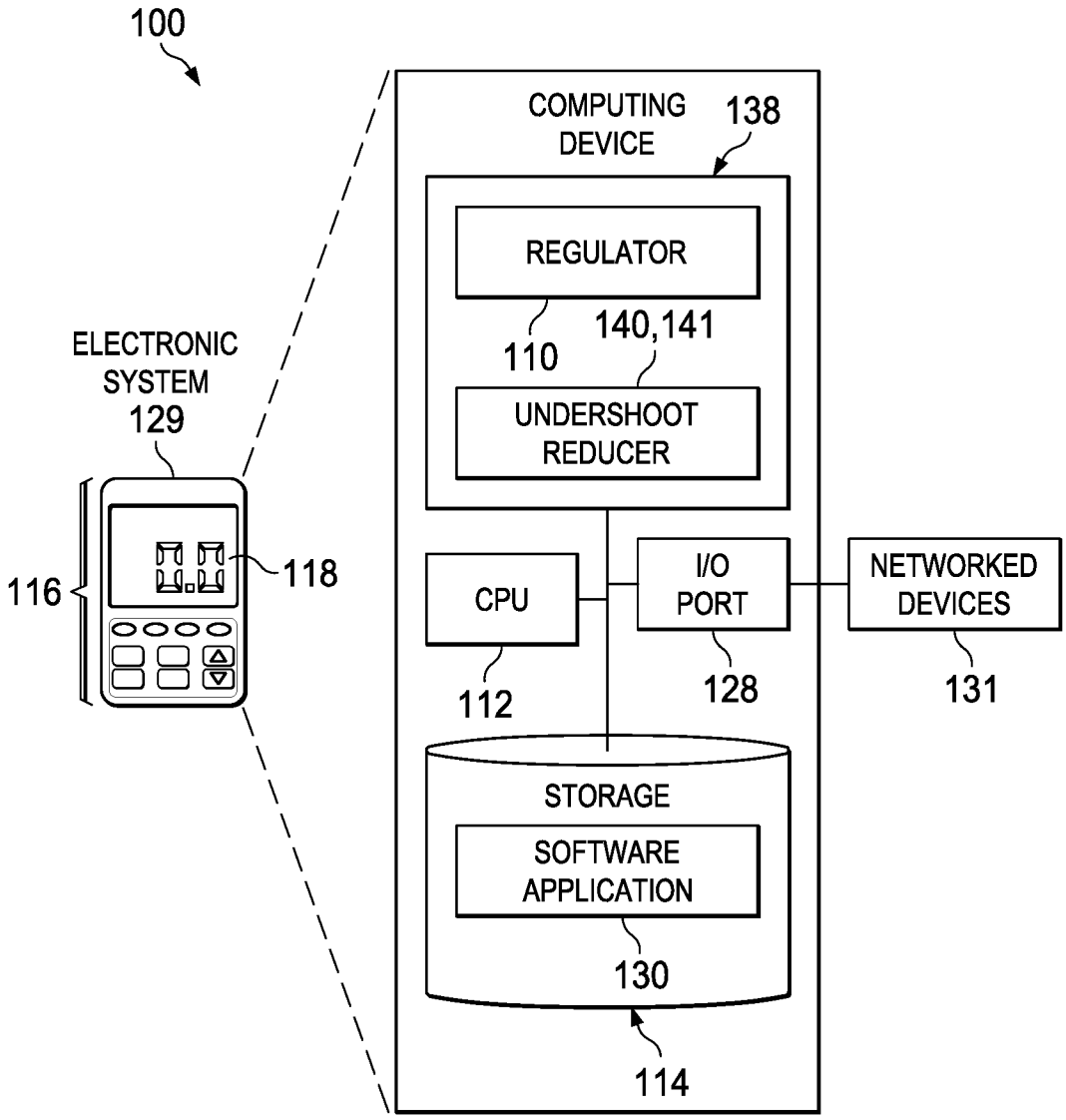
output has a second slope opposite in direction to the first slope.

17. The circuit of claim 16, wherein the first threshold is higher than the second threshold.

18. The circuit of claim 17, wherein the power control signal is generated to raise the power supply voltage when the indication of the power supply voltage output rises above the second threshold and when no signal to raise to raise the power supply voltage has been asserted.

19. The circuit of claim 16, wherein the first slope is a negative slope and the second slope is a positive slope.

20. The circuit of claim 16, wherein the first slope is a positive slope and the second slope is a negative slope.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128
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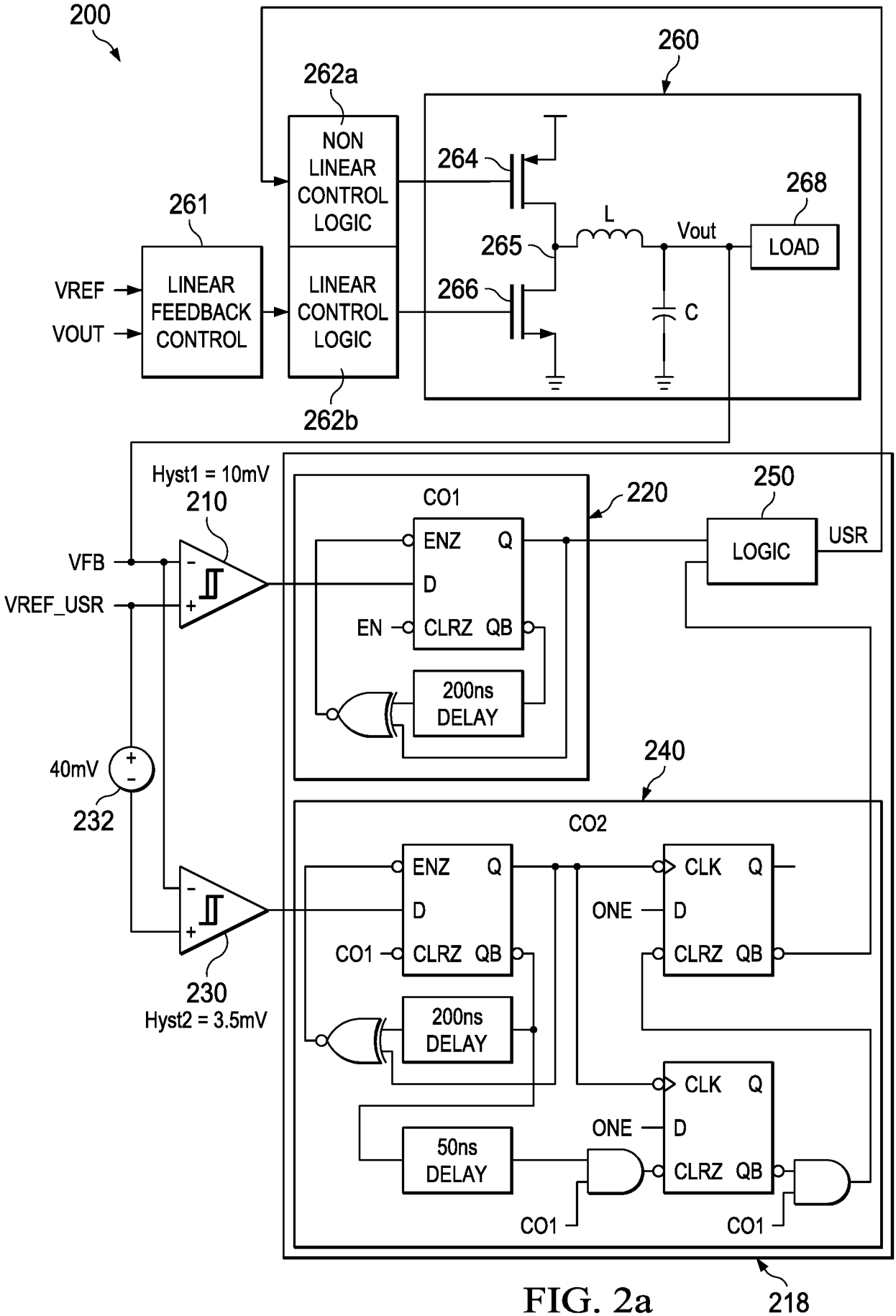
STORAGE
SOFTWARE APPLICATION
130
114

FIG. 1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C
VOUT
262b
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CO1
220
250
ENZ
Q
LOGIC
USR
VFB
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ENZ
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CLK
Q
D
ONE
D
CO1
CLRZ
QB
CLRZ
QB
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Hyst2 = 3.5mV
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FIG. 2a

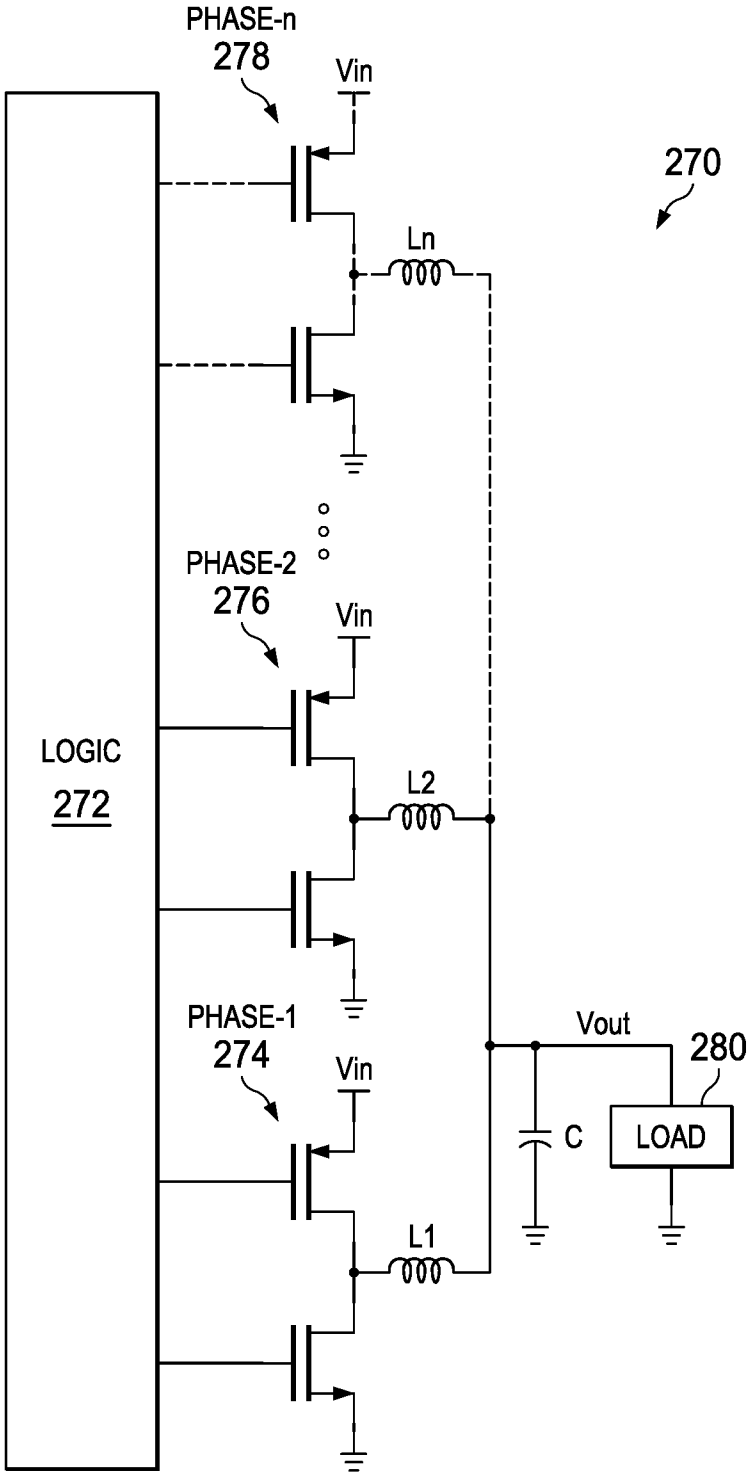
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FIG. 2B

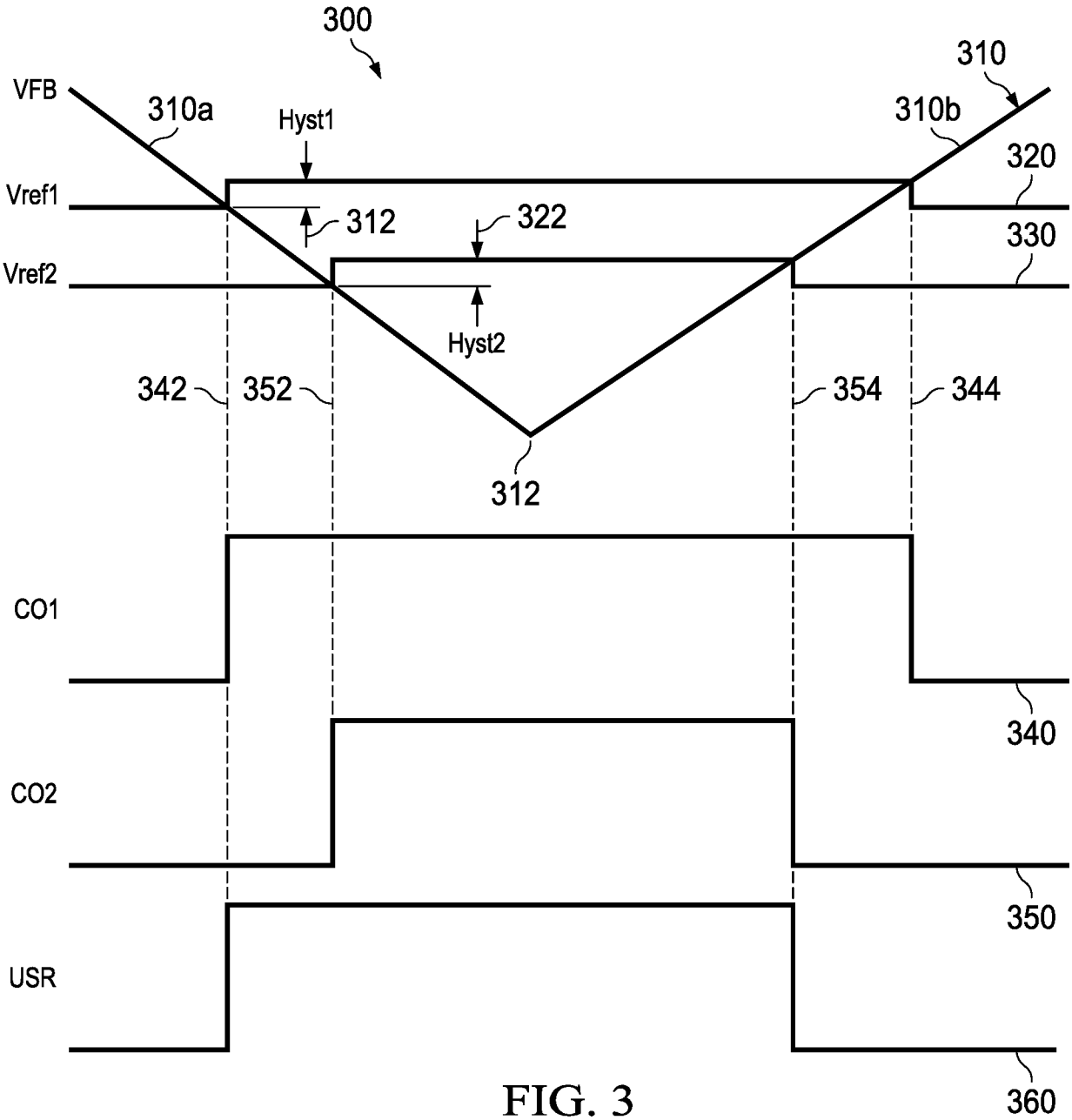
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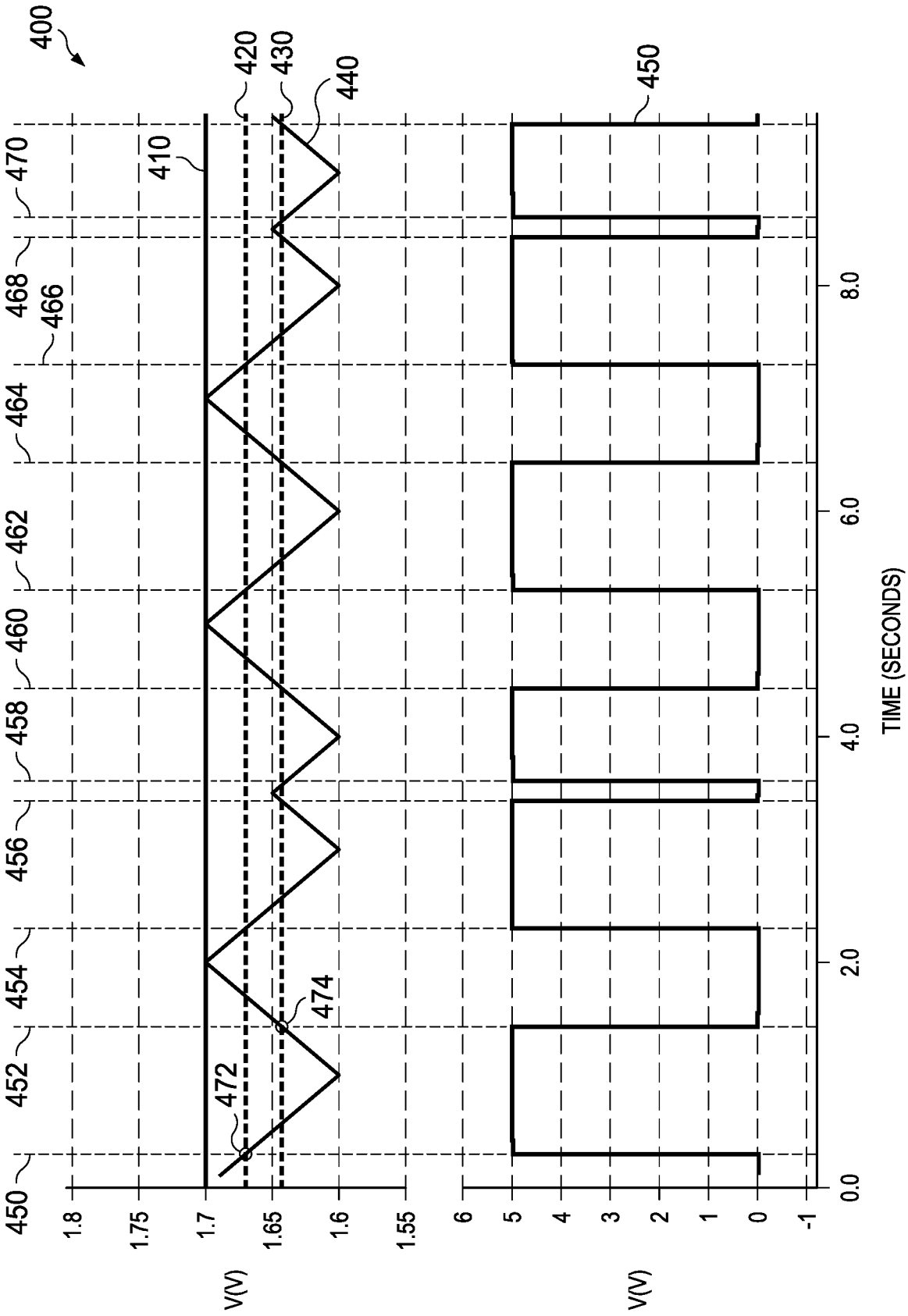
FIG. 3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1.7
1.65
1.6
1.55
V(V)
6
5
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V(V)
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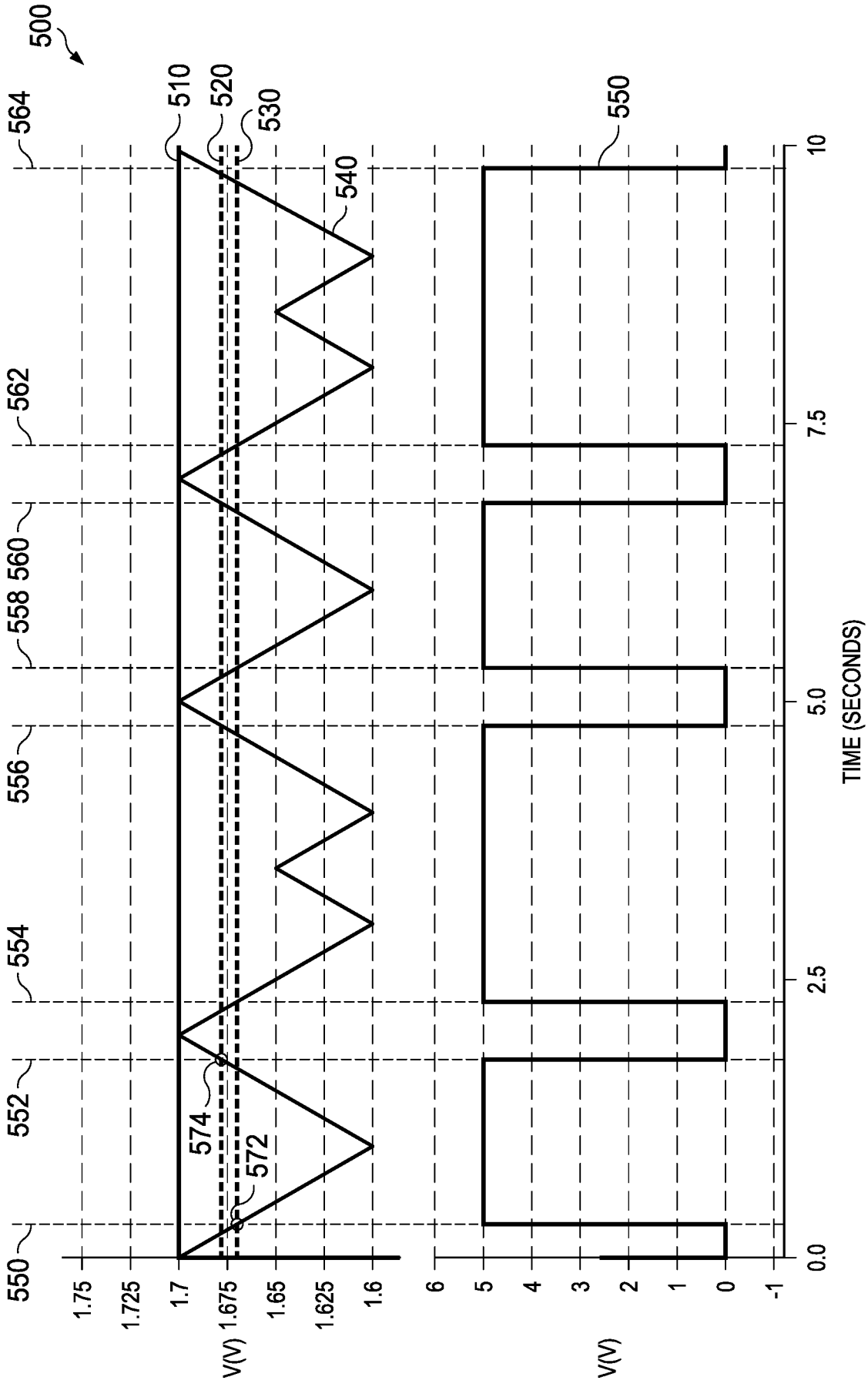
TIME (SECONDS)

FIG. 4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1.65
1.625
1.6
V(V)
6
5
4
3
2
1
0
-1
V(V)
0.0
2.5
5.0
7.5
10
TIME (SECONDS)

FIG. 5

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 2016/027336

A. CLASSIFICATION OF SUBJECT MATTER

G05F 1/56 *(2006.01)*

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G0F 51/56, H02M 3/156

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

PatSearch (RUPTO internal), USPTO, PAJ, Esp@cenet, DWPI, EAPATIS, PATENTSCOPE, Information Retrieval System of FIPS

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	KR20030055995 A (SAMSUNG ELECTRONICS CO., LTD) 04.07.2003	1-20
A	US 7982445 B1 (NATIONAL SEMICONDUCTOR CORPORATION) 19.07.2011	1-20
A	US 7423414 B1 (NATIONAL SEMICONDUCTOR CORPORATION) 09.09.2008	1-20

☐ Further documents are listed in the continuation of Box C.

☐ See patent family annex.

* Special categories of cited documents:

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"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
23 August 2016 (23.08.2016)	01 September 2016 (01.09.2016)

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