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(54) **Title:** SIC SEMICONDUCTOR DEVICE COMPRISING A DOUBLE GRID STRUCTURE

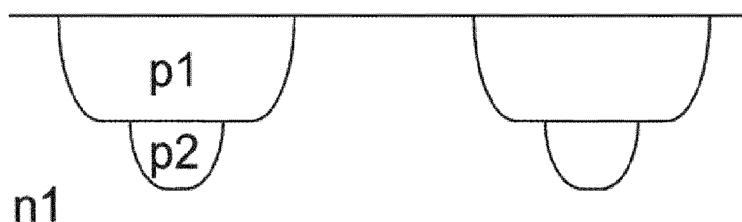

Fig. 1

(57) **Abstract:** In a doped grid structure in SiC each grid p1 has at least one smaller ledge p2 positioned centered under. The grid p1 and ledge p2 are in a first doped SiC and share the electric field. This increase the electric field shielding efficiency of the grid which is reducing the electric field on the surface of the device. This increase the blocking voltage and lower the leakage current without adding forward resistance. Alternatively, a wider grid spacing can be used with this design, leading to lower on-resistance. The structure is more tolerant to process variations such as misalignment, dose and energy variation in ion implantation, etching depth etc.

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SIC SEMICONDUCTOR DEVICE COMPRISING A DOUBLE GRID STRUCTURE

Technical field

[0001]The present invention relates to an embedded doped structure in SiC, a grid such as a buried grid or a surface grid.

Background

[0002]An embedded doping structure or buried grid (BG) can be used to shield the electric field close to the surface of a power semiconductor. Examples of such power semiconductors include but are not limited to a Schottky diode and a MOSFET switch. This is especially important for wide bandgap devices like devices made of SiC where the electric field in the semiconductor can be 6-10 times higher than in silicon and thus higher than the critical electric field allowed by the device design criteria in material interfacing the semiconductor like e.g. the surface passivation like SiO_2.

[0003]The design of the grid is critical for the function of the grid to withstand high voltage in blocking and not to limit on-resistance in forward condition. The electric field crowding in the vicinity of the grid corner results in higher leakage current and early breakdown.

[0004]In the prior art there have been a number of attempts to address field crowding in embedded doping structures such as buried grids.

[0005]First ion implantation gives an inherent rounding due to straggling and channelling of the implanted ions. However it is a problem that the shape cannot be optimized. The depth of the grid is also limited using ion implantation.

[0006]Etching a rounded bottom has also been attempted but trench shape inhomogeneity may lead to variations in the conducting and blocking properties.

[0007]US 6,897,133 discloses a method for producing a Schottky diode in SiC by etching and regrowth. A round shape is made by etching which is then filled with doped material by epitaxial growth.

[0008]US 8,633,560 discloses etching a rounded shape which is doped by ion implantation.

[0009]EP 2 884 538 discloses a doped grid structure in SiC with enhancement regions (12) formed adjacent, preferably contiguous, to floating regions (11). The conductivity types are opposite so that a pn-junction is formed. The purpose is to counteract an enlarged space charge region, which would decrease the resistance.

[0010]EP 2 889 915 discloses a semiconductor device comprising a floating region (11).

[0011]US 2014/0001489 discloses a double recessed trench Schottky barrier device. In the double recessed structure, a metal layer is formed in the deepest recess. The purpose of this invention is to add a narrow MOS region below a Schottky contact to reduce the electric field at the device surface.

<u>Summary</u>

[0012]It is an object of the present invention to obviate at least some of the disadvantages in the prior art and provide an improved grid as well as a method for its manufacture.

[0013]After extensive research it has been found that advantages can be obtained by introducing a ledge p2 under the grid p1, the electric field close to the open channel of the grid is then divided up in two points.

[0014]In a first aspect there is provided a grid structure in SiC comprising a plurality of grids p1, wherein each grid p1 has at least one ledge p2 of the same conductivity type positioned centered under each grid p1, wherein the lateral dimension of the ledges p2 is smaller than the lateral dimension of the grid p1 above the ledge p2, wherein the grid structure comprises a first layer of

doped SiC n1, wherein parts of the first layer of doped SiC n1 are in contact with parts of the second doped SiC n2, of the opposite conductivity type compared to the plurality of grids (p1, 5q, 5b), wherein each grid p1 is positioned so that it is in contact with the first layer of doped SiC n1, the second doped SiC n2, and the ledge p2, and wherein each ledge p2 is positioned so that it is in contact with the first layer of doped SiC n1, and the grid p1.

[0015]In a second aspect there is provided a method of manufacturing a grid structure as outlined above, comprising at least one method selected from the group consisting of epitaxial growth and ion implantation.

[0016]Advantages include that the structure reduces the maximum electric field in the grid structure which can reduce also the electric field in other parts of a device such as Schottky contacts and MOS interfaces. p1 and p2 share the electric field which modulate the field peaks at each point and thus increases the functionality and efficiency of the grid structure.

[0017] The grid structure gives a device, including but not limited to a Schottky barrier diode with higher maximal blocking voltage and lower leakage current without adding resistance in conduction. Lower resistance in forward corresponding to higher conduction for the same blocking voltage can also be obtained as well as blocking at higher temperature without adding resistance in conduction.

[0018]Another advantage is that the grid structure is more tolerant to process variations such as misalignment, dose and energy variation in ion implantation, etching depth etc. For example the tolerance towards variation in dose and energy of ion implantation results in a wider fabrication process window, which in turn makes the manufacturing less complicated and less expensive.

[0019]A wider grid spacing could be used with double-grid design since the electric field in the grid structure is lower than in conventional single grid design.

[0020]The dose (thickness × doping) of the drift could be increased since the electric field is modulated on the double grids, which could decrease the on-resistance by >7% in one embodiment.

Brief description of the drawings

[0021]The invention is described with reference to the following drawings in which:

[0022]Fig. 1 shows a schematic cross-sectional view of the grid structure according to the invention with a first doped semiconductor material n1, a second doped semiconductor material n2, two grids p1, and two ledges p2 of the same conductivity type positioned centered under each grid p1.

[0023]Fig. 2a and 2b show a schematic cross-sectional view of the grid structure according to the invention as in Fig. 1 however there is a Schottky contact applied onto n2. Fig 2b further shows the doped grid structure with the width W1 and height H of the grid p1 as well as the width W2 and height H2 of the ledge p2. The spacing between the grids p1 is denoted as S.

[0024]Fig. 3a shows a result of a simulation of a grid structure according to the state of the art. The electric field is shown. The middle of the figure depicts the spacing between two grids p1 but there are no ledges p2. It can be seen that the electric field is high around the corners of p1.

[0025]Fig. 3b shows a result of a simulation of a grid structure according to the invention with ledges p2 under the grids p1. The same geometry and conditions as in fig. 3a apply, but ledges p2 have been added. It can be seen that the electric field near the corners of p1 is not so high. The electric field distribution is depicted both in figs 3a and 3b at similar blocking voltage. The double grid according to the invention has 10% lower electric field than the conventional single grid device which results in more than 4 times lower leakage current and >10% higher blocking voltage. This is achieved at a comparable characteristic in conduction as a conventional single grid.

[0026]Fig. 4 shows five different fabrication process sequences for the grid structure according to the invention including the fully epitaxial process, ion-

implantation, and the combination of both techniques. The self-aligned fully-implanted process is provided in an embodiment for better electric field distribution and the combined epitaxial-implanted processes are provided in an embodiment for better forward characteristics. The double grid can also be fabricated with other fabrication processes. Fig 4 shows the following steps for five different versions: 1 fully epitaxial grid, 2 Fully Implanted Grid (Recessed Hard Mask), 3 Implanted + Epitaxial Grid, 4 Self-Aligned Implanted Grid, 5 Implanted + Epitaxial Grid.

Figs 4-1 to 4-8 show 1. Fully Epitaxial Grid:

4-1 Epilayers (Drift + Channel)

4-2 Hard mask formation (W2)

4-3 Etching SiC (deep grid)

4-4 Hard mask formation (W1) (widening by etching or forming new)

4-5 Etching SiC (shallow grid)

4-6 Hard mask removal

4-7 p-SiC overgrowth (Dose2 & Dose1)

4-8 Planarization + n-SiC overgrowth

Figs 4-9 to 4-14 show 2. Fully Implanted Grid (Recessed Hard Mask)

4-9 Epilayers (Drift + Channel)

4-10 1st hard mask formation (W1)

4-11 2nd hard mask formation (W2)

4-12 Ion implantation

4-13 Hard mask removal

4-14 n-SiC overgrowth

Figs 4-15 to 4-22 show 3. Implanted + Epitaxial Grid

4-15 Epilayers (Drift + Channel)

4-16 Hard mask formation (W2)

4-17 Ion Imp. Dose 2 (deep grid)

4-18 Hard mask formation (W1) (widening by etching or forming new)

4-19 Etching SiC (shallow grid)

4-20 Hard mask removal

4-21 p-SiC overgrowth (shallow grid)

4-22 Planarization + n-SiC overgrowth

Figs 4-23 to 4-29 show 4. Self-Aligned Implanted Grid

4-23 Epilayers (Drift + Channel)

4-24 Hard mask formation (W2)

4-25 1st Imp. Dose 2 (deep grid)

4-26 Hard mask widening (W1)

4-27 2nd Imp. Dose 1 (shallow grid)

4-28 Hard mask removal

4-29 n-SiC overgrowth

Figs 4-30 to 4-36 show 5. Implanted + Epitaxial Grid

4-30 Epilayers (Drift + Channel)

4-31 Hard mask formation (W2)

4-32 Ion Imp. Dose 2 (deep grid)

4-33 Hard mask removal

4-34 p-SiC overgrowth

4-35 Hard mask formation (W1)

4-36 Etching the p-SiC layer (shallow grid)

4-37 n-SiC overgrowth + Planarization

Detailed description

[0027]Before the invention is disclosed and described in detail, it is to be understood that this invention is not limited to particular compounds, configurations, method steps, substrates, and materials disclosed herein as such compounds, configurations, method steps, substrates, and materials may vary somewhat. It is also to be understood that the terminology employed herein is used for the purpose of describing particular embodiments only and is not intended to be limiting since the scope of the present invention is limited only by the appended claims and equivalents thereof.

[0028]It must be noted that, as used in this specification and the appended claims, the singular forms “a”, “an” and “the” include plural referents unless the context clearly dictates otherwise.

[0029]If nothing else is defined, any terms and scientific terminology used herein are intended to have the meanings commonly understood by those of skill in the art to which this invention pertains.

[0030] “Buried grid” as used throughout the description and the claims denotes a grid structure of a material with one conductivity type in a material with the opposite conductivity type.

[0031]“Conductivity type” as used throughout the description and the claims denotes the type of conduction in a semiconductor material. N-type denotes electron conduction meaning that excess electrons move in the semiconductor giving a current flow and p-type denotes hole conduction, meaning that excess holes move in the semiconductor giving a current flow. A n-type semiconductor material is achieved by donor doping and a p-type semiconductor by acceptor dopants. In SiC, nitrogen is commonly used as donor dopant and aluminum as acceptor dopant. If a material is a doped semiconductor such as SiC, the material either has conductivity type p or conductivity type n.

[0032] “Doped” as used throughout the description and the claims denotes that an intrinsic semiconductor such as SiC has got added impurities to modulate its electrical properties and become an extrinsic semiconductor.

[0033] “Epitaxial” as used throughout the description and the claims denotes that the material has been manufactured with epitaxial growth, in this case epitaxial growth of SiC.

[0034] “Substrate” as used throughout the description and the claims denotes a piece of material on which the power device is built up. In a first aspect there is provided a doped grid structure in SiC comprising a plurality of grids (p1, 5a, 5b), wherein each grid (p1, 5a, 5b) has at least one ledge (p2, 6a, 6b) of the same conductivity type as the grids (p1, 5a, 5b) positioned centered under each grid (p1, 5a, 5b), wherein the lateral dimension of the ledges (p2, 6a, 6b) is smaller than the lateral dimension of the grid (p1, 5a, 5b) above the ledge (p2, 6a, 6b), wherein the grid structure comprises a first layer of doped SiC (n1), of the opposite conductivity type compared to the plurality of grids (p1, 5q, 5b), wherein each grid (p1, 5a, 5b) is positioned so that it is in contact with the first layer of doped SiC (n1), and the ledge (p2, 6a, 6b), and wherein each

ledge (p2, 6a, 6b) is positioned so that it is in contact with the first layer of doped SiC (n1), and the grid (p1, 5a, 5b).

[0035]In one embodiment the grid structure comprises a second doped SiC (n2) of the same conductivity type compared to the first layer of doped SiC (n1), wherein parts of the first layer of doped SiC (n1) are in contact with parts of the second doped SiC (n2), and wherein each grid (p1, 5a, 5b) is positioned so that it is in contact with the first layer of doped SiC (n1), the second doped SiC (n2), and the ledge (p2, 6a, 6b).

[0036]The criterion to be centered is determined so that the center of mass is determined for p1 and p2 respectively. p1 and p2 are centered in relation to each other if they are positioned so that the distance between their centers of mass is as short as possible.

[0037]In one embodiment the thickness x doping concentration of the grid p1 and the ledge p2 is in the interval 1e12 – 1e17 cm-2. The thickness x doping concentration is referred to as the dose. The thickness is defined as follows: First the centers of mass of p1 and p2 respectively are determined. Then p1 and p2 are positioned so that the distance between their centers of mass is as short as possible, i.e. now p1 and p2 are centered. The line between the centers of mass of p1 and p2 define the directions up and down. Up is in the direction of p1 and down is in the direction of p2. This defines the directions up and down respectively. Four planes are defined, all planes being perpendicular to the distance between the centers of mass of p1 and p2: A first plane intersecting the uppermost point of p1, a second plane intersecting the lowermost point of p1, a third plane intersecting the uppermost point of p2 and a fourth plane intersecting the lowermost point of p2. Then the thickness of p1 is the distance between the first and second planes and the thickness of p2 is the distance between the third and fourth planes. Lateral dimension of p1 is defined as the largest possible distance inside p1 and perpendicular to the line between the centers of mass of p1 and p2, and through the center of mass of p1. Lateral dimension of p2 is defined as the largest possible distance inside

p2 and perpendicular to the line between the centers of mass of p1 and p2, and through the center of mass of p2.

[0038]In the grid structure according to the invention, p1 can have a higher doping level compared to a similar device without ledge p2 since the corners of the grid p1 are shielded from high electric field by p2. Thereby, when contacted it improves the minority carrier injection from the grid into the drift layer.

[0039]It is conceived that n denotes n-type semiconductor material and that p denotes a p-type semiconductor material. However a skilled person realizes that for most semiconductor devices which comprise n- and p-doped material, it is possible to change conductivity type for all n- and p-doped materials so that all n become p and all p become n and still obtain a similar device. In the present invention all n can be changed to p and vice versa.

[0040]In one embodiment there is a further ledge P3 positioned centered under each ledge p2, and wherein the lateral dimension of the ledge P3 is smaller than the lateral dimension of the ledge p2 above. It is also conceived to have further ledges P4, P5 and so on. Each additional ledge should be centered and should have a lateral size smaller than the ledge above. Also for the additional ledges the definitions with centering and directions up and down as above apply.

[0041]In one embodiment the grid structure is a buried grid. The buried grid can be used in any device where such a grid is useful.

[0042]In an alternative the grid structure is a surface grid.

[0043]In a second aspect there is provided a method of manufacturing a doped grid structure in SiC as detailed above, said method comprising at least one method selected from the group consisting of epitaxial growth and ion implantation.

[0044]In one embodiment the method is self-aligning a ledge (p2, 6a, 6b) centered under each grid (p1, 5a, 5b).

[0045]In one embodiment at least the ledge (p2, 6a, 6b) is manufactured with ion implantation, wherein a region within the grid (p1, 5a, 5b) above the ledge (p2, 6a, 6b) has a higher doping concentration compared to the rest of the grid (p1, 5a, 5b), and wherein ions are implanted both in the ledge (p2, 6a, 6b) and the region within the grid (p1, 5a, 5b) above the ledge (p2, 6a, 6b). In one version of such an embodiment an Ohmic contact is applied on the region within p1 above p2 with the higher doping concentration compared to the rest of p1.

[0046]There are a number of different manufacturing methods. In the following there are given examples of manufacturing methods. It is conceived that the application is not limited to these methods of manufacture. The examples are given in order to facilitate the use of the invention for a person skilled in the art.

[0047]In one embodiment a cavity with a width W1 and a deeper cavity with a width W2 corresponding to the desired dimensions of the grid (p1, 5a, 5b) and the ledge (p2, 6a, 6b) respectively are etched using masks (7) with different widths (W1, W2), and where after the ledge (p2, 6a, 6b) is filled by epitaxial growth with a first layer of doped SiC (6a) and the grid (p1, 5a, 5b) is subsequently filled by epitaxial growth with a second doped SiC (5a) of the same conductivity type as the first layer of doped SiC (6a). This method is illustrated in Fig 4 1 Fully Epitaxial Grid. The method in this particular embodiment comprises the steps abbreviated Epilayers, Hard mask formation (W2), Etching the SiC (deep grid), Hard mask formation (widening by etching or forming new) (W1), Etching the SiC (shallow grid), Hard mask removal, p-SiC overgrowth (dose2 & dose1), planarization and n-SiC overgrowth .

[0048]In one embodiment the substrate is planarized to remove excess material added by epitaxial growth.

[0049]In one embodiment a mask (7) is applied on a SiC substrate, said mask (7) comprising at least a first and a second layer, said first layer having an opening with a width W1, said first layer being essentially impermeably to ions during ion implantation and a second layer having an opening with a width W2, said second layer being partially permeable to ions during ion implantation, the

widths W1 and W2 corresponding to the desired dimensions of the grid (p1, 5a, 5b) and the ledge (p2, 6a, 6b) respectively, the method comprising implantation of ions through the mask and the overlain openings with widths W1 and W2 to obtain an implanted grid (p1, 5a, 5b) (5b) and an implanted ledge (p2, 6a, 6b) (6b). This method is illustrated in Fig 4, 2 Fully Implanted Grid (Recessed Hard Mask). In this embodiment the method comprises the steps abbreviated as Epilayers, 1st hard mask formation , 2nd hard mask formation, ion implantation, hard mask removal, and n-SiC overgrowth .

[0050]In one embodiment a mask (7) is applied on a SiC substrate, said mask having an opening with a width W2, said mask being essentially impermeably to ions during ion implantation, the width W2 corresponding to the desired dimension of the ledge (p2, 6a, 6b), the method comprising implantation of ions through the opening with width W2 to obtain an implanted ledge (p2, 6a, 6b) (6b), said method comprising subsequent widening of the mask to a width W1 and etching a cavity with width W1 followed by filling the cavity with doped SiC (5a) by epitaxial growth followed by planarization. This method is illustrated in Fig 4, 3 Implanted + Epitaxial Grid. In one embodiment the method comprises the steps abbreviated as Epilayers, Hard mask etching (W2), Ion implantation dose 2 deep grid, hard mask formation (W1) (widening or forming new), etching the SiC (shallow grid), hard mask removal, p-SiC overgrowth (shallow grid), Planarization + n-SiC overgrowth .

[0051]In one embodiment a mask (7) is applied on a SiC substrate, said mask having an opening with a width W2, said mask being essentially impermeably to ions during ion implantation, the width W2 corresponding to the desired dimension of the ledge (p2, 6a, 6b), the method comprising implantation of ions through the mask and the opening with width W2 to obtain an implanted ledge (p2, 6a, 6b)(6b), said method comprising subsequent widening of the mask to a width W1 and subsequent implantation of ions through the mask and the opening with width W1 to obtain an implanted grid (p1, 5a, 5b)(5b). This method is illustrated in Fig 4, 4 Self-Aligned Implanted Grid. In one embodiment the method encompasses the steps abbreviated as Epilayers,

Hard mask formation (W2), 1st ion implantation dose 2 (deep grid), Hard mask widening (W1), 2nd ion implantation dose 1 (shallow grid), hard mask removal, and n-SiC overgrowth.

[0052]In one embodiment a mask (7) is applied on a SiC substrate, said mask having an opening with a width W2, said mask being essentially impermeably to ions during ion implantation, the width W2 corresponding to the desired dimension of the ledge (p2, 6a, 6b), the method comprising implantation of ions through the mask and the opening with width W2 to obtain an implanted ledge (p2, 6a, 6b)(6b), said method comprising subsequent addition by epitaxial growth of a layer of doped SiC (5a) followed by etching away parts of said layer of doped SiC with a mask to form isolated parts p1 (5a). This method is illustrated in Fig 4, 5 implanted + epitaxial grid. In one embodiment this method encompasses the steps abbreviated as Epilayers, Hard mask formation (W2), ion implantation dose 2 (deep grid), hard mask removal, p-SiC overgrowth, hard mask formation (W1), etching p-SiC (shallow grid), hard mask removal, n-SiC overgrowth + planarization.

[0053]In one embodiment a further layer of a second doped SiC (n2) is added by epitaxial growth in any of the methods described above. This forms a buried grid.

[0054]Designing the grid with several ledges has for instance the following effects:

[0055]It reduces the maximum electric field in the grid structure for a similar grid spacing (S in Fig. 2b), so a wider grid spacing could be used with double-grid design since the electric field on the structure is lower than for conventional single grid designs.

[0056]A drift with higher conductivity (higher doping concentration or less thickness) can be used since the electric field is modulated on the double grids, which could increase the current density and decrease the specific resistance by >7% in some embodiments.

[0057]p1 could have higher doping concentration since the grid corner is shielded from high electric field by p2. Thus, when contacted it improves the minority carrier injection from the grid into the drift layer n1 for surge current protection.

[0058]Compared to the conventional grid design, the double grid is more tolerant to process variations such as misalignment, dose and energy variation in ion implantation, etching depth etc.

[0059]The grid layer p2 is placed centered under grid layer p1. The lateral dimension of p2 is smaller than p1.

[0060]In preferred embodiment the dose (thickness × doping concentration) of p1 and p2 ranges from 1e12 to 1e17 cm-2.

[0061]In one embodiment the invention is utilized with 3 or more ledges to divide up the electric field on more corner points. The efficiency gain is however limited and in most cases not motivated in relation to added fabrication complexity. Embodiments with 3 or more ledges may be useful for special applications.

[0062]The lateral (W1 & W2) and vertical (H1 & H2) dimensions of the p1 and p2 and their geometry are important for the functionality of the double grid. A double grid design with too close p1 and p2 corners results in similar design to a single grid with a rounded corner. On the other hand, the electric field crowding occurs on either p1 or p2 corners when the double grid design has too wide p1 and p2 corners. Therefore, the electric field will not be divided between the p1 and p2 and the double grid will not function optimally. The location where the maximum electric field occurs depends upon the lateral and vertical distance as well as the dose of the p1 and p2 corners.

- - -

CLAIMS

1. A doped grid structure in SiC comprising a plurality of grids (p1, 5a, 5b), wherein each grid (p1, 5a, 5b) has at least one ledge (p2, 6a, 6b) of the same conductivity type as the grid (p1, 5a, 5b) positioned centered under each grid (p1, 5a, 5b), wherein the lateral dimension of the ledge (p2, 6a, 6b) is smaller than the lateral dimension of the grid (p1, 5a, 5b) above the ledge (p2, 6a, 6b), wherein the grid structure comprises a first layer of doped SiC (n1) of the opposite conductivity type compared to the plurality of grids (p1, 5q, 5b), wherein each grid (p1, 5a, 5b) is positioned so that it is in contact with the first layer of doped SiC (n1), and the ledge (p2, 6a, 6b), and wherein each ledge (p2, 6a, 6b) is positioned so that it is in contact with the first layer of doped SiC (n1), and the grid (p1, 5a, 5b).

2. The grid structure according to claim 1, wherein the grid structure comprises a second doped SiC (n2) of the same conductivity type compared to the first layer of doped SiC (n1), wherein parts of the first layer of doped SiC (n1) are in contact with parts of the second doped SiC (n2), and wherein each grid (p1, 5a, 5b) is positioned so that it is in contact with the first layer of doped SiC (n1), the second doped SiC (n2), and the ledge (p2, 6a, 6b).

3. The grid structure according to any one of claims 1-2, wherein the thickness x doping concentration of the grid (p1, 5a, 5b) and the ledge (p2, 6a, 6b) is in the interval 1e12 – 1e17 cm^{-2}.

4. The grid structure according to any one of claims 1-3, wherein there is a further ledge (P3) positioned centered under each ledge (p2, 6a, 6b), and wherein the lateral dimension of the ledge (P3) is smaller than the lateral dimension of the ledge (p2, 6a, 6b) above.

5. The grid structure according to any one of claims 1-4, wherein the grid structure is a buried grid.

6. The grid structure according to any one of claims 1-4, wherein the grid structure is a surface grid.

7. The grid structure according to any one of claims 1-6, wherein the doping concentration of the grid (p1, 5a, 5b) and the ledge (p2, 6a, 6b) are different.

8. A method of manufacturing a doped grid structure in SiC according to any one of claims 1-6, comprising at least one method selected from the group consisting of epitaxial growth and ion implantation.

9. The method according to claim 8, wherein the method is self-aligning a ledge (p2, 6a, 6b) centered under each grid (p1, 5a, 5b).

10. The method according to any one of claims 8-9, wherein at least the ledge (p2, 6a, 6b) is manufactured with ion implantation, wherein a region within the grid (p1, 5a, 5b) above the ledge (p2, 6a, 6b) has a higher doping concentration compared to the rest of the grid (p1, 5a, 5b), and wherein ions are implanted both in the ledge (p2, 6a, 6b) and the region within the grid (p1, 5a, 5b) above the ledge (p2, 6a, 6b).

11. The method according to claim 10, wherein an Ohmic contact is applied on the region within p1 above p2 with the higher doping concentration compared to the rest of p1.

12. The method according to any one of claims 8-9, wherein a cavity with a width W1 and a deeper cavity with a width W2 corresponding to the desired dimensions of the grid (p1, 5a, 5b) and the ledge (p2, 6a, 6b) respectively are etched using masks (7) with different widths, and where after the ledge (p2, 6a, 6b) is filled by epitaxial growth with a first layer of doped SiC and the grid (p1, 5a, 5b) is subsequently filled by epitaxial growth with a second doped SiC.

13. The method according to claim 12, where the substrate surface is planarized to remove excess material added by epitaxial growth.

14. The method according to any one of claims 8-9, wherein a mask (7) is applied on a SiC substrate, said mask comprising at least a first and a second layer, said first layer having an opening with a width W1, said first layer being essentially impermeably to ions during ion implantation and a second layer

having an opening with a width W2, said second layer being partially permeable to ions during ion implantation, the widths W1 and W2 corresponding to the desired dimensions of the grid (p1, 5a, 5b) and the ledge (p2, 6a, 6b) respectively, the method comprising implantation of ions through the mask and the overlain openings with widths W1 and W2 to obtain an implanted grid (p1, 5a, 5b) and an implanted ledge (p2, 6a, 6b).

15. The method according to any one of claims 8-9, wherein a mask (7) is applied on a SiC substrate, said mask having an opening with a width W2, said mask being essentially impermeably to ions during ion implantation, the width W2 corresponding to the desired dimension of the ledge (p2, 6a, 6b), the method comprising implantation of ions through the mask and the opening with width W2 to obtain an implanted ledge (p2, 6a, 6b), said method comprising subsequent application of a mask (7) with width W1 and etching a cavity with width W1 followed by filling the cavity with doped SiC by epitaxial growth followed by planarization.

16. The method according to any one of claims 8-9, wherein a mask (7) is applied on a SiC substrate, said mask having an opening with a width W2, said mask being essentially impermeably to ions during ion implantation, the width W2 corresponding to the desired dimension of the ledge (p2, 6a, 6b), the method comprising implantation of ions through the mask and the opening with width W2 to obtain an implanted ledge (p2, 6a, 6b), said method comprising subsequent widening of the mask (7) to a width W1 and subsequent implantation of ions through the mask and the opening with width W1 to obtain an implanted grid (p1, 5a, 5b).

17. The method according to any one of claims 8-9, wherein a mask (7) is applied on a SiC substrate, said mask having an opening with a width W2, said mask being essentially impermeably to ions during ion implantation, the width W2 corresponding to the desired dimension of the ledge (p2, 6a, 6b), the method comprising implantation of ions through the mask and the opening with width W2 to obtain an implanted ledge (p2, 6a, 6b), said method comprising

subsequent addition by epitaxial growth of a layer of doped SiC followed by etching away parts of said layer of doped SiC to form isolated parts p1.

18. The method according to claim any one of 13, 14, 15, 16, and 17 wherein a further layer of a second doped SiC (n2) is added by epitaxial growth.

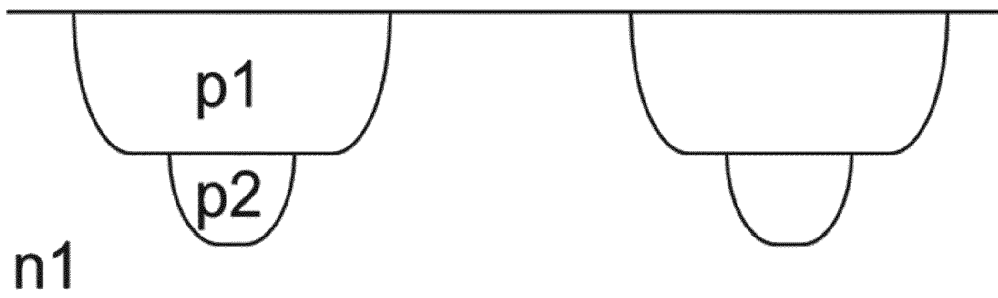


Fig. 1

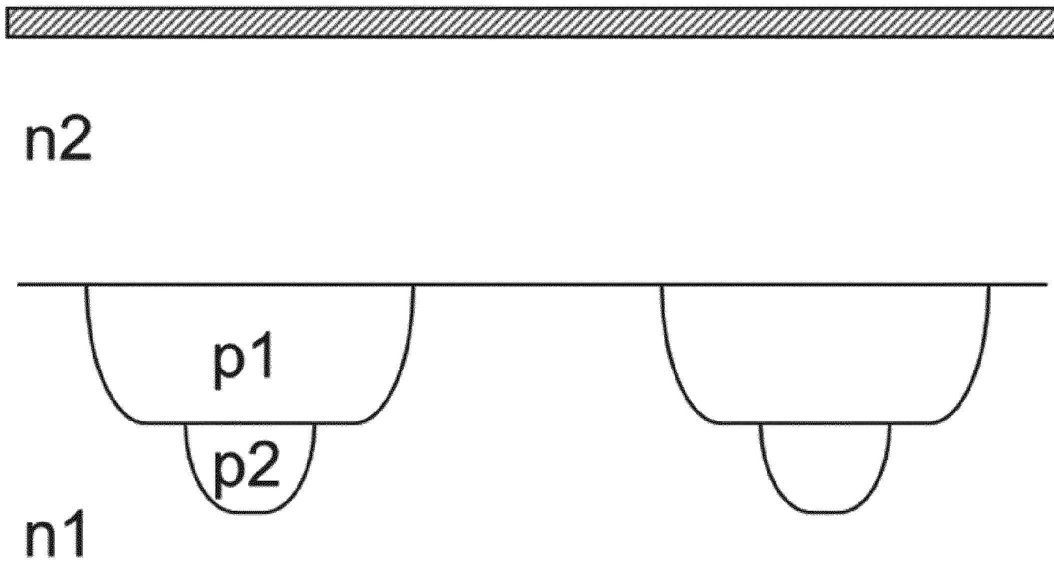


Fig. 2

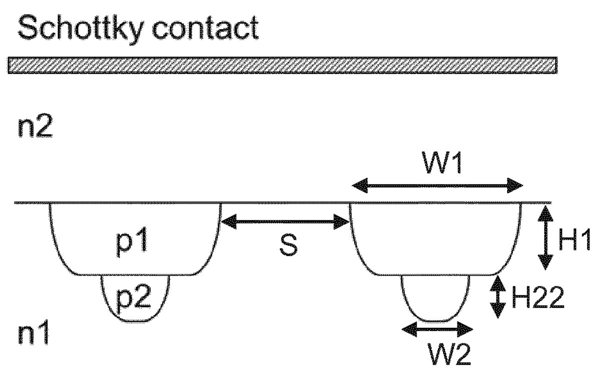


Fig 2b

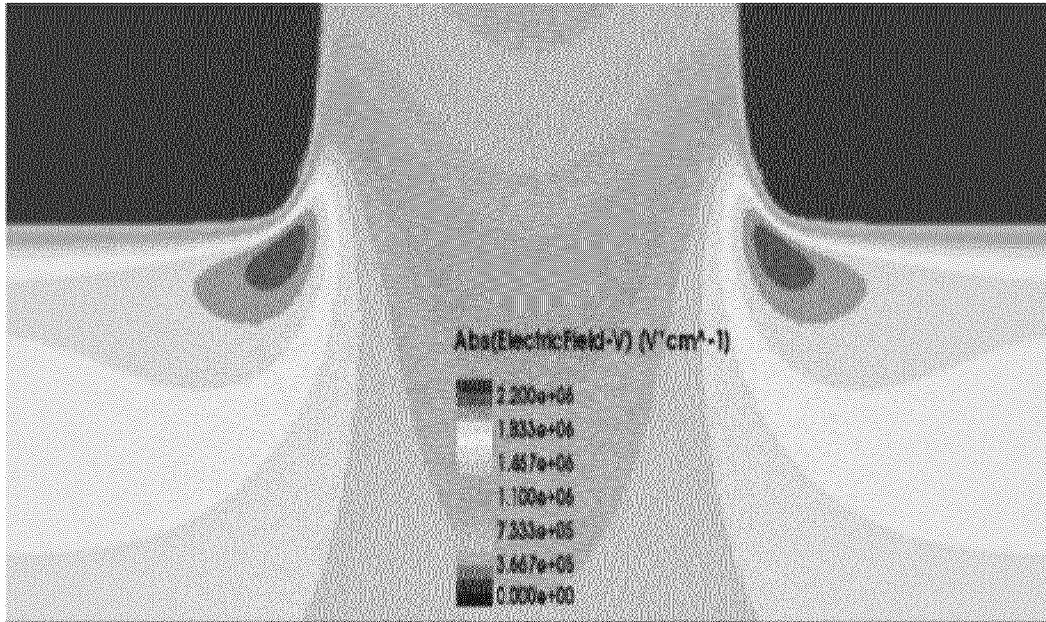


Fig. 3a

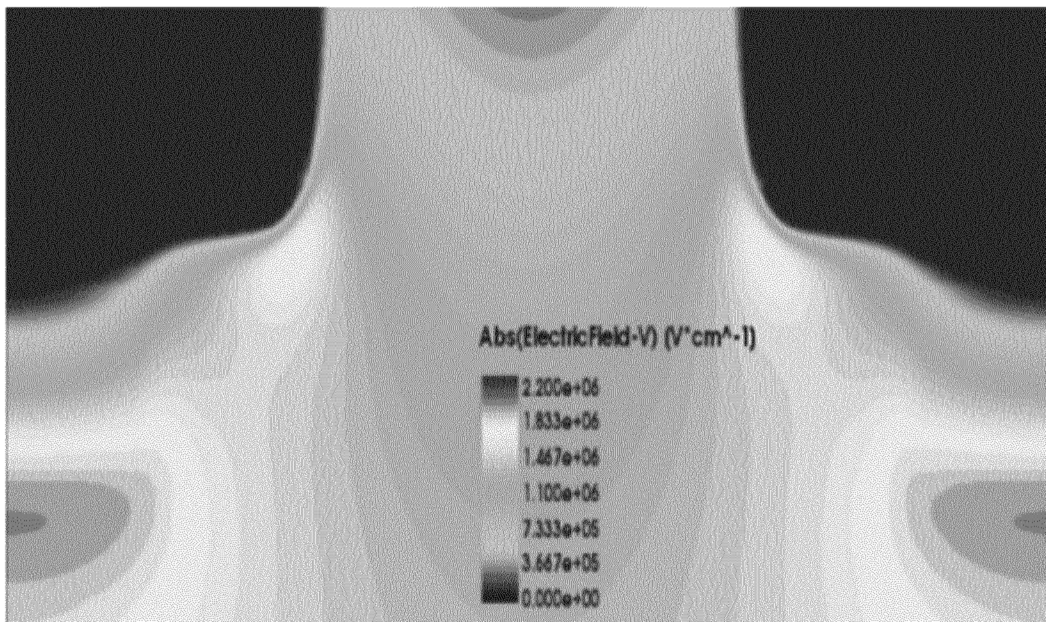


Fig. 3b

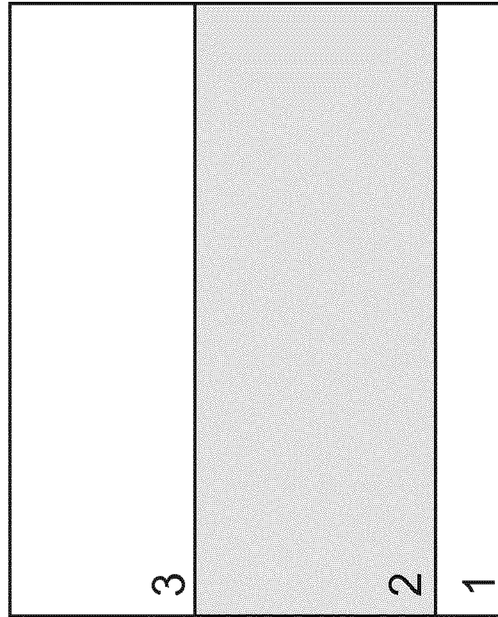


Fig 4-1

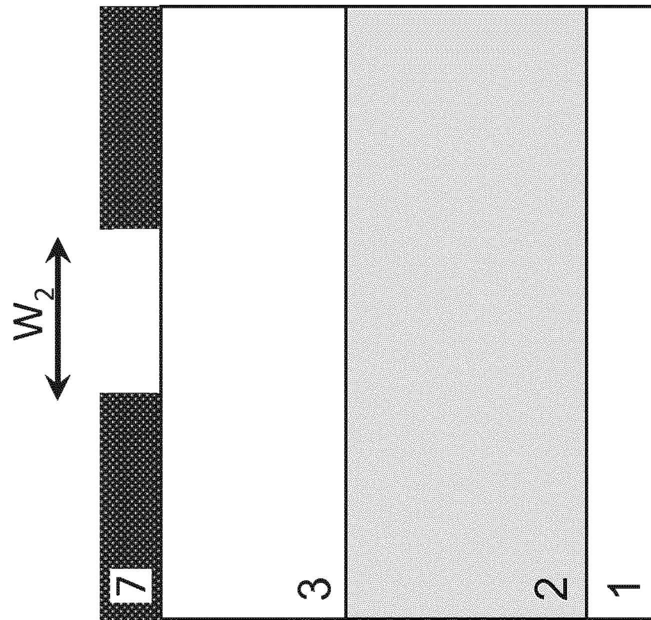
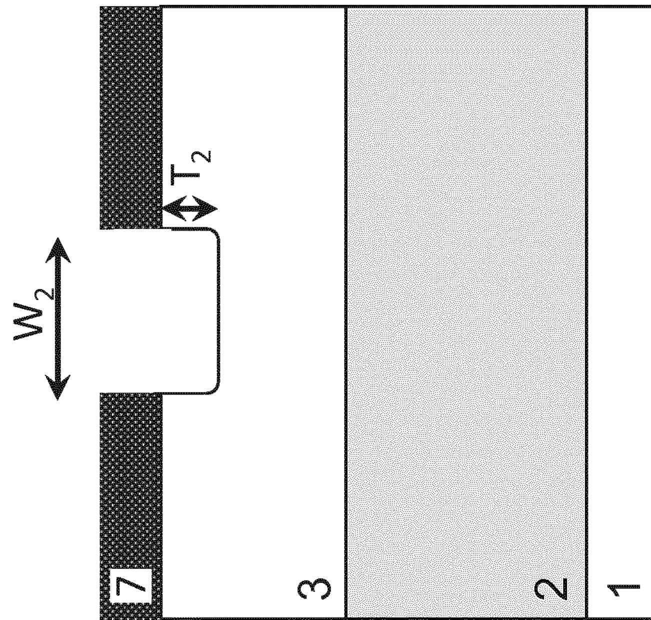


Fig 4-2



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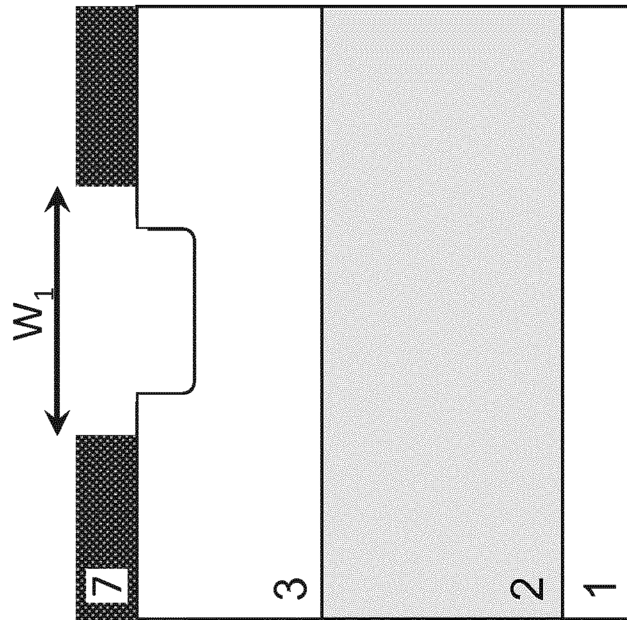

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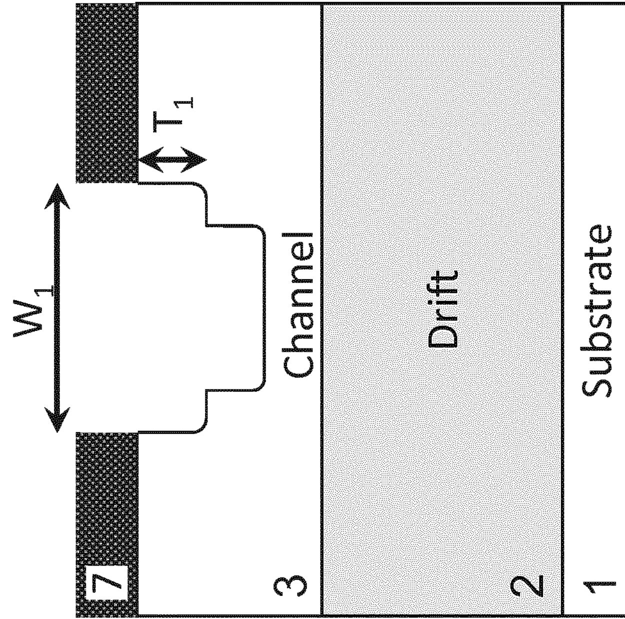

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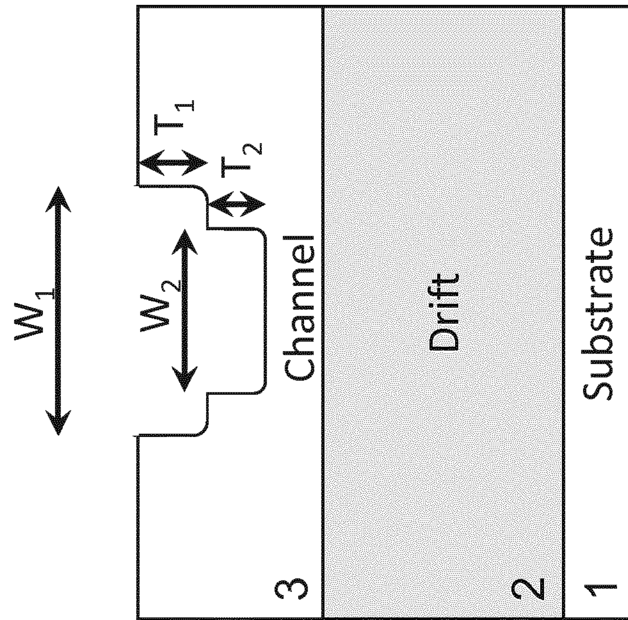

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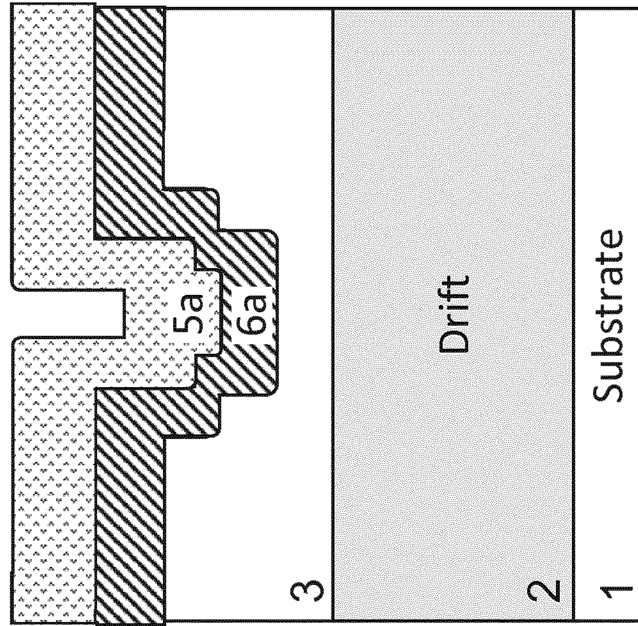

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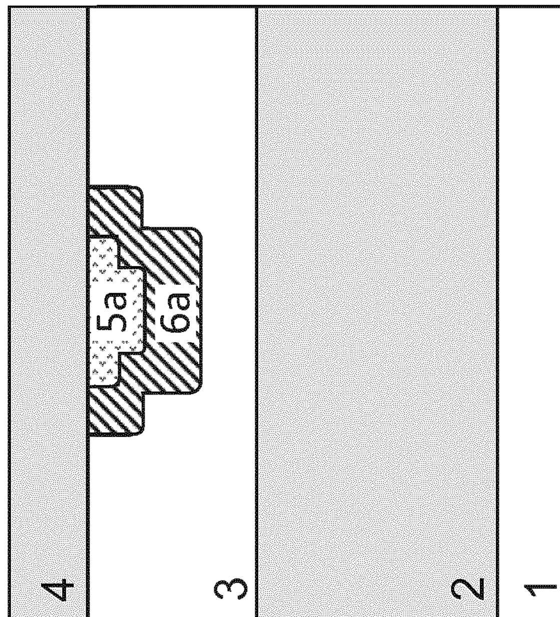

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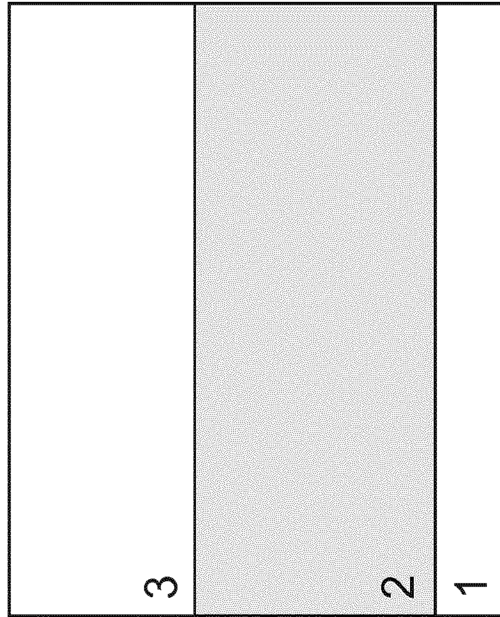

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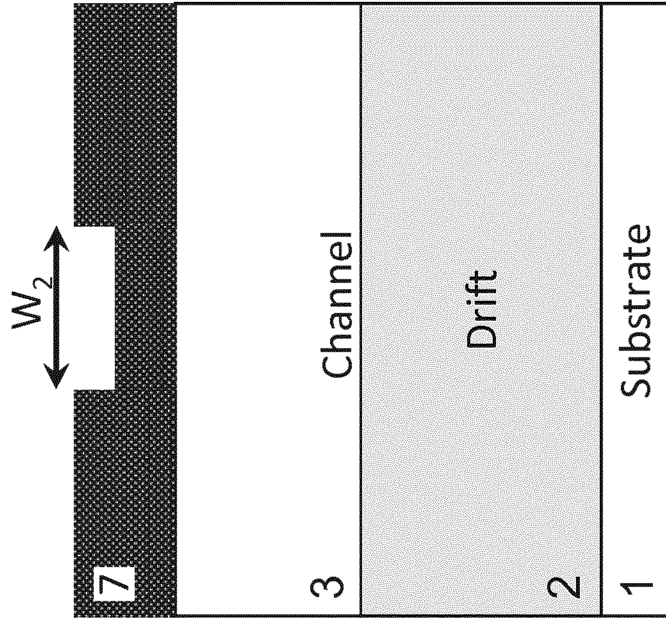

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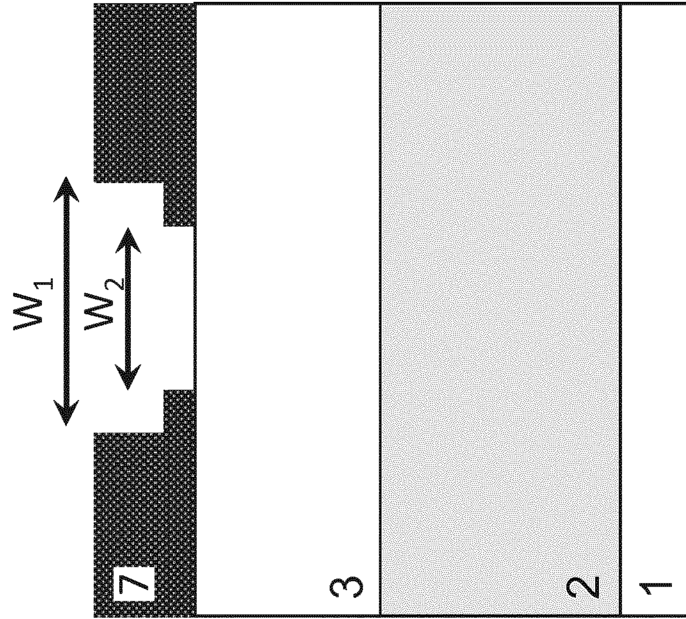

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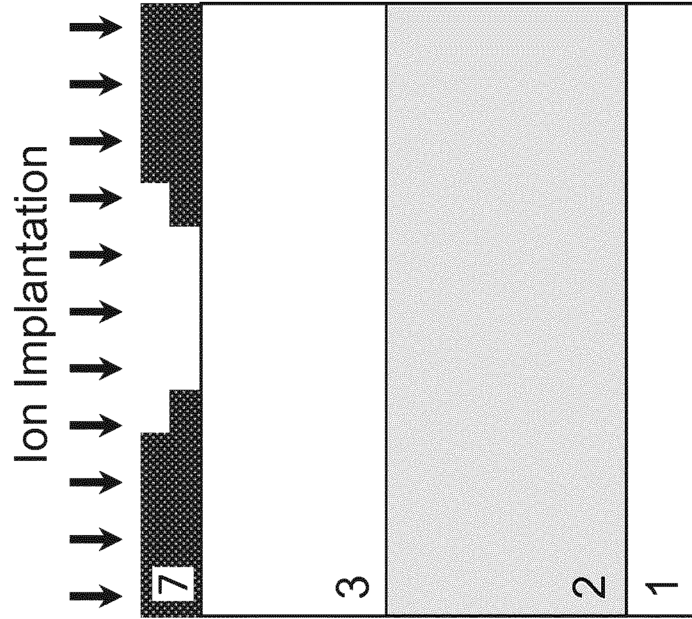

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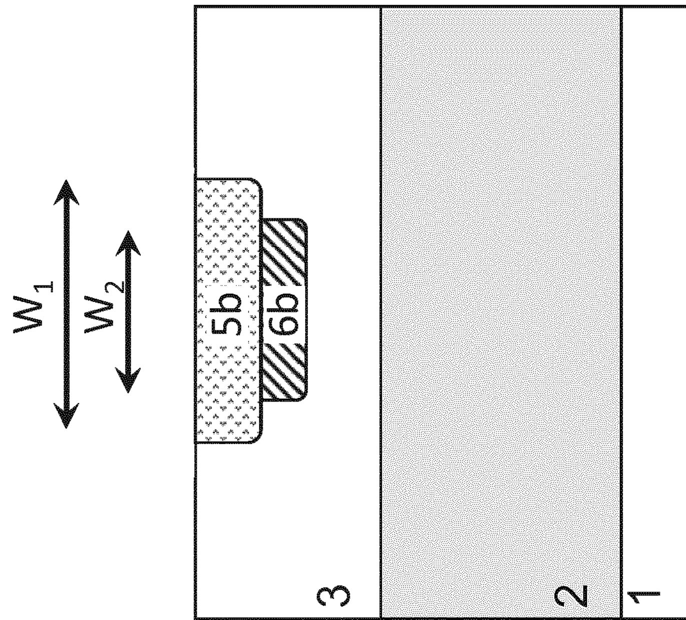

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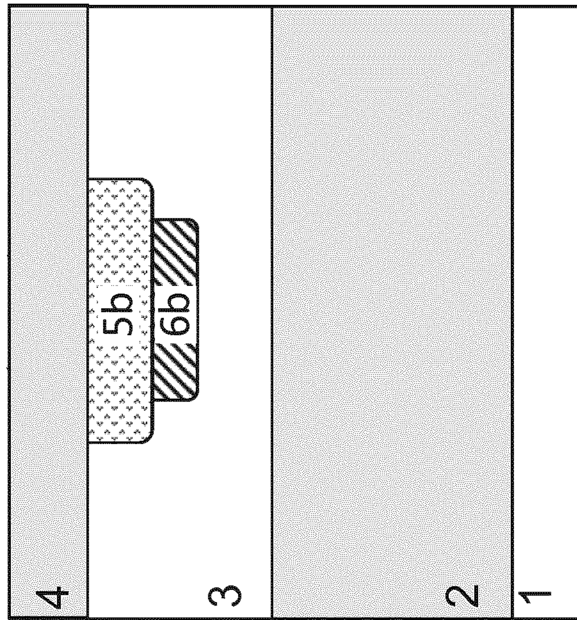

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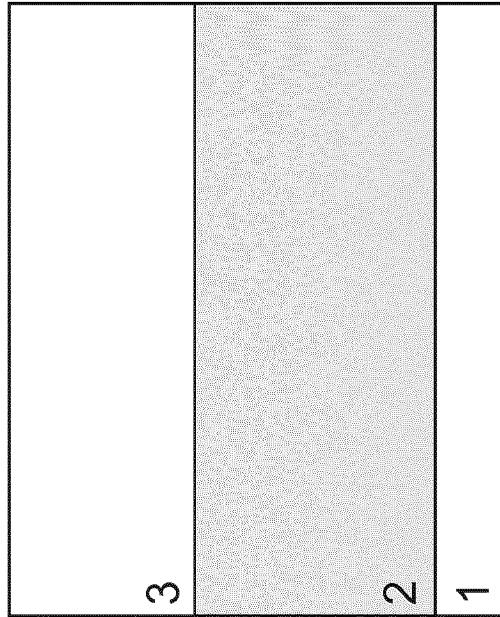

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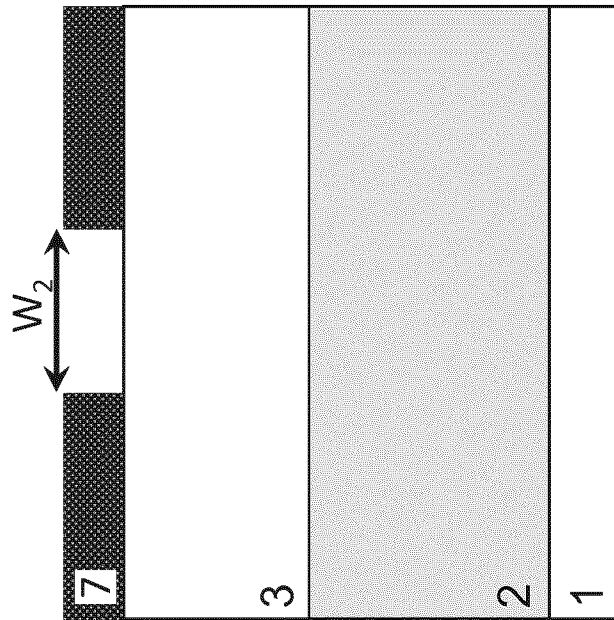

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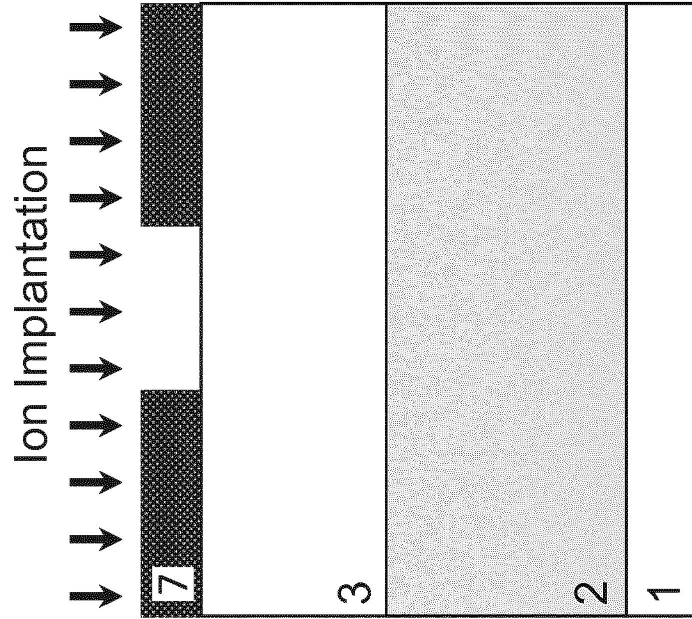

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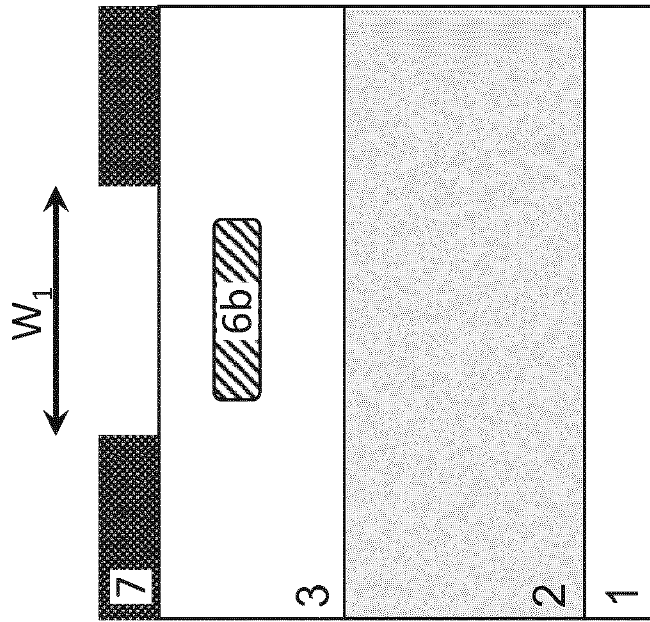

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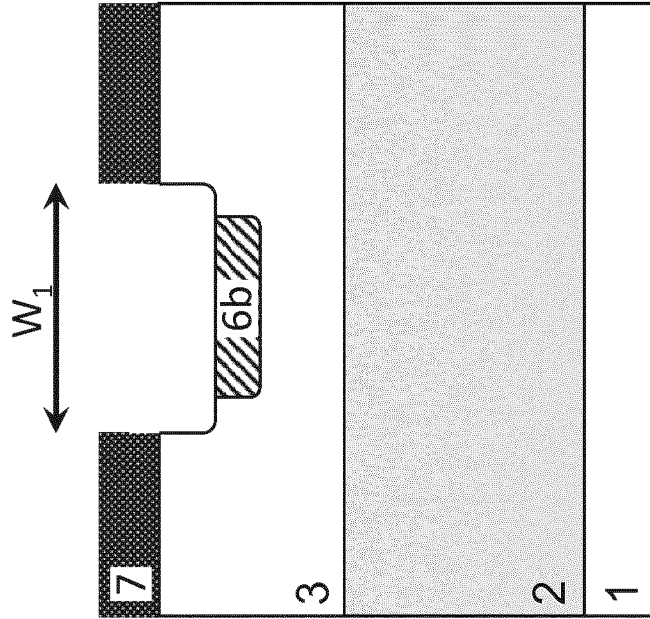

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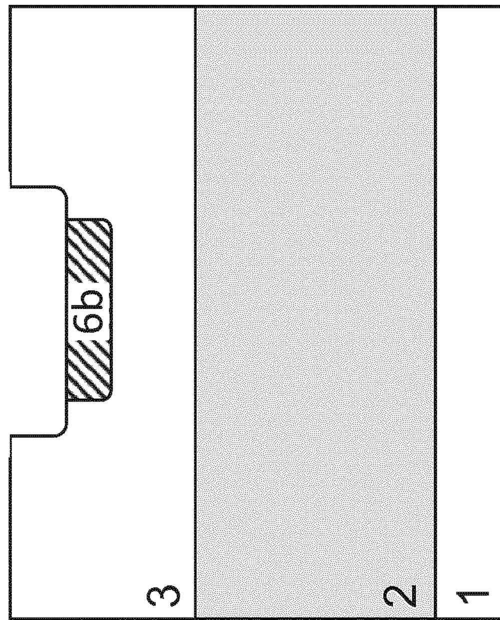

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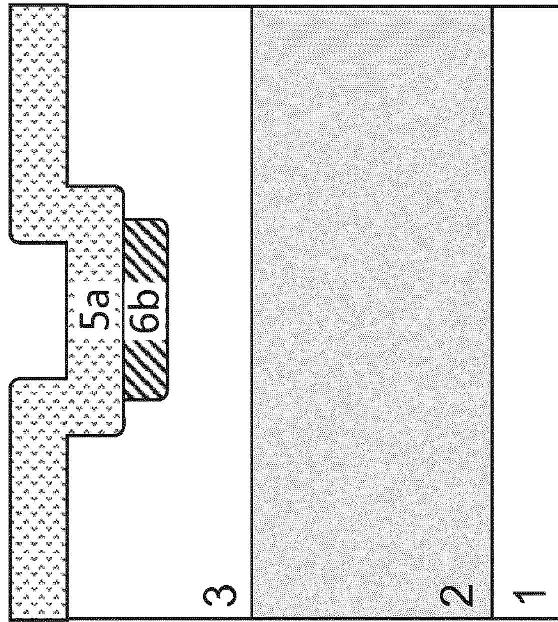

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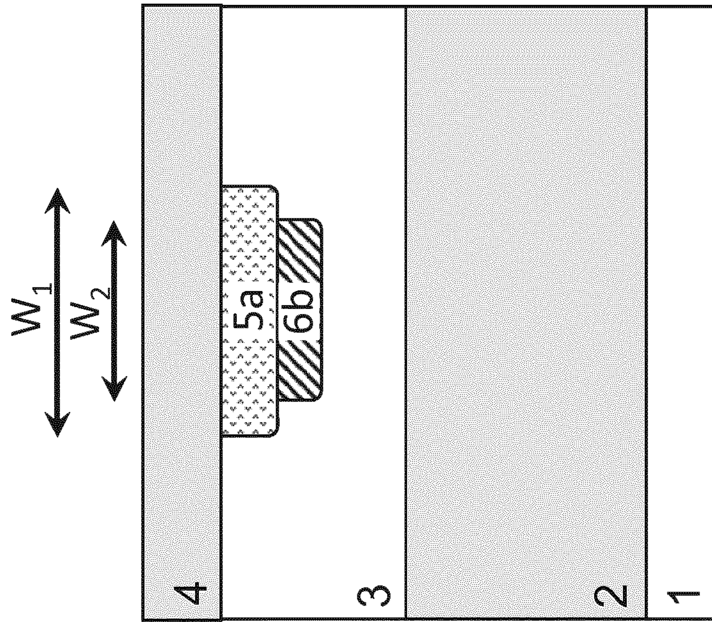

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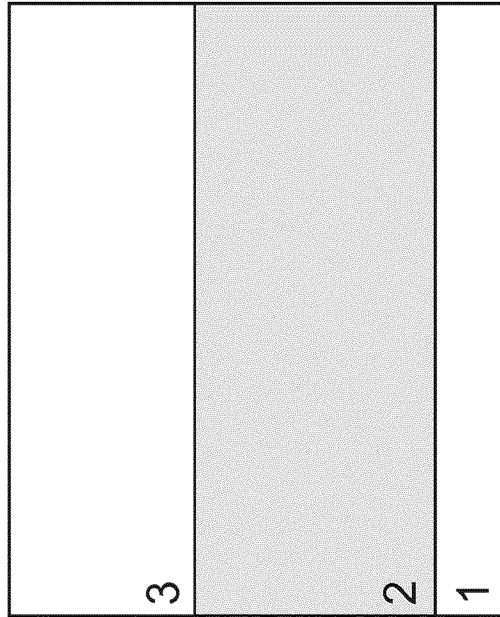

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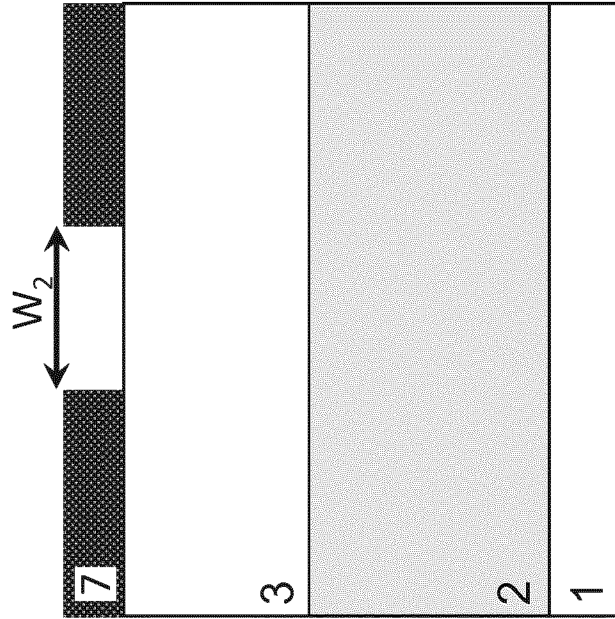
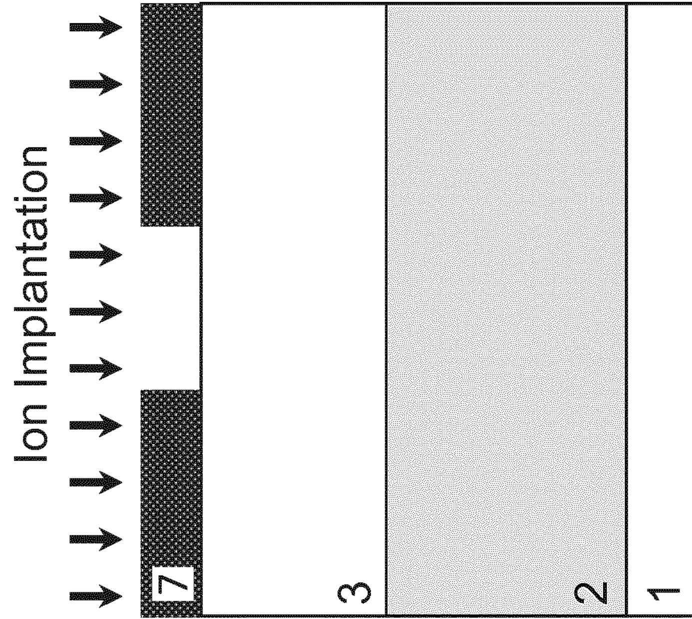


Fig 4-24



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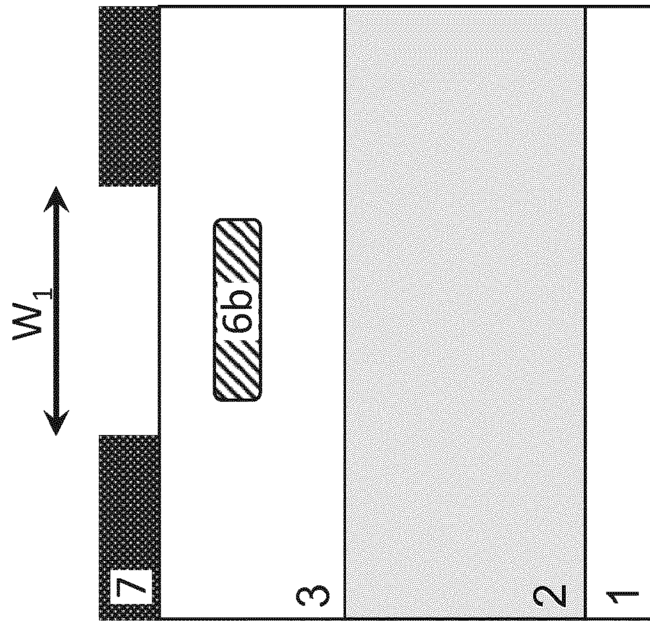

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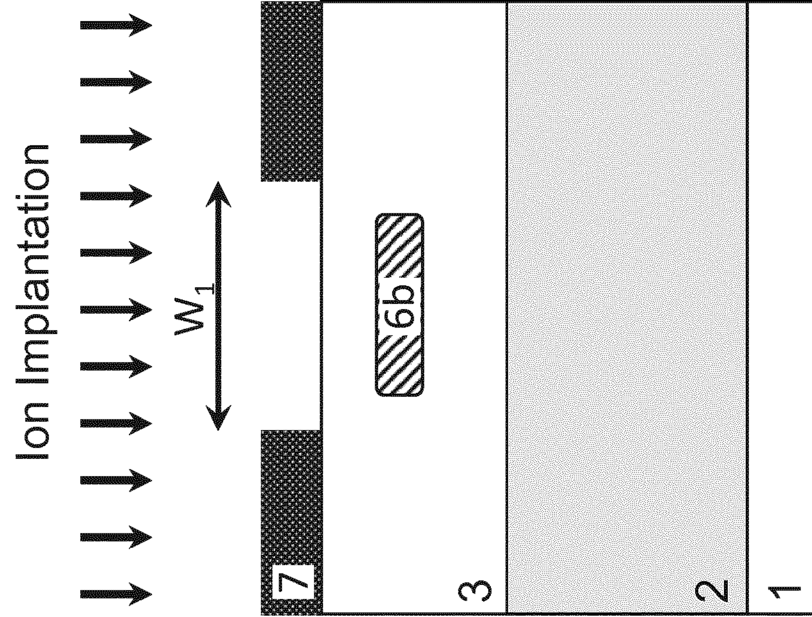

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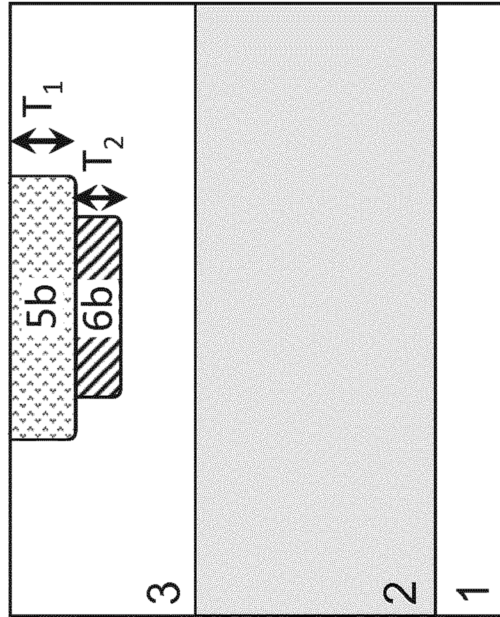

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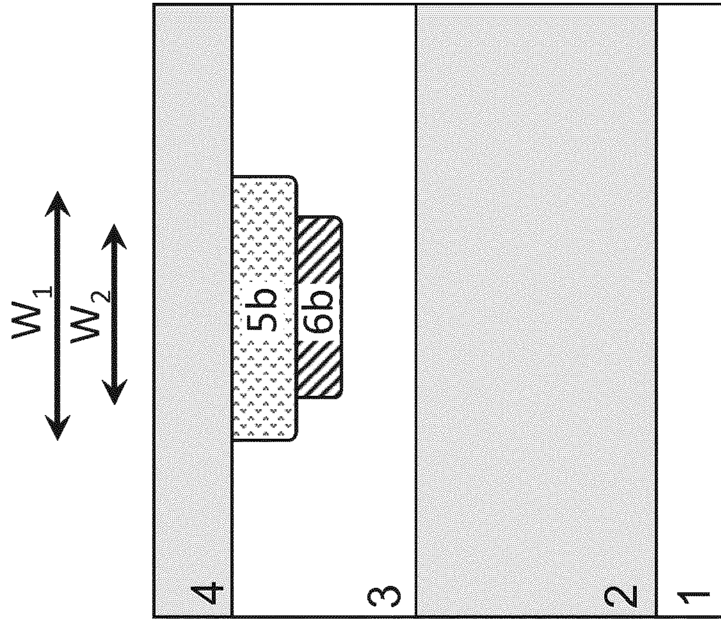

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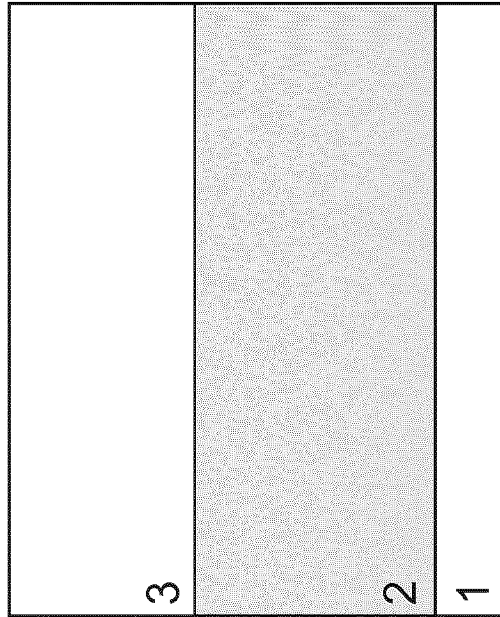
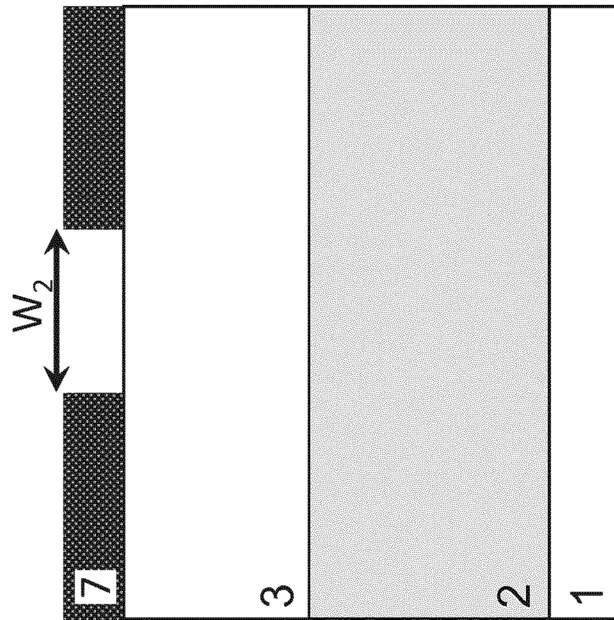


Fig 4-30



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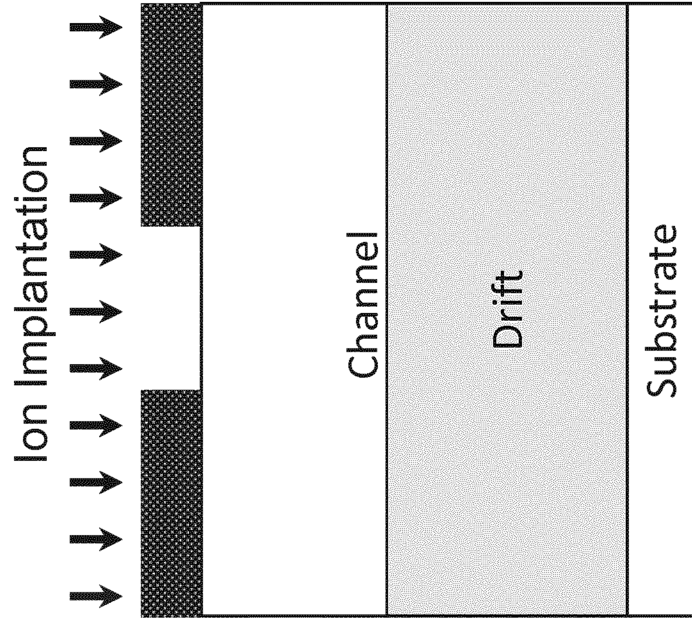

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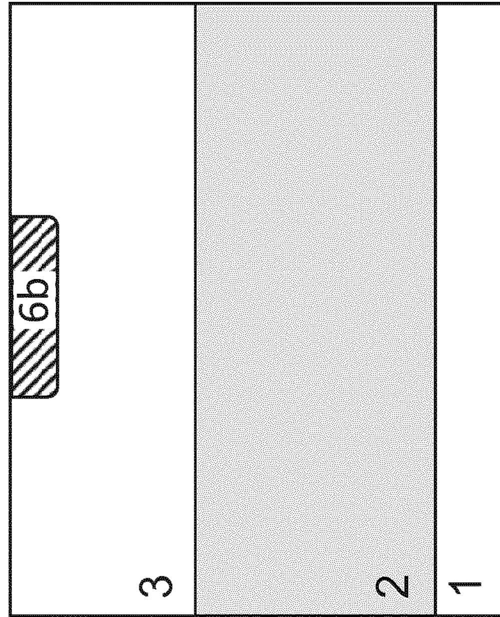

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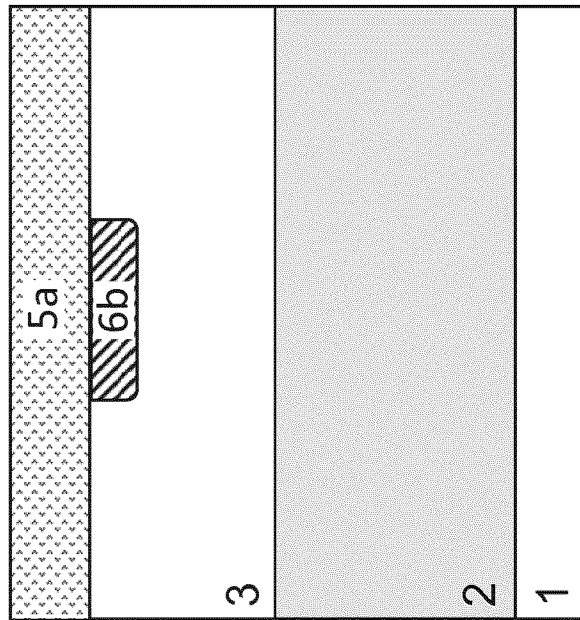

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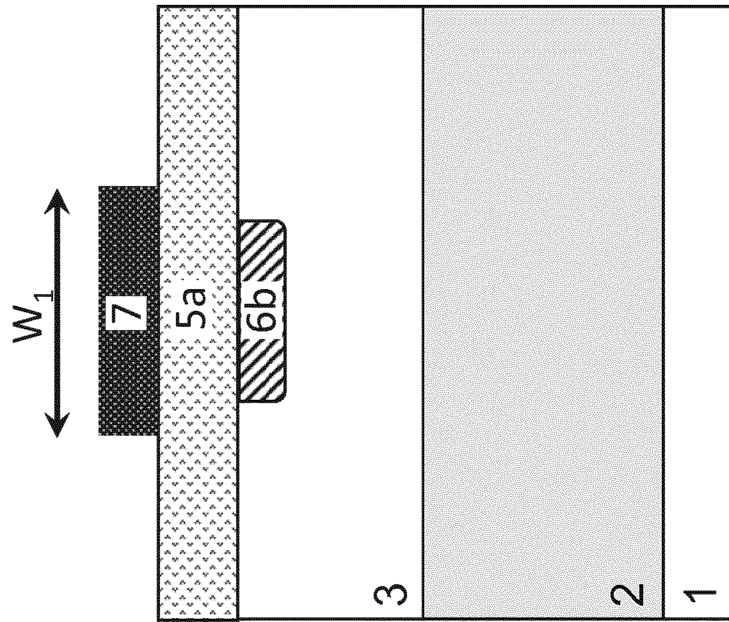

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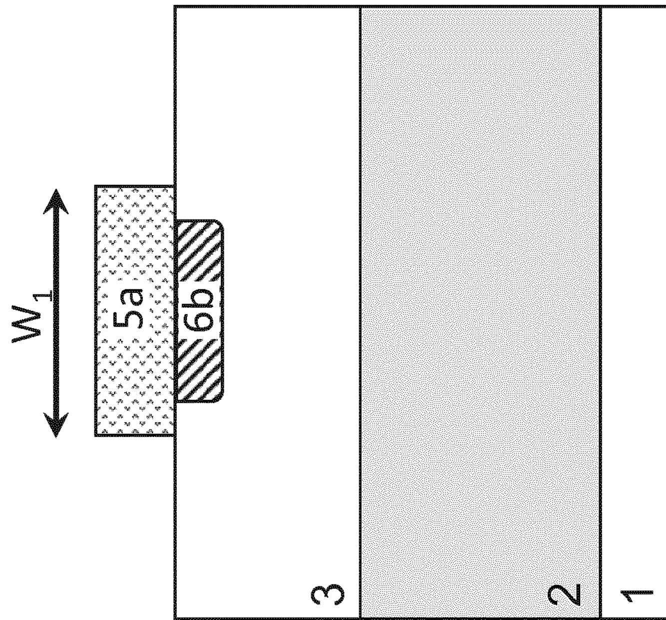

Fig 4-36

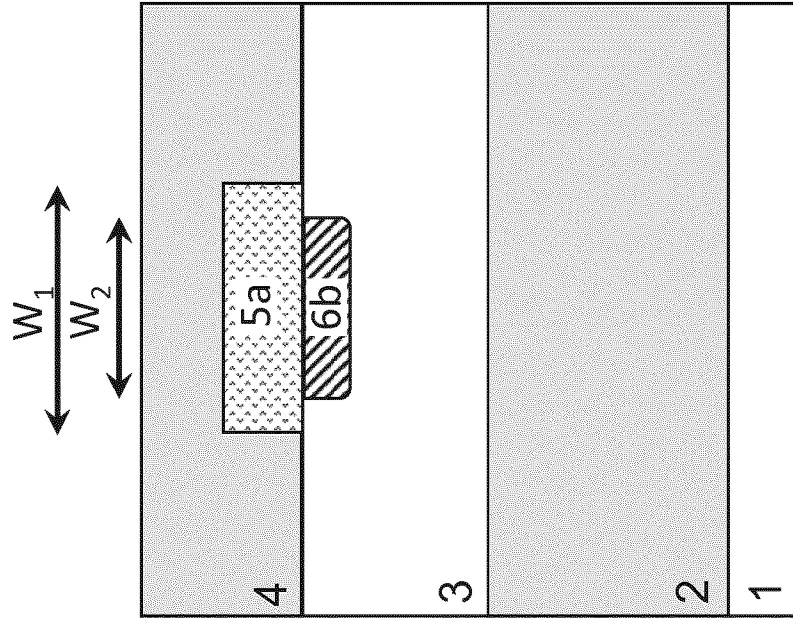

Fig 4-37

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2018/074907

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L29/872 H01L21/329 H01L29/16 H01L29/06 H01L29/36 H01L21/266
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2009/146209 A1 (AKIYAMA MIWAKO [JP] ET AL) 11 June 2009 (2009-06-11)	1,4-6, 8-10, 12-14,16
A	Fig. 1,3,4,7 and 8 and the related text; paragraph [0092]	15,17,18

X	US 2015/048384 A1 (TANAKA RINA [JP] ET AL) 19 February 2015 (2015-02-19)	1,3,4, 6-8, 10-13
A	paragraphs [0034] - [0047], [0089]; figures 1,3,15	15,17,18

X	JP 2003 069040 A (DENSO CORP) 7 March 2003 (2003-03-07)	1,4,5, 7-10,12, 13
A	Fig. 8 and 9 and the related text	15,17,18

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[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
16 November 2018	29/11/2018

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2, NL - 2280 HV Rijswijk, Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Melodia, Andrea

1

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X A	WO 2016/204035 A1 (SUMITOMO ELECTRIC INDUSTRIES [JP]) 22 December 2016 (2016-12-22) Fig. 19-21 and the related text -----	1,2,5,7, 8,10,12, 13 15,17,18
A	US 6 897 133 B2 (ST MICROELECTRONICS SA [FR]) 24 May 2005 (2005-05-24) cited in the application figures 3A-3C -----	12,13
A	JP H03 289141 A (NISSAN MOTOR) 19 December 1991 (1991-12-19) Fig. 1(a)-(d) and the related text -----	12

1

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/EP2018/074907

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