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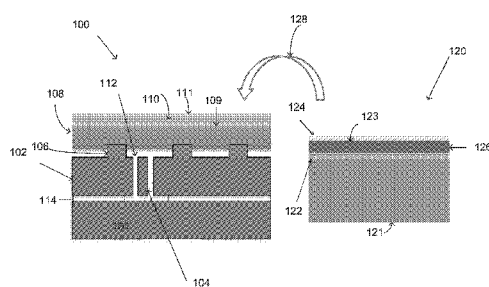


FIG. 1a

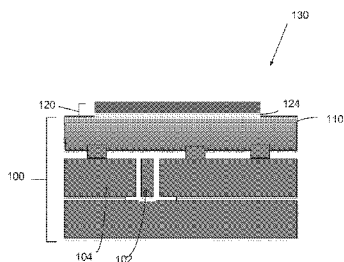


FIG. 1b

(57) Abstract: Methods of forming integrated MEMS structures are described. Those methods and structures may include forming at least one MEMS structure on a first substrate, forming a first bonding layer on a top surface of the first substrate, and then coupling the first bonding layer disposed on the first substrate to a second substrate, wherein the second substrate comprises a device layer. The bonding may comprise a layer transfer process, wherein an integrated MEMS device is formed.

**METHODS OF FORMING BURIED MICROELECTRICOMECHANICAL
STRUCTURES COUPLED WITH DEVICE SUBSTRATES AND STRUCTURES
FORMED THEREBY**

5 BACK GROUND OF THE INVENTION

As microelectronic technology advances for higher performance, increasing number of sensors, such as accelerometers, gyroscopes and compasses, for example, are being used in such applications as mobile phones and tablets. Many different types of microelectronic devices/chips, such as complementary metal oxide semiconductor (CMOS) chips, for example, may be used
10 together with such sensors in many computing and communication platforms.

BRIEF DESCRIPTION OF THE DRAWINGS

While the specification concludes with claims particularly pointing out and distinctly claiming certain embodiments, the advantages of these embodiments can be more readily
15 ascertained from the following description of the invention when read in conjunction with the accompanying drawings in which:

FIGS. 1a-1b represent cross-sectional views of structures according to various embodiments.

FIGS. 2a-2g represent cross-sectional views of structures according to embodiments.

20 FIG. 2h represents a flow chart of a method according to embodiments.

FIG. 3 represents a cross-sectional view of a structure according to embodiments.

FIG. 4 represents a schematic of a system according to embodiments.

DETAILED DESCRIPTION OF THE PRESENT INVENTION

25 In the following detailed description, reference is made to the accompanying drawings that show, by way of illustration, specific embodiments in which the methods and structures may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the embodiments. It is to be understood that the various embodiments, although different, are not necessarily mutually exclusive. For example, a particular feature, structure, or
30 characteristic described herein, in connection with one embodiment, may be implemented within other embodiments without departing from the spirit and scope of the embodiments. In addition, it is to be understood that the location or arrangement of individual elements within each disclosed embodiment may be modified without departing from the spirit and scope of the embodiments. The following detailed description is, therefore, not to be taken in a limiting

sense, and the scope of the embodiments is defined only by the appended claims, appropriately interpreted, along with the full range of equivalents to which the claims are entitled. In the drawings, like numerals may refer to the same or similar functionality throughout the several views.

5 Methods and associated structures of forming and utilizing microelectronic structures, such as integrated microelectromechanical systems (MEMS) structures, are described. Those methods/structures may include forming at least one MEMS structure on a first substrate, forming a first bonding layer on a top surface of the first substrate, and then coupling the first bonding layer disposed on the first substrate to a second substrate, wherein the second substrate
10 comprises a device layer. The bonding may comprise a layer transfer process, wherein an integrated MEMS device is formed. The integrated MEMS structures of the various embodiments disclosed herein enable the decoupling of sensor fabrication from chip/device fabrication.

 FIGS. 1a-1b illustrate cross-sectional views of embodiments of forming microelectronic
15 structures, such as integrated MEMS structures. In an embodiment, a first substrate 100 may comprise any suitable material with which to form at least one MEMS structure. In an embodiment, the first substrate 100 may comprise at least one of a silicon on insulator material, a non-silicon material, a single crystal silicon material, a polysilicon material, a piezoelectric material and/or other electromechanical transduction sensitive material. The substrate 100 may
20 comprise a fixed element 102, and a moveable element 104. The fixed element 102 may be fixed to a lower portion 101 of the first substrate 100 by the use of an adhesion layer 114.

 The moveable element 104 and the fixed element 102 may comprise portions of a MEMS device(s), wherein the MEMS device may comprise at least one of a sensor, a microsensor, a resonator, an actuator, a microactuator, a transducer, a gyroscope, an accelerometer, and a
25 compass, for example. The first substrate 100 may comprise at least one of any type of MEMS structure, according to a particular application. In general MEMS technology refers to very small or miniaturized mechanical and electro-mechanical devices driven by electricity. The MEMS structures of the first substrate may be formed by any suitable fabrication processes. There may be at least one MEMS devices/structures, and in some cases there may be a plurality of MEMS
30 structures disposed within the first substrate 100, although for purposes of illustration portions of one MEMS is depicted in the figures.

 The first substrate 100 may further comprise at least one pillar structure 106. An upper portion 108 of the first substrate 100 may be disposed on the pillar 106. In an embodiment, the upper portion 108 and the pillar 106 may comprise a high temperature material, such as an

epitaxially grown material, for example. In an embodiment, the pillar and upper portion 106, 108 may comprise an epitaxially grown silicon material. In an embodiment, the upper portion 108 of the first substrate 100 may hermetically seal the at least one MEMS device of the first substrate 100. In an embodiment, the upper portion 108 may surround the perimeter of the MEMS structure 130.

The first substrate 100 may further comprise a first bonding layer 110, that may be disposed on a top surface 109 of the upper portion of the substrate 108. In an embodiment, the first bonding layer 110 may be disposed over substantially the entire top surface 109 of the upper portion 108 of the first substrate 100. In an embodiment, a gap 112 may exist between the lower portion 101 and the upper portion 108 of the first substrate 100. In an embodiment, a second substrate 120 may comprise a donor portion 121, an implanted region 122, and a device layer 126, wherein the device layer 126 may comprise any type of device, such as a microelectronic device/die and a CMOS device/chip.

The device layer 126 may comprise circuitry elements such as transistor structures including trigate and nanowire transistor structures, and any other suitable circuitry elements. The circuitry elements may comprise logic circuitry for use in a processor die, for example. Metallization layers and insulative material may be included in the device layer 126, as well as conductive contacts/bumps that may couple metal layers/interconnects to external devices. In an embodiment, the bumps may comprise copper. In an embodiment, the second substrate 120 may further comprise a second bonding layer 124. In an embodiment, the second bonding layer 124 may comprise any type of material that may be bonded to the first bonding layer 110 of the first substrate 100. In an embodiment, the second bonding layer 124 may be disposed over an entire top surface 123 of the device layer 126. In an embodiment, a layer transfer process 128, which may comprise an oxide to oxide or a metal to metal bonding process, for example, may be employed to bond the first substrate 100 to the second substrate 120 to form an integrated MEMS structure 130 (FIG. 1b). In an embodiment, the second bonding layer 224 may be directly bonded to the device layer 226, and the device layer 226 may be directly bonded to the first bonding layer 210.

In an embodiment, the integrated MEMS structure/device 130 may comprise the first substrate 100 bonded to the second substrate 120, wherein the first bonding layer 110 of the first substrate 100 is bonded to the second bonding layer 124 of the second substrate 120. In an embodiment, the integrated MEMS structure 130 may comprise any suitable types of material for the first and the second substrates, and may comprise any types and numbers of MEMS devices according to the particular application. For example, in an embodiment, device layer of

the second substrate of the integrated MEMS structures 130 may comprise a high voltage integrated circuit (IC) comprising non-silicon materials, and the first substrate 100 may comprise a select sensor. In another embodiment, the device layer of the integrated MEMS structure may comprise a radio frequency (RF) chip.

5 FIGS. 2a-2g depict cross-sectional views of additional embodiments of forming integrated MEMS structures. In FIG. 2a, a substrate 200, which may comprise a silicon on insulator substrate 200 in an embodiment, may comprise a fixed element 202 and a moveable element 204. The fixed element 202 and the moveable element 204 may comprise portions of at least one MEMS structure/device. In an embodiment, the fixed element 202 may comprise anchors and or
10 electrodes. In an embodiment, the fixed element 202 may be fixed to a lower portion of the substrate 201 by an adhesion layer 214, such as an oxide layer in some cases.

 In an embodiment, a sacrificial conformal material 205 may be formed around the moveable element 204 and on a top surface of the substrate 200 (FIG. 2b). The sacrificial conformal layer 205 may comprise a dielectric material, such as an oxide or nitride dielectric
15 material, for example. The sacrificial conformal material 205 may be patterned and etched using any suitable patterning and etching techniques, to form openings 207, such as contact openings 207, in the sacrificial conformal material 205. In an embodiment, a high temperature material 213 may be formed within the openings 207, and may be formed on a top surface of the sacrificial conformal material 205 (FIG. 2c).

20 In an embodiment, the high temperature material 213 may comprise an epitaxially grown material, such as an epitaxial material comprising silicon, for example, and may be formed/grown at a temperature between about 500 to about 1000 degrees Celsius. In an embodiment, the high temperature material 213 may be patterned and etched to form desired features according to the particular application. The sacrificial conformal material 205 may be
25 subsequently removed from the substrate 200 using any suitable removal/etching technique (FIG. 2d). In an embodiment, the sacrificial conformal material 205 may be removed utilizing a vapor HF etching process, for example. In an embodiment, pillar structures 206 and an upper portion 208 comprising the high temperature material may be formed.

 A gap (which may comprise an air gap) may exist around the moveable element 204 and
30 between the pillar structures 206. The pillar structures 206 and the upper portion 208 of the high temperature material may provide a seal for the substrate 200 comprising the MEMS devices, and may further comprise a hermetic seal. The high temperature material may surround a perimeter of the first substrate comprising the MEMS devices in an embodiment.

A bonding layer 210 may be formed on a top surface 209 of the upper portion 208 of the high temperature material (FIG. 2e). The bonding layer 210 may comprise any suitable material with which to bond the first substrate 200, with another substrate, by utilizing a bonding process, such as a layer transfer process. In an embodiment, the bonding layer 210 may comprise a dielectric layer, such as a chemical vapor deposition (CVD) dielectric material or a thermally grown oxide or nitride material. In another embodiment, the bonding layer 210 may comprise a polished silicon material, or a conductive material, such as a metal.

In an embodiment, the first substrate 200 may be bonded to a second substrate 220 (FIG. 2f). In an embodiment, a top surface of a second bonding layer 224 disposed on a device layer 226 of the second substrate 220 may be bonded with the top surface 211 of the first bonding layer 210 utilizing a layer transfer process 228. In an embodiment, the second bonding layer 224 may comprise any material that is capable of bonding with the first bonding layer 210. In an embodiment, the second bonding layer 224 may comprise such materials as a dielectric material, such as a CVD or a thermally grown oxide or nitride material, a polished silicon material, or a conductive material. The second substrate 220 may further comprise a separating layer 222, which may comprise an ion implanted layer, such as a hydrogen implanted layer, in some cases, wherein the separating layer 222 may be cleaved/separated from a donor portion 221 of the second substrate 220.

In an embodiment, the second substrate 220 may be layer transferred utilizing the layer transfer process 228 to bond with the first substrate 200, wherein the device layer 226 is joined to the first substrate 200 by the bonding between the first and second bonding layers 210, 224 (FIG. 2g). The donor portion 221 of the second substrate 220 may be removed/separated from the second substrate 220 by cleaving the donor portion 221 at the separating layer 222. Thus, an integrated MEMS device/structure 230 may be formed, wherein the formation of the MEMS structures are decoupled from the device layer 226 fabrication. The device layer 226 may comprise any type of device, such as a CMOS device, an RF IC, a high voltage IC etc.

In an embodiment, further patterning and etching may be performed on the integrated MEMS device 130, wherein conductive contacts may be formed between portions of the MEMS structures of the first substrate 200 and portions/devices of the device layer 226 of the second substrate 220. For example, conductive contact structures may be formed between at least one of a transistor, a capacitor and a resistor of the device layer 226 and the moveable element 204 of the first substrate 200. In an embodiment, the bonding layers 210, 224 may provide isolation for such conductive contact structures. In an embodiment, the integrated MEMS device 130 may be

further coupled with additional devices/die, and may comprise a portion of a system on a chip, either alone or combined with additional chips/devices so coupled, in some embodiments.

FIG. 2h depicts a flow chart of a method of forming an integrated MEMS structure according to another embodiment. At step 250, at least one MEMS structure may be formed on a first substrate. At step 260 a first bonding layer may be formed on the first substrate. At step 270, the first bonding layer on the first substrate may be coupled to a second bonding layer of a second substrate, wherein the second substrate comprises a device layer. At step 280, conductive contacts may be formed between the at least one MEMS structure and the device layer.

In an embodiment, the device layer may comprise one of a microelectronic memory die and a central processing unit die in some cases, but may comprise any type of suitable device according to the particular application in other cases. In an embodiment, the device layer may be further coupled with a package structure, such as an organic core package, and a coreless, bumpless build up layer (BBUL) package structure.

In an embodiment, the device layer may be coupled with any suitable type of package structures capable of providing electrical communications between a microelectronic device, such as a die and a next-level component to which the package structures may be coupled (e.g., a circuit board). In another embodiment, the device layer may be coupled with a package structure that may comprise any suitable type of package structures capable of providing electrical communication between a die and an upper integrated circuit (IC) package coupled with the device layer.

A device layer described in the various Figures herein may comprise a silicon logic die or a memory die, for example, or any type of suitable microelectronic device/die. In some embodiments the device layer may further comprise a plurality of dies, which may be stacked upon one another, depending upon the particular embodiment. In some cases the die(s) of the device layer may be located/attached/embedded on either the front side, back side or on/in some combination of the front and back sides of a package structure. In an embodiment, the die(s) may be partially or fully embedded in a package structure of the embodiments.

The various embodiments of the integrated MEMS structures included herein enable the decoupling of device fabrication, such as CMOS fabrication, and MEMS fabrication. The embodiments also allow for the continued decrease in scale of device layer circuitry without impacting MEMS feature size. By decoupling MEMS fabrication, hermetic seal formation is enabled because of the incorporation of a high temperature epitaxial seal. High voltage IC's with select sensors utilizing non-Silicon CMOS, as well as RF filters and RF switch applications are enabled, which may operate above about 31.8 GHz, for example. Inertial sensors such as

accelerometers and gyroscopes can be implemented with a chipset or a system on a chip. Timing resonators are enabled that may be buried under the CMOS for use in mobile communication IC's for lower power applications and improved system performance.

Turning now to FIG. 3, illustrated is an embodiment of a computing system 300. The system 300 includes a number of components disposed on a mainboard 310 or other circuit board. Mainboard 310 includes a first side 312 and an opposing second side 314, and various components may be disposed on either one or both of the first and second sides 312, 314. In the illustrated embodiment, the computing system 300 includes a package structure 340 disposed on the mainboard's first side 312, wherein the package structure 340 may comprise any of the integrated MEMS structure embodiments described herein.

System 300 may comprise any type of computing system, such as, for example, a hand-held or mobile computing device (e.g., a cell phone, a smart phone, a mobile internet device, a music player, a tablet computer, a laptop computer, a nettop computer, etc.). However, the disclosed embodiments are not limited to hand-held and other mobile computing devices and these embodiments may find application in other types of computing systems, such as desk-top computers and servers.

Mainboard 310 may comprise any suitable type of circuit board or other substrate capable of providing electrical communication between one or more of the various components disposed on the board. In one embodiment, for example, the mainboard 310 comprises a printed circuit board (PCB) comprising multiple metal layers separated from one another by a layer of dielectric material and interconnected by electrically conductive vias. Any one or more of the metal layers may be formed in a desired circuit pattern to route – perhaps in conjunction with other metal layers – electrical signals between the components coupled with the board 310. However, it should be understood that the disclosed embodiments are not limited to the above-described PCB and, further, that mainboard 310 may comprise any other suitable substrate.

In addition to the package structure 340, one or more additional components may be disposed on either one or both sides 312, 314 of the mainboard 310. By way of example, as shown in the figures, components 301a may be disposed on the first side 312 of the mainboard 310, and components 301b may be disposed on the mainboard's opposing side 314. Additional components that may be disposed on the mainboard 310 include other IC devices (e.g., processing devices, memory devices, signal processing devices, wireless communication devices, graphics controllers and/or drivers, audio processors and/or controllers, etc.), power delivery components (e.g., a voltage regulator and/or other power management devices, a power supply such as a battery, and/or passive devices such as a capacitor), and one or more user

interface devices (e.g., an audio input device, an audio output device, a keypad or other data entry device such as a touch screen display, and/or a graphics display, etc.), as well as any combination of these and/or other devices.

In one embodiment, the computing system 300 includes a radiation shield. In a further embodiment, the computing system 300 includes a cooling solution. In yet another embodiment, the computing system 300 includes an antenna. In yet a further embodiment, the assembly 300 may be disposed within a housing or case. Where the mainboard 310 is disposed within a housing, some of the components of computer system 300 – e.g., a user interface device, such as a display or keypad, and/or a power supply, such as a battery – may be electrically coupled with the mainboard 310 (and/or a component disposed on this board) but may be mechanically coupled with the housing.

FIG. 4 is a schematic of a computer system 400 according to an embodiment. The computer system 400 (also referred to as the electronic system 400) as depicted can embody/include a package structure/integrated MEMS structure that includes any of the several disclosed embodiments and their equivalents as set forth in this disclosure. The computer system 400 may be a mobile device such as a netbook computer. The computer system 400 may be a mobile device such as a wireless smart phone. The computer system 400 may be a desktop computer. The computer system 400 may be a hand-held reader. The computer system 400 may be integral to an automobile. The computer system 400 may be integral to a television.

In an embodiment, the electronic system 400 is a computer system that includes a system bus 420 to electrically couple the various components of the electronic system 400. The system bus 420 is a single bus or any combination of busses according to various embodiments. The electronic system 400 includes a voltage source 430 that provides power to the integrated circuit 410. In some embodiments, the voltage source 430 supplies current to the integrated circuit 410 through the system bus 420.

The integrated circuit 410 is electrically, communicatively coupled to the system bus 420 and includes any circuit, or combination of circuits according to an embodiment, including the package/device of the various embodiments included herein. In an embodiment, the integrated circuit 410 includes a processor 412 that can include any type of packaging structures according to the embodiments herein. As used herein, the processor 412 may mean any type of circuit such as, but not limited to, a microprocessor, a microcontroller, a graphics processor, a digital signal processor, or another processor. In an embodiment, the processor 412 includes any of the embodiments of the package structures disclosed herein. In an embodiment, SRAM embodiments are found in memory caches of the processor.

Other types of circuits that can be included in the integrated circuit 410 are a custom circuit or an application-specific integrated circuit (ASIC), such as a communications circuit 414 for use in wireless devices such as cellular telephones, smart phones, pagers, portable computers, two-way radios, and similar electronic systems. In an embodiment, the processor 412 includes on-die memory 416 such as static random-access memory (SRAM). In an embodiment, the processor 412 includes embedded on-die memory 416 such as embedded dynamic random-access memory (eDRAM).

In an embodiment, the integrated circuit 410 is complemented with a subsequent integrated circuit 411. In an embodiment, the dual integrated circuit 411 includes embedded on-die memory 417 such as eDRAM. The dual integrated circuit 411 includes an RFIC dual processor 413 and a dual communications circuit 415 and dual on-die memory 417 such as SRAM. The dual communications circuit 415 may be configured for RF processing.

At least one passive device 480 is coupled to the subsequent integrated circuit 411. In an embodiment, the electronic system 400 also includes an external memory 440 that in turn may include one or more memory elements suitable to the particular application, such as a main memory 442 in the form of RAM, one or more hard drives 444, and/or one or more drives that handle removable media 446, such as diskettes, compact disks (CDs), digital variable disks (DVDs), flash memory drives, and other removable media known in the art. The external memory 440 may also be embedded memory 448. In an embodiment, the electronic system 400 also includes a display device 450, and an audio output 460. In an embodiment, the electronic system 400 includes an input device such as a controller 470 that may be a keyboard, mouse, touch pad, keypad, trackball, game controller, microphone, voice-recognition device, or any other input device that inputs information into the electronic system 400. In an embodiment, an input device 470 includes a camera. In an embodiment, an input device 470 includes a digital sound recorder. In an embodiment, an input device 470 includes a camera and a digital sound recorder.

Although the foregoing description has specified certain steps and materials that may be used in the methods of the embodiments, those skilled in the art will appreciate that many modifications and substitutions may be made. Accordingly, it is intended that all such modifications, alterations, substitutions and additions be considered to fall within the spirit and scope of the embodiments as defined by the appended claims. In addition, the Figures provided herein illustrate only portions of exemplary microelectronic devices and associated package structures that pertain to the practice of the embodiments. Thus the embodiments are not limited to the structures described herein.

IN THE CLAIMS

What is claimed is:

1. A method of forming a structure comprising:
forming at least one MEMS structure on a first substrate;
5 forming a first bonding layer on a top surface of the first substrate; and
coupling the first bonding layer disposed on the first substrate to a second substrate, wherein the coupling is achieved utilizing a layer transfer process, to form an integrated MEMS structure.
- 10 2. The method of claim 1 further comprising wherein the at least one MEMS structure comprises at least one of a resonator, an actuator, a gyroscope, a sensor, an accelerometer, a compass, a moving element.
3. The method of claim 1 further comprising wherein the first substrate comprises a
15 single crystal silicon substrate.
4. The method of claim 1 further comprising wherein the first substrate is hermetically sealed utilizing a process above about 1000 degrees Celsius.
- 20 5. The method of claim 4 further comprising wherein the first substrate is sealed utilizing an epitaxial silicon process, wherein the epitaxial silicon is disposed over substantially the entire top surface of an upper portion of the first substrate.
6. The method of claim 1 further comprising wherein the second substrate comprises a
25 device layer.
7. The method of claim 1 further comprising wherein the first bonding layer comprises one of a metal and an oxide layer.
- 30 8. The method of claim 1 further comprising wherein the second substrate comprises a high voltage IC.
9. The method of claim 1 further comprising wherein the second substrate comprises one of a CMOS and an RF device.

10. The method of claim 1 further comprising wherein the first substrate is bonded to the second substrate by utilizing at least one of an oxide to oxide and a metal to metal layer transfer process.

5

11. The method of claim 1 further comprising wherein the second substrate comprises a second bonding layer disposed on substantially an entire top surface of the second substrate.

12. A method of forming a structure comprising:

10

forming a moveable and a fixed structure in a first substrate;

forming a sacrificial conformal material around the fixed structure and on a top surface of the first substrate;

forming openings in the sacrificial material disposed on the top surface of the first substrate;

15

forming a high temperature material in the openings;

forming a first bonding layer on the high temperature material; and

layer transferring the first substrate onto a second substrate, wherein the second substrate comprises a device layer.

20

13. The method of claim 12 further comprising wherein the moveable and fixed structures comprise portions of a MEMS device.

14. The method of claim 12 further comprising wherein the layer transfer comprises an oxide to oxide layer transfer process.

25

15. The method of claim 12 further comprising wherein the high temperature material comprises an epitaxially grown material.

16. The method of claim 12 further comprising wherein the first substrate comprises a silicon on insulator substrate.

30

17. The method of claim 12 further comprising wherein the second substrate comprises a device substrate comprising a second bonding layer on a top surface.

18. The method of claim 17 further comprising wherein the second bonding layer is layer transferred to the first bonding layer of the first substrate.

19. The method of claim 12 further comprising wherein the device layer comprises one
5 of an RFIC and a high voltage IC.

20. The method of claim 12 further comprising wherein the sacrificial material is removed utilizing a vapor HF process.

10 21. The method of claim 12 further comprising wherein a donor wafer is released from the second substrate during the layer transfer process.

22. The method of claim 13 further comprising wherein MEMS devices are coupled to the second substrate by forming conductive contacts between portions of individual device
15 structures within the second substrate and the MEMS structures.

23. A structure comprising:
at least one MEMS structure disposed within a first substrate;
a first bonding layer disposed on a top surface of the first substrate; and
20 a second bonding layer disposed on a surface of a second substrate, wherein the second substrate comprises a device layer, and wherein the first bonding layer is directly bonded to the second bonding layer.

24. The structure of claim 23 further comprising wherein the first bonding layer
25 comprises at least one of a metal layer and an oxide layer, and wherein the first bonding layer is disposed on substantially the entire top surface of the first substrate.

25. The structure of claim 23 further comprising wherein the at least one MEMS structure comprises at least one of a resonator, an actuator, a gyroscope, a sensor, an
30 accelerometer, and a compass.

26. The structure of claim 23 further comprising wherein the first substrate comprises a single crystal silicon substrate.

27. The structure of claim 23 further comprising wherein the first substrate comprises a hermetic seal material around a top surface.

28. The structure of claim 27 further comprising wherein the hermetic sealed comprises
5 an epitaxial material disposed over the top surface of the first substrate.

29. The structure of claim 23 further comprising wherein the second substrate comprises at least one microelectronic die.

10 30. The structure of claim 23 further comprising wherein the first bonding layer comprises one of a metal and an oxide layer, and wherein the second bonding layer comprises a material that is capable of bonding with the first bonding layer.

31. The structure of claim 23 further comprising wherein the second substrate comprises
15 one of a high voltage IC and an RF IC.

32. The structure of claim 23 further comprising wherein the first substrate comprises a silicon on insulator substrate.

20 33. The method of claim 23 further comprising wherein at least one of the MEMS structures are coupled to the device layer by conductive contacts disposed between portions of individual device structures within the device layer and the MEMS structures.

34. The structure of claim 23 wherein the second substrate further comprises at least one
25 of a CPU and a memory die.

35. The structure of claim 23 wherein the second substrate further comprises a portion of a system on a chip.

30 36. The structure of claim 23 further comprising a system comprising:
bus communicatively coupled to the structure; and
an eDRAM communicatively coupled to the bus.

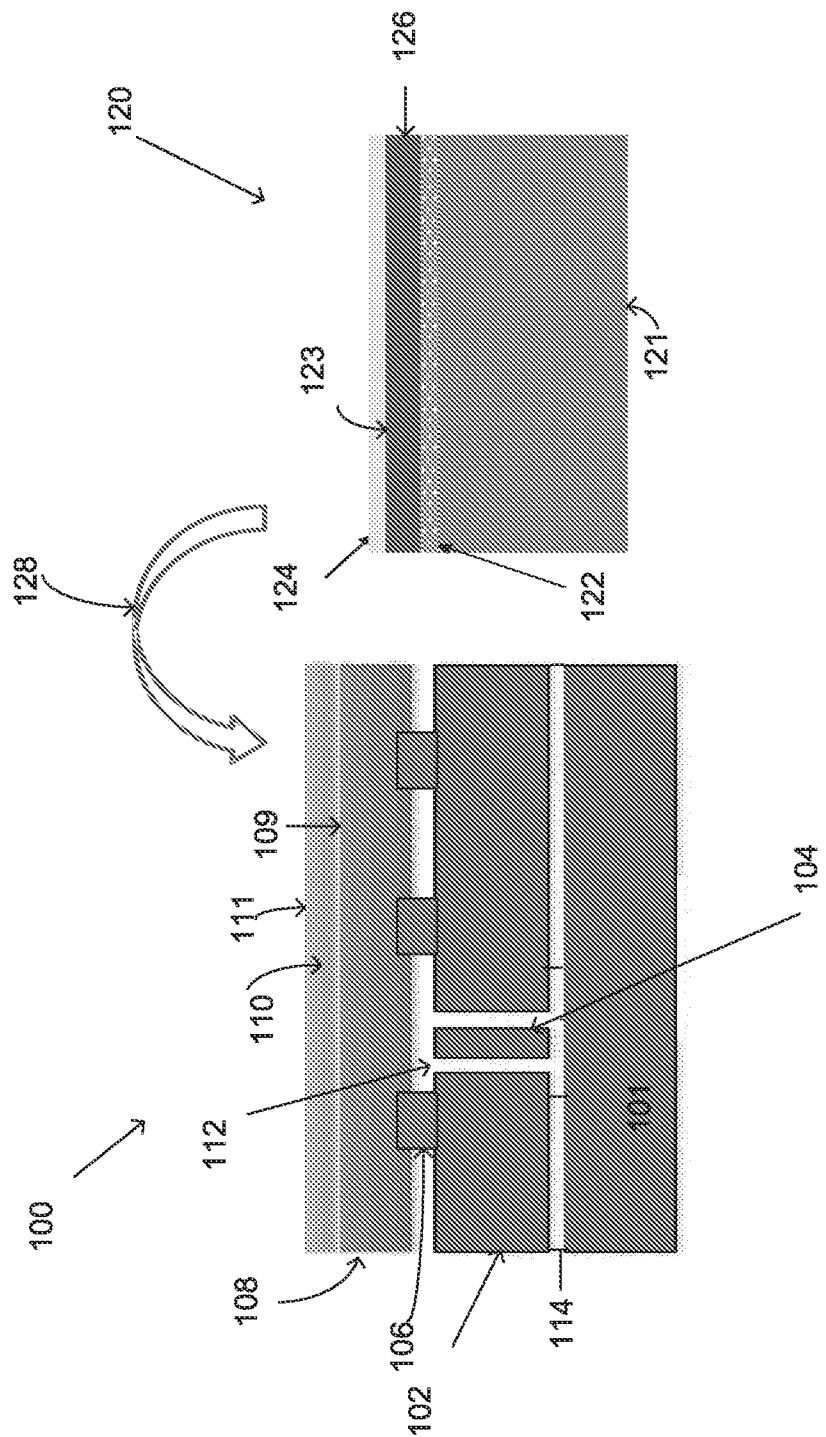


FIG. 1a

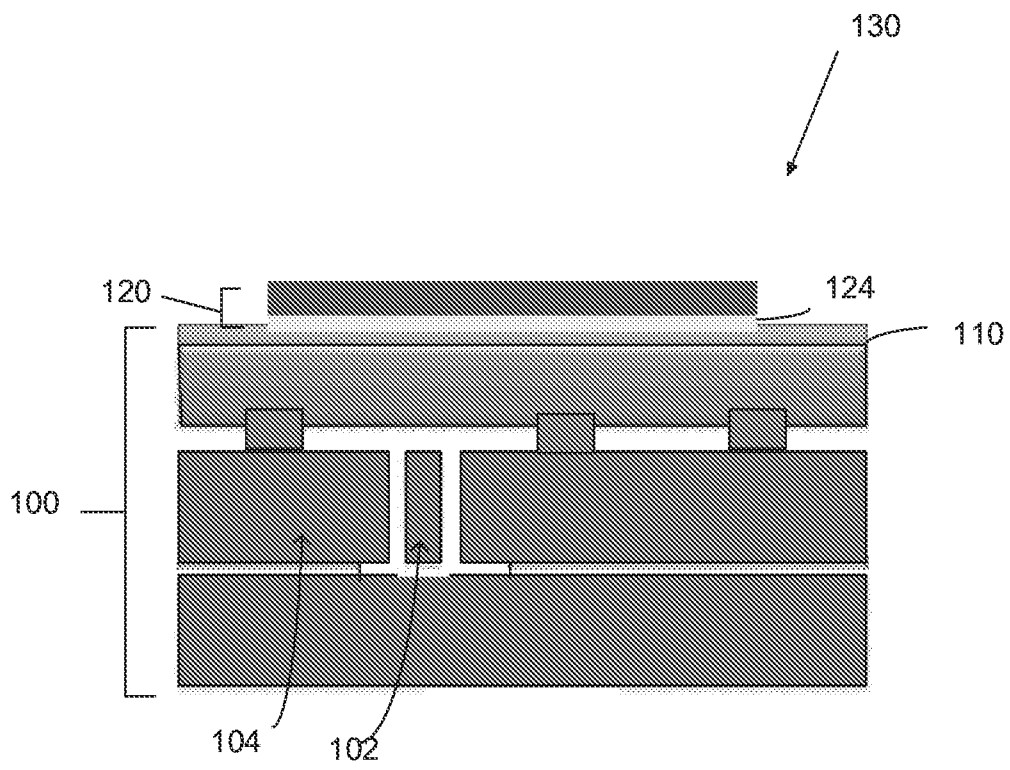


FIG. 1b

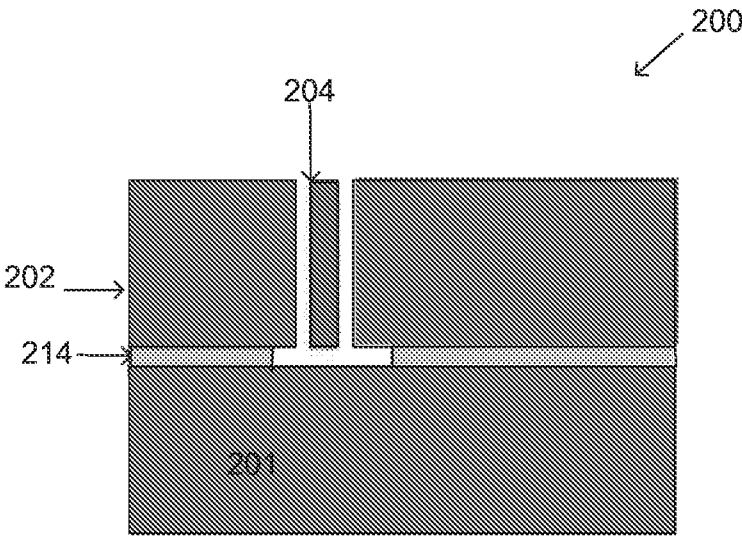


FIG. 2a

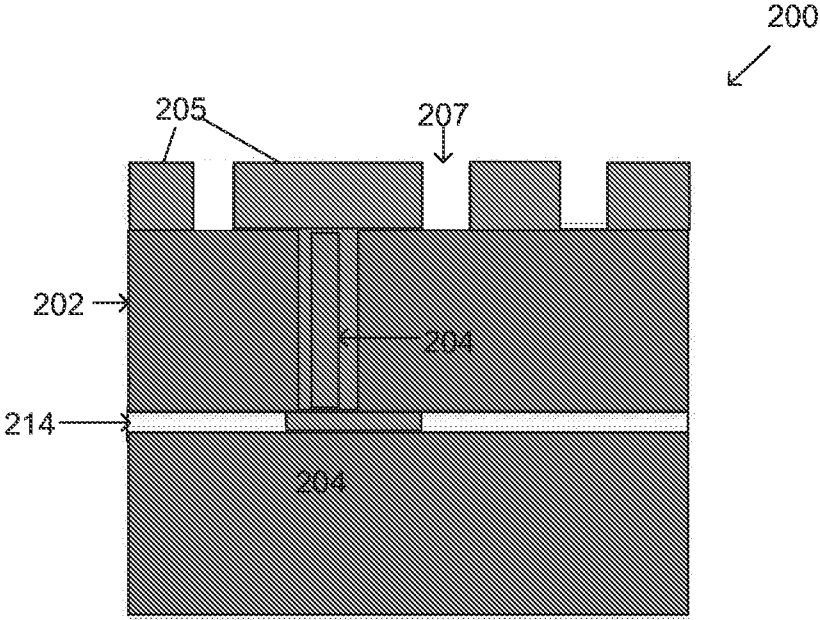


FIG. 2b

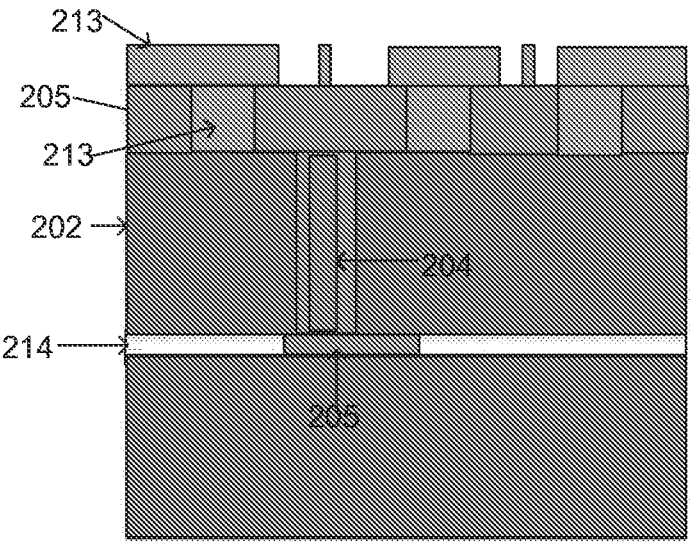


FIG. 2c

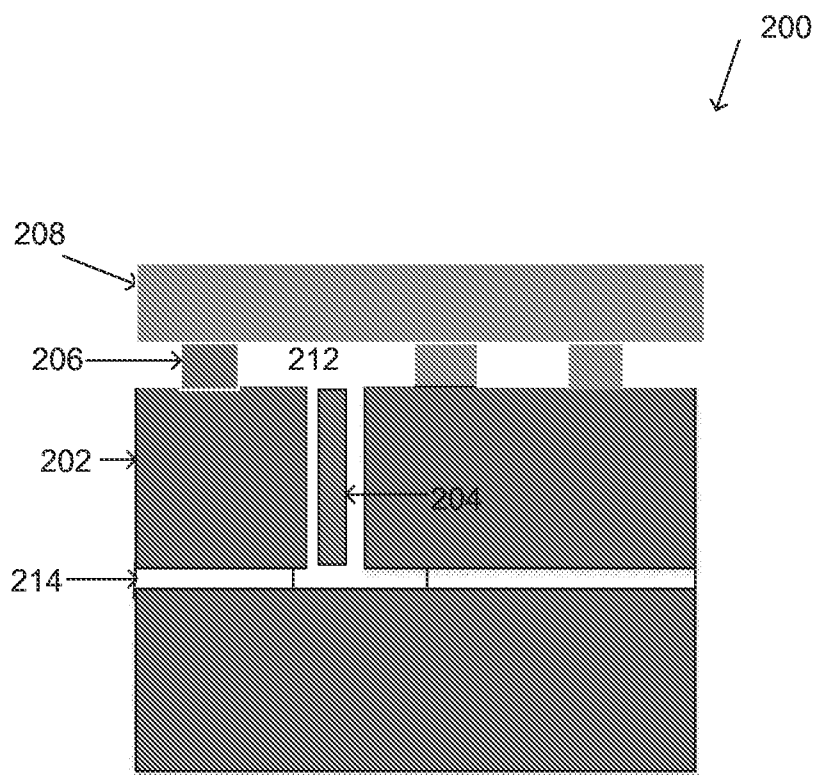


FIG. 2d

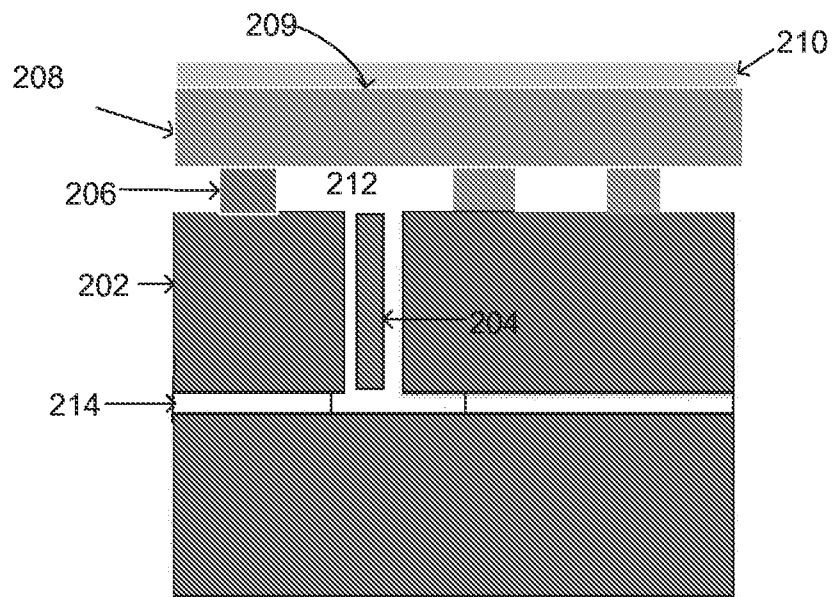


FIG. 2e

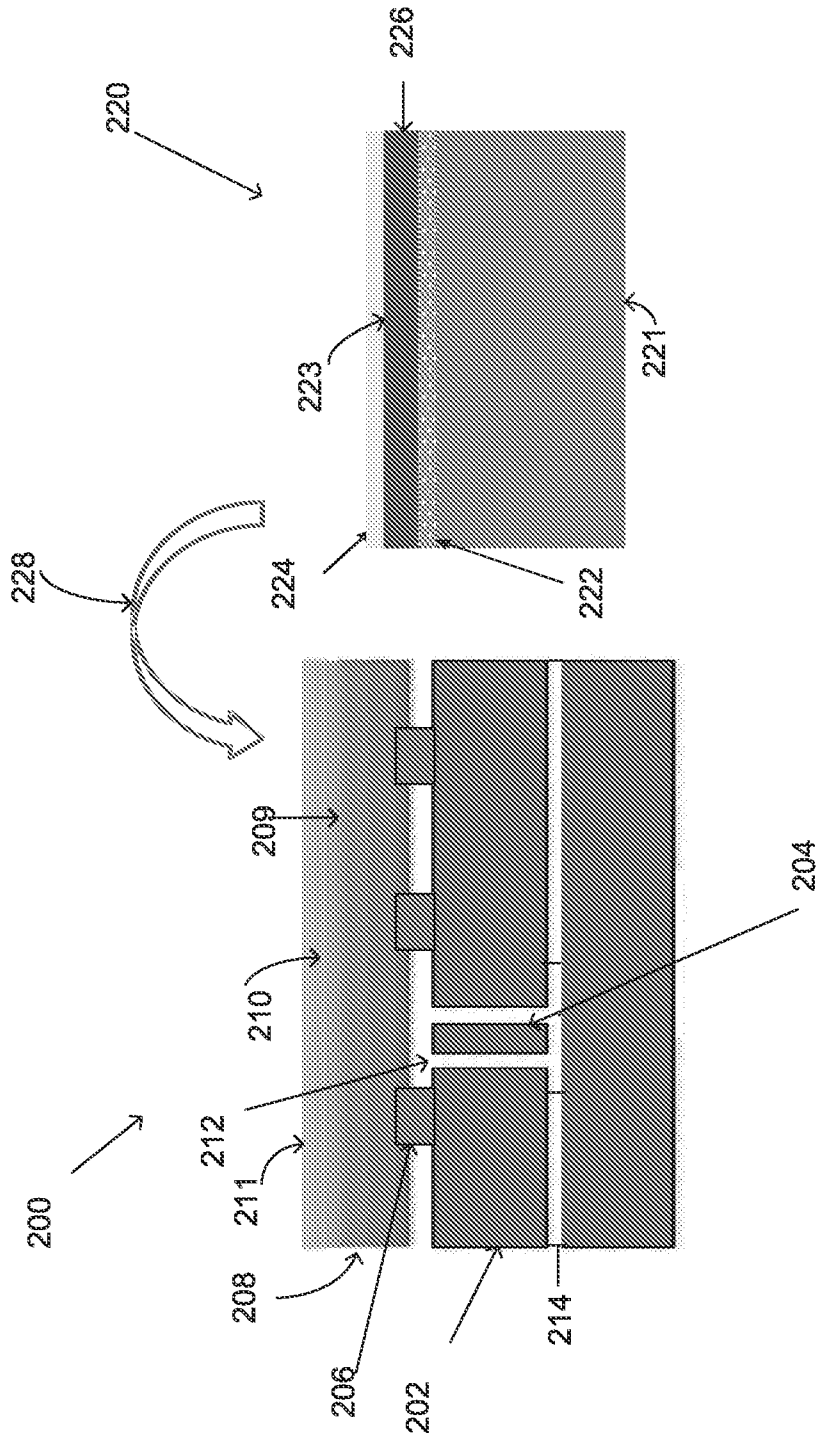


FIG. 2f

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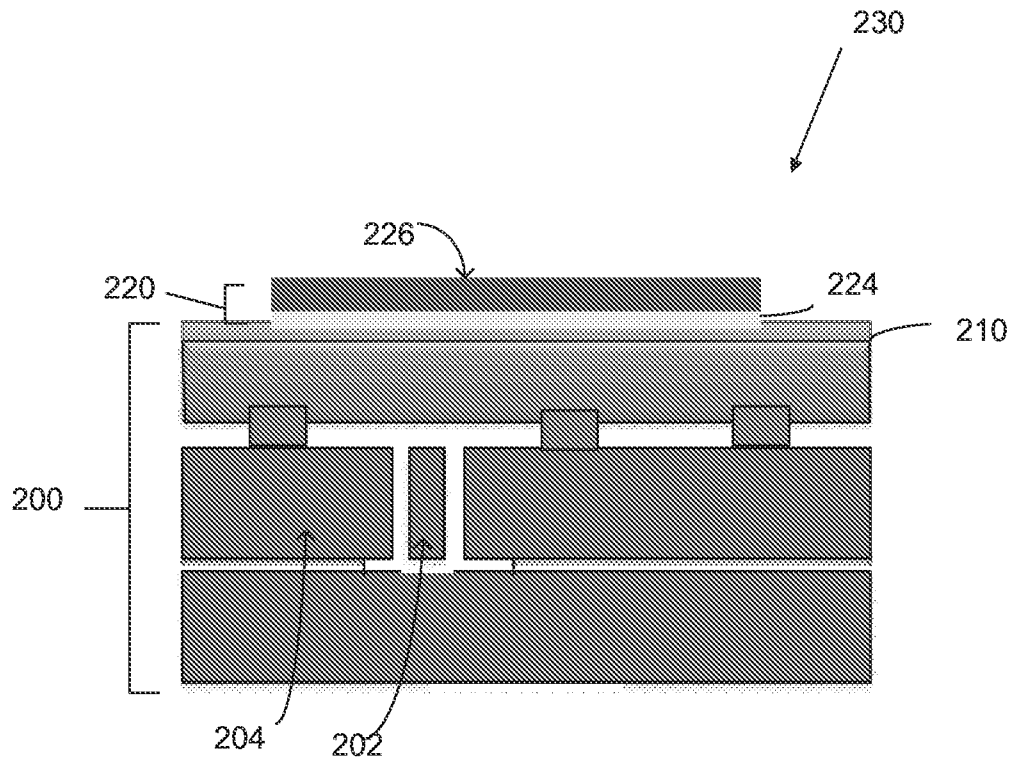


FIG. 2g

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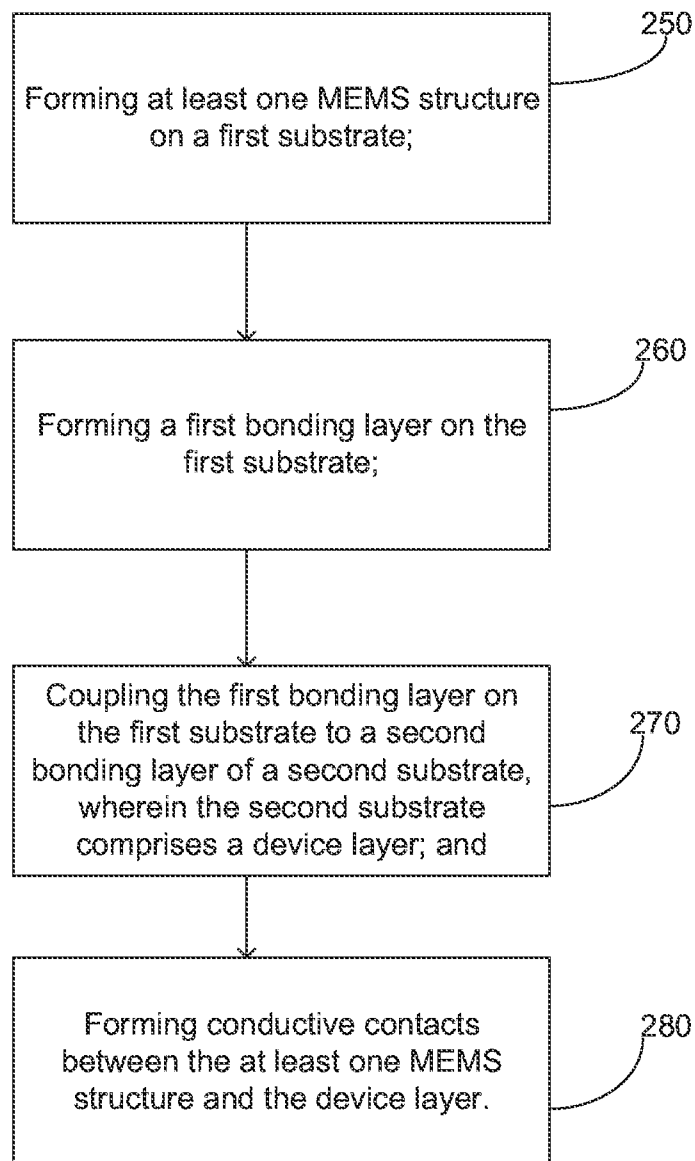


FIG. 2h

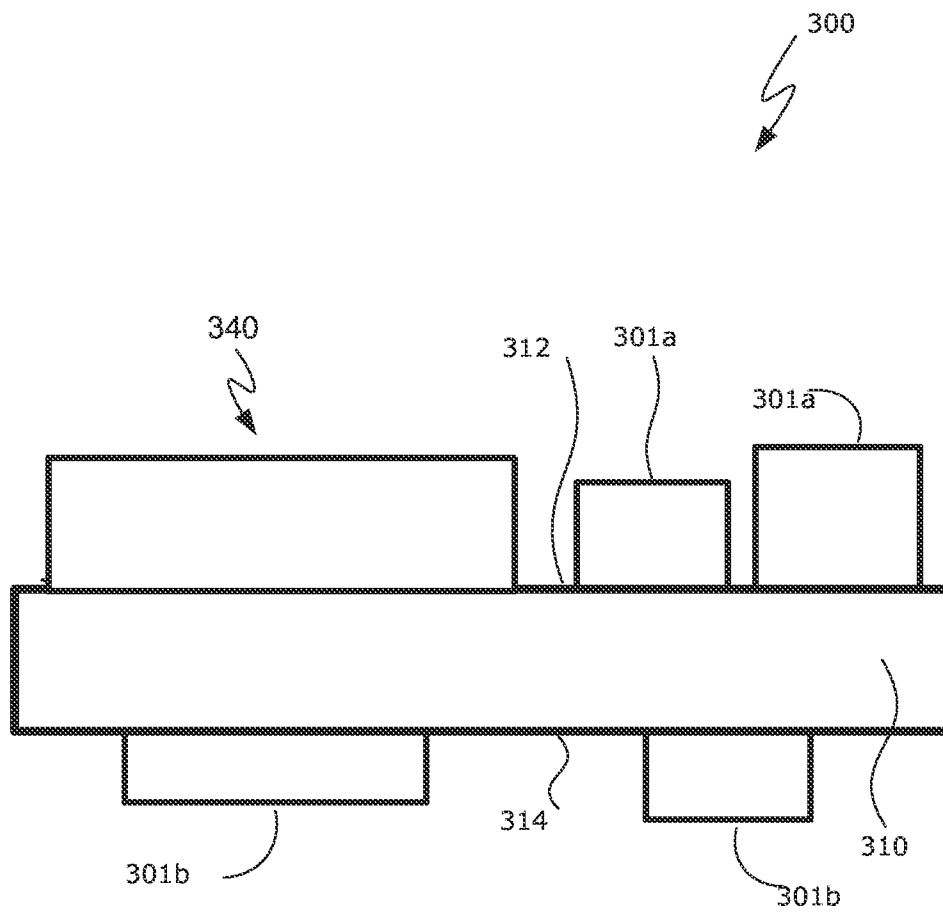


FIG. 3

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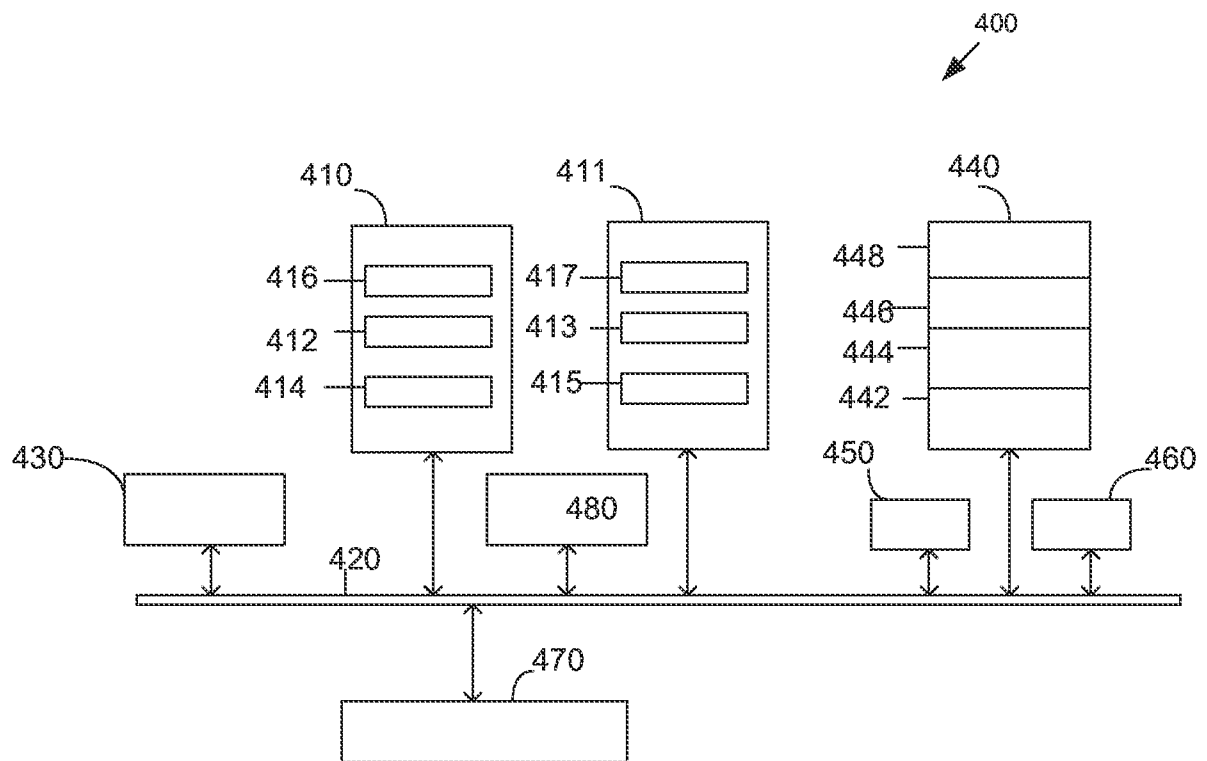


FIG. 4

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2014/025522**A. CLASSIFICATION OF SUBJECT MATTER****B81B 7/02(2006.01)i, B81C 1/00(2006.01)i, H01L 23/12(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

B81B 7/02; H01L 21/46; H01L 29/84; H01L 21/30; H01L 21/02; H01L 21/00; B81C 1/00; H01L 23/12

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: MEMS, bonding, packaging, layer transfer, and hermetical seal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2006-0252229 A1 (JOLY et al.) 09 November 2006 See abstract, paragraphs [0040]-[0057] and figures 1-5.	1-3, 6-11, 23-26 , 29-36
Y		4, 5, 12-22, 27, 28
Y	US 2007-0042521 A1 (YAMA, GARY) 22 February 2007 See abstract, paragraphs [0050], [0057]-[0064], [0072] and figures 1, 4A-4G.	4, 5, 12-22, 27, 28
A	US 2011-0073967 A1 (CHEN et al.) 31 March 2011 See abstract, paragraphs [0028]-[0033] and figures 1, 4.	1-36
A	US 2008-0160723 A1 (HANNEBAUER, ROBERT STEVEN) 03 July 2008 See abstract, paragraphs [0056]-[0061] and figures 4, 5.	1-36
A	US 2004-0178473 A1 (DENTRY et al.) 16 September 2004 See abstract, paragraphs [0087]-[0090] and figures 19A, 19B.	1-36



Further documents are listed in the continuation of Box C.



See patent family annex.

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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

07 July 2014 (07.07.2014)

Date of mailing of the international search report

08 July 2014 (08.07.2014)

Name and mailing address of the ISA/KR

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

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