(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
6 November 2014 (06.11.2014)

WIPO | PCT

(10) International Publication Number
WO 2014/179796 A1

(51) International Patent Classification:
H01L 29/772 (2006.01) *H01L 21/335* (2006.01)

(21) International Application Number:
PCT/US2014/036788

(22) International Filing Date:
5 May 2014 (05.05.2014)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
13/886,429 3 May 2013 (03.05.2013) US

(63) Related by continuation (CON) or continuation-in-part (CIP) to earlier application:
US 13/886,429 (CON)
Filed on 3 May 2013 (03.05.2013)

(71) Applicant: **TEXAS INSTRUMENTS INCORPORATED** [US/US]; P.O. Box 655474, Mail Station 3999, Dallas, TX 75265-5474 (US).

(71) Applicant *(for JP only)*: **TEXAS INSTRUMENTS JAPAN LIMITED** [JP/JP]; 24-1, Nishi-Shinjuku 6-chome, Shinjuku-ku, Tokyo, 160-8366 (JP).

(72) Inventors: **PENDHARKAR, Sameer**; 2032 Burnside Dr., Allen, TX 75013 (US). **TIPIRNENI, Naveen**; 5305 Coachman Court, Plano, TX 75023 (US). **JOH, Jungwoo**; 744 Brick Row, Apt. #2361, Richardson, TX 75081 (US).

(74) Agents: **FRANZ, Warren, L.** et al.; TEXAS INSTRUMENTS INCORPORATED, Deputy General Patent Counsel, P.O. Box 655474, Mail Station 3999, Dallas, TX 75265-5474 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

Published:

— *with international search report (Art. 21(3))*

— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments (Rule 48.2(h))*

(54) Title: III-NITRIDE TRANSISTOR LAYOUT

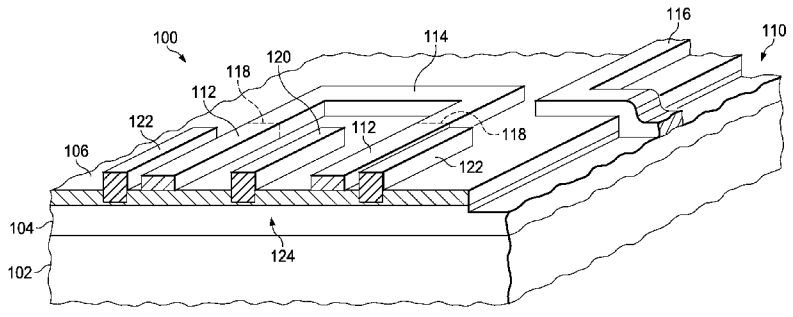


FIG. 1D

(57) Abstract: A semiconductor device (100) containing a GaN FET (124) has an isolating gate structure (112) outside the channel area which is operable to block current in the two-dimensional electron gas between two regions of the semiconductor device. The isolating gate structure(112) is formed concurrently with the gate of the GaN FET, and has a same structure as the gate.

WO 2014/179796 A1

III-NITRIDE TRANSISTOR LAYOUT

[0001] This relates to the field of semiconductor devices. More particularly, this invention relates to gallium nitride FETs in semiconductor devices.

BACKGROUND

[0002] Field effect transistors (FETs) made of III-N materials such as GaN exhibit desirable properties for power switches, such as high bandgaps and high thermal conductivity compared to silicon FETs. However, GaN FETs are undesirably susceptible to leakage current from the drain to the source through the two-dimensional electron gas outside the area.

SUMMARY

[0003] A semiconductor device containing a GaN FET has an isolating gate structure outside the area which is operable to block current in the two-dimensional electron gas between two regions of the semiconductor device. The isolating gate structure is formed concurrently with the gate of the GaN FET, and has a same structure as the gate.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] FIGS. 1A-1D are cross sections of an example semiconductor device.

[0005] FIGS. 2-7 are top views of semiconductor devices with example configurations of isolating gate structures.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0006] The following co-pending patent applications are hereby incorporated by reference: Application No. US 13/886,378; US 2014/0042452 A1; Application No. US 13/886,652 (TI-71492WO corresponding PCT application filed simultaneously herewith); Application No. US 13/886,688 (TI-72417WO corresponding PCT application filed simultaneously herewith); Application No. US 13/886,709; and Application No. US 13/886,744 (TI-72605WO corresponding PCT application filed simultaneously herewith).

[0007] A semiconductor device containing a GaN FET has an isolating gate

structure outside the area which blocks current in the two-dimensional electron gas between two regions of the semiconductor device. The isolating gate structure is formed concurrently with the gate of the GaN FET.

[0008] III-N semiconductor materials are materials in which Group III (boron group) elements (boron, aluminum, gallium, indium) provide a portion of the atoms in the semiconductor material and nitrogen atoms provide the remainder. Examples of III-N semiconductor materials are gallium nitride, boron gallium nitride, aluminum gallium nitride, indium nitride, and indium aluminum gallium nitride. III-N materials may be written with variable subscripts to denote a range of possible stoichiometries. For example, aluminum gallium nitride may be written as $Al_xGa_{1-x}N$ and indium aluminum gallium nitride may be written as $In_xAl_yGa_{1-x-y}N$. GaN FET is an example of a field effect transistor that includes III-N semiconductor materials.

[0009] FIGS. 1A-1D are cross sections of an example semiconductor device. Referring to FIG. 1A, the semiconductor device 100 is formed on a substrate 102, for example, an electrical isolation layer. The electrical isolation layer may be, for example, 300 to 2000 nanometers of semi-insulating gallium nitride. The electrical isolation layer may be, for example, semi-insulating to provide a desired level of electrical isolation between layers below the electrical isolation layer and layers above the electrical isolation layer. The substrate 102 may also include, for example a silicon base wafer and an isolation layer of aluminum nitride and a buffer layer of graded $Al_xGa_{1-x}N$ between the silicon base wafer and the electrical isolation layer.

[0010] A low-defect layer 104 is formed on the electrical isolation layer of the substrate 102. The low-defect layer 104 may be, for example, 25 to 1000 nanometers of gallium nitride. The low-defect layer 104 may be formed so as to minimize crystal defects which may have an adverse effect on electron mobility, which may result in the low-defect layer 104 being doped with carbon, iron or other dopant species, for example with a doping density less than 10^{17} cm^{-3}.

[0011] A barrier layer 106 is formed on the low-defect layer 104. The barrier

layer 106 may be, for example, 8 to 30 nanometers of $Al_xGa_{1-x}N$ or $In_xAl_yGa_{1-x-y}N$. A composition of group III elements in the barrier layer 234 may be, for example, 24 to 28 percent aluminum nitride and 72 to 76 percent gallium nitride. Forming the barrier layer 106 on the low-defect layer 104 generates a two-dimensional electron gas in the low-defect layer 104 just below the barrier layer 106 with an electron density of, for example, 1×10^{12} to 2×10^{13} cm^{-2}. The barrier layer 106 may include an optional cap layer, for example of gallium nitride, at a top surface of the barrier layer 106.

[0012] An isolation mask 108 is formed over the barrier layer 106 so as to expose an area of the barrier layer 106 for an isolation region. The isolation mask 108 may include, for example, 200 nanometers to 2 microns of photoresist formed by a photolithographic process.

[0013] Referring to FIG. 1B, an isolation process is performed which forms an isolation region 110 in the barrier layer 106 and the low-defect layer 104, in the area exposed by the isolation mask 108. In one version of the instant example, depicted in FIG. 1B, the isolation process may be an isolation etch which removes material from the barrier layer 106 and the low-defect layer 104 so as to form an isolation trench 110. In another version of the instant example, the isolation process may be an isolation implant which implants dopants into the barrier layer 106 and the low-defect layer 104 to form a heavily doped isolation barrier. The isolation region 110 reduces or eliminates electrical current in the two-dimensional electron gas from crossing the isolation region 110. The isolation region 110 may extend across the semiconductor device 100 or may enclose a region within the semiconductor device 100. The isolation mask 108 may be removed after the isolation region 110 is formed.

[0014] Referring to FIG. 1C, a gate formation process is performed which concurrently forms a gate 112, a first isolating gate structure 114 abutting the gate 112 and a second isolating gate structure 116 separate from the gate 112. The gate 112 and the first isolating gate structure 114 are contiguous; boundary line 118 is provided in FIGS. 1C-1D to depict their respective extents. The second isolating gate structure 116

may overlap the isolation region 110 as depicted in FIG. 1C. The first isolating gate structure 114 may also optionally overlap the isolation region 110.

[0015] The gate 112, the first isolating gate structure 114 and the second isolating gate structure 116 may be, for example, metal gate structures directly on the barrier layer 106 forming schottky junctions between the metal and the III-N material of the barrier layer 106. In another example, the gate 112, the first isolating gate structure 114 and the second isolating gate structure 116 may be insulated metal gate structures in which metal gate structures are formed on a gate dielectric layer on the barrier layer 106. In a further example, the gate 112, the first isolating gate structure 114 and the second isolating gate structure 116 may be III-N semiconductor gate structures which do not disrupt the two-dimensional electron gas unless a bias is applied to the semiconductor gate structures. In another example, the gate 112, the first isolating gate structure 114 and the second isolating gate structure 116 may be p-type III-N semiconductor gate structures which disrupt the two-dimensional electron gas when no bias is applied to the p-type semiconductor gate structures.

[0016] Referring to FIG. 1D, at least one drain contact 120 and at least one source contact 122 are formed in the barrier layer 106. The drain contact 120 and source contact 122 may be, for example, disposed below the top surface of the barrier layer 106 an make tunneling electrical connections to the two-dimensional electron gas in the low-defect layer 104. The gate 112, the drain contact 120 and the source contact 122 are parts of a GaN FET 124 of the semiconductor device 100.

[0017] The first isolating gate structure 114 and the second isolating gate structure 116 electrically isolate one or more regions of the two-dimensional electron gas from one another. In some types of gate structures, such as the p-type semiconductor gate structure, electrical isolation may be accomplished without applying a bias to the first and second isolating gate structures 114 and 116 relative to the barrier layer 106. In other types of gate structures, such as the semiconductor gate structure or the schottky metal gate structure, electrical isolation may be accomplished by applying a negative bias

to the first and second isolating gate structures 114 and 116 relative to the barrier layer 106. In the example depicted in FIG. 1D, the two-dimensional electron gas contiguous with the drain contact 120 is electrically isolated from the two-dimensional electron gas contiguous with the source contacts 122 by the first isolating gate structure 114. Similarly, the two-dimensional electron gas contiguous with the source contacts 122 is electrically isolated from the two-dimensional electron gas on an opposite side of the second isolating gate structure 116. Field plates, not shown, may be formed adjacent to the gate to reduce electric fields in the barrier layer 106 and the low-defect layer 104. The field plates may include extensions of the gate 112 and the first isolating gate structure 114 and the second isolating gate structure 116, and may include extensions of the source contacts 122.

[0018] FIGS. 2-7 illustrate semiconductor devices with example configurations of isolating gate structures. Referring to FIG. 2, a semiconductor device 200 is formed in and on a substrate 202, for example as described in reference to FIG. 1A. A two-dimensional electron gas is formed in the substrate 202 by a barrier layer over an low-defect layer. A gate 212 and a gate isolating structure 214 are formed concurrently over a top surface of the substrate 202. In the instant example, the gate 212 has two parallel segments and the gate isolating structure 214 has two arced segments. The gate isolating structure 214 segments are contiguous with the gate 212 segments; boundary line 218 is provided in FIG. 2 to depict their respective extents. The gate 212 and the gate isolating structure 214 have a closed loop configuration.

[0019] Two drain contacts 220 are formed outside the closed loop of the gate 212 and the gate isolating structure 214, one on each side of the closed loop, oriented parallel to the gate 212. A source contact 222 is formed inside the closed loop of the gate 212 and the gate isolating structure 214, also oriented parallel to the gate 212. The gate 212, the drain contacts 220 and the source contact 222 are parts of a GaN FET 224 of the semiconductor device 200. In the instant example, the gate isolating structure 214 electrically isolates the two-dimensional electron gas that is contiguous with the source

contact 222 from the two-dimensional electron gas that is contiguous with the drain contacts 220.

[0020] Referring to FIG. 3, a semiconductor device 300 is formed in and on a substrate 302, for example as described in reference to FIG. 1A. A two-dimensional electron gas is formed in the substrate 302 by a barrier layer over an low-defect layer. A gate 312 and a gate isolating structure 314 are formed concurrently over a top surface of the substrate 302. In the instant example, the gate 312 has two parallel segments and the gate isolating structure 314 has two C-shaped segments contiguous with the gate 312 segments; boundary line 318 is provided in FIG. 3 to depict their respective extents. The gate isolating structure 314 segments may optionally be connected by a portion of gate structure, as depicted in FIG. 3.

[0021] A source contact 322 is formed between the gate 312 segments, oriented parallel to the gate 312 segments. Two drain contacts 320 are formed adjacent to the gate 312 segments opposite the source contact 322, one on each side of the gate 312 segments. The gate 312, the drain contacts 320 and the source contact 322 are parts of a GaN FET 324 of the semiconductor device 300. The gate isolating structure 314 has two C-shaped segments connect with the gate 312 segments to form two closed loop configurations, each enclosing one of the drain contacts 320. In the instant example, the gate isolating structure 314 electrically isolates the two-dimensional electron gas that is contiguous with the drain contacts 320 from the two-dimensional electron gas that is contiguous with the source contact 322.

[0022] Referring to FIG. 4, a semiconductor device 400 is formed in and on a substrate 402, for example as described in reference to FIG. 1A. An isolation structure 410, for example an isolation trench structure or an isolation implanted structure, is formed as described in reference to FIG. 1A and FIG. 1B to enclose a region of the substrate 402. A two-dimensional electron gas is formed in the substrate 402 by a barrier layer over an low-defect layer.

[0023] A first gate 412, a first gate isolating structure 414, a second gate 424, a

second gate isolating structure 426 and a third gate isolating structure 428 are formed concurrently over a top surface of the substrate 402. The third gate isolating structure 428 extends across the region enclosed by the isolation structure 410 and may overlap the isolation structure 410.

[0024] In the instant example, the first gate 412 has two parallel segments and the first gate isolating structure 414 has three arced segments contiguous with the first gate 412 segments; first boundary line 418 is provided in FIG. 4 to depict their respective extents. Two first drain contacts 420 are formed outside the two first gate 412 segments, one on each side of the first gate 412 segments, oriented parallel to the first gate 412 segments. A first source contact 422 is formed between the first gate 412 segments, also oriented parallel to the first gate 412 segments. The first gate 412, the first drain contacts 420 and the first source contact 422 are parts of a first GaN FET 436 of the semiconductor device 400. The three first gate isolating structure 414 arced segments and the two first gate 412 parallel segments have an open loop configuration with a narrow pinch-off region separating two of the three first gate isolating structure 414 arced segments. The two-dimensional electron gas is blocked from the narrow pinch-off region, possibly upon application of a bias to the first gate isolating structure 414. In the instant example, the first gate isolating structure 414 electrically isolates the two-dimensional electron gas that is contiguous with the first source contact 422 from the two-dimensional electron gas that is contiguous with the first drain contacts 420. Including the narrow pinch-off region may facilitate fabrication of the first gate 412 and the first gate isolating structure 414, for example using a liftoff process for metal gates.

[0025] The second gate 424 and the second gate isolating structure 426 have a similar configuration; second boundary line 430 is provided in FIG. 4 to depict their respective extents. A second source contact 432 is formed between parallel segments of the second gate 424 and second drain contacts 434 are formed outside the second gate 424. The second gate 424, the second drain contacts 434 and the second source contact 432 are parts of a second GaN FET 438 of the semiconductor device 400. The second

gate isolating structure 426 electrically isolates the two-dimensional electron gas that is contiguous with the second source contact 432 from the two-dimensional electron gas that is contiguous with the second drain contacts 434. Additionally, the third gate isolating structure 428 electrically isolates the two-dimensional electron gas that is contiguous with the first drain contacts 420 from the two-dimensional electron gas that is contiguous with the second drain contacts 434. The first drain contacts 420 may advantageously be biased to a different potential than the second drain contacts 434 without incurring undesirable leakage current. In one version of the instant example, the first GaN FET 436 and the second GaN FET 438 may both be depletion mode FETs. In another version, the first GaN FET 436 and the second GaN FET 438 may both be enhancement mode FETs. In a further version, the first GaN FET 436 may be a depletion mode FET and the second GaN FET 438 may both be an enhancement mode FET.

[0026] Referring to FIG. 5, a semiconductor device 500 is formed in and on a substrate 502, for example as described in reference to FIG. 1A. A two-dimensional electron gas is formed in the substrate 502 by a barrier layer over an low-defect layer. A gate 512 and a gate isolating structure 514 are formed concurrently over a top surface of the substrate 502. In the instant example, the gate 512 has two parallel segments and the gate isolating structure 514 has segments contiguous with the gate 512 segments; boundary line 518 is provided in FIG. 5 to depict their respective extents. The gate 512 and the gate isolating structure 514 form a closed loop configuration which surrounds an input/output (I/O) structure 536 and at least one drain contact 520. The I/O structure 536 may be, for example, a probe pad or a bond pad, and may be directly electrically connected to the at least one drain contact 520 or may be electrically coupled to the at least one drain contact 520 through overvoltage protection circuitry. At least one source contact 522 is formed outside the closed loop configuration of the gate 512 and the gate isolating structure 514. The source contact 522 is disposed adjacent to the gate 512 opposite the drain contacts 520. The gate 512, the source contact 522 and the drain contacts 520 are parts of a GaN FET 524 of the semiconductor device 500. In the instant

example, the gate isolating structure 514 electrically isolates the two-dimensional electron gas that is contiguous with the drain contacts 520 from the two-dimensional electron gas that is contiguous with the source contact 522. Disposing the I/O structure 536 inside the closed loop configuration of the gate 512 and the gate isolating structure 514 advantageously allows biasing the drain contacts 520 without undesired leakage current from the I/O structure 536.

[0027] Referring to FIG. 6, a semiconductor device 600 is formed in and on a substrate 602, for example as described in reference to FIG. 1A. A two-dimensional electron gas is formed in the substrate 602 by a barrier layer over an low-defect layer. A first gate 612 and a first gate isolating structure 614, delineated by a first boundary line 618, and a first source contact 622 and first drain contacts 620 are formed, as described in reference to FIG. 2, in a first region 638 of the semiconductor device 600. The first gate 612, the first source contact 622 and the first drain contacts 620 are parts of a first GaN FET 654 of the semiconductor device 600. In the first region 638, the first gate isolating structure 614 electrically isolates the two-dimensional electron gas that is contiguous with the first source contact 622 from the two-dimensional electron gas that is contiguous with the first drain contacts 620.

[0028] In a second region 640 of the semiconductor device 600, a second gate 624 and a second gate isolating structure 626, delineated by a second boundary line 630, and a second source contact 632 and second drain contacts 634 have a similar configuration as their counterparts in the first region 638. The second gate 624, the second source contact 632 and the second drain contacts 634 are parts of a second GaN FET 656 of the semiconductor device 600. The second gate isolating structure 626 electrically isolates the two-dimensional electron gas that is contiguous with the second source contact 632 from the two-dimensional electron gas that is contiguous with the second drain contacts 634. Similarly, in a third region 642 of the semiconductor device 600, a third gate 644 and a third gate isolating structure 646, delineated by a third boundary line 648, and a third source contact 650 and third drain contacts 652 have a

similar configuration as their counterparts in the first region 638. The third gate 644, the third source contact 650 and the third drain contacts 652 are parts of a third GaN FET 658 of the semiconductor device 600. The third gate isolating structure 646 electrically isolates the two-dimensional electron gas that is contiguous with the third source contact 650 from the two-dimensional electron gas that is contiguous with the third drain contacts 652.

[0029] A fourth gate isolating structure 660 surrounds and separates the first region 638, the second region 640 and the third region 642. The first drain contacts 620, the second drain contacts 634 and the third drain contacts 652 may advantageously be biased to different potentials without incurring undesired leakage currents.

[0030] Referring to FIG. 7, a semiconductor device 700 is formed in and on a substrate 702, for example as described in reference to FIG. 1A. A two-dimensional electron gas is formed in the substrate 702 by a barrier layer over an low-defect layer. A first gate 712 and a first gate isolating structure 714 contiguous with the first gate 712 are formed concurrently. A first boundary line 718 delineates the extents of the first gate 712 and the first gate isolating structure 714. The first gate isolating structure 714 surrounds a drain contact 720. A first source contact 722 is formed adjacent to the first gate 712 opposite from the drain contact 720. The first gate 712, the drain contact 720 and the first source contact 722 are parts of a first GaN FET 734 of the semiconductor device 700. The first gate isolating structure 714 electrically isolates the two-dimensional electron gas that is contiguous with the first source contact 722 from the two-dimensional electron gas that is contiguous with the drain contact 720.

[0031] A second gate 724 is formed proximate to the drain contact 720 opposite from the first gate 712. A second gate isolating structure 726 is contiguous with the second gate 724 and surrounds a second source contact 732. The second gate 724, the drain contact 720 and the second source contact 732 are parts of a second GaN FET 736 of the semiconductor device 700. A second boundary line 730 delineates the extents of the second gate 724 and the second gate isolating structure 726. The second gate

isolating structure 726 surrounds the second source contact 732, so that the two-dimensional electron gas that is contiguous with the second source contact 732 is electrically isolated from the two-dimensional electron gas that is contiguous with the drain contact 720. The first gate isolating structure 714 surrounds the second gate 724 and the second gate isolating structure 726. The second source contact may advantageously be floated or operated at a different potential from the first source contact 722. The second source contact 732 and the second gate 724 may be part of a sense transistor which advantageously senses a drain potential on the drain contact 720 without disrupting current through the first source contact 722.

[0032] Those skilled in the art will appreciate that modifications may be made to the described embodiments, and also that many other embodiments are possible, within the scope of the claims.

CLAIMS

What is claimed is:

1. A semiconductor device, comprising:

a substrate comprising III-N semiconductor material;

a low-defect layer of III-N semiconductor material disposed on the substrate;

a barrier layer of III-N semiconductor material disposed on the low-defect layer;

a gallium nitride field effect transistor (GaN FET), comprising:

a gate disposed over the barrier layer;

a drain contact disposed over the low-defect layer; and

a source contact disposed over the low-defect layer; and

a gate isolating structure disposed over the barrier layer having a same structure as the gate, the gate isolating structure being operable to electrically isolate a first region of the semiconductor device from a second regions of the semiconductor device.

2. The semiconductor device of claim 1, wherein the gate isolating structure is contiguous with the gate.

3. The semiconductor device of claim 1, wherein the gate isolating structure is separate from the gate.

4. The semiconductor device of claim 1, wherein:

the first region is contiguous with the drain contact; and

the second region is contiguous with the source contact.

5. The semiconductor device of claim 1, wherein:

the GaN FET is a first GaN FET;

the semiconductor device includes a second GaN FET;

the first region is contiguous with the first GaN FET; and
the second region is contiguous with the second GaN FET.

6. The semiconductor device of claim 1, wherein:
the semiconductor device includes an isolation structure; and
the gate isolating structure extends to and overlaps the isolation structure.

7. The semiconductor device of claim 1, wherein the gate isolating structure surrounds an input/output (I/O) structure.

8. The semiconductor device of claim 1, wherein the gate isolating structure surrounds the GaN FET.

9. The semiconductor device of claim 1, wherein the gate isolating structure includes a metal gate layer.

10. The semiconductor device of claim 1, wherein the gate isolating structure includes a semiconductor gate layer of III-N semiconductor material.

11. A method of forming a semiconductor device, comprising the steps of:
providing a substrate comprising III-N semiconductor material;
forming an low-defect layer of III-N semiconductor material on the substrate;
forming a barrier layer of III-N semiconductor material on the low-defect layer;
forming a GaN FET, by a process comprising the steps of:
forming a gate over the barrier layer;
forming a drain contact over the low-defect layer; and
forming a source contact over the low-defect layer; and
forming a gate isolating structure over the barrier layer concurrently with the gate,

the gate isolating structure being operable to electrically isolate a first region of the semiconductor device from a second regions of the semiconductor device.

12. The method of claim 11, wherein the gate isolating structure is contiguous with the gate.

13. The method of claim 11, wherein the gate isolating structure is separate from the gate.

14. The method of claim 11, wherein:
the first region is contiguous with the drain contact; and
the second region is contiguous with the source contact.

15. The method of claim 11, wherein the GaN FET is a first GaN FET, and further including the step of forming a second GaN FET, wherein:
the first region is contiguous with the first GaN FET; and
the second region is contiguous with the second GaN FET.

16. The method of claim 11, further including the step of forming an isolation structure, and the gate isolating structure is formed to extend to and overlap the isolation structure.

17. The method of claim 11, wherein the gate isolating structure surrounds an input/output (I/O) structure.

18. The method of claim 11, wherein the gate isolating structure surrounds the GaN FET.

19. The method of claim 11, wherein the step of forming the gate isolating structure includes forming a metal gate layer.

20. The method of claim 11, wherein the step of forming the gate isolating structure includes forming a semiconductor gate layer of III-N semiconductor material.

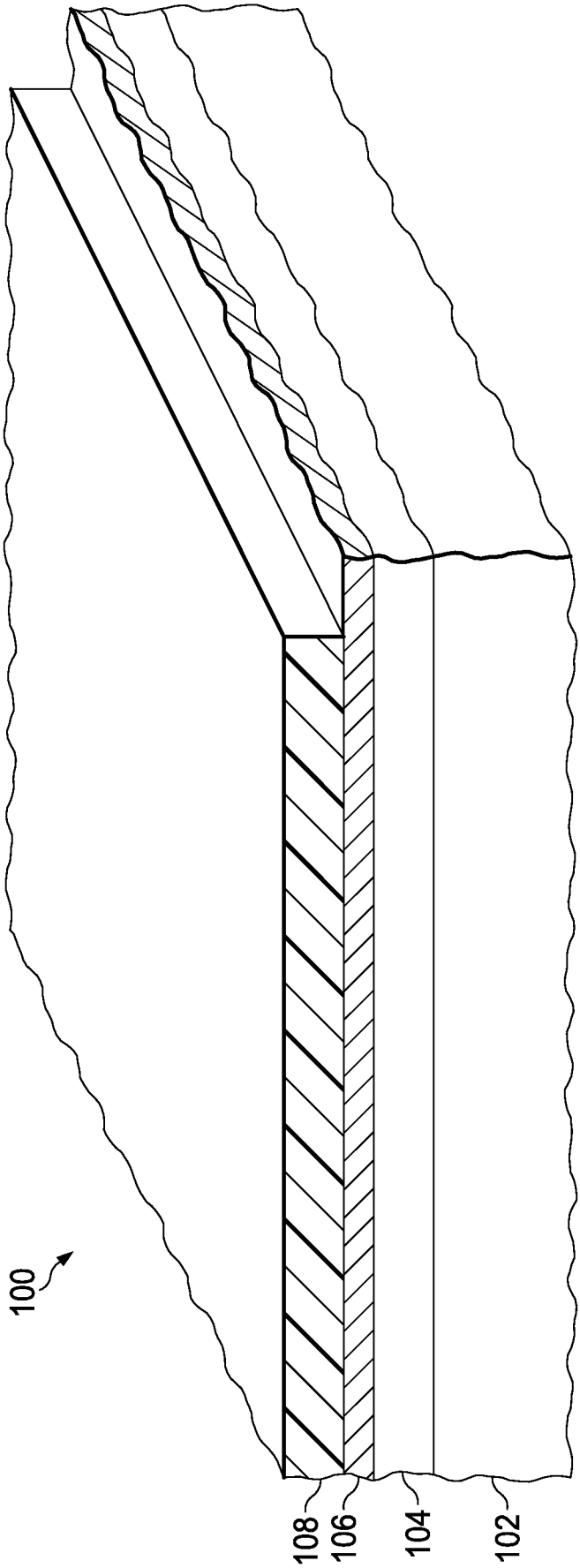


FIG. 1A

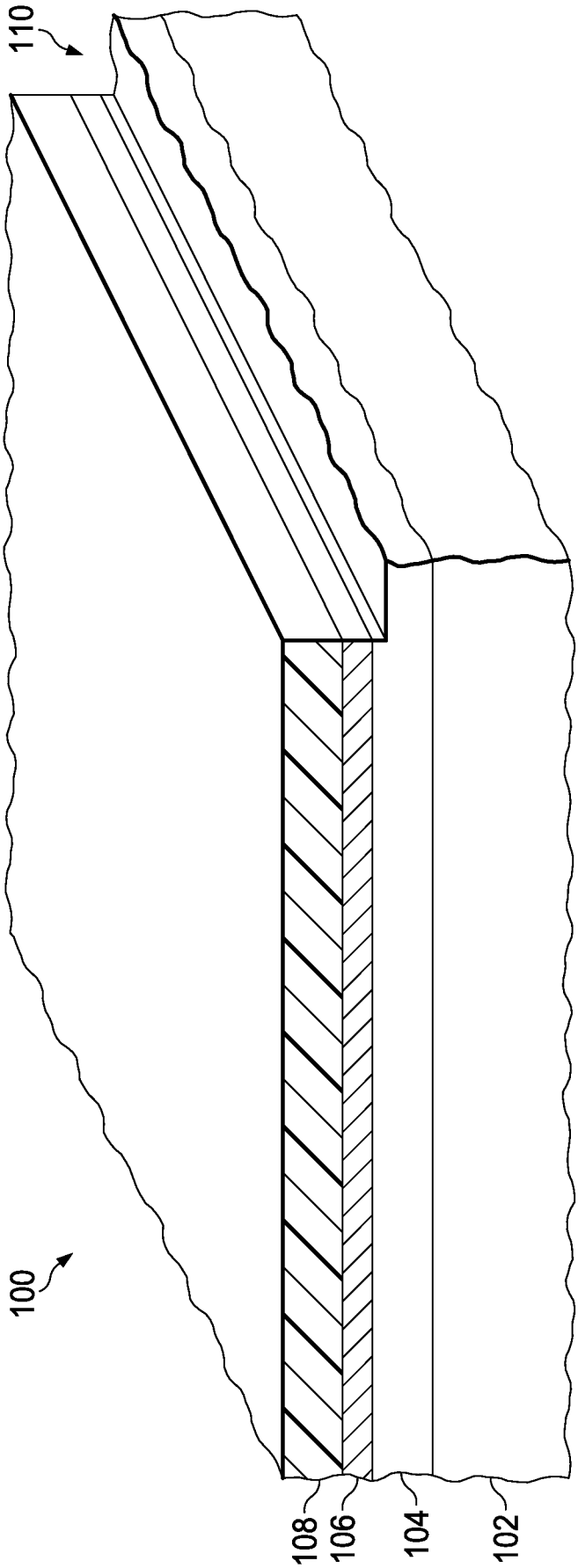


FIG. 1B

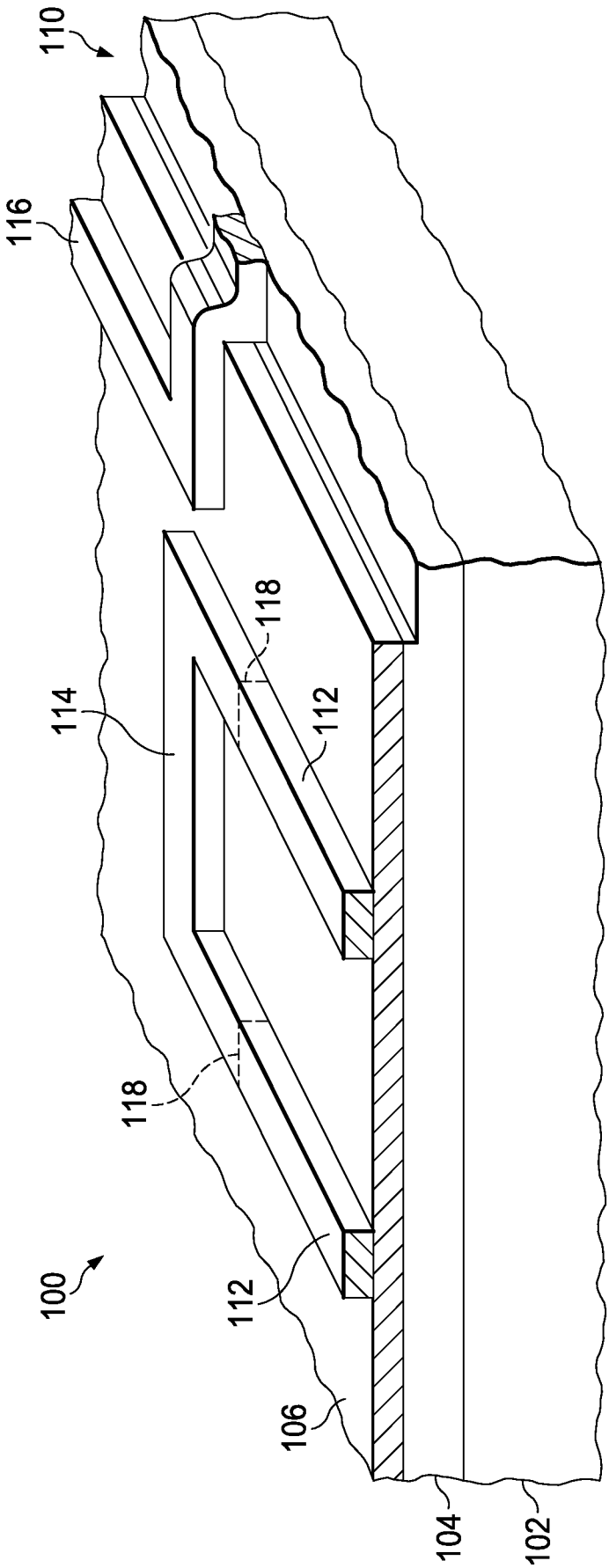


FIG. 1C

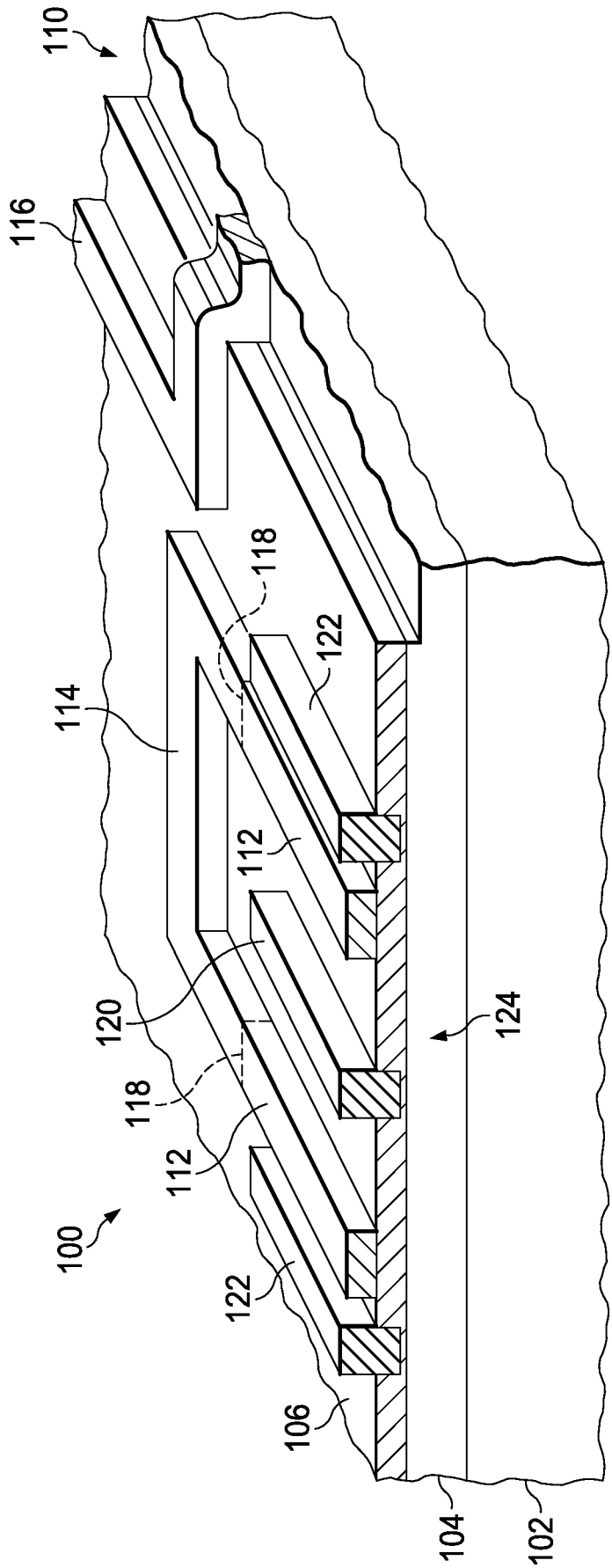


FIG. 1D

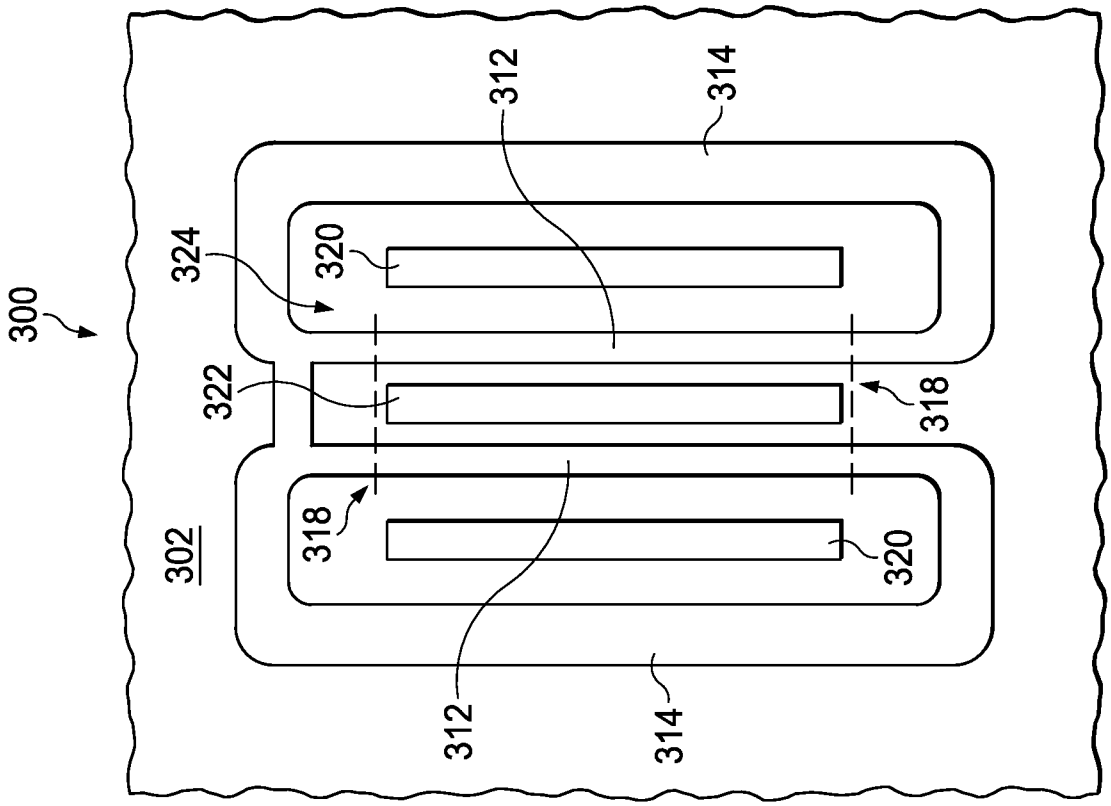

300
302
312
314
320
322
324
318
312
314
320
318

FIG. 3

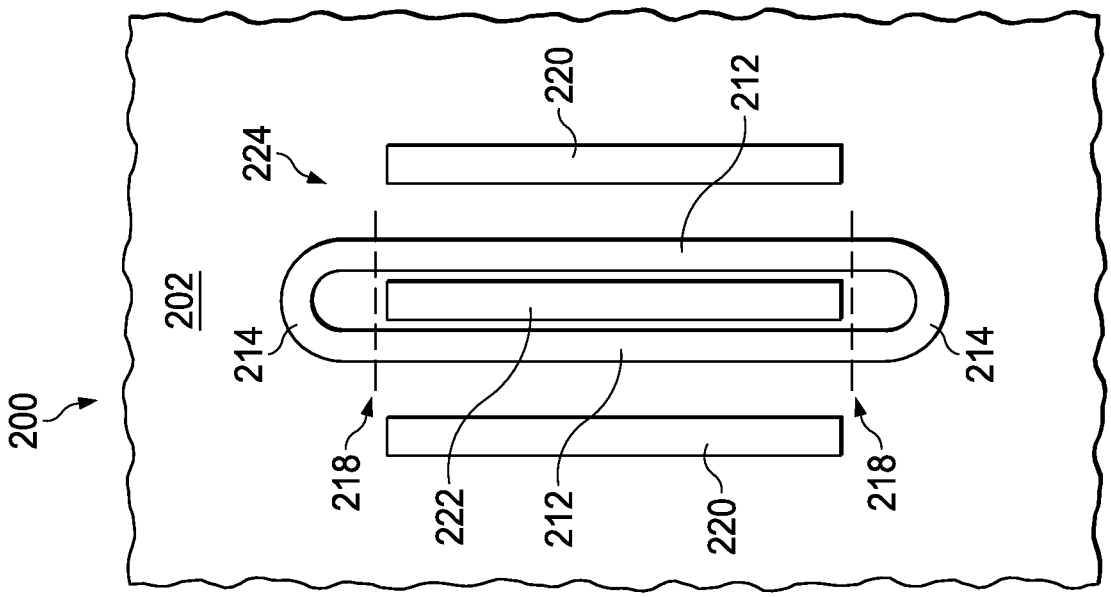

200
202
224
220
212
214
214
218
222
212
220
218

FIG. 2

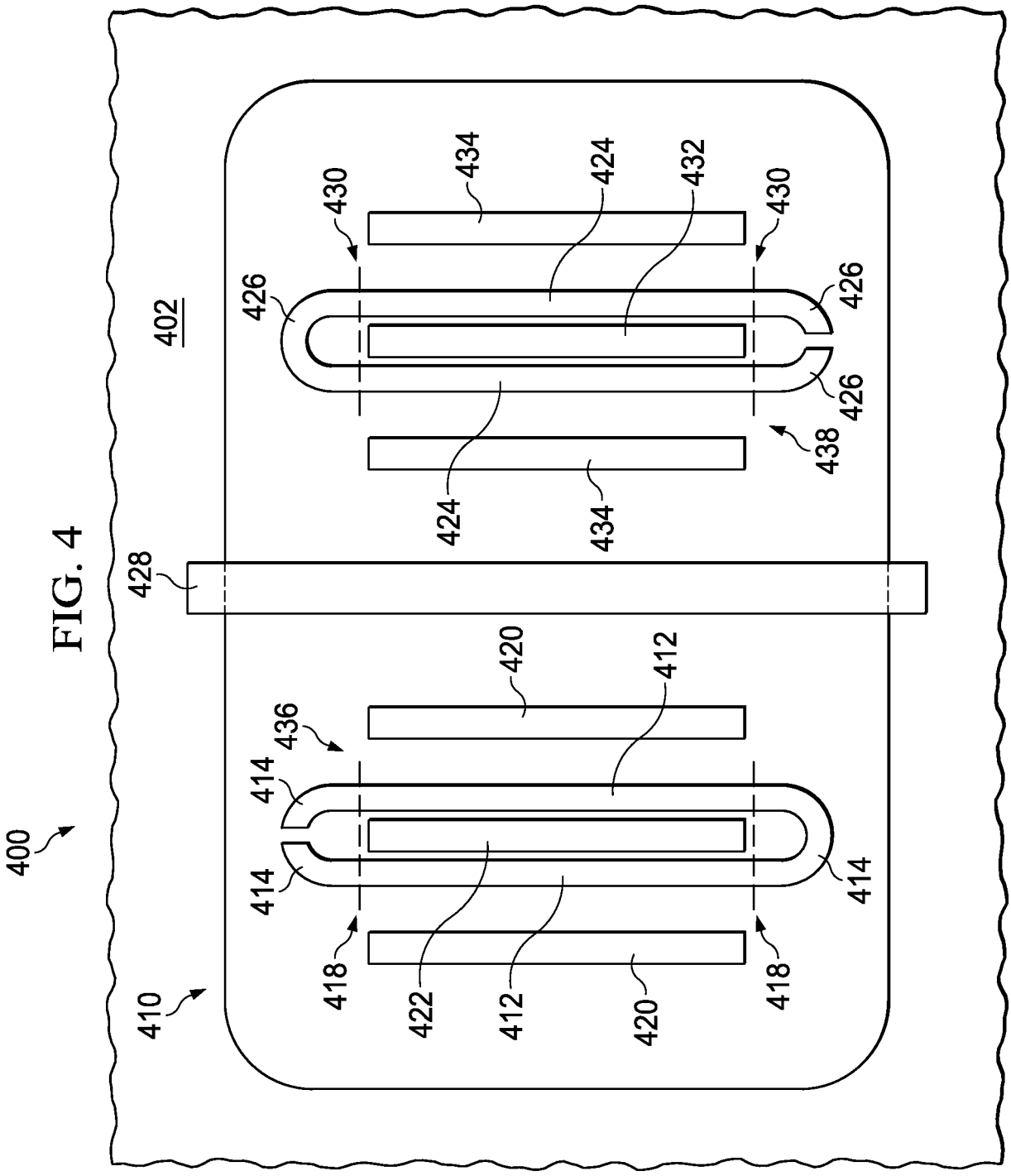


FIG. 4

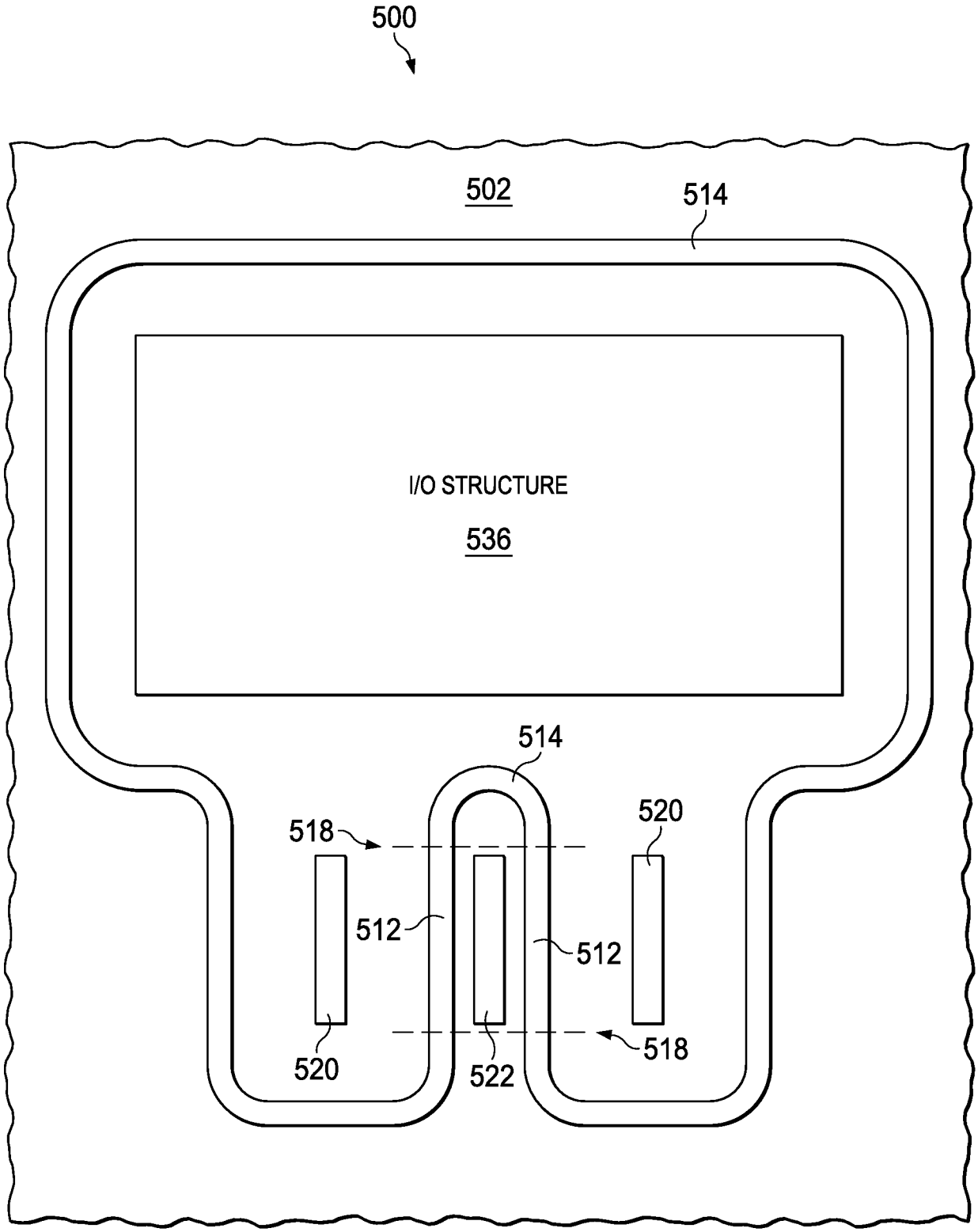
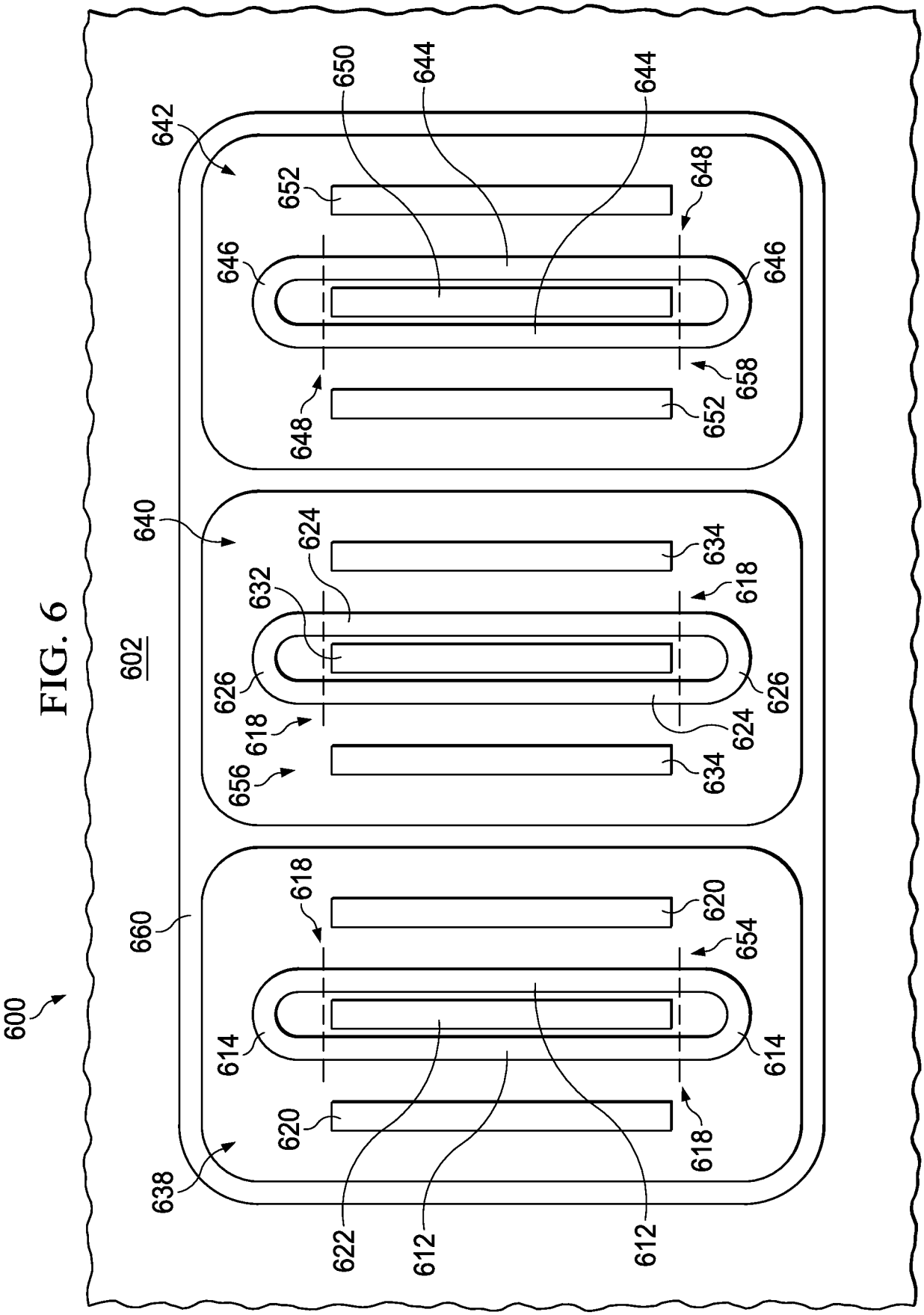


FIG. 5

FIG. 6


600
602
638
660
640
642
614
618
620
622
612
624
626
632
634
656
644
646
648
650
652
654
658

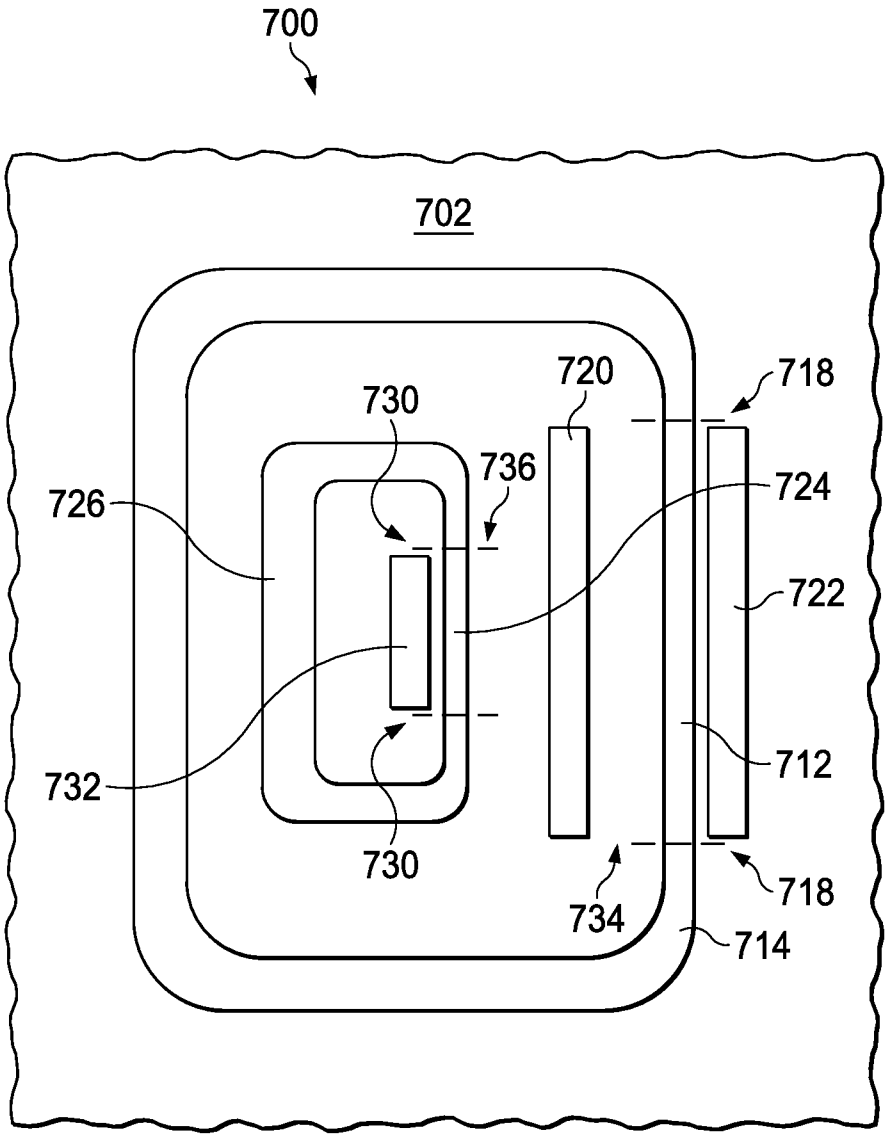


FIG. 7

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 2014/036788

A. CLASSIFICATION OF SUBJECT MATTER

H01L 29/772 *(2006.01)*
H01L 21/335 *(2006.01)*

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 21/00, 21/04, 21/18, 21/334, 21/335, 29/00, 29/66, 29/68, 29/772

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

PatSearch (RUPTO internal), USPTO, PAJ, Esp@cenet, DWPI, EAPATIS, PATENTSCOPE, Information Retrieval System of FIPS

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2013/0087803 A1 (EPOWERSOFT, INC.) 11.04.2013, fig. 3J, [0003], [0042], [0043], [0044], [0059], claims 11, 22	1, 2, 4, 6, 9-12, 14, 16, 19, 20
A		3, 5, 7, 8, 13, 15, 17, 18
A	US 2012/0193677 A1 (TRANSPHORM INC.) 02.08.2012	1-20
A	US 8389977 B2 (TRANSPHORM INC.) 05.03.2013	1-20
A	US 8384129 B2 (THE UNITED STATES OF AMERICA, AS REPRESENTED BY THE SECRETARY OF THE NAVY) 26.02.2013	1-20

☐ Further documents are listed in the continuation of Box C.

☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
19 September 2014 (19.09.2014)	30 September 2014 (30.09.2014)
Name and mailing address of the ISA/RU: FIPS, Russia, 123995, Moscow, G-59, GSP-5, Berezhkovskaya nab., 30-1 Facsimile No. +7 (499) 243-33-37	Authorized officer M. Salnikov Telephone No. 499-240-25-91

Form PCT/ISA/210 (second sheet) (July 2009)