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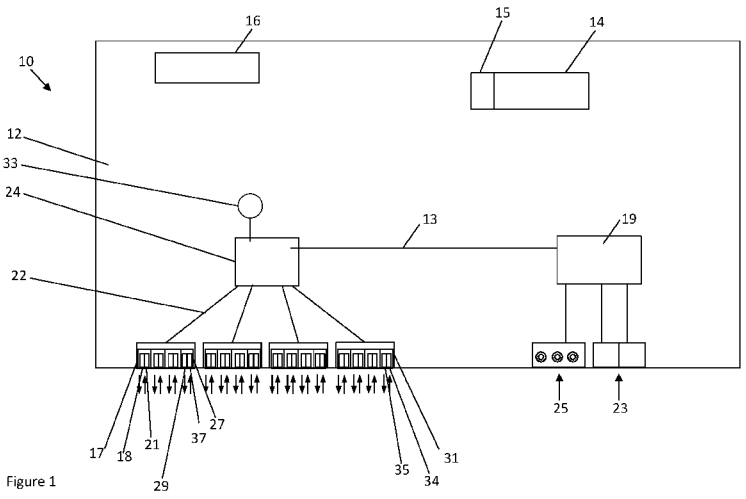

Figure 1

(57) Abstract: Disclosed herein is a system (10) for multiplexing a plurality of payloads. The system (10) comprises a plurality of receivers (18, 29) for receiving a plurality of line encoded data streams. The system (10) is configured to retrieve from the plurality of line encoded data streams a plurality of block sequences. The plurality of block sequences carry the plurality of payloads. The system (10) comprises a transmitter configured to transit a line encoded output data stream. Also disclosed herein is a method for multiplexing a plurality of payloads.

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A SYSTEM FOR MULTIPLEXING A PLURALITY OF PAYLOADS AND A METHOD FOR MULTIPLEXING A PLURALITY OF PAYLOADS

Technical field

The disclosure herein generally relates to a system for multiplexing a plurality of payloads and a method for multiplexing a plurality of payloads.

Background

In many computer networks, a plurality of payloads carried by a plurality of data streams are multiplexed onto a single output data stream.

Each of the plurality of payloads may be, for example, an Ethernet payload, a InfiniBand payload, a FiberChannel payload, a FireWire payload, a PCIe payload, or generally any suitable payload. In the context of this document, a payload may be, for example, a frame, a packet, a datagram, a segment, a cell or generally any suitable type of data package.

Each of the plurality of data streams may be carried on respective network cables or wireless channels, for example. Each of the plurality of network cables or wireless channels may be, for example, connected to a networking device in the form of a network switch or router.

The networking devices may perform a series of steps to multiplex the plurality of payloads. The networking device retrieves from a data stream a plurality of blocks that carry a payload. The networking device may decode Ethernet blocks (for example 64b/66b Ethernet blocks) from a data stream, and communicate the decoded blocks to a MAC and reconciliation sub-layer via a XGMII or XAUI interface for further processing. Block encoding is used in a physical layer to ensure that there are sufficient transitions (between 1's and 0's, for example) in the data stream to facilitate clock extraction, and to maintain a fixed DC bias (usually a 0 DC bias) to allow for

AC coupling. Block encoding is used in many communication protocols including 1G and 10G Ethernet, and FireWire. Some forms of block encoding, including 10G Ethernet and Hamming codes, include error detection and error correction. The payload is extracted from the blocks. Subsequently, the payload destination address is determined by reading it from the extracted payload. The networking device then selects the output channel for the payload using the extracted destination address. The payload is then coded into another plurality of blocks for transmission by a transmitter on the selected output channel.

These steps are repeated for each of the plurality of payloads carried by the plurality of data streams.

Theseries of steps performed by the networking device to multiplex the plurality of data streams may be too inefficient in some application, especially for applications requiring low latency, examples of which include but are not limited to the trading of financial instruments and supercomputing.

Summary

Disclosed herein is a method for multiplexing a plurality of payloads. The method comprises the step of receiving a plurality of line encoded data streams. The method comprises the step of retrieving from the plurality of line encoded data streams a plurality of block sequences. The plurality of block sequences carry the plurality of payloads. The method comprises the step of transmitting a line encoded output data stream having incorporated therein the plurality of block sequences retrieved from the plurality of line encoded data streams.

The multiplexing is, consequently, performed at the block level, not higher levels as for prior art networking devices. The blocks are multiplexed directly rather than being decoded or converted to another form. The payload need not be extracted, and an address may not be extracted from within the payload. This may improve latency and/or reduce electronic complexity. Reduced

latency may be desirable for applications including but not limited to financial trading and supercomputing.

In an embodiment, the step of receiving the plurality of line encoded data streams comprises the step of a plurality of receivers receiving the plurality of line encoded data streams. The plurality of line encoded data streams may be received via a plurality of network cables. The plurality of line encoded data streams may be received via a network. The step of retrieving from the plurality of line encoded data streams the plurality of block sequences carrying the plurality of payloads may comprise the step of the plurality of receivers retrieving the plurality of block sequences carrying the plurality of payloads from the plurality of line encoded data streams. The plurality of receivers may regenerate the plurality of line encoded data streams. The step of retrieving from the plurality of line encoded data streams the plurality of block sequences may comprise the step of the plurality of receivers performing a serial-to-parallel conversion on each of the plurality of block sequences. The step of retrieving from the plurality of line encoded data streams the plurality of block sequences may comprise the step of the plurality of receivers performing a block alignment operation on each of the plurality of block sequences. The plurality of receivers may descramble each of the plurality of block sequences.

The network may comprise at least one of a personal area network, a local area network (LAN), a campus area network (CAN), a metropolitan area network (MAN), and a wide area network (WAN, for example, the Internet).

In an embodiment, the step of transmitting the line encoded output data stream comprises the step of a transmitter transmitting the line encoded output data stream. The step of transmitting the line encoded output data stream may comprise the step of the line encoded output data stream being communicated over a network cable in communication with the transmitter. The step of the transmitter transmitting the line encoded output data stream comprises the step of the line encoded output data stream being communicated over the network. The plurality of block

sequences carrying the plurality of payloads so retrieved may be communicated to the transmitter.

An embodiment comprises the step of generating the line encoded output data stream having incorporated therein the plurality of block sequences retrieved from the plurality of line encoded data streams.

An embodiment comprises the step of detecting the plurality of block sequences by detecting at least one of a start-of-payload block and an end-of-payload block for each block sequence of the plurality of block sequences. The plurality of block sequences so identified may be stored in a plurality of memories. Each of the plurality of memories may be paired with one of the plurality of line encoded data streams. The plurality of memories may comprise a plurality of first-in-first-out buffers (FIFOs). The order in which the plurality of block sequences are communicated from the plurality of memories may be scheduled.

An embodiment comprises the step of controlling an inter-payload spacing on the line encoded output data stream.

An embodiment comprises the step of generating a plurality of detection signals each indicating one of the start and an end of a respective block sequence of the plurality of block sequences. The order in which the plurality of block sequences are communicated from the plurality of memories may be scheduled using the plurality of detection signals. Retrieval of each block sequence of the plurality of block sequences from the plurality of memories may be scheduled in the order that the respective detection signals are received.

An embodiment comprises the step of communicating the plurality of block sequences to a transmitter. The transmitter may generate the line encoded output data stream having incorporated therein the plurality of block sequences retrieved from the plurality of line encoded data streams.

An embodiment comprises the step of the line encoded output data stream being communicated over a network cable in communication with the transmitter. An embodiment comprises the step of the line encoded output data stream being communicated over the network.

In an embodiment, the line encoded output data stream may comprise an output block stream comprising the plurality of block sequences retrieved from the plurality of line encoded data streams and a plurality of control blocks disposed between the plurality of block sequences.

In an embodiment, each of the plurality of block sequences incorporated into the line encoded output data stream are scrambled.

An embodiment comprises the step of shaping the line encoded output data stream. An embodiment comprises the step of shaping the power spectrum of the line encoded output data stream.

In an embodiment, the bit rate of each of the plurality of line encoded data streams is the same as the bit rate of the line encoded output data stream.

In an embodiment, the plurality of block sequences comprises at least one of a plurality of 64b/66b encoded blocks, a plurality of 64b/67b encoded blocks, a plurality of 6b/8b encoded blocks, a plurality of 8b/10b encoded blocks, a plurality of 128b/132b encoded blocks, a plurality of 128b/132b encoded blocks, and a plurality of Hamming encoded blocks.

In an embodiment, the plurality of payloads comprise at least one of a plurality of Ethernet payloads, a plurality of InfiniBand payloads, a plurality of FiberChannel payloads, a plurality of FireWire payloads and a plurality of PCIe payloads.

In an embodiment, the plurality of line encoded data streams are a plurality of block encoded data streams.

In an embodiment, the line encoded output data stream is a block encoded output data stream.

In an embodiment, each of the plurality of payloads of the plurality of line encoded data streams has a rate selected from the group comprising 100 Mb/s, 1 Gb/s, 25 Gb/s, 50 Gb/s, and 100 Gb/s. The plurality of blocks incorporated in the line encoded output data stream may carry the plurality of payloads at a rate selected from the group comprising 100 Mb/s, 1 Gb/s, 25 Gb/s, 50 Gb/s, and 100 Gb/s.

In an embodiment, any one or more of the steps described above are performed by a logic device. The logic device may be at least one of a complex programmable logic device (CPD), a field programmable gate array (FPGA) and an application specific integrated circuit (ASIC).

An embodiment comprises the steps of:

retrieving from the plurality of line encoded data streams another block sequence carrying another payload;

commencing transmission of the other payload;

determine if the transmission of the other payload should be aborted using information in the other block sequence; and

if so determined, aborting the transmission of the other payload.

In an embodiment, the step of aborting transmission of the other payload comprises incorporating into the line encoded output data steam an abort block. The abort block may be, for example,one of an end-of-packet block and an error-indicating block. The plurality of line encoded data streams may be communicated to the CPD, FPGA or ASIC via a crosspoint switch.

Disclosed herein is a system for multiplexing a plurality of payloads. The system comprises a plurality of receivers for receiving a plurality of line encoded data streams. The system is configured to retrieve from the plurality of line encoded data streams a plurality of block sequences. The plurality of block sequences carry the plurality of payloads. The system comprises a transmitter configured to transit a line encoded output data stream having

incorporated therein the plurality of block sequences retrieved from the plurality of line encoded data streams.

In an embodiment, the plurality of receivers are configured to connect to a plurality of network cables that in use communicate the plurality of line encoded data streams.

In an embodiment, the transmitter is configured to connect to another network cable that in use communicates the output data stream.

In an embodiment, the plurality of receivers comprises a plurality of PHYs. The plurality of PHYs may be configured to regenerate the plurality of line encoded data streams. The plurality of PHYs may be configured to convert the plurality of block sequences from serial form to parallel form. The plurality of PHYs may be configured to align blocks of each of the plurality of block sequences. The plurality of PHYs may be configured to descramble each of the plurality of block sequences.

An embodiment comprises communication circuitry configured to multiplex the plurality of block sequences and communicate the plurality of block sequences so multiplexed from the plurality of receivers to the transmitter.

In an embodiment, the communication circuitry is at least in part within a logic device. The logic device may comprise at least one of a complex programmable logic device (CPD), a field programmable gate array (FPGA), and an Application Specific Integrated Circuit (ASIC).

An embodiment comprises a block sequence detector configured to detect the plurality of block sequences by determining at least one of a start-of-payload block and an end-of-payload block for each block sequence of the plurality of block sequences, and generate a plurality of detection signals each indicating at least one of a start-of-payload block and an end-of-payload block for each of the plurality of block sequences. A plurality of memories may be in communication with the block sequence detector. Each of the plurality of memories may be paired with one of the

plurality of line encoded data streams. The plurality of memories may comprise a plurality of first-in-first-out buffers (FIFOs).

An embodiment may comprise a scheduler configured to receive the plurality of detection signals and to schedule communication of the plurality of block sequences from the plurality of memories using the plurality of detection signals. The scheduler may be configured to schedule communication of the plurality of block sequences from the plurality of memories in the order that a respective detection signal of the plurality of detection signals are received. The scheduler may cause a switch to communicate the plurality of block sequences from the plurality of memories in the order in which a respective detection signal of the plurality of detection signals are received. The scheduler may cause the switch to communicate the plurality of block sequences from the plurality of memories to the transmitter. The scheduler may control an inter-payload spacing on the line encoded output data stream by scheduling the time for communication of the plurality of block sequences from the plurality of memories.

In an embodiment, the transmitter is configured to generate an output block stream comprising the plurality of block sequences retrieved from the plurality of line encoded data streams and a plurality of control blocks between the plurality of block sequences.

In an embodiment, the transmitter is configured to scramble each of the plurality of block sequences incorporated into the line encoded output data stream.

In an embodiment, the transmitter is configured to shape the line encoded output data stream. The transmitter may be configured to shape the power spectrum of the line encoded output data stream.

In an embodiment, each of the plurality of receivers and the transmitter have the same bit rate.

In an embodiment, the plurality of block sequences comprise at least one of a plurality of 64b/66b encoded blocks, a plurality of 64b/67b encoded blocks, a plurality of 6b/8b encoded

blocks, a plurality of 8b/10b encoded blocks, a plurality of 128b/132b encoded blocks, a plurality of 128b/132b encoded blocks, and a plurality of Hamming encoded blocks.

In an embodiment, the plurality of payloads comprise at least one of a plurality of Ethernet payloads, a plurality of InfiniBand payloads, a plurality of Fiber Channel payloads, a plurality of FireWire payloads and a plurality of PCIe payloads.

In an embodiment, the plurality of line encoded data stream are a plurality of block encoded data streams.

In an embodiment, the line encoded output data stream is a block encoded output data stream.

In an embodiment, each of the plurality of payloads of the plurality of line encoded data streams has a rate selected from the group comprising 100 Mb/s, 1 Gb/s, 25 Gb/s, 50 Gb/s, and 100 Gb/s.

In an embodiment, the plurality of blocks incorporated in the line encoded output data stream may carry the plurality of payloads at a rate selected from the group comprising 100 Mb/s, 1 Gb/s, 25 Gb/s, 50 Gb/s, and 100 Gb/s.

An embodiment comprises at least one of a complex programmable logic device, a field programmable gate array (FPGA) and an application specific integrated circuit (ASIC).

In an embodiment, the block sequence detector is configured to receive from the plurality of line encoded data streams another block sequence carrying another payload and the scheduler is configured to cause the transmitter to commence transmission of the other payload, the block sequence detector is configured to determine if the transmission of the other payload should be aborted using information in the other block sequence and if so determined cause the transmission of the other payload to be aborted. The block sequence detector may be configured to determine if the transmission of the other payload should be aborted using information in the other block sequence and if so determined abort the transmission of the other payload by causing

incorporation in the output data stream of an abort block. The abort block may be one of an end-of-packet block and an error-indicating block.

An embodiment comprises a crosspoint switch in communication with the plurality of receivers and the CPD, FPGA or ASIC.

Any of the various features of each of the above disclosures, and of the various features of the embodiments described below, can be combined as suitable and desired.

Brief description of the figures

Embodiments will now be described by way of example only with reference to the accompanying figures in which:

Figure 1 shows an embodiment of a system for multiplexing a plurality of payloads.

Figure 2 shows a table showing the 64b/66b blocking code structure defined by the standard IEEE 802.3.

Figure 3 shows a schematic diagram of an example configuration of a FPGA.

Figure 4 is a table of an example of an augmented 64b/66b block code structure.

Figures 5 and 6 show other embodiments of a system for multiplexing a plurality of payloads.

Description of embodiments

Figure 1 shows an embodiment of a system for multiplexing a plurality of payloads, the system being generally indicated by the numeral 10. The system 10 comprises a plurality of receivers 18, 29 for receiving a plurality of line encoded data streams. The system is configured to retrieve from the plurality of line encoded data streams a plurality of block sequences. The plurality of block sequences carry the plurality of payloads. The system comprises a transmitter 34

configured to transmit a line encoded output data stream having incorporated therein the plurality of block sequences retrieved from the plurality of line encoded data streams.

The system may generally be used in any multiplexing application where low latency is required, for example in cluster computing and supercomputing applications. In another example of the application, the plurality of

line encoded data streams may be generated by financial instrument transaction ordering computers, for example. The transmitter may, for example, be in communication with a machine in the form of a server, for example. The server may, for example, be in a stock exchange and be configured to execute orders for the buying and selling of financial instruments carried on the plurality of line encoded data streams.

The plurality of line encoded data streams are a plurality of block encoded data streams (which comprise the plurality of block sequences). The plurality of blocks are each a 64b/66b encoded block. Figure 2 shows a table showing the 64b/66b blocking code structure defined by the standard IEEE 802.3. The first byte of 8 bytes in each row 50 – 64 is a block type field showing a block type code in hexadecimal notation. Some example block types are detailed in the table of figure 2:

- Row 50 is the structure of an idle block (where each of the 7 bit C fields is 0000000 in binary);
- Row 52 is the structure of a start-of-packet block wherein the last three bytes are payload;
- Row 54 is the structure of a link status block;
- Row 55 is the structure of another start-of-packet block wherein the last seven bytes are payload;
- Row 57 is the structure of a end-of-packet block wherein none of the bytes are payload; and

- Row 58 is the structure of another end-of-packet block wherein the second byte is payload;

Any suitable type of blocks, however, may be used, for example any of 64b/67b blocks, 6b/8b blocks, 8b/10b blocks, 128b/132b blocks, 128b/132b encoded blocks, and Hamming encoded blocks. Common to the blocks in the embodiments disclosed herein is that the block encoding provides a mechanism for indicating that the block contains the start and/or end of a payload. Similarly, the line encoded output data stream is a block encoded output data stream.

The payloads generally, but not necessarily, comprise, for example, a payload header, and another payload. The payloads may also have a trailer. Communications may be structured in accordance with the Open Systems Interconnection (OSI) Model, in which each payload may be itself another packet of another layer of the OSI model. For example, at the physical layer the packet is a collection of bits, which are grouped into blocks. The plurality of payloads in this embodiment comprise an Ethernet packet. The Ethernet packet may, for example, have an internet protocol (IP) packet. The IP packet payload may comprise a TCP or UDP packet (or "segment"). This layered structure may continue to the Application layer.

This embodiment of the system 10 has a multilayer printed circuit board 12 having components mounted thereto which generally, but not necessarily, are connected to each other by conductive pathways, which may comprise, for example, tracks, signal traces, strip lines and/or micro strip lines, and wires, as appropriate. Generally, but not necessarily, the printed circuit board 12 is housed by a rack mountable enclosure having dimensions of 1 rack unit, although any suitable enclosure may be used or not used as desired. The printed circuit board has various surface mounted and/or through hole components mounted thereto.

A mains supply 14 may be mounted to the printed circuit board 12, the main supply in use producing a relatively low voltage, such as 12, 24 or 48 volts as suitable, from a relatively high voltage source, for example, a 110V or 240V electricity grid. There may be a DC regulator in the

form of a switched mode power supply module 15 mounted to the printed circuit board 12 that receives the low voltage output from the mains supply 14 and powers two or more active conductive rails integral to the circuit board 12. Alternatively, the mains supply and DC regulator may be mounted within the enclosure separate from the printed circuit board 12.

At least one fan 16 may be mounted to the circuit board 12 or alternatively the enclosure. The at least one fan may provide airflow across the multilayer printed circuit board to extract waste heat.

The printed circuit board 12 may also have mounted thereto a management unit 19 comprising, in this but not necessarily all embodiments, an ARM processor (or alternatively an Intel ATOM or PENTIUM processor, for example) communicating with serial and/or Ethernet interfaces 23 for receiving instructions via an Ethernet (or other) management network or other source, for example. The management unit 19 may also control active indicia 25 in the form of LED status lights mounted at the front of the enclosure.

The embodiment of the system 10 of figure 1 has a plurality of ports, for example ports17, 27. The plurality of ports 17, 27 are configured to connect to a plurality of network cables that in use conduct the plurality of line encoded data streams. Each of the plurality of ports is associated with one of the plurality of line encoded data streams. The transmitter 34 is also configured to connect to another network cable that in use communicates the output data stream. Consequently, the system may be part of a network in the form of, for example, a PAN, LAN, MAN, WAN or generally any suitable form of network.

The plurality of ports 17, 27, in this but not all embodiments, each have both of a receiver 18, 29 in the form of an optical-to-electrical (o/e) converter and a transmitter in the form of an electrical-to-optical (o/e) converter 21, 37 for bidirectional communication. In alternative embodiments described further below, the plurality of ports 17, 27 provide an electrical to electrical interface, for example supporting BASE-T Ethernet or direct attached copper cables.

In this embodiment, but not necessarily in all embodiments, the plurality of ports are configured to accept a network cable in the form of an optical network cable, specifically each of the plurality of ports are configured to receive two LC connectors terminating respective optical fibre cables that click into the port, but any suitable connectors (FC, SC for example) may be used. One of the optical fibers is for electromagnetic communications received by the port, and the other is for electromagnetic communications sent by the port. The plurality of ports 17, 27 and port 31 have an enhanced small form factor pluggable (SFP+) transceiver. Generally, however, any suitable transceiver may be used, for example any of gigabit interface converter (GBIC), small form factor plugable (SFP), 10 gigabit small form factor pluggable (XFP), 10 Gigabit Media Independent Interface (XAUI), C form-factor pluggable (CFP), quad small form-factor pluggable (QSFP), CXP specified by the Infiniband Trade Association, and a Thunderbolt transceiver. The plurality of ports may alternatively be configured to receive an electrical network cable in the form of, for example, a copper network cable.

The transceivers may be housed in enclosures in the form of SFP cages fixed to the printed circuit board 12. The cages provide an electrical connection between electrical contacts on the transceivers and the conductive tracks. The cages may also act as Faraday cages to reduce electromagnetic interference, and extract heat from the transceiver. In alternative embodiments, the transceivers may be mounted directly to the printed circuit board.

The plurality of ports 17, 27 generate electrical signals from the received optical signals, and subsequently communicate the electrical signals to the printed circuit board 12. The ports may support an Ethernet protocol, for example gigabit Ethernet, and receive and/or transmit Ethernet packets, but other embodiments may have transceivers that support Fibre Channel, FireWire, PCIe, USB or any other suitable protocol or standard. The plurality of payloads may comprise at least one of a plurality of Ethernet payloads, a plurality of InfiniBand payloads, a plurality of FiberChannel payloads, a plurality of FireWire payloads and a plurality of PCIe payloads. Generally but not necessarily the plurality of payloads are all of the same type. The ports may be

each configured for line encoded data streams carrying information having a rate selected from the group comprising 100 Mb/s, 1 Gb/s, 25 Gb/s, 50 Gb/s, and 100 Gb/s, for example, however generally any suitable rate may be selected. The line encoded output data stream and the plurality of line encoded data streams each carry information at a rate selected from the group comprising 100 Mb, 1 Gb, 25 Gb, 50 Gb, and 100 Gb. The actual line rate of the block encoded data is higher than these numbers. For example, 1 GB Ethernet has a line rate of 10/8x1Gb.s = 1.25 Gb/s, and 10G Ethernet is 66/64x 10Gb/s = 10.3125 Gb/s. The line rates are higher than the information rate because of block encoding overhead. Generally, but not necessarily, the plurality of line encoded data streams and the line encoded output data stream have the same rate. The system, however, may receive a plurality of line encoded data streams at one bit rate and transmit the line encoded output data stream at another protocol rate.

The conductive tracks 22 (which may comprise a plurality of micro-striplines, for example), provides a conduit for communications between the ports 17, 27, 31 and a logic device 24. In this embodiment the logic device 24 comprises a field programmable gate array (FPGA). In other embodiments, the logic device may be any suitable logic device, for example an application-specific integrated circuit (ASIC) and/or a complex programmable logic device (CPLD). Some embodiments comprise more than one logic device.

The field programmable array 24 may have any suitable architecture. In one embodiment, the FPGA architecture comprises an array of configurable logic blocks, I/O leads or pins, and routing channels. Generally but not necessarily, the logic blocks comprises of logical cells that may comprise of, for example, a look up table, a full adder, and a D-type flip flop. Clock signals may be routed through special purpose dedicated clock networks within the FPGA in communication with a reference clock 33 mounted on the printed circuit board 12. The FPGA 24 may also include higher-level functionality including embedded multipliers, generic digital signal processing blocks, embedded processors, high-speed I/O logic for communication with

components external of the FPGA (for example), and embedded memories that may be used by buffers.

The reference clock 33 has a frequency of 156.25 MHz, but generally any other suitable frequency may be used as appropriate, for example 125 MHz or a multiple of 156.25 MHz.

The internal structure of the FPGA is configured to form a plurality of modules. The modules are initially specified, for example, using a hardware description language, examples of which include VHDL and VERILOG. The functionality to be implemented on the FPGA is described in a hardware description language. The description is compiled, synthesized and mapped to the FPGA using appropriate EDA tools to a configuration file that, when loaded or programmed into the FPGA, causes the FPGA to implement the functionality described.

Figure 3 shows a schematic diagram of an example configuration of the FPGA 24 having a plurality of modules therein connected with a plurality of busses. The electrical signal 70 generated by an o/e converter at port 17 (or straight off the line in the case of the data stream being transmitted over a copper network cable) is received by a PHY in the form of a receive (Rx) PHY 72 on the FPGA 24. In this but not all embodiments, there is a plurality of clock and data recovery (CDR) devices electrically disposed between the plurality of ports and the FPGA 24. In alternative embodiments, the CDR devices may be incorporated in the FPGA 24. The Rx PHY 72 comprises circuitry that implements physical layer functions. Usually, a Rx PHY is in communication with a MAC, however this embodiment has no MAC on the FPGA 24 because the payloads are processed below the MAC layer. Similarly, the electrical signal 74 generated by another o/e converter at port 27 is received by another Rx PHY 76. In this embodiment there are more than two receivers, each comprising a port in communication with a respective Rx PHY. Embodiments may have 2, 3, 16, 32, 64 or generally any number of ports and PHYs.

The plurality of PHYs are configured to:

- convert the plurality of block sequences from serial form to parallel form;
- align blocks of each of the plurality of block sequences; and
- descramble each of the plurality of block sequences.

The plurality of PHYs are configured to regenerate the plurality of line encoded data streams. Another embodiment, however, does not regenerate the plurality of line encoded data streams.

The output of each of the Rx PHYs 72, 74 is the plurality of block sequences in parallel form, in proper alignment, and descrambled from their line encoded form. In this embodiment, each block of the plurality of block sequences is a 64b/66b block. The FPGA 24 has communication circuitry 78 that is configured to receive from the plurality of receivers via buses 80, 82 the plurality of block sequences, multiplex the plurality of block sequences, and then communicate the plurality of block sequences so multiplexed to the transmitter 34 via bus 84. The transmitter 34 is in the form of an o/e converter and is part of port 31. Port 31 also has a receiver 35 in the form of an e/o converter, which together with the transmitter 34 provides bidirectional communication. In alternative embodiments, port 31 provides electrical to electrical interfaces, for example supporting BASE-T Ethernet or direct attach copper cables. Port 34 comprises a transceiver as described above with respect to the plurality of ports 17, 27.

The Rx PHYs 72, 76 are in communication with a block sequence detector 86 on the FPGA 24. The block sequence detector 86 receives the plurality of block sequences from the plurality of Rx PHYs 72, 76. The block sequence detector is configured to detect the plurality of block sequences by determining at least one of a start-of-payload (SOP) block and an end-of-payload (EOP) block for each block sequence of the plurality of block sequences. The block sequence detector 86 determines the header (sync and block type field) of each block of the plurality of block sequences to determine whether each block is a start-of-payload block, an end-of-payload block, or a data block. The block sequence detector also generates a plurality of detection signals each indicating at least one of a start-of-payload block and an end-of-payload block for

each of the plurality of block sequences. In this embodiment, the block sequence detector 86 comprises a plurality of sub modules 98, 100 for respective Rx PHYs.

A plurality of memories 88, 90 on the FPGA 24 are in communication with the block sequence detector 86. While the block sequence detector 86 is in this embodiment in series with the plurality of memories 88, 90, it may alternatively be in parallel with them or generally disposed any suitable way. Each of the plurality of memories is paired with one of the plurality of line encoded data streams and the associated port. The block sequence detector generates a plurality of word sequences that are subsequently sent to the memories 88, 90. Each word of the plurality of word sequences comprises a block of a respective block sequence of the plurality of block sequences. The words are, in this but not all embodiments, longer than a block. The bit positions in the plurality of word sequences not occupied by blocks of the plurality of block sequences are signalling bits for signalling. The signalling bits may signal, for example, that the word comprises one of a start-of-payload block and an end-of-payload block (i.e. are detection signals). By incorporating the detection signals in the words, the SOP and EOP control blocks only need to be identified once in the FPGA, reducing processing and hence may further reduce latency. Figure 4 shows an example of an augmented block code structure. The augmentation includes words comprising additional bit positions to the block sequence. The additional bit positions include a bit that indicates if the associated block is a control block (CTL), if the block is an Start of Packet block (SOP), if the SOP occurs in the middle of the block (SOP1), if the packet is an End of Packet block (EOP) and a binary representation of the number of data bytes in the EOP block (EOP_POS).

In this but not necessarily in all embodiments, the plurality of memories 88, 90 comprise a plurality of first-in-first-out buffers (FIFOs),. The memories 88, 90 are configured for storing words generated by the block sequence detector. The memories 88, 90 are configured to receive a trigger signal and in response read out a word comprising a block of the plurality of block sequences. The trigger signal for a block of a payload may be received while the block's payload

is still being received. This technique may not be employed, however, when a payload is received while another is being transmitted. Another embodiment has a store-and-forward approach. Ideally, the trigger is received as soon as a block is received, but in the case significant jitter on one or both of the receive clock (the Rx PHY's clock) and the transmit clock (the Tx PHY's clock) the trigger may be delayed to ensure data is guaranteed to be available on the output of the FIFO when required.

In this embodiment, each Rx PHY 74, 76 has a respective Rx PHY clock from which they receive a Rx PHY clock signal. The Tx PHY 106 also has a respective Tx PHY clock from which it receives a Tx PHY clock signal. The boundary between a domain of any one of the Rx PHY clocks and the Tx PHY clock is at the plurality of memories 88,89. The plurality of memories minimise the amount of circuitry required for crossing clock domains.

On the FPGA is a scheduler 92 configured to receive the plurality of detection signals and to schedule communication of the plurality of block sequences from the plurality of memories using the plurality of detection signals. The scheduler 92 maintains its own scheduler queue 102 indicating the order of transmission. When reading a series of blocks from one of the memories 88,90, the scheduler 92 ensures that the each block sequence is completely read out (a SOP block, at least one data block, and an EOP block). The scheduler 92 then reads the scheduler queue to determine which memory 88,90 to source the next packet from.

There are many possible schedules, for example a round robin scheduling algorithm may be used. In this but not all embodiments, the communication of the plurality of block sequences are generally scheduled in the order that they are detected, which is generally preferred for financial trading applications. In the case that signals received from two or more Rx PHYs are temporally indistinguishable, the scheduler 92 may execute another algorithm to determine which port has priority. For example, the algorithm may be a round robin algorithm or arbitrarily give one of the ports priority. Random port selection may also be used.

Alternative embodiments may have the memories communicate with the scheduler when the next block to be read out is an EOP block, or the block detector communicates to the scheduler how many blocks are in each of the plurality of block sequences.

Data busses 94, 95 communicate the plurality of detection signals from the block sequence detector 86 to the scheduler 92. In this but not all embodiments, words from the block detector 86 are communicated to the scheduler 92, the detection signal being incorporated therein as described above. The scheduler 92 is configured to schedule communication of the plurality of block sequences from the plurality of memories 88, 90 in the order that a respective detection signal of the plurality of detection signals is received. The scheduler 92 causes a switch 94 in the form of a multi-way switch to communicate the plurality of block sequences from the plurality of memories in the order in which a respective detection signal of the plurality of detection signals are received. The scheduler 92 causes the switch to communicate the plurality of block sequences from the plurality of memories 88, 90 to the transmitter 34. It does this by sending memory selection information indicative of which memory the switch should address via bus 96. The scheduler 92 also sends a trigger signal via conduit 87, 89 to the memories 88, 90 indicating that they should read out a stored block. The scheduler 92 also controls an inter-payload spacing on the line encoded output data stream by scheduling the send time for each trigger signal.

The transmitter comprises a control block generator 104 configured to receive the plurality of block sequences from the switch 94. The control block generator 104 transmits the plurality of block sequences to a PHY in the form of a transmit (Tx) PHY 106, and a plurality of control blocks, for example idle blocks, in spaces between the plurality of block sequences. The control blocks may alternatively be link state or other in band control information. The Tx PHY 106 is configured to scramble each of the plurality of block sequences incorporated into the line encoded output data stream. The Tx PHY 106 is also configured, in this but not all embodiments, to shape the line encoded output data stream, and/or shaping the power spectrum of the line encoded output data stream.

The system 10 is configured to filter out blocks carrying payloads and satisfying a condition, however not all embodiments are able to filter out blocks carrying payloads. The block sequence detector 86 may receive from the plurality of line encoded data streams another block sequence carrying another payload and the scheduler 92 is configured to cause the transmitter 106 to commence transmission of the other payload. The block sequence detector 86 is configured to determine if the transmission of the other payload by the transmitter 106 should be aborted using information that the block sequence detector 86 retrieved from the other block sequence. If it is determined that transmission of the other payload should be aborted, for example if it satisfies a condition, the block sequence detector causes the transmission of the other payload to be aborted. The information in the other block sequence may be, for example, a source and/or destination address, for example a MAC or IP address, or generally any suitable address (an "address condition").

Transmission of the other payload is aborted, in this embodiment, by the block sequence detector 86 causing incorporation of an abort block on the output data stream.

Consequently, present embodiments may enhance network security and have the function of a firewall that controls network traffic on an applied rule set. The rule set may be, for example, filtering on the basis of addresses as described above, the detection of an abort code or generally any suitable rule. It will be appreciated however, that the filtering is occurring at level 1 of the OSI Model of the network. Consequently, the payload is not unpacked from a block sequence, inspected, then packed onto a new block sequence which reduces the latency addition of the present embodiments.

Figure 5 shows another embodiment of a system for multiplexing a plurality of payloads, the system being generally indicated by the numeral 200. Parts that are identical or similar to those of the system 10 of figure 1 are similarly numbered. The system 200 has all the functions of the system 10 and functions that are additional to system 10. The system 200 has communications

circuitry 205, which operate similarly or identically to the communications circuitry 78 of system 10 and to which the above disclosure with respect to communications circuitry 78 apply. The communications circuitry is, in this embodiment, configured as a 15:1 multiplexer (15 inputs and 1 output). The communications circuitry 205 is incorporated into a logic device in the form of an FPGA 24. The system 200 has a crosspoint switch 206 in communication with a plurality of ports (e.g. port 212) and the logic device 24. The communications circuitry 205 is configured to receive from a plurality of receivers (e.g. receiver 210) of the plurality of ports (e.g. port 212) via the cross point switch 206 a plurality of block sequences, multiplex the plurality of block sequences, and then communicate the plurality of block sequences so multiplexed via the crosspoint switch 206 to a transmitter 214 of a port in the form of a service port 216. The crosspoint switch 206 is also configured to broadcast the signals received on the receiver 218 associated with the port 216. In use, for example, the plurality of ports (e.g. 212) may be connected to a plurality of financial instrument transaction ordering computers and the service port 216 may be in communication with a trading engine located at, for example, a financial market.

Figure 6 shows still another embodiment of a system for multiplexing a plurality of payloads, the system being generally indicated by the numeral 300. Parts that are identical or similar to those of the system 10 of figure 1 are similarly numbered. The system 300 has all the functions of the system 10 and functions that are additional to system 10. The system 300 has a plurality of communications circuitry modules 202, 204, which each operate similarly or identically to the communications circuitry 78 of system 10 and to which the above disclosure with respect to communications circuitry 78 apply. Each of the plurality of communications circuitry modules is, in this embodiment, configured as a 7:1 multiplexer. The plurality of communications circuitry modules 202, 204 are incorporated into a logic device in the form of an FPGA 24. The system 300 has a crosspoint switch 206 in communication with a plurality of ports (e.g. port 312) and the logic device 24. Each of the communications circuitry modules 202 and 204 are each

configured to receive from the plurality of receivers (e.g. receiver 310) of the plurality of ports (e.g. port 312) via the cross point switch 206 the plurality of block sequences, multiplex the plurality of block sequences, and then communicate the plurality of block sequences so multiplexed via the crosspoint switch 206 to a transmitter (e.g. transmitter 314) of a service port 316. The crosspoint switch 206 is also configured to broadcast the signals received on the receiver associated with the transmitter port. In use, for example, the plurality of ports (e.g. 312) may be connected to a plurality of financial instrument transaction ordering computers, and the port in the form of a service port 316 may be in communication with a trading engine located at, for example, a financial market. The system 300 may communicate with two trading engines because it has two communication circuitry modules.

The systems 200 and 300 have a plurality of clock and data recovery modules 208 in communication with the plurality of ports and the logic device 24.

Generally, the logic device 24 (in this example in the form of a FPGA) of either one of the systems 200, 300 may be configured to have any of, for example: a 15:1 multiplexer, two 7:1 multiplexers; a 31:1 multiplexer; a 24:1 multiplexer and a 8:1 multiplexer; two 16:1 multiplexers; a 16:1 multiplexer and two 8:1 multiplexers; four 8:1 multiplexers; sixteen 2:1 multiplexers; and any suitable combination. The cross point switch is generally suitably configured for the chosen multiplexer configuration. Using a FPGA enables the system to be reconfigured at will.

Now that embodiments have been described, it will be appreciated that some embodiments have some of the following advantages:

- The multiplexing is performed at the block level rather than being decoded or converted to another form first, reducing latency and/or electronic complexity.

- Payloads may be filtered from the plurality of line encoded data streams to enhance network security, for example, while adding relatively little latency to payloads processed by embodiments.

Variations and/or modifications may be made to the embodiments described without departing from the spirit or ambit of the invention. For example, the plurality of line encoded data streams may be wirelessly received (for example via Wi-Fi or generally any suitable protocol), and the line encoded output data stream may be wirelessly transmitted (for example via Wi-Fi or generally any suitable protocol). The present embodiments are, therefore, to be considered in all respects as illustrative and not restrictive.

Prior art, if any, described herein is not to be taken as an admission that the prior art forms part of the common general knowledge in any jurisdiction.

In the claims which follow and in the preceding description of the invention, except where the context requires otherwise due to express language or necessary implication, the word "comprise" or variations such as "comprises" or "comprising" is used in an inclusive sense, that is to specify the presence of the stated features but not to preclude the presence or addition of further features in various embodiments of the invention.

Claims

1. A method for multiplexing a plurality of payloads, the method comprising the steps of:

receiving a plurality of line encoded data streams;

retrieving from the plurality of line encoded data streams a plurality of block sequences, the plurality of block sequences carrying the plurality of payloads; and

transmitting a line encoded output data stream having incorporated therein the plurality of block sequences retrieved from the plurality of line encoded data streams.

2. A method defined by claim 1 wherein the step of receiving the plurality of line encoded data streams comprises the step of a plurality of receivers receiving the plurality of line encoded data streams.

3. A method defined by claim 2 wherein the plurality of line encoded data streams are received via a plurality of network cables.

4. A method defined by either one of claim 2 and claim 3 wherein the step of retrieving from the plurality of line encoded data streams the plurality of block sequences carrying the plurality of payloads comprises the step of the plurality of receivers retrieving the plurality of block sequences carrying the plurality of payloads from the plurality of line encoded data streams.

5. A method defined by any one of claims 2 to 4 comprising the step of the plurality of receivers regenerating the plurality of line encoded data streams.

6. A method defined by any one of claims 2 to 4 wherein the step of retrieving from the plurality of line encoded data streams the plurality of block sequences comprises the step of the plurality of receivers performing a serial-to-parallel conversion on each of the plurality of block sequences.

7. A method defined by any one of the claims 2 to 5 wherein the step of retrieving from the plurality of line encoded data streams the plurality of block sequences comprises the step of the plurality of receivers performing a block alignment operation on each of the plurality of block sequences.

8. A method defined by any one of the claims 2 to 7 comprising the step of the plurality of receivers descrambling each of the plurality of block sequences.

9. A method defined by any one of the preceding claims, wherein the step of transmitting the line encoded output data stream comprises the step of a transmitter transmitting the line encoded output data stream.

10. A method defined by claim 9 wherein the step of transmitting the line encoded output data stream comprises the step of the line encoded output data stream being communicated over a network cable in communication with the transmitter.

11. A method defined by either one of claim 9 and claim 10 comprising the step of communicating the plurality of block sequences carrying the plurality of payloads so retrieved to the transmitter.

12. A method defined by any one of the preceding claims comprising the step of generating the line encoded output data stream having incorporated therein the plurality of block sequences retrieved from the plurality of line encoded data streams.

13. A method defined by any one of the claims 1 to 12 comprising the step of detecting the plurality of block sequences by detecting at least one of a start-of-payload block and a end-of-payload block for each block sequence of the plurality of block sequences.

14. A method defined by claim 13 comprising the step of storing the plurality of block sequences so identified in a plurality of memories.

15. A method defined by claim 14 wherein each of the plurality of memories are paired with one of the plurality of line encoded data streams.

16. A method defined by either one of claim 14 and claim 15 wherein the plurality of memories comprises a plurality of first-in-first-out buffers (FIFOs).

17. A method defined by any one of the claims 14 to 16 comprising the step of scheduling the order in which the plurality of block sequences are communicated from the plurality of memories.

18. A method defined by any one of the preceding claims comprising the step of controlling an inter-payload spacing on the line encoded output data stream.

19. A method defined by any one of the claims 14 to 18 comprising the step of generating a plurality of detection signals each indicating one of the start and an end of a respective block sequence of the plurality of block sequences.

20. A method defined by claim 19 comprising the step of scheduling the order in which the plurality of block sequences are communicated from the plurality of memories using the plurality of detection signals.

21. A method defined by claim 20 comprising the step of scheduling retrieval of each block sequence of the plurality of block sequences from the plurality of memories in the order that their respective detection signals are received.

22. A method defined by any one of claims 14 to 21 comprising the step of communicating the plurality of block sequences to a transmitter that generates the line encoded output data stream having incorporated therein the plurality of block sequences retrieved from the plurality of line encoded data streams.

23. A method defined by claim 22 comprising the step of the line encoded output data stream being communicated over a network cable in communication with the transmitter.

24. A method defined by any one of the preceding claims wherein the line encoded output data stream comprises an output block stream comprising the plurality of block sequences retrieved from the plurality of line encoded data streams and a plurality of control blocks disposed between the plurality of block sequences.

25. A method defined by claim 24 wherein each of the plurality of block sequences incorporated into the line encoded output data stream are scrambled.

26. A method defined by any one of the preceding claims comprising the step of shaping the transmitted line encoded output data stream.

27. A method defined by any one of the preceding claims comprising the step of shaping the power spectrum of the transmitted line encoded data stream.

28. A method defined by any one of the preceding claims wherein the bit rate of each of the plurality of line encoded data streams is the same as the bit rate of the line encoded output data stream.

29. A method defined by any one of the preceding claims wherein the plurality of block sequences comprises at least one of a plurality of 64b/66b encoded blocks, a plurality of 64b/67b encoded blocks, a plurality of 6b/8b encoded blocks, a plurality of 8b/10b encoded blocks, a plurality of 128b/132b encoded blocks, a plurality of 128b/132b encoded blocks, and a plurality of Hamming encoded blocks.

30. A method defined by any one of the preceding claims wherein the plurality of payloads comprise at least one of a plurality of Ethernet payloads, a plurality of InfiniBand

payloads, a plurality of FiberChannel payloads, a plurality of FireWire payloads and a plurality of PCIe payloads.

31. A method defined by any one of the preceding claims wherein the plurality of line encoded data stream are a plurality of block encoded data streams.

32. A method defined by any one of the preceding claims wherein the line encoded output data stream is a block encoded output data stream.

33. A method defined by any one of the preceding claims wherein each of the plurality of payloads of the plurality of line encoded data streams has a rate selected from the group comprising 100 Mb/s, 1 Gb/s, 25 Gb/s, 50 Gb/s, and 100 Gb/s.

34. A method defined by any one of the preceding claims wherein the plurality of blocks incorporated in the line encoded output data stream carries the plurality of payloads at a bit rate selected from the group comprising 100 Mb/s, 1 Gb/s, 25 Gb/s, 50 Gb/s, and 100 Gb/s.

35. A method defined by any one of the preceding claims wherein any selection of the steps thereof are performed by one of a complex programmable logic device, a field programmable gate array (FPGA) and an application specific integrated circuit (ASIC).

36. A system for multiplexing a plurality of payloads, the system comprising:

a plurality of receivers for receiving a plurality of line encoded data streams and configured to retrieve from the plurality of line encoded data streams a plurality of block sequences, the plurality of block sequences carrying the plurality of payloads; and

a transmitter configured to transit a line encoded output data stream having incorporated therein the plurality of block sequences retrieved from the plurality of line encoded data streams.

37. A system defined by claim 36 wherein the plurality of receivers are configured to connect to a plurality of network cables that in use communicate the plurality of line encoded data streams.

38. A system defined by either one of claim 36 and claim 37 wherein the transmitter is configured to connect to another network cable that in use communicates the output data stream.

39. A system defined by any one of the claims 36 to 38 wherein the plurality of receivers comprises a plurality of PHYs.

40. A system defined by claim 39 wherein the plurality of PHYs are configured to regenerate the plurality of line encoded data streams.

41. A system defined either one of claim 38 and claim 39 wherein the plurality of PHYs are configured to convert the plurality of block sequences from serial form to parallel form.

42. A system defined by any one of the claims 39 to 42 wherein the plurality of PHYs are configured to align blocks of each of the plurality of block sequences.

43. A system defined by any one of the claims 39 to 42 wherein the plurality of PHYs are configured to descramble each of the plurality of block sequences.

44. A system defined by any one of the claims 36 to 43 comprising communication circuitry configured to multiplex the plurality of block sequences and communicate the plurality of block sequences so multiplexed from the plurality of receivers to the transmitter.

45. A system defined by claim 44 wherein the communication circuitry is at least in part within at least one of a complex programmable logic device, a field programmable gate array (FPGA) and an Application Specific Integrated Circuit (ASIC).

46. A system defined by any one of the claims 36 to 45 wherein the transmitter is configured to generate an output block stream comprising the plurality of block sequences retrieved from the plurality of line encoded data streams and a plurality of control blocks between the plurality of block sequences.

47. A system defined by any one of the claims 36 to 46 wherein the transmitter is configured to scramble each of the plurality of block sequences incorporated into the line encoded output data stream.

48. A system defined by any one of the claims 36 to 47 wherein the transmitter is configured to regenerate each of the plurality of block sequences incorporated into the line encoded output data stream.

49. A system defined by claim 48 wherein the transmitter is configured to shape the power spectrum of the line encoded output data stream.

50. A system defined by any one of the claims 36 to 49 wherein each of the plurality of receivers and the transmitter have the same bit rate.

51. A system defined by any one of the claims 36 to 50 wherein the plurality of block sequences comprises at least one of a plurality of 64b/66b encoded blocks, a plurality of 64b/67b encoded blocks, a plurality of 6b/8b encoded blocks, a plurality of 8b/10b encoded blocks, a plurality of 128b/132b encoded blocks, a plurality of 128b/132b encoded blocks, and a plurality of Hamming encoded blocks.

52. A system defined by any one of the claims 36 to 51 wherein the plurality of payloads comprise at least one of a plurality of Ethernet payloads, a plurality of InfiniBand payloads, a plurality of FiberChannel payloads, a plurality of FireWire payloads and a plurality of PCIe payloads.

53. A system defined by any one of the claims 36 to 52 wherein the plurality of line encoded data streams are a plurality of block encoded data streams.

54. A system defined by any one of the claims 36 to 53 wherein the line encoded output data stream is a block encoded output data stream.

55. A system defined by any one of the claims 36 to 54 wherein each of the plurality of payloads of the plurality of line encoded data streams has a rate selected from the group comprising 100 Mb/s, 1 Gb/s, 25 Gb/s, 50 Gb/s, and 100 Gb/s.

56. A system defined by any one of the claims 36 to 55 wherein the line encoded output data stream carries the plurality of payloads at a rate selected from the group comprising 100 Mb/s, 1 Gb/s, 25 Gb/s, 50 Gb/s, and 100 Gb/s.

57. A system defined by any one of the claims 36 to 56 comprising one of complex programmable logic device, a field programmable gate array (FPGA) and an application specific integrated circuit (ASIC).

58. A system defined by any one of the claims 36 to 57 comprising a block sequence detector configured to detect the plurality of block sequences by determining at least one of a start-of-payload block and an end-of-payload block for each block sequence of the plurality of block sequences and generate a plurality of detection signals each indicating at least one of a start-of-payload block and an end-of-payload block sequence of the plurality of block sequences.

59. A system defined by claim 58 comprising a plurality of memories in communication with the block sequence detector, each of the plurality of memories being paired with one of the plurality of line encoded data streams.

60. A system defined by claim 59 wherein the plurality of memories comprises a plurality of first-in-first-out buffers (FIFOs).

61. A system defined by either one of claim 59 and claim 60 comprising a scheduler configured to receive the plurality of detection signals and to schedule communication of the plurality of block sequences from the plurality of memories using the plurality of detection signals.

62. A system defined by claim 61 wherein the scheduler is configured to schedule communication of the plurality of block sequences from the plurality of memories in the order that a respective detection signal of the plurality of detection signals are received.

63. A system defined by either one of claim 61 and claim 62 wherein the scheduler causes a switch to communicate the plurality of block sequences from the plurality of memories in the order in which a respective detection signal of the plurality of detection signals are received.

64. A system defined by claim 63 wherein the scheduler causes the switch to communicate the plurality of block sequences from the plurality of memories to the transmitter.

65. A system defined by either one of claim 63 and claim 64 wherein the scheduler controls an inter-payload spacing on the line encoded output data stream by scheduling the time for communication of the plurality of block sequences from the plurality of memories.

66. A system defined by any one of the claims 62 to 67 wherein the block sequence detector is configured to receive from the plurality of line encoded data streams another block sequence carrying another payload and the scheduler is configured to cause the transmitter to commence transmission of the other payload, the block sequence detector is configured to determine if the transmission of the other payload should be aborted

using information in the other block sequence and if so determined cause the transmission of the other payload to be aborted.

67. A system defined by claim 66 wherein the block sequence detector is configured to determine if the transmission of the other payload should be aborted using information in the other block sequence and if so determined abort the transmission of the other payload by causing incorporation of the output data stream of an abort block.

68. A system defined by claim 67 wherein the abort block is one of an end-of-packet block and an error-indicating block.

69. A system defined by claim 45 to 68 when dependent on claim 57 comprising a crosspoint switch in communication with the plurality of ports and the complex programmable logic device.

70. A method defined by any one of the claims 1 to 35 comprising the steps of:

retrieving from the plurality of line encoded data streams another block sequence carrying another payload;

commencing transmission of the other payload;

determine if the transmission of the other payload should be aborted using information in the other block sequence; and

if so determined, aborting the transmission of the other payload.

71. A method defined by claim 70 wherein the step of aborting transmission of the other payload comprises incorporating into the line encoded output data steam an abort block.

72. A method defined by claim 71 wherein the abort block is one of an end-of-packet block and an error-indicating block.

73. A method defined by any one of the claims 70 to 72 when dependent on claim 35 wherein the plurality of line encoded data streams are communicated to the complex programmable device via a crosspoint switch.

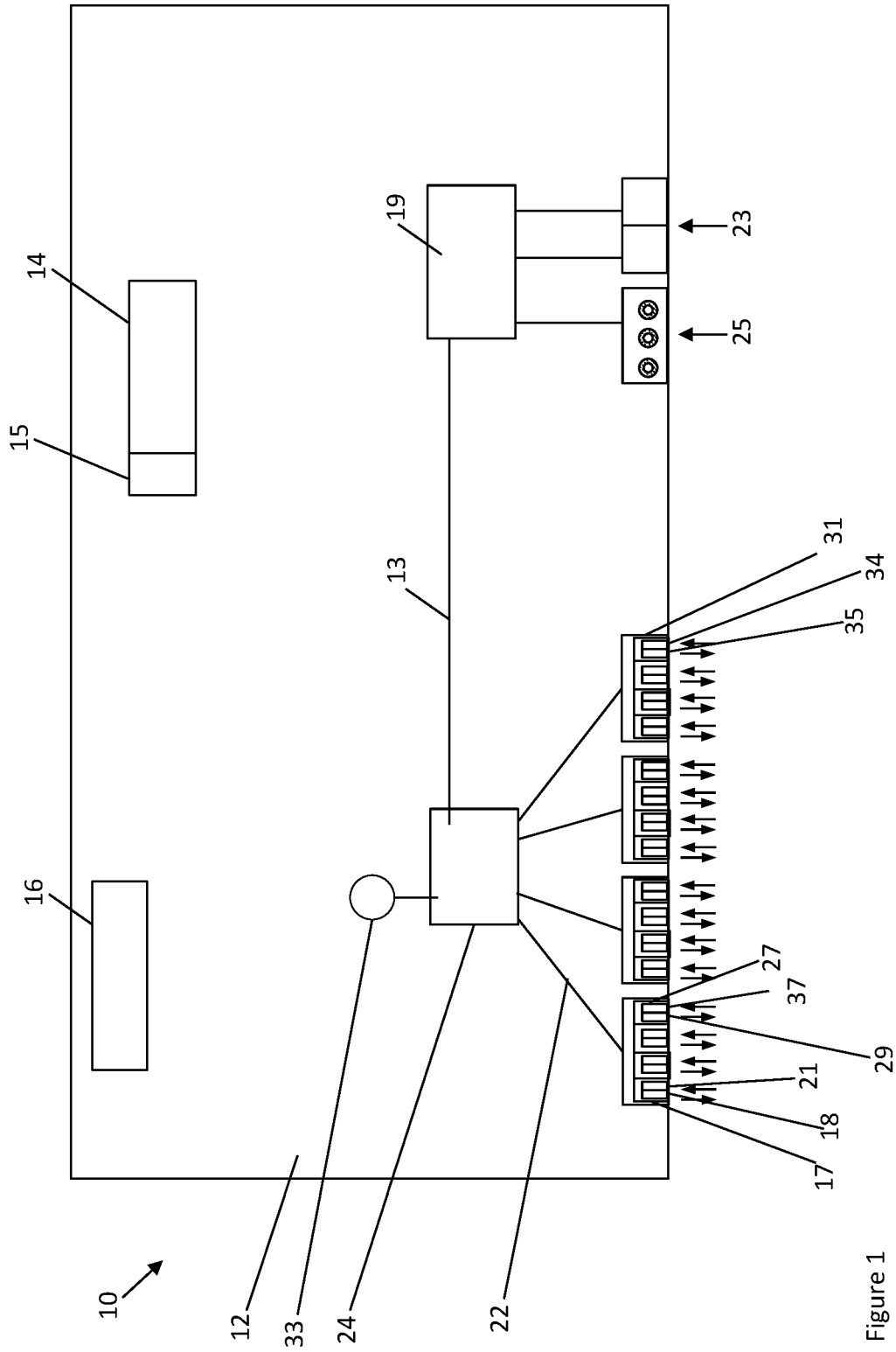

Figure 1

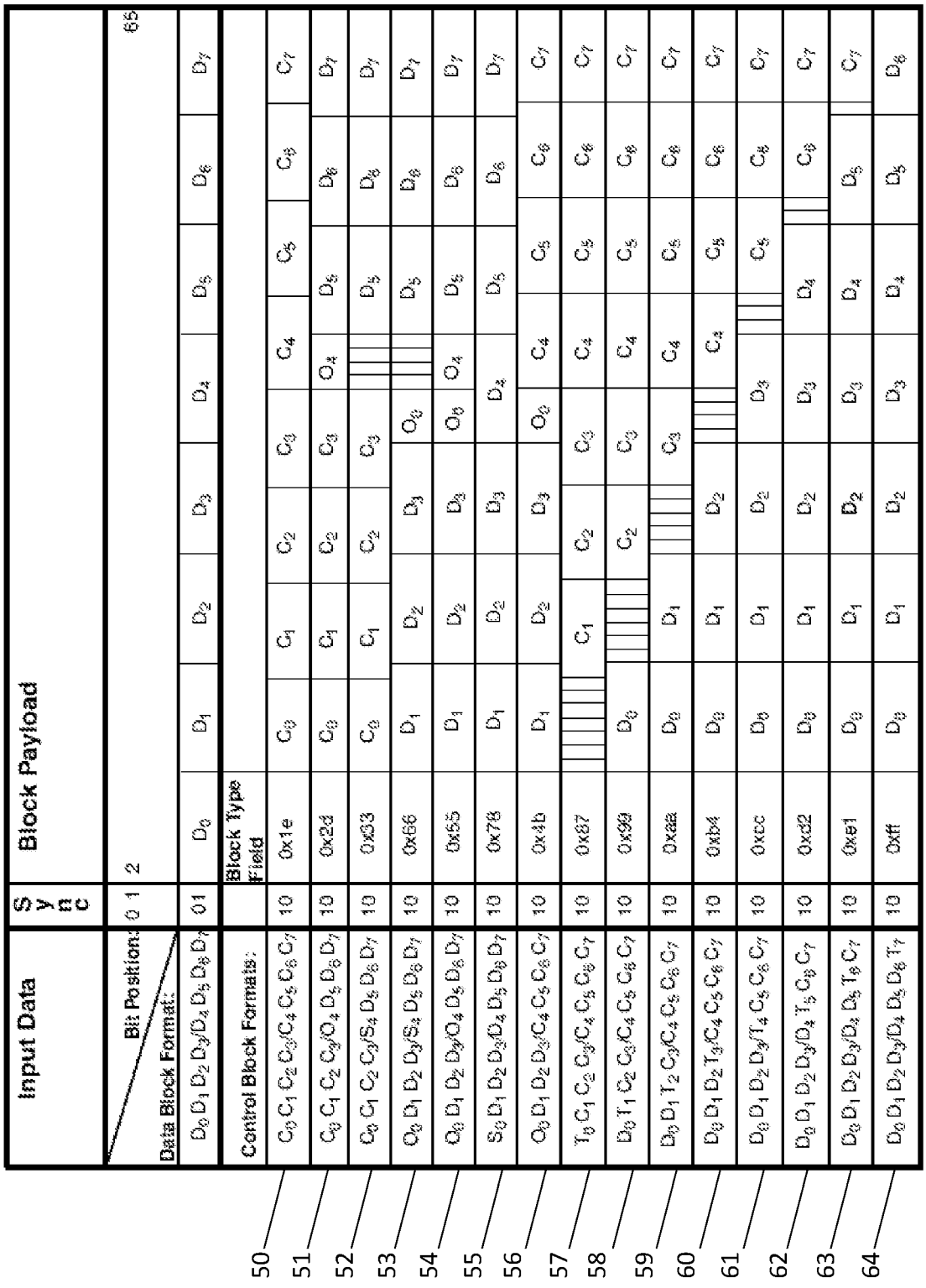
Input Data
Sync
Block Payload
Bit Position:
0 1 2
65
Data Block Format:
Control Block Formats:
Block Type Field
50
51
52
53
54
55
56
57
58
59
60
61
62
63
64

Figure 2

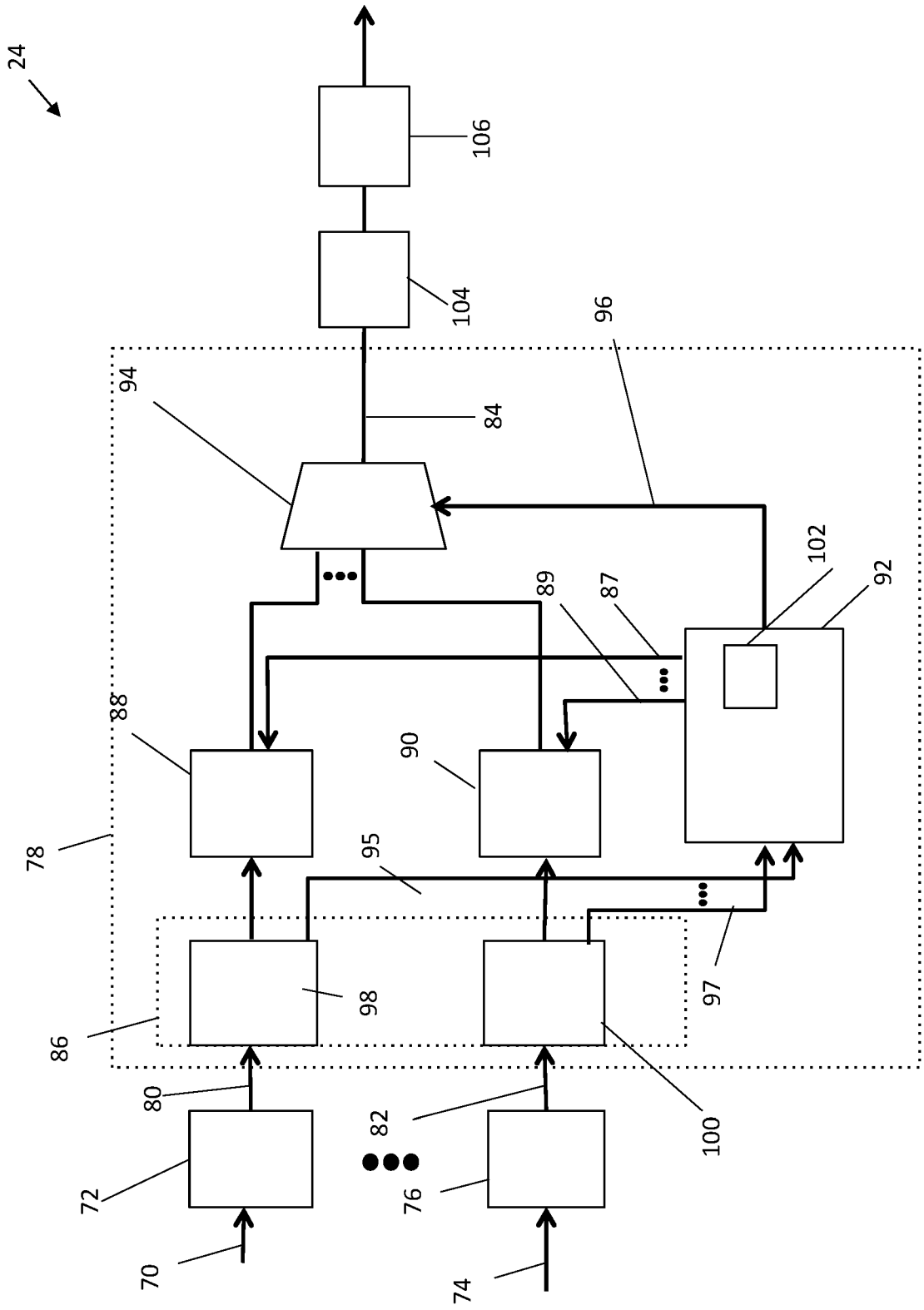
24
106
104
96
94
84
102
92
89
87
88
90
78
95
98
97
86
80
82
100
72
76
70
74

Figure 3

Input Data	Sync	Block Payload									NON BLOCK FIFO WORD DATA				
											CTL	SOP	SOP1	EOP	EOP_POS
Bit Position: / Data Block Format:	0 1	2								65	66	67	68	69	70-72
$D_0\ D_1\ D_2\ D_3/D_4\ D_5\ D_6\ D_7$	01	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7		0	0	0	0	000
Control Block Formats:		Block Type Field													
$C_0\ C_1\ C_2\ C_3/C_4\ C_5\ C_6\ C_7$	10	0x1e	C_0	C_1	C_2	C_3	C_4	C_5	C_6	C_7	1	0	0	0	000
$C_0\ C_1\ C_2\ C_3/O_4\ D_5\ D_6\ D_7$	10	0x2d	C_0	C_1	C_2	C_3	O_4	D_5	D_6	D_7	1	0	0	0	000
$C_0\ C_1\ C_2\ C_3/S_4\ D_5\ D_6\ D_7$	10	0x33	C_0	C_1	C_2	C_3		D_5	D_6	D_7	1	1	1	0	000
$O_0\ D_1\ D_2\ D_3/S_4\ D_5\ D_6\ D_7$	10	0x66	D_1	D_2	D_3	O_0		D_5	D_6	D_7	1	1	1	0	000
$O_0\ D_1\ D_2\ D_3/O_4\ D_5\ D_6\ D_7$	10	0x55	D_1	D_2	D_3	O_0	O_4	D_5	D_6	D_7	1	0	0	0	000
$S_0\ D_1\ D_2\ D_3/D_4\ D_5\ D_6\ D_7$	10	0x78	D_1	D_2	D_3	D_4		D_5	D_6	D_7	1	1	1	0	000
$O_0\ D_1\ D_2\ D_3/C_4\ C_5\ C_6\ C_7$	10	0x4b	D_1	D_2	D_3	O_0	C_4	C_5	C_6	C_7	1	0	0	0	000
$T_0\ C_1\ C_2\ C_3/C_4\ C_5\ C_6\ C_7$	10	0x87		C_1	C_2	C_3	C_4	C_5	C_6	C_7	1	0	0	1	000
$D_0\ T_1\ C_2\ C_3/C_4\ C_5\ C_6\ C_7$	10	0x99	D_0		C_2	C_3	C_4	C_5	C_6	C_7	1	0	0	1	001
$D_0\ D_1\ T_2\ C_3/C_4\ C_5\ C_6\ C_7$	10	0xaa	D_0	D_1		C_3	C_4	C_5	C_6	C_7	1	0	0	1	010
$D_0\ D_1\ D_2\ T_3/C_4\ C_5\ C_6\ C_7$	10	0xb4	D_0	D_1	D_2		C_4	C_5	C_6	C_7	1	0	0	1	011
$D_0\ D_1\ D_2\ D_3/T_4\ C_5\ C_6\ C_7$	10	0xcc	D_0	D_1	D_2	D_3		C_5	C_6	C_7	1	0	0	1	100
$D_0\ D_1\ D_2\ D_3/D_4\ T_5\ C_6\ C_7$	10	0xd2	D_0	D_1	D_2	D_3	D_4		C_6	C_7	1	0	0	1	101
$D_0\ D_1\ D_2\ D_3/D_4\ D_5\ T_6\ C_7$	10	0xe1	D_0	D_1	D_2	D_3	D_4	D_5		C_7	1	0	0	1	110
$D_0\ D_1\ D_2\ D_3/D_4\ D_5\ D_6\ T_7$	10	0xff	D_0	D_1	D_2	D_3	D_4	D_5	D_6		1	0	0	1	111

Figure 4

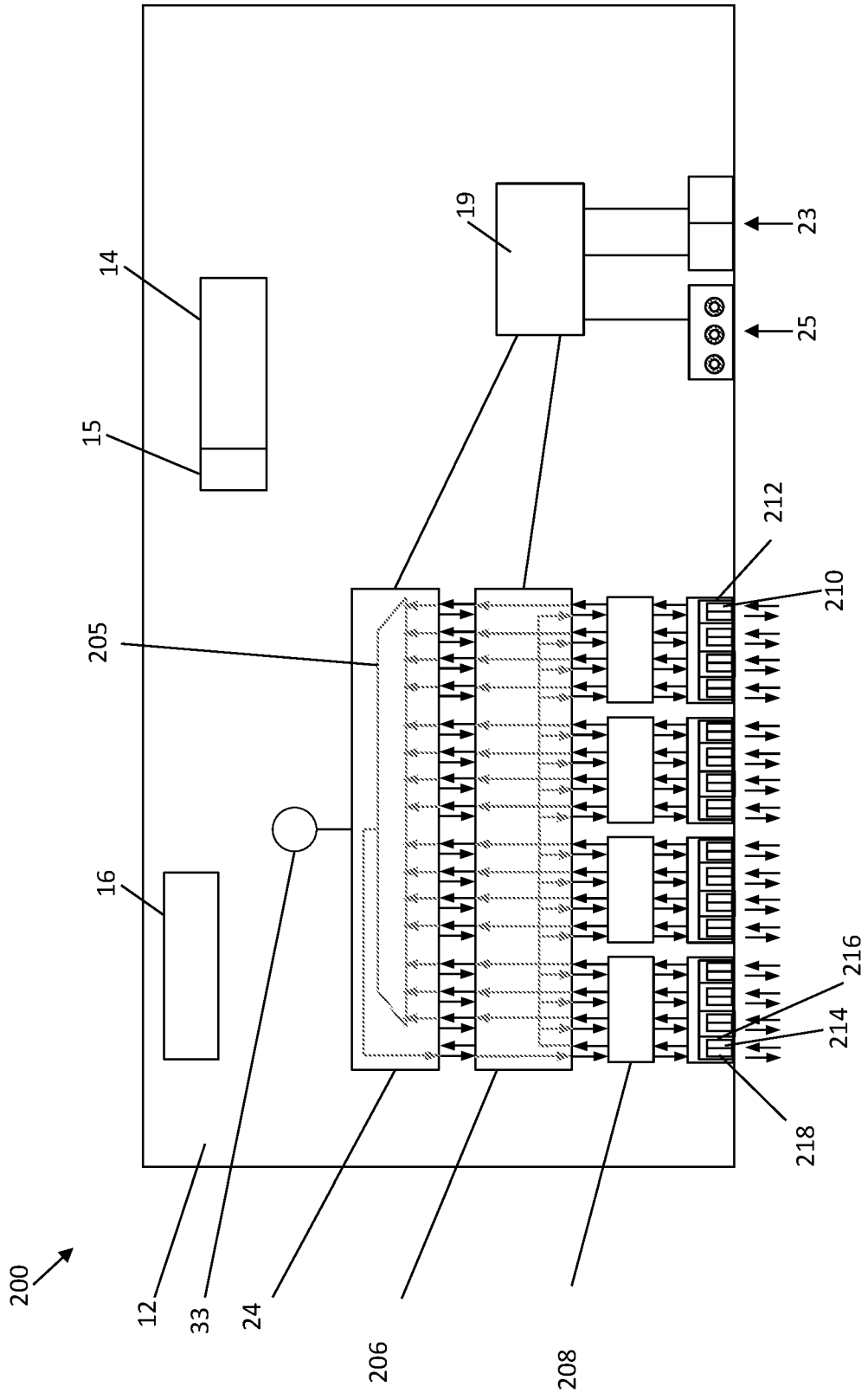

Figure 5

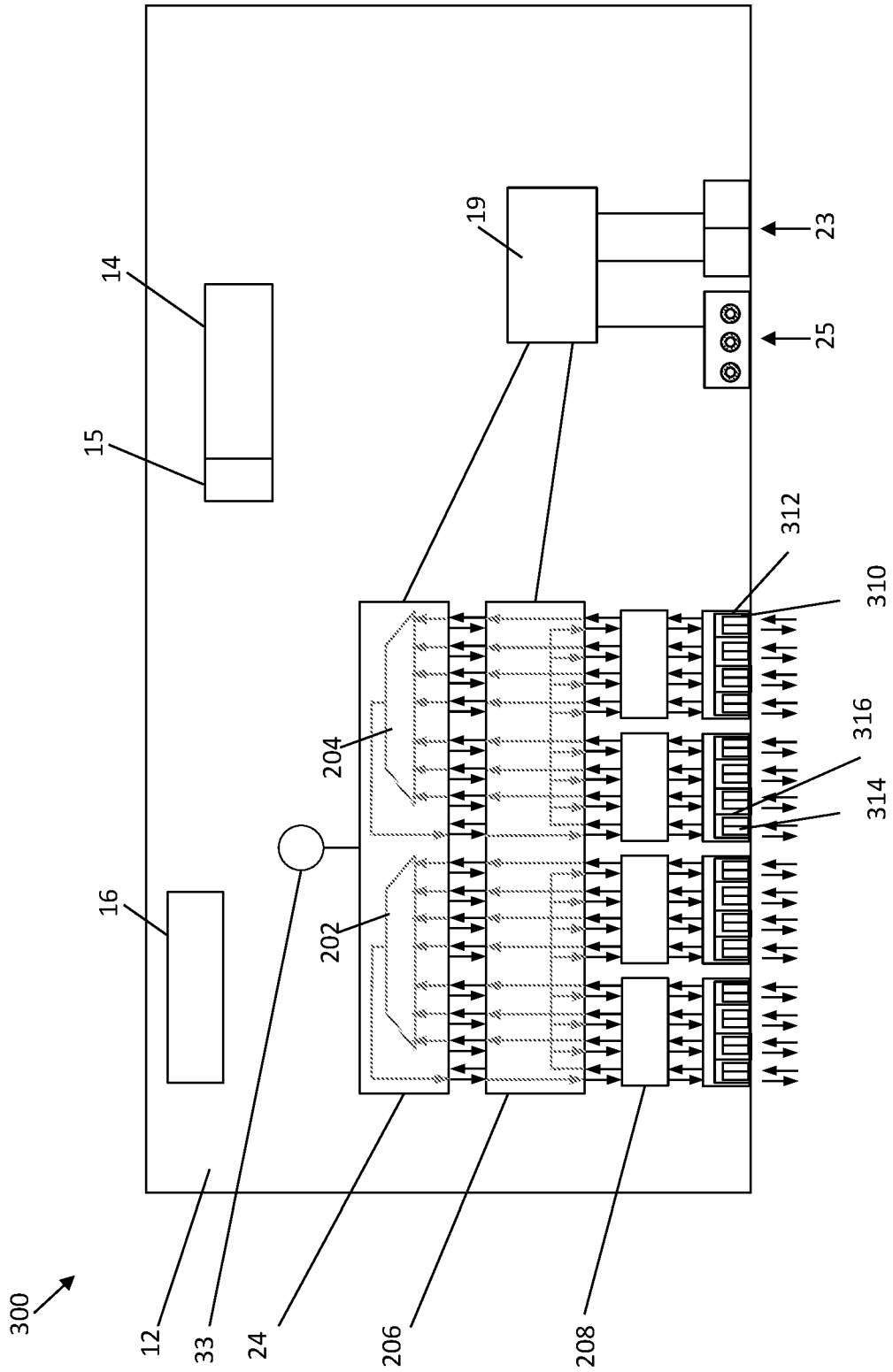

Figure 6

INTERNATIONAL SEARCH REPORT

International application No.
PCT/AU2016/050298

A. CLASSIFICATION OF SUBJECT MATTER

H04J 3/04 (2006.01) H04J 3/22 (2006.01)

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

Internal databases provided by IP Australia, AUSPAT, Espacenet, Lens searched for inventor and applicant names; **Google Web/Patents** search with keywords [Ethernet multiplexing, Gigabit Ethernet multiplexing, low latency network multiplexing, multiplex and (Ethernet or Firewire or PCIe or Infiniband)] and similar terms.

WPIAP, EPODOC database search with keywords [multiplex, payload, Ethernet, Infiniband, FireWire, PCIe, FibreChannel, line coding, 8B/10B, 64B/65B, SERDES] and similar terms.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
	Documents are listed in the continuation of Box C	

[X] Further documents are listed in the continuation of Box C [X] See patent family annex

* Special categories of cited documents:

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"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
30 June 2016	30 June 2016
Name and mailing address of the ISA/AU	**Authorised officer**
AUSTRALIAN PATENT OFFICE PO BOX 200, WODEN ACT 2606, AUSTRALIA Email address: pct@ipaustralia.gov.au	Marthinus Van Der Westhuizen AUSTRALIAN PATENT OFFICE (ISO 9001 Quality Certified Service) Telephone No. 0262832283

INTERNATIONAL SEARCH REPORT C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		International application No. **PCT/AU2016/050298**
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	US 2003/0185251 A1 (ICHINO et al.) 02 October 2003 title, abstract; fig.1, fig.2; para 0004-0011 whole document	1-6, 8-27, 29-34, 36-41, 43, 44, 46-49, 51-56, 58-65 7, 42, 66-68, 70-72
X	US 2010/0103954 A1 (CERRETA et al.) 29 April 2010 title, abstract; fig.1, 5, 7; para 0014, 0024, 0029	1-3, 9-12, 35-38, 44, 45, 57, 69 and 73
X	US 2012/0027020 A1 (SHIGIHARA et al.) 02 February 2012 title, abstract; fig.1, 3, 8, 9, 21; para 0001-0007, 0079, 0085, 0105	1, 9-12, 28, 36, 50
Y	US 7308006 B1 (BANERJEE et al.) 11 December 2007 title, abstract; fig.3; col.2 lines 1-14; col.6 line 46 to col.7 line 29	7, 42, 66-68, 70-72

INTERNATIONAL SEARCH REPORT Information on patent family members	International application No. **PCT/AU2016/050298**

This Annex lists known patent family members relating to the patent documents cited in the above-mentioned international search report. The Australian Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

Patent Document/s Cited in Search Report		**Patent Family Member/s**	
Publication Number	**Publication Date**	**Publication Number**	**Publication Date**
US 2003/0185251 A1	02 October 2003	US 2003185251 A1	02 Oct 2003
		CA 2423056 A1	28 Sep 2003
		CN 1449132 A	15 Oct 2003
		JP 2003289286 A	10 Oct 2003
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		US 8472482 B2	25 Jun 2013
US 2012/0027020 A1	02 February 2012	US 2012027020 A1	02 Feb 2012
		US 8792496 B2	29 Jul 2014
		JP 5467535 B2	09 Apr 2014
		WO 2010110413 A1	30 Sep 2010
US 7308006 B1	11 December 2007	US 7308006 B1	11 Dec 2007

End of Annex

Due to data integration issues this family listing may not include 10 digit Australian applications filed since May 2001.