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(54) Title: METHOD FOR IMPROVING TRANSISTOR PERFORMANCE

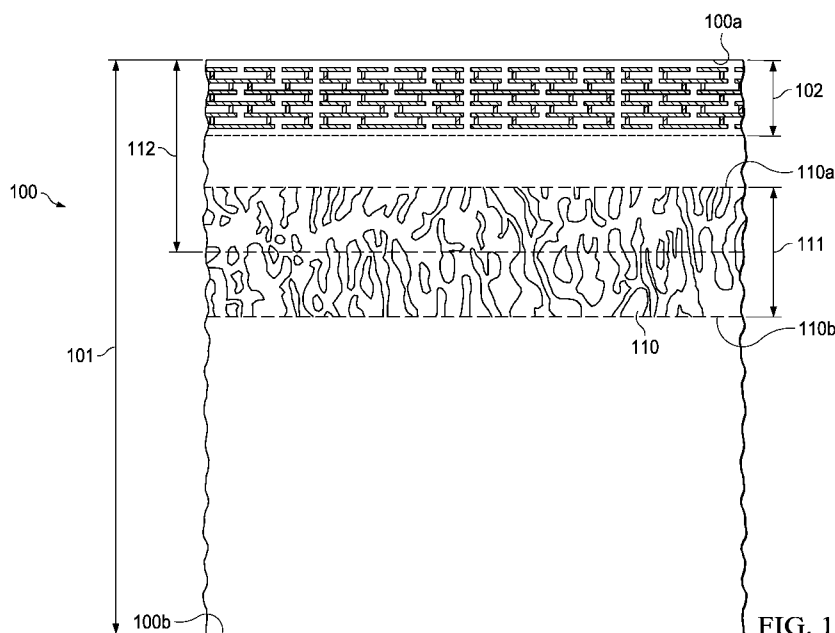


FIG. 1

(57) Abstract: A method to improve transistor performance uses a wafer (100) of single-crystalline semiconductor with a first zone (102) of field effect transistors (FETs) and circuitry at the wafer (100) surface, and an infrared (IR) laser with a lens for focusing the IR light to a second depth (112) farther from the wafer (100) surface than a first depth of the first zone (102). The focused laser beam is moved parallel to the wafer (100) surface across the wafer (100) to cause local multi-photon absorption at the second depth (112) for transforming the single-crystalline semiconductor into a second zone (111) of polycrystalline semiconductor with high density of dislocations. The second zone (111) has a height and lateral extensions, and permanently stresses the single-crystalline semiconductor. The stress increases a majority carrier mobility in the channel of the FETs, improving the transistor performance.



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- *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

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METHOD FOR IMPROVING TRANSISTOR PERFORMANCE

[0001] This relates generally to semiconductor devices and processes, and more particularly to a structure and fabrication method of creating intrinsic semiconductor lattice strain to increase carrier mobility and enhance field effect transistor performance.

BACKGROUND

[0002] When a body of a semiconductor such as silicon is in contact with another solid state material, stress in the semiconductor may usually be caused by one of two situations: Stress may be caused by a mismatch of the coefficients of thermal expansion (CTE) between the two materials, or stress may be caused by differences of the lattice constants of the two bodies.

[0003] Mechanical stress, when applied to a semiconductor lattice, leads to splitting of the conduction band and thus alters the effective mass of the majority carrier, leading to changes of the carrier mobility. For nMOS field effect transistors (FETs) with electrons as majority carriers, tensile stress to the channel lattice enhances the electron mobility in the channel. For pMOS FETs with holes as majority carriers, compressive stress to the channel lattice enhances the hole mobility in the channel. In both examples, the improvement of the carrier mobility leads to a decrease of the on-resistance between drain and source (R_{DSon}) and thus to improved FET efficiency. One frequently practiced technique to achieve such improved FET performance is the deposition of tensile silicon nitride layers on nMOS transistors, and compressive silicon nitride layers in pMOS transistors.

[0004] The effect that localized stress near the channel of a field effect transistor can result in improved electrical performance has been put to practice in the last few years by the production of semiconductor devices having a need for through-silicon vias (TSVs). The fabrication of TSVs starts while the device chips are still in un-thinned wafer form. Holes distributed across each chip area in the desired pattern are etched with uniform diameter and to a certain depth. The etching may be performed by chemical etching or be focused laser light. Then, a dielectric compound such as silicon nitride or silicon dioxide is deposited on the TSV sidewalls in order to create a thin insulating layer between the semiconductor material and the intended conductive

layers inside the TSV. Next, a metal seed layer (such as tantalum nitride or a refractory metal) is deposited on the insulating layer, followed by the deposition of the thicker metal filling (preferably copper). Thereafter, the wafer is thinned, by grinding or etching or both, until the bottom of the via holes are exposed and the TSVs are opened. The conductive via may be closed off by a solderable layer of nickel and palladium.

[0005] While the stress caused by the TSVs may result in large keep-out zones for three-dimensional integrated circuits (ICs), recent studies of TSV placements have resulted in stress-aware layouts to help IC transistors to benefit from the enhanced carrier mobility in the stress zones. For example, a study by Yang et al., based upon mobility dependence on stress and orientation between FET channel and TSV, showed how the optimum placement of TSVs can help improve the majority charge carrier mobility and thus result in improved transistor performance (see Yang, Jae-Seok, et al., “TSV stress aware timing analysis with applications to 3D-IC layout optimization”, Proceedings of the 47th Design Automation Conference; ACM, June 13-18, 2010, pp. 803-806).

SUMMARY

[0006] In described examples of a process flow, a wafer of single-crystalline semiconductor material (such as silicon) is provided. The wafer has a surface and includes chips with field-effect transistors and integrated circuitry. The circuitry extends to a first depth from the surface. Also, an infrared (IR) laser is selected, so that its wavelength can be focused to a second depth greater than the first depth and allows a high percentage of the focused energy to be absorbed by the single-crystalline semiconductor lattice without ablation. The preferred wavelength range for the operation is between 900 nm and 1000 nm, allowing an internal transmittance between about 50% and 70%. The absorbed energy can then transform the single-crystalline semiconductor lattice into an amorphous polycrystalline region with high density of dislocations.

[0007] After focusing the IR laser to the second depth, where the optical damage by multi-photon absorption creates modification of the single-crystalline semiconductor into polycrystalline material with a high density of dislocations, the focused beam is moved parallel to the surface across the wafer. The moving local multi-photon absorption at the second depth forms a zone of the polycrystalline semiconductor. Zones of various extension may be created. The movement may be repeated until a polycrystalline zone of about 30 μm height is created.

The polycrystalline zone creates an intrinsic permanent strain in the single-crystalline lattice near the FET structures, which in turn results in increased mobility of the majority device carriers and thus a more efficient FET performance, such as by lowering the R_{DSon} resistance.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] FIG. 1 shows a cross section of portion of a semiconductor chip with the integrated circuit zone near the chip surface and the embedded zone of amorphous polysilicon for creating strain in the single-crystal lattice.

[0009] FIG. 2A is a schematic representation of the effect of stresses in an nMOS field effect transistor: Tensile stresses enhance electron mobility in the gate channel.

[0010] FIG. 2B is a schematic representation of the effect of stresses in a pMOS field effect transistor: Compressive stresses enhance hole mobility in the gate channel.

[0011] FIG. 3 illustrates the methodology of moving the focus of an infrared laser parallel to the surface of a single-crystalline semiconductor chip, creating a zone of amorphous semiconductor.

[0012] FIG. 4 shows the diagram of a process flow for using focused infrared laser light to create a zone of amorphous polysilicon embedded in single-crystal silicon.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0013] The intrinsic resistance of a field effect transistor (FET) is important for performance. Decreasing the intrinsic resistance (usually the on-resistance of the channel between source and drain of a field effect transistor) increases the transistor efficiency. Localized stresses near a transistor may result in improved electrical performance by enhancing majority carrier mobility, and numerous semiconductor products may be improved by a method (preferably a low cost method) to create such localized stress throughout the product, where field effect transistors operate.

[0014] Example embodiments solve the problem of creating an intrinsic strain near a FET in a semiconductor chip, and thus an increased mobility of the FET majority carrier in the gate channel, by using the focused energy of an infrared stealth laser to form optical damage by multi-photon absorption in a location determined by the position of the laser focus. The multi-photon absorption produces a region of amorphous poly-semiconductor near an FET.

[0015] By moving the focused laser parallel to the chip surface, a zone of amorphous semiconductor is created. The amorphous poly-semiconductor creates a permanent intrinsic

strain in the single-crystalline lattice near the FET structure. The strain, in turn, increases the mobility of the majority carrier in the gate channel of the FET.

[0016] Example embodiments use a focused infrared laser light moving along a direction to create (at the depth of the focus) an embedded precise layer of amorphous poly-semiconductor, which permanently stresses the single-crystalline bulk semiconductor and thus increases the majority carrier mobility in the channel of a field effect transistor.

[0017] FIG. 1 illustrates as an example of crystal alteration of a portion of a chip made of a single-crystalline semiconductor, such as silicon; the chip portion is generally designated 100. Other bulk semiconductors include silicon germanium, gallium nitride, gallium arsenide, and any other compound used in fabrication of semiconductor devices. Chip 100 has a first surface 100a, a second surface 100b, and a thickness 101. In preferred embodiments, thickness 101 is in the range from about 70 μm to 150 μm (but may be thinner or thicker).

[0018] A zone (with transistors and circuitry) is near first surface 100a. This integrated circuit zone is referred to herein as first zone; it has a first depth 102 from first surface 100a. In the example of FIG. 1, first depth 102 is between about 6 μm and 12 μm dependent on the number of metallization levels employed. In preferred embodiments, the first zone includes one or more field effect transistors (FETs) made according to MOS technology. The FETs may be nMOS or pMOS devices dependent on the conductivity type and the majority carrier of the bulk semiconductor.

[0019] FIG. 1 illustrates a second zone 110 of polycrystalline semiconductor with a high density of dislocations. In the example of FIG. 1, second zone 110 has a height 111 of about 30 μm ; in other embodiments, the height may be thicker or thinner. Second zone 110 further has borderlines 110a and 110b, which are substantially planar and parallel to chip surfaces 100a and 100b. The middle line of second zone 110 is spaced by a distance 112 from the chip surface 110a; in the example of FIG. 1, distance 112 is between about 30 μm and 50 μm ; in other devices, it may be smaller or greater. In some devices, borderline 110a may reach near the borderline of the circuitry zone (first zone).

[0020] As described hereinbelow, the polycrystalline semiconductor of zone 110 is created from the single-crystalline bulk semiconductor by the optical damage caused in multi-photon absorption of the energy of a focused infrared laser, which has been directed towards, and is moving parallel to, the chip surface 100a. The amorphous poly-semiconductor creates a

permanent intrinsic strain in the single-crystalline lattice near the zone of integrated circuitry with the FET structures. The strain, in turn, affects the mobility of the majority carriers in the gate channels of the FETs.

[0021] The strain of a lattice multiplied by the modulus of the material results in the stress in the lattice (mechanical stress is measured in pascals, Pa). Because lattice stress leads to splitting of the conduction band, the effective mass of a carrier can be altered; this effect results in changes of the carrier mobility. If the goal is to improve the carrier mobility, semiconductor devices of pMOS and nMOS technologies require different stress types, because the majority carriers are different; in nMOS devices, electrons are majority carriers, in pMOS devices, holes are the majority carriers.

[0022] FIGs. 2A and 2B summarize the stress types necessary to improve majority carrier mobility in field effect transistors (FETs), schematically depicted to emphasize the channel between source and drain. As FIG. 2A shows, for an nMOS FET with electrons as majority carriers, tensile stress in the x-direction between source and drain can increase the electron mobility in the channel between source and drain. FIG. 2B depicts the corresponding situation for a pMOS FET; with holes as majority carriers, compressive stress in the x-direction between source and drain can increase the hole mobility in the channel between source and drain. In either case, increased carrier mobility is proportional to increased carrier speed and thus improved FET performance.

[0023] Another embodiment is a method for creating the stresses in the semiconductor lattice to improve carrier mobility and thus the performance of transistors. The method is illustrated in FIG. 3 and summarized in FIG. 4. The method starts by providing a wafer 300 of a single-crystalline semiconductor (process 401). The wafer has a surface 300a and multiple device chips. The wafer has completed those front-end processes, which result in fabrication of field effect transistors (FETs) and circuitry in a zone of depth 302 from surface 300a. In FIG. 3, wafer 300 is shown having its final thickness 301 after the process of back-grinding; yet for practical reasons, the laser process to be described is preferably executed while the wafer still has its original thickness before back-grinding.

[0024] In process 402, an infrared (IR) laser is provided, which is suitable for stealth technology, also referred to as Mahoh technology. Suitable lasers are commercially available from a number of companies in the U.S., Japan, and other sources; a few of these companies are

Hamamatsu, Disco, and Accretech. In the so-called stealth methodology, a laser is selected for its light operating according to a plot of Internal Transmittance (in %) as a function of the Wavelength (in nm). At IR wavelengths shorter than about 800 nm, the laser energy is high enough to be used for ablating an object, so that the transmittance is negligible (about 0 %). This wavelength regime is often referred to as laser dicing. At wavelengths longer than about 1100 nm, the laser energy is weak enough to be transmitted through the object, so that the transmittance is about 100 %. The wavelength regime is often referred to as stealth dicing.

[0025] As an example, in stealth technology, or Mahoh technology, the IR wavelength may be between 900 nm and 1000 nm, and the transmittance is in the range between 30 % and 70 %, and preferably about 50 %. For the method illustrated in FIG. 3, the IR light is designated 350 and the focusing lens 351. An example IR laser engine may produce 1.2 W pulsed power so that at the focal area the semiconductor bulk experiences internal modification by optical damage caused by multi-photon absorption. The focal area may be fixed to a usual size of about 15 μm diameter. The depth 312 of the focal area can be controlled working from the bottom of the semiconductor wafer up; in FIG. 3, the wafer of thickness 301 has the bottom at the wafer surface opposite surface 300a with the circuitry and transistors in first zone 302. The transformation of the single-crystalline semiconductor material into poly-crystalline semiconductor with high density of dislocations occurs within second zone 311 and can be controlled by laser power, feed rate, and wavelength. For its effect on FETs and circuitry in first zone 302, the proximity of second zone 311 relative to first zone 302 may reach from just a few micrometers to about 50 μm .

[0026] As described, the IR light 350 of the laser falls into a range of wave lengths, which can readily be absorbed by the semiconductor lattice (preferably monocrystalline silicon). In process 403, a lens 351 focuses the IR light to a focal point, which is spaced from surface 300a with the FTEs. For the example of FIG. 1, distance 312 may be in the 30 μm to 50 μm range. The energy of the laser light is absorbed by the single-crystalline semiconductor in so-called multi-photon absorption, which disturbs the single crystallinity of the lattice so that the resulting optical damage and energy absorption morphs the single-crystalline semiconductor into a polycrystalline and amorphous configuration within a zone of width 311. In the example of FIG. 1, width 311 is about 30 μm wide. The borders of second zone 311 are parallel to the wafer surface 300a and approximately planar. Zone 311 may be subdivided into sections with lateral

dimensions smaller than the length of device chip. The high density of dislocations in the polycrystalline semiconductor exerts stress on the single-crystalline lattice of the semiconductor between zones 311 and 302. As described hereinabove, this stress enhances the mobility of majority carriers in FETs positioned in suitable orientation.

[0027] In process 404, the focused infrared laser beam is moved parallel to the wafer surface 300a across wafer 300. This movement extends zone 311 of polycrystalline semiconductor in the direction parallel to surface 300a. For some devices, the movement thus the polycrystalline extension may be short. However, for other devices, the movement may extend across the whole wafer, so that the polycrystalline zone extends across the whole length of each chip. In either case, the height of the polycrystalline zone is approximately 30 μm .

[0028] The laser movement may be repeated several times to widen the area of the polycrystalline zone (second zone), until the whole area of active circuitry is paralleled by a zone of polycrystalline semiconductor with an area sized to equal the circuitry area. The borders of the second zone are approximately planar and parallel to the wafer surface 300a.

[0029] After the second zone of polycrystalline semiconductor is created, a dicing process singulates wafer 300 into discrete device chips. Each chip includes a zone of polycrystalline semiconductor embedded in the single-crystalline bulk semiconductor.

[0030] Example embodiments are applicable to any semiconductor material, including silicon, silicon germanium, gallium arsenide, gallium nitride, or any other semiconductor or compound material used in manufacturing. As another example, example embodiments are applicable to any zone of polycrystalline semiconductor embedded in single-crystalline semiconductor, regardless of the geometries of the second zone (such as lateral dimensions, thickness and planarity), the degree of poly-crystallinity, and the position of the second zone relative to the first zone of circuitry. As another example, the semiconductor chip may be free of an encapsulation, or it may be in an additional package.

[0031] Modifications are possible in the described embodiments, and other embodiments are possible, within the scope of the claims.

CLAIMS

What is claimed is:

1. A method of improving transistor performance, the method comprising:
providing a wafer of a single-crystalline semiconductor, the wafer having a surface and a plurality of device chips including a first zone of field effect transistors (FETs) and circuitry extending to a first depth from the surface;
providing an infrared (IR) laser having a lens for focusing the IR light to a second depth from the wafer surface, the second depth greater than the first depth; and
moving the focused laser beam parallel to the surface across the wafer to cause local multi-photon absorption at the second depth for transforming the single-crystalline semiconductor into a second zone of polycrystalline semiconductor with high density of dislocations, the second zone having a height and lateral extensions.
2. The method of claim 1 wherein the polycrystalline semiconductor of the zone is amorphous.
3. The method of claim 1 wherein the infrared laser is a stealth laser.
4. The method of claim 1 wherein the first depth is between about 6 μm and 12 μm dependent on the number of metallization levels employed.
5. The method of claim 1 wherein the second depth is between approximately 6 μm and 50 μm .
6. The method of claim 1 wherein the height of the zone is between about 10 μm and 30 μm .
7. The method of claim 1 wherein the zone may be subdivided into sections having lateral dimensions smaller than the length of a device chip.
8. The method of claim 1 wherein the borders of the zone of amorphous polycrystalline semiconductor are parallel to the wafer surface and approximately planar.
9. The method of claim 1 further including the process of singulating the wafer into discrete device chips, each chip having a zone of polycrystalline semiconductor embedded in the single crystalline semiconductor.
10. A semiconductor device comprising:
a chip of single-crystalline semiconductor having a surface and a first zone of field effect transistors (FETs) and circuitry extending to a first depth from the surface, the first zone

parallel to the chip surface; and

a second zone of polycrystalline semiconductor with high density of dislocations, the second zone parallel to the chip surface and having a center plane at a second depth from the chip surface, the second depth greater than the first depth, the second zone having a height and lateral extensions.

11. The device of claim 10 wherein the first depth is between about 6 μm and 12 μm dependent on the number of metallization levels employed.

12. The device of claim 10 wherein the second depth is between approximately 6 μm and 50 μm .

13. The device of claim 10 wherein the height of the zone is between about 10 μm and 30 μm .

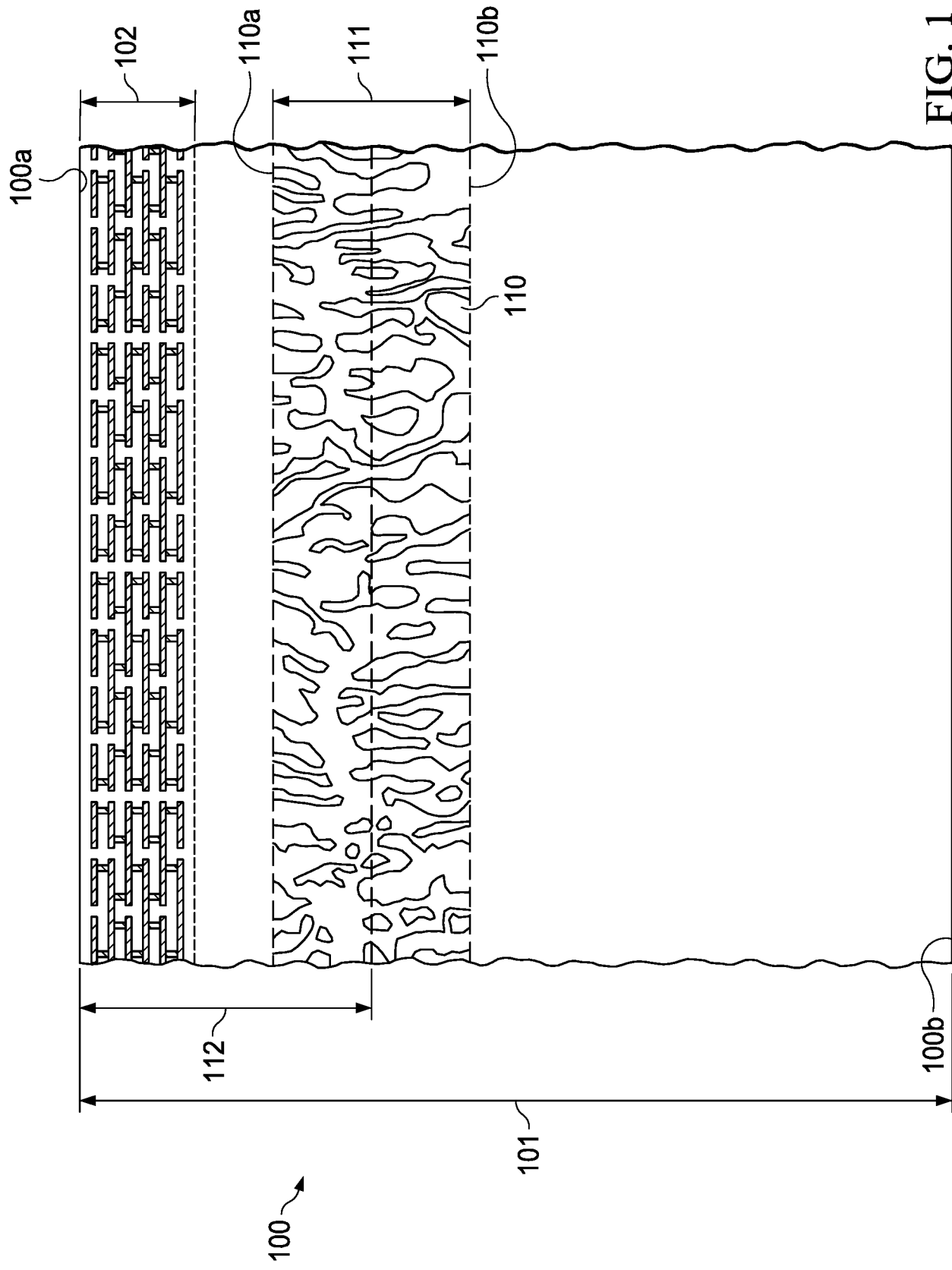


FIG. 1

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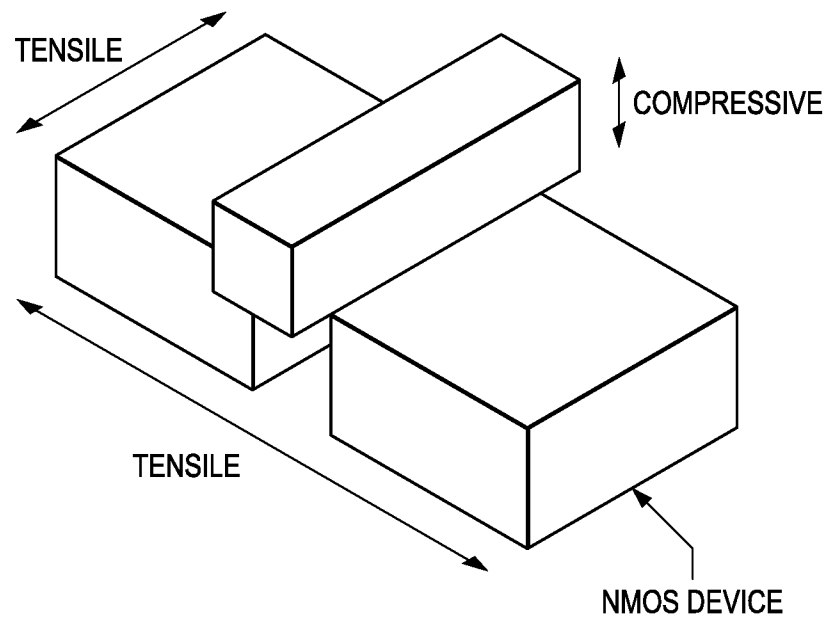


FIG. 2A

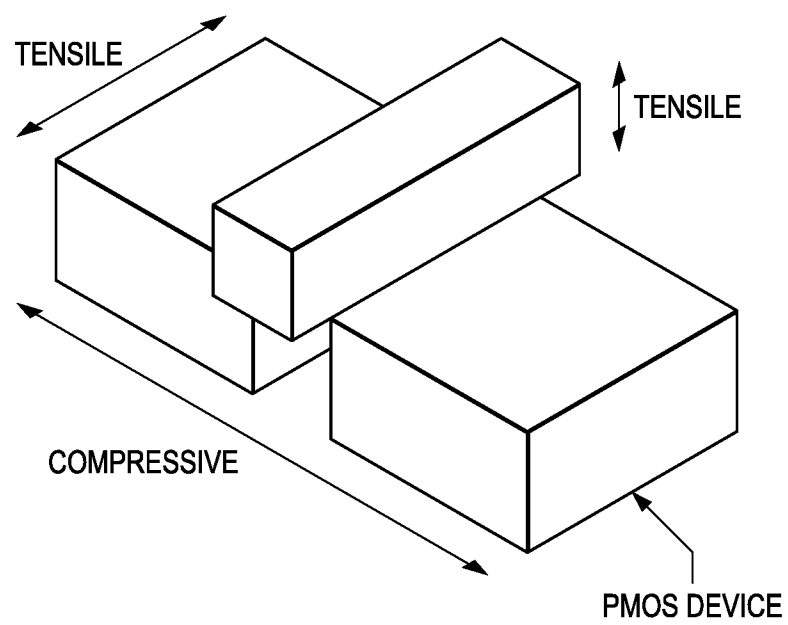
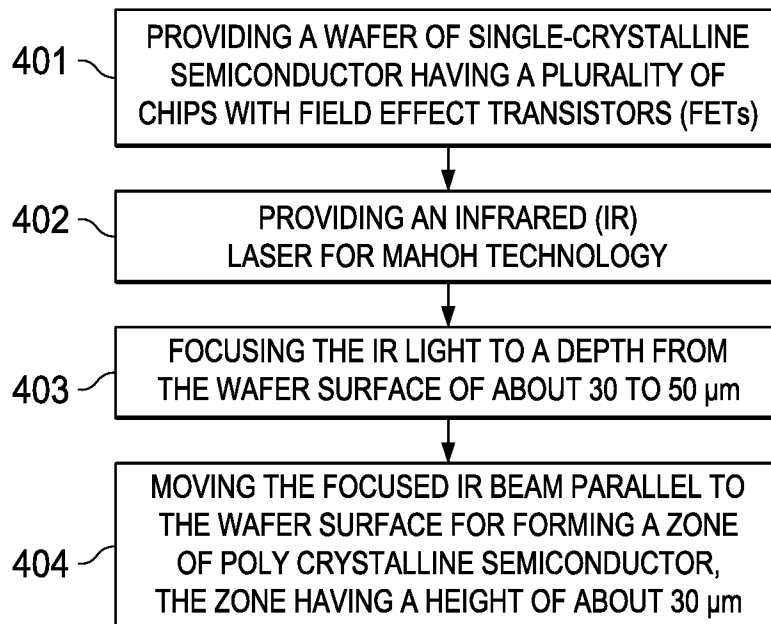
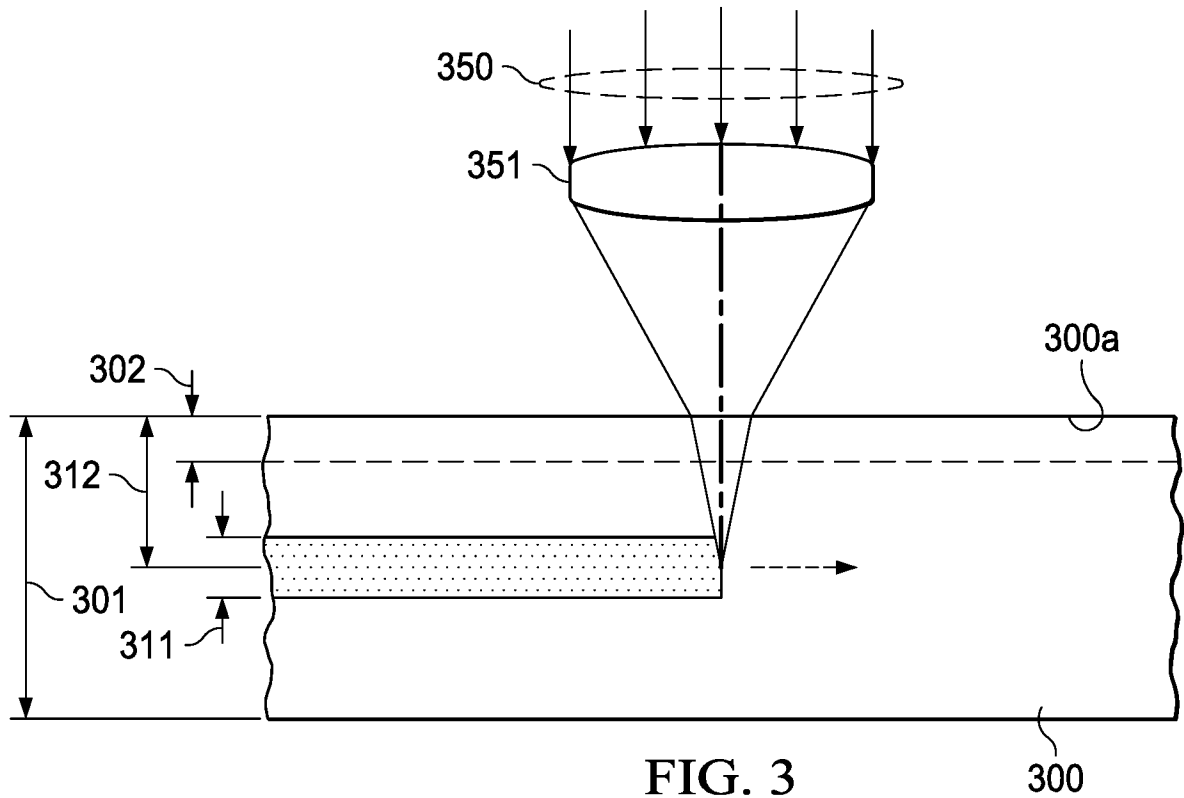


FIG. 2B

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INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 2017/029212

A. CLASSIFICATION OF SUBJECT MATTER		
<i>H01L 21/331 (2006.01)</i>		
According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED		
Minimum documentation searched (classification system followed by classification symbols)		
H01L 21/00, 21/02, 21/04, 21/18, 21/26, 21/268, 21/301, 21/33, 21/324, 21/331, H01L 27/00, 27/108		
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched		
Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6333532 B1 (INTERNATIONAL BUSINESS MACHINES CORPORATION) 25.12.2001, col.2, lines 45-55, col.3, lines 13-15, 55-57, fig.2b	10
Y		1-2, 8
A		3-7, 9, 11-13
Y	US 2004/0053452 A1 (SANYO ELECTRIC CO., LTD.) 18.03.2004, [0017], [0078], fig.14	1-2, 8
A	WO 2015/017097 A1 (APPLIED MATERIALS, INC) 05.02.2015	1-13
A	US 2011/0256736 A1 (SUNG-IL CHO et al.) 20.10.2011	1-13
☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.		
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Date of the actual completion of the international search		Date of mailing of the international search report
08 August 2017 (08.08.2017)		24 August 2017 (24.08.2017)
Name and mailing address of the ISA/RU: Federal Institute of Industrial Property, Berezhkovskaya nab., 30-1, Moscow, G-59, GSP-3, Russia, 125993 Facsimile No: (8-495) 531-63-18, (8-499) 243-33-37		Authorized officer M. Adireeva Telephone No. (499) 240-25-91