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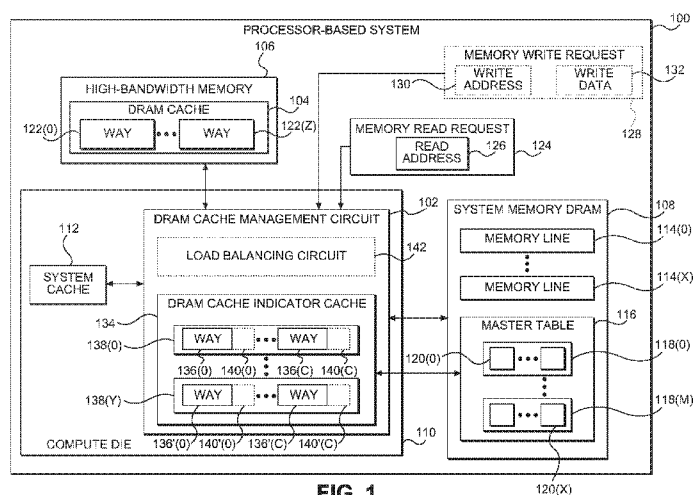
(54) Title: PROVIDING SCALABLE DYNAMIC RANDOM ACCESS MEMORY (DRAM) CACHE MANAGEMENT USING
DRAM CACHE INDICATOR CACHES

FIG. 1

(57) **Abstract:** Providing scalable dynamic random access memory (DRAM) cache management using DRAM cache indicator caches is provided. In one aspect, a DRAM cache management circuit is provided to manage access to a DRAM cache in high-bandwidth memory. The DRAM cache management circuit comprises a DRAM cache indicator cache, which stores master table entries that are read from a master table in a system memory DRAM and that contain DRAM cache indicators. The DRAM cache indicators enable the DRAM cache management circuit to determine whether a memory line in the system memory DRAM is cached in the DRAM cache of high-bandwidth memory, and, if so, in which way of the DRAM cache the memory line is stored. Based on the DRAM cache indicator cache, the DRAM cache management circuit may determine whether to employ the DRAM cache and/or the system memory DRAM to perform a memory access operation in an optimal manner.



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**PROVIDING SCALABLE DYNAMIC RANDOM ACCESS MEMORY (DRAM)
CACHE MANAGEMENT USING DRAM CACHE INDICATOR CACHES**

PRIORITY CLAIM

[0001] The present application claims priority to U.S. Provisional Patent Application Serial No. 62/298,088 filed on February 22, 2016 and entitled “PROVIDING SCALABLE DYNAMIC RANDOM ACCESS MEMORY (DRAM) CACHE MANAGEMENT USING DRAM CACHE INDICATOR CACHES,” the contents of which is incorporated herein by reference in its entirety.

[0002] The present application claims priority to U.S. Patent Application Serial No. 15/228,320 filed on August 4, 2016 and entitled “PROVIDING SCALABLE DYNAMIC RANDOM ACCESS MEMORY (DRAM) CACHE MANAGEMENT USING DRAM CACHE INDICATOR CACHES,” the contents of which is incorporated herein by reference in its entirety.

BACKGROUND

I. Field of the Disclosure

[0003] The technology of the disclosure relates generally to dynamic random access memory (DRAM) management, and, in particular, to management of DRAM caches.

II. Background

[0004] The advent of die-stacked integrated circuits (ICs) composed of multiple stacked dies that are vertically interconnected has enabled the development of die-stacked dynamic random access memory (DRAM). Die-stacked DRAMs may be used to implement what is referred to herein as “high-bandwidth memory.” High-bandwidth memory provides greater bandwidth than conventional system memory DRAM, while providing similar access latency. In some implementations, high-bandwidth memory may also be “near” memory, or memory that is physically located closer to a memory interface than other system memory DRAM. High-bandwidth memory may be used to implement a DRAM cache to store frequently accessed data that was previously read from a system memory DRAM and evicted from a higher level cache, such as a Level 3 (L3) cache as a non-limiting example. Providing a DRAM cache in high-bandwidth memory may reduce memory contention on the system memory DRAM, and thus, in effect, increase overall memory bandwidth.

[0005] However, management of a DRAM cache in a high-bandwidth memory can pose challenges. The DRAM cache may be orders of magnitude smaller in size than system memory DRAM. Thus, because the DRAM cache can only store a subset of the data in the system memory DRAM, efficient use of the DRAM cache depends on intelligent selection of memory addresses to be stored. Accordingly, a DRAM cache management mechanism should be capable of determining which memory addresses should be selectively installed in the DRAM cache, and should be further capable of determining when the memory addresses should be installed in and/or evicted from the DRAM cache. It may also be desirable for a DRAM cache management mechanism to minimize impact on access latency for the DRAM cache, and to be scalable with respect to the DRAM cache size and/or the system memory DRAM size.

[0006] Some approaches to DRAM cache management utilize a cache for storing tags corresponding to cached memory addresses, similar to how conventional caches may be managed. Under one such approach, all of the tags associated with a DRAM cache are stored in static random access memory (SRAM) on a compute die separate from the high-bandwidth memory. However, this approach may not be sufficiently scalable to the DRAM cache size, as larger DRAM cache sizes may require larger area for tags that are not desired and/or are too large to store in SRAM. Another approach involves locating the tags within the DRAM cache itself, instead of within the SRAM on the compute die, and using a hit/miss predictor to determine whether a given memory address is stored within the DRAM cache. While this latter approach minimizes the usage of SRAM in the compute die, any incorrect predictions will result in data being read from the system memory DRAM. For example, if the hit/miss predictor incorrectly predicts that the memory address is located in the DRAM cache, a latency penalty is incurred from an unnecessary read to the DRAM cache before reading the memory address from the system memory DRAM. Conversely, if the hit/miss predictor incorrectly predicts that the memory address is not located in the DRAM cache, an opportunity to avoid an unnecessary read to the system memory DRAM may be wasted. Unnecessary additional reads incur additional access latency, which may negate any performance improvements resulting from using the DRAM cache.

[0007] Thus, it is desirable to provide scalable DRAM cache management to improve memory bandwidth while minimizing SRAM consumption and latency penalties.

SUMMARY OF THE DISCLOSURE

[0008] Aspects disclosed in the detailed description include providing scalable dynamic random access memory (DRAM) cache management using DRAM cache indicator caches. In some aspects, a DRAM cache management circuit is provided to manage access to a DRAM cache in a high-bandwidth memory. The DRAM cache management circuit comprises a DRAM cache indicator cache that is used to cache master table entries that contain DRAM cache indicators, and that are read from a master table in a system memory DRAM. The DRAM cache indicators enable the DRAM cache management circuit to determine whether a memory line in the system memory DRAM is cached in the DRAM cache (i.e., implemented using the high-bandwidth memory), and, if so, in which way of the DRAM cache the memory line is stored. Based on the DRAM cache indicator cache, the DRAM cache management circuit can determine whether a memory operation may be performed using the DRAM cache and/or using the system memory DRAM. Some aspects of the DRAM cache management circuit may further provide a load balancing circuit. In circumstances in which data may be read from either the DRAM cache or the system memory DRAM, the DRAM cache management circuit may use the load balancing circuit to select an appropriate source from which to read data.

[0009] Further aspects of the DRAM cache management circuit may be configured to operate in a write-through mode or a write-back mode. In the latter aspect, the DRAM cache indicator cache may provide a dirty bit for each memory line stored therein. In some aspects, the DRAM cache and/or the DRAM cache indicator cache may be replenished based on a probabilistic determination by the DRAM cache management circuit. For example, the DRAM cache management circuit may be configured to replenish the DRAM cache and/or the DRAM cache indicator cache at random intervals such that only a percentage of randomly selected data is written to the DRAM cache and/or the DRAM cache indicator cache.

[0010] In another aspect, a DRAM cache management circuit is provided. The DRAM cache management circuit is communicatively coupled to a DRAM cache that is part of a high-bandwidth memory, and is further communicatively coupled to a system memory DRAM. The DRAM cache management circuit comprises a DRAM cache indicator cache that is configured to cache a plurality of DRAM cache indicators read from a master table in the system memory DRAM. The plurality of DRAM cache indicators indicate whether a corresponding memory line of the system memory DRAM

is cached in the DRAM cache. The DRAM cache management circuit is configured to receive a memory read request comprising a read address. The DRAM cache management circuit is further configured to determine whether the read address is found in the DRAM cache indicator cache. The DRAM cache management circuit is also configured to, responsive to determining that the read address is not found in the DRAM cache indicator cache, read data at the read address in the system memory DRAM. The DRAM cache management circuit is additionally configured to, responsive to determining that the read address is found in the DRAM cache indicator cache, determine, based on the DRAM cache indicator cache, whether the read address is found in the DRAM cache. The DRAM cache management circuit is further configured to, responsive to determining that the read address is not found in the DRAM cache, read data at the read address in the system memory DRAM. The DRAM cache management circuit is also configured to, responsive to determining that the read address is found in the DRAM cache, read data for the read address from the DRAM cache.

[0011] In another aspect, a method for providing scalable DRAM cache management is provided. The method comprises receiving, by a DRAM cache management circuit, a memory read request comprising a read address. The method further comprises determining whether the read address is found in a DRAM cache indicator cache of the DRAM cache management circuit. The method also comprises, responsive to determining that the read address is not found in the DRAM cache indicator cache, reading data at the read address in a system memory DRAM. The method additionally comprises, responsive to determining that the read address is found in the DRAM cache indicator cache, determining, based on the DRAM cache indicator cache, whether the read address is found in a DRAM cache that is part of a high-bandwidth memory. The method also comprises, responsive to determining that the read address is not found in the DRAM cache, reading data at the read address in the system memory DRAM. The method additionally comprises, responsive to determining that the read address is found in the DRAM cache, reading data for the read address from the DRAM cache.

[0012] In another aspect, a DRAM cache management circuit is provided. The DRAM cache management circuit comprises a means for receiving a memory read request comprising a read address. The DRAM cache management circuit further comprises a means for determining whether the read address is found in a DRAM cache

indicator cache of the DRAM cache management circuit. The DRAM cache management circuit also comprises a means for reading data at the read address in a system memory DRAM, responsive to determining that the read address is not found in the DRAM cache indicator cache. The DRAM cache management circuit additionally comprises a means for determining, based on the DRAM cache indicator cache, whether the read address is found in a DRAM cache that is part of a high-bandwidth memory, responsive to determining that the read address is found in the DRAM cache indicator cache. The DRAM cache management circuit further comprises a means for reading data at the read address in the system memory DRAM, responsive to determining that the read address is not found in the DRAM cache. The DRAM cache management circuit also comprises a means for reading data for the read address from the DRAM cache, responsive to determining that the read address is found in the DRAM cache.

[0013] In another aspect, a non-transitory computer-readable medium is provided, having stored thereon computer-executable instructions. When executed by a processor, the computer-executable instructions cause the processor to receive a memory read request comprising a read address. The computer-executable instructions further cause the processor to determine whether the read address is found in a DRAM cache indicator cache of a DRAM cache management circuit. The computer-executable instructions also cause the processor to, responsive to determining that the read address is not found in the DRAM cache indicator cache, read data at the read address in a system memory DRAM. The computer-executable instructions additionally cause the processor to, responsive to determining that the read address is found in the DRAM cache indicator cache, determine, based on the DRAM cache indicator cache, whether the read address is found in a DRAM cache that is part of a high-bandwidth memory. The computer-executable instructions further cause the processor to, responsive to determining that the read address is not found in the DRAM cache, read data at the read address in the system memory DRAM. The computer-executable instructions also cause the processor to, responsive to determining that the read address is found in the DRAM cache, read data for the read address from the DRAM cache.

BRIEF DESCRIPTION OF THE FIGURES

[0014] Figure 1 is a block diagram of a processor-based system including a high-bandwidth memory providing a dynamic random access memory (DRAM) cache, and

an exemplary DRAM cache management circuit for providing scalable DRAM cache management using a DRAM cache indicator cache;

[0015] Figures 2A-2B are block diagrams illustrating exemplary master table entries and DRAM cache indicator cache contents for two exemplary DRAM caches that may be managed by the DRAM cache management circuit of Figure 1;

[0016] Figure 3 is a flowchart illustrating exemplary operations of the DRAM cache management circuit of Figure 1 for performing a read operation using the DRAM cache indicator cache and the DRAM cache of Figure 1;

[0017] Figures 4A-4C are flowcharts illustrating exemplary operations of the DRAM cache management circuit of Figure 1 for performing a write operation resulting from an eviction of “clean” (i.e., unmodified) data from a Level 3 (L3) cache in a write-through mode or a write-back mode;

[0018] Figures 5A-5C are flowcharts illustrating exemplary operations of the DRAM cache management circuit of Figure 1 for performing a write operation resulting from an eviction of “dirty” (i.e., modified) data from an L3 cache in a write-through mode;

[0019] Figures 6A-6D are flowcharts illustrating exemplary operations of the DRAM cache management circuit of Figure 1 for performing a write operation resulting from an eviction of dirty data from an L3 cache in a write-back mode; and

[0020] Figure 7 is a block diagram of an exemplary processor-based system that can include the DRAM cache management circuit of Figure 1.

DETAILED DESCRIPTION

[0021] With reference now to the drawing figures, several exemplary aspects of the present disclosure are described. The word “exemplary” is used herein to mean “serving as an example, instance, or illustration.” Any aspect described herein as “exemplary” is not necessarily to be construed as preferred or advantageous over other aspects.

[0022] Aspects disclosed in the detailed description include providing scalable dynamic random access memory (DRAM) cache management using DRAM cache indicator caches. As described herein, a DRAM cache management scheme is “scalable” in the sense that the size of the resources utilized by the DRAM cache management scheme is relatively independent of the capacity of the DRAM cache being managed. Accordingly, in this regard, Figure 1 is a block diagram of an exemplary

processor-based system 100 that provides a DRAM cache management circuit 102 for managing a DRAM cache 104 that is part of a high-bandwidth memory 106. The processor-based system 100 includes a system memory DRAM 108, which, in some aspects, may comprise one or more dual in-line memory modules (DIMMs) (not shown). The processor-based system 100 further provides a compute die 110, on which a system cache 112 (such as a Level 3 (L3) cache, as a non-limiting example) is located. The processor-based system 100 may encompass any one of known digital logic elements, semiconductor circuits, processing cores, and/or memory structures, among other elements, or combinations thereof. Aspects described herein are not restricted to any particular arrangement of elements, and the disclosed techniques may be easily extended to various structures and layouts on semiconductor dies or packages. It is to be understood that some aspects of the processor-based system 100 may include elements in addition to those illustrated in Figure 1.

[0023] To improve memory bandwidth, the DRAM cache 104 within the high-bandwidth memory 106 of the processor-based system 100 may be used to cache memory addresses (not shown) and data (not shown) that were previously read from memory lines 114(0)-114(X) within the system memory DRAM 108, and/or evicted from the system cache 112. As non-limiting examples, some aspects may provide that data may be cached in the DRAM cache 104 only upon reading the data from the system memory DRAM 108, while in some aspects data may be cached in the DRAM cache 104 only when evicted from the system cache 112. According to some aspects, data may be cached in the DRAM cache 104 upon reading data from the system memory DRAM 108 for reads triggered by processor loads and dirty evictions from the system cache 112.

[0024] The DRAM cache 104 within the high-bandwidth memory 106 may be accessed independently of and in parallel with the system memory DRAM 108. As a result, memory bandwidth may be effectively increased by reading from both the DRAM cache 104 and the system memory DRAM 108 at the same time. In some aspects, the DRAM cache 104 may implement a random replacement policy to determine candidates for eviction within the DRAM cache 104.

[0025] A master table 116 stored in the system memory DRAM 108 is used to track which memory lines 114(0)-114(X) of the system memory DRAM 108 are stored in the DRAM cache 104. It is to be understood that, as used herein, a “memory line” of the system memory DRAM 108 refers to a portion of the system memory DRAM 108

having a length equal to a length of a cache line (not shown) of the system cache 112. The master table 116 contains master table entries 118(0)-118(M) for storing DRAM cache indicators 120(0)-120(X) for each of the memory lines 114(0)-114(X) of the system memory DRAM 108. Some aspects may provide that the size of each of the master table entries 118(0)-118(M) corresponds to a memory access granularity of the underlying memory. As a non-limiting example, for a memory access granularity of 64 bytes, each of the master table entries 118(0)-118(M) likewise comprises 64 bytes. Thus, in aspects in which each of the DRAM cache indicators 120(0)-120(X) comprises four (4) bits, each of the 64-byte master table entries 118(0)-118(M) of the master table 116 can store DRAM cache indicators 120(0)-120(X) for 128 memory lines 114(0)-114(X) of the system memory DRAM 108.

[0026] In some aspects, each of the DRAM cache indicators 120(0)-120(X) in the master table 116 indicates not only whether a corresponding memory line 114(0)-114(X) of the system memory DRAM 108 is stored in the DRAM cache 104 of the high-bandwidth memory 106, but also in which way 122(0)-122(Z) of the DRAM cache 104 the corresponding memory line 114(0)-114(X) is stored. For example, in some aspects, each of the DRAM cache indicators 120(0)-120(X) comprises four (4) bits, and the DRAM cache 104 may provide 15 ways 122(0)-122(14) (i.e., 2^4-1). A DRAM cache indicator 120(0)-120(X) having a value of zero (0) indicates that the corresponding memory line 114(0)-114(X) of the system memory DRAM 108 is not stored in the DRAM cache 104. A DRAM cache indicator 120(0)-120(X) having a value N that is greater than zero (0) indicates that the corresponding memory line 114(0)-114(X) of the system memory DRAM 108 is stored in the DRAM cache 104 in way 122(N-1), where $0 \leq N-1 \leq Z$.

[0027] It is to be understood that, in some aspects, the master table entries 118(0)-118(M) of the master table 116 may provide DRAM cache indicators 120(0)-120(X) that are larger or smaller than four (4) bits according to the number of ways 122(0)-122(Z) provided by the DRAM cache 104. As a non-limiting example, for a number Q of bits in each DRAM cache indicator 120(0)-120(X), the DRAM cache 104 may provide a number of ways 122(0)-122(Z) where $Z=2^Q-1$. Thus, a DRAM cache indicator 120(0)-120(X) comprising two (2) bits corresponds to a DRAM cache 104 that is organized into three (3) ways 122(0)-122(2), while a DRAM cache indicator 120(0)-120(X) comprising three (3) bits corresponds to a DRAM cache 104 providing seven (7) ways 122(0)-122(6). Different configurations of the DRAM cache indicators

120(0)-120(X) and the DRAM cache 104 are discussed in greater detail below with respect to Figures 2A and 2B.

[0028] Because the master table entries 118(0)-118(M) of the master table 116 store DRAM cache indicators 120(0)-120(X) for every memory line 114(0)-114(X) in the system memory DRAM 108, the size of the master table 116 increases as the size of the system memory DRAM 108 increases. For example, in aspects in which the DRAM cache indicators 120(0)-120(X) within the master table 116 are four (4) bits each, the total size of the master table 116 is 0.4% of the size of the system memory DRAM 108. Consequently, accessing the master table 116 for each memory operation may incur latency penalties that could offset the performance benefits of using the DRAM cache 104. Thus, it is desirable to provide a scalable mechanism for managing access to the DRAM cache 104 to improve memory bandwidth while minimizing latency penalties.

[0029] In this regard, the DRAM cache management circuit 102 is provided to manage access to the DRAM cache 104. The DRAM cache management circuit 102 is located on the compute die 110, and is communicatively coupled to the high-bandwidth memory 106 and the system memory DRAM 108. The DRAM cache management circuit 102 may also be read from and written to by the system cache 112. As discussed in greater detail below, the DRAM cache management circuit 102 may perform a memory read operation in response to receiving a memory read request 124 comprising a read address 126 specifying a memory address from which to retrieve data. In some aspects, the DRAM cache management circuit 102 may further perform a memory write operation in response to receiving a memory write request 128 comprising a write address 130 to which write data 132 is to be written.

[0030] To reduce access latency that may result from accesses to the master table 116, the DRAM cache management circuit 102 provides a DRAM cache indicator cache 134. The DRAM cache indicator cache 134 is used by the DRAM cache management circuit 102 to cache frequently accessed master table entries 118(0)-118(M) (and the DRAM cache indicators 120(0)-120(X) stored therein) within ways 136(0)-136(C), 136'(0)-136'(C) of DRAM cache indicator cache lines 138(0)-138(Y). In some aspects, the size of each of the ways 136(0)-136(C), 136'(0)-136'(C) of the DRAM cache indicator cache 134 corresponds to the size of the master table entries 118(0)-118(M) in the master table 116. Some aspects may provide that the size of each of the ways 136(0)-136(C), 136'(0)-136'(C) of the DRAM cache indicator cache 134 may be larger than the size of the master table entries 118(0)-118(M) in the master table 116. As a

non-limiting example, the ways 136(0)-136(C), 136'(0)-136'(C) of the DRAM cache indicator cache 134 may include dirty indicators 140(0)-140(C), 140'(0)-140'(C), which add one (1) bit per way 136(0)-136(C), 136'(0)-136'(C). Thus, in aspects in which the ways 136(0)-136(C), 136'(0)-136'(C) are 64 bytes in size with four (4) bits per DRAM cache indicator 120(0)-120(X), a total of 128 extra bits may be required to provide the dirty indicators 140(0)-140(C), 140'(0)-140'(C).

[0031] Some aspects of the DRAM cache management circuit 102 may further provide a load balancing circuit 142 to improve memory bandwidth and reduce memory access contention. In circumstances in which a requested memory address can be read from either the system memory DRAM 108 or the DRAM cache 104, the load balancing circuit 142 identifies the most appropriate source from which to read the memory address. For example, in some aspects, the load balancing circuit 142 may monitor latencies of reads from the DRAM cache 104 and the system memory DRAM 108, and may select the source having a better average latency in the recent past. In this manner, the load balancing circuit 142 may distribute memory accesses between the system memory DRAM 108 and the DRAM cache 104 to optimize the use of system resources.

[0032] In some aspects, the DRAM cache management circuit 102 may be implemented as a “write-through” cache management system. In a write-through implementation, dirty (i.e., modified) data evicted from the system cache 112 is written by the DRAM cache management circuit 102 to both the DRAM cache 104 of the high-bandwidth memory 106 and the system memory DRAM 108. As a result, the data within the DRAM cache 104 and the data within the system memory DRAM 108 are always synchronized. Because both the DRAM cache 104 and the system memory DRAM 108 in a write-through implementation are guaranteed to contain correct data, the load balancing circuit 142 of the DRAM cache management circuit 102 may freely load-balance memory read operations between the DRAM cache 104 and the system memory DRAM 108. However, the write-through implementation of the DRAM cache management circuit 102 may not result in decreased write bandwidth to the system memory DRAM 108, because each write to the DRAM cache 104 will correspond to a write to the system memory DRAM 108.

[0033] Some aspects of the DRAM cache management circuit 102 may be implemented as a “write-back” cache management system, in which the DRAM cache indicator cache 134 of the DRAM cache management circuit 102 includes the dirty

indicators 140(0)-140(C), 140'(0)-140'(C) for each way 136(0)-136(C), 136'(0)-136'(C) therein. Each of the dirty indicators 140(0)-140(C), 140'(0)-140'(C) indicates whether data stored in the DRAM cache 104 corresponding to the way 136(0)-136(C), 136'(0)-136'(C) within the DRAM cache indicator cache 134 is dirty (i.e., whether the data was written to the DRAM cache 104 but not to the system memory DRAM 108). If the data is not dirty, the data may be read from either the DRAM cache 104 or the system memory DRAM 108, as determined by the load balancing circuit 142 of the DRAM cache management circuit 102. However, if the dirty indicator 140(0)-140(C), 140'(0)-140'(C) indicates that the data stored in the DRAM cache 104 is dirty, load balancing is not possible, as the DRAM cache 104 is the only source for the modified data. Accordingly, the DRAM cache management circuit 102 reads the dirty data from the DRAM cache 104.

[0034] The write-back implementation of the DRAM cache management circuit 102 may reduce memory write bandwidth consumption to the system memory DRAM 108, but the DRAM cache management circuit 102 eventually must write back dirty data evicted from the DRAM cache 104 to the system memory DRAM 108. In some aspects of the write-back implementation of the DRAM cache management circuit 102, when a DRAM cache indicator cache line 138(0)-138(Y) is evicted from the DRAM cache indicator cache 134, the DRAM cache management circuit 102 is configured to copy all dirty data in the DRAM cache 104 corresponding to the evicted DRAM cache indicator cache line 138(0)-138(Y) to the system memory DRAM 108.

[0035] Some aspects of the DRAM cache management circuit 102 may further improve memory bandwidth by performing some operations (e.g., operations involving memory accesses to the system memory DRAM 108 and/or the DRAM cache 104, as non-limiting examples) according to corresponding probabilistic determinations made by the DRAM cache management circuit 102. Each probabilistic determination may be used to tune the frequency of the corresponding operation, and may be stateless (i.e., not related to the outcome of previous probabilistic determinations). For example, according to some aspects of the DRAM cache management circuit 102, data evicted by the system cache 112 may be written to the DRAM cache 104 based on a probabilistic determination, such that only a percentage of randomly-selected data evicted by the system cache 112 is written to the DRAM cache 104. Similarly, some aspects of the DRAM cache management circuit 102 may be configured to replenish the DRAM cache indicator cache 134 (e.g., by copying a master table entry 118(0)-118(M) for the read

data from the master table 116 to the DRAM cache indicator cache 134) based on a probabilistic determination. Thus, it is to be understood that each operation described herein as occurring “probabilistically” may or may not be performed in a given instance, and further that the occurrence or lack thereof of a given probabilistic operation may further trigger additional operations by the DRAM cache management circuit 102.

[0036] To illustrate exemplary master table entries 118(0)-118(M) and DRAM cache indicator 120(0)-120(X) contents for some implementations of the DRAM cache 104 of Figure 1, Figures 2A-2B are provided. Figure 2A illustrates an implementation of the DRAM cache 104 comprising 15 ways, while Figure 2B illustrates an implementation of the DRAM cache 104 comprising three (3) ways. For the sake of clarity, elements of Figure 1 are referenced in describing Figures 2A and 2B.

[0037] In Figure 2A, an exemplary master table entry 200 (which may correspond to one of the master table entries 118(0)-118(M) of Figure 1) having a size of 64 bytes is illustrated. The master table entry 200 includes DRAM cache indicators 202(0)-202(127) (corresponding to the DRAM cache indicators 120(0)-120(X) of Figure 1), each of which is four (4) bits in size. Accordingly, the master table entry 200 stores the DRAM cache indicators 202(0)-202(127) for 128 memory lines 114(0)-114(X) of the system memory DRAM 108. To cache the DRAM cache indicators 202(0)-202(127), the DRAM cache indicator cache 134 provides DRAM cache indicator cache lines 204(0)-204(511) (corresponding to the DRAM cache indicator cache lines 138(0)-138(Y) of Figure 1). Each of the DRAM cache indicator cache lines 204(0)-204(511) is made up of eight (8) ways, such as ways 206(0)-206(7), 208(0)-208(7) of the DRAM cache indicator cache lines 204(0), 204(511), respectively. Each of the ways 206(0)-206(7), 208(0)-208(7) corresponds to the ways 136(0)-136(C), 136'(0)-136'(C) of Figure 1, and may store one (1) master table entry, such as the master table entry 200.

[0038] Referring now to Figure 2B, a master table entry 210 of 64 bytes is shown. In the example of Figure 2B, the master table entry 210 includes DRAM cache indicators 212(0)-212(255), each of which is two (2) bits in size. Accordingly, the master table entry 210 stores the DRAM cache indicators 212(0)-212(255) for 256 memory lines of the system memory DRAM 108. The DRAM cache indicator cache 134 in this example provides DRAM cache indicator cache lines 214(0)-214(511) to cache the DRAM cache indicators 212(0)-212(255). Each of the DRAM cache indicator cache lines 214(0)-214(511) is made up of eight (8) ways, such as ways 216(0)-216(7), 218(0)-218(7) of the DRAM cache indicator cache lines 214(0),

214(511), respectively. Each of the ways 216(0)-216(7), 218(0)-218(7) may store one (1) master table entry, such as the master table entry 210.

[0039] Figure 3 is a flowchart illustrating exemplary operations of the DRAM cache management circuit 102 of Figure 1 for performing a read operation using the DRAM cache indicator cache 134 and the DRAM cache 104 of Figure 1. Elements of Figure 1 are referenced in describing Figure 3 for the sake of clarity. In Figure 3, operations begin with the DRAM cache management circuit 102 receiving the memory read request 124 comprising the read address 126 (e.g., as a result of a miss on the system cache 112) (block 300). Accordingly, the DRAM cache management circuit 102 may be referred to herein as “a means for receiving a memory read request comprising a read address.” The DRAM cache management circuit 102 determines whether the read address 126 is found in the DRAM cache indicator cache 134 of the DRAM cache management circuit 102 (block 302). The DRAM cache management circuit 102 may thus be referred to herein as “a means for determining whether the read address is found in a DRAM cache indicator cache of the DRAM cache management circuit.”

[0040] If the read address 126 of the memory read request 124 is not found in the DRAM cache indicator cache 134, the DRAM cache management circuit 102 reads data at the read address 126 in the system memory DRAM 108 (block 304). In this regard, the DRAM cache management circuit 102 may be referred to herein as “a means for reading data at the read address in a system memory DRAM, responsive to determining that the read address is not found in the DRAM cache indicator cache.” In parallel with reading the data at the read address 126, some aspects of the DRAM cache management circuit 102 may probabilistically replenish the DRAM cache indicator cache 134 (block 306). By replenishing the DRAM cache indicator cache 134, the likelihood that subsequent reads (which may be spatially adjacent to the read data) will result in a DRAM cache indicator cache 134 hit may be increased.

[0041] Probabilistically replenishing the DRAM cache indicator cache 134 in some aspects may include copying a master table entry 118(0)-118(M) for the read data from the master table 116 to the DRAM cache indicator cache 134, as a non-limiting example. Some aspects may provide that operations of block 306 for replenishing the DRAM cache indicator cache 134 may include reading a master table entry 118(0)-118(M) spanning the read address 126 from the master table 116 in the system memory DRAM 108. The master table entry 118(0)-118(M) is then installed in the DRAM cache indicator cache 134. If the installation of the master table entry 118(0)-118(M)

causes an eviction of one of the ways 136(0)-136(C), 136'(0)-136'(C) from the DRAM cache indicator cache 134, the contents of the evicted way 136(0)-136(C), 136'(0)-136'(C) (without any dirty indicators 140(0)-140(C), 140'(0)-140'(C) that may be present) are written to the master table 116 in the system memory DRAM 108. In aspects in which the DRAM cache management circuit 102 is configured to operate in a write-back mode, any dirty DRAM cache lines indicated by the evicted way 136(0)-136(C), 136'(0)-136'(C) are also copied from the DRAM cache 104 to the system memory DRAM 108.

[0042] If the DRAM cache management circuit 102 determines at decision block 302 that the read address 126 is found in the DRAM cache indicator cache 134, the DRAM cache management circuit 102 next determines whether the read address 126 is found in the DRAM cache 104 that is part of the high-bandwidth memory 106, based on the DRAM cache indicator cache 134 (block 308). Accordingly, the DRAM cache management circuit 102 may be referred to herein as “a means for determining, based on the DRAM cache indicator cache, whether the read address is found in a DRAM cache that is part of a high-bandwidth memory, responsive to determining that the read address is found in the DRAM cache indicator cache.” In some aspects, determining whether the read address 126 is found in the DRAM cache 104 may include determining if the way number for the read address 126 in the DRAM cache indicator cache 134 is non-zero. If so, the read address 126 is in the DRAM cache 104. Otherwise, if the way number for the read address 126 in the DRAM cache indicator cache 134 is zero (0), the read address 126 is not in the DRAM cache 104.

[0043] If the read address 126 is not found in the DRAM cache 104, the DRAM cache management circuit 102 reads data at the read address 126 in the system memory DRAM 108 (block 310). The DRAM cache management circuit 102 thus may be referred to herein as “a means for reading data at the read address in the system memory DRAM, responsive to determining that the read address is not found in the DRAM cache.” However, if the DRAM cache management circuit 102 determines at decision block 308 that the read address 126 is found in the DRAM cache 104, the DRAM cache management circuit 102 in some aspects determines whether the data for the read address 126 in the DRAM cache 104 is clean (or, alternatively, whether the DRAM cache management circuit 102 is configured to operate in a write-through mode) (block 312). If the data in the DRAM cache 104 is not clean and/or the DRAM cache management circuit 102 is not operating in a write-through mode, the requested data can

only be read safely from the DRAM cache 104. Accordingly, the DRAM cache management circuit 102 reads the data for the read address 126 from the DRAM cache 104 (block 314). In this regard, the DRAM cache management circuit 102 may be referred to herein as “a means for reading data for the read address from the DRAM cache, responsive to determining that the read address is found in the DRAM cache.”

[0044] If the DRAM cache management circuit 102 determines at decision block 312 that the data in the DRAM cache 104 is clean and/or the DRAM cache management circuit 102 is operating in a write-through mode, the requested data can be read safely from either the system memory DRAM 108 or the DRAM cache 104. Accordingly, the load balancing circuit 142 of the DRAM cache management circuit 102 identifies a preferred data source from among the DRAM cache 104 and the system memory DRAM 108 based on load balancing criteria such as bandwidth and latency, as non-limiting examples (block 316). If the load balancing circuit 142 determines that the system memory DRAM 108 is the preferred data source, the data at the read address 126 may be read from the system memory DRAM 108 (block 318). Similarly, if the load balancing circuit 142 determines that the DRAM cache 104 is the preferred data source, the data for the read address 126 may be read from the DRAM cache 104 (block 320).

[0045] To illustrate exemplary operations of the DRAM cache management circuit 102 of Figure 1 for performing a write operation resulting from an eviction of clean (i.e., unmodified) data from the system cache 112 in a write-through mode or a write-back mode, Figures 4A-4C are provided. For the sake of clarity, elements of Figure 1 are referenced in describing Figures 4A-4C. Operations in Figure 4A begin with the DRAM cache management circuit 102 receiving the memory write request 128 comprising the write address 130 and the write data 132 (block 400). In this example, the write data 132 represents clean (i.e., unmodified) data evicted from the system cache 112, and thus is referred to herein as “clean evicted data 132.”

[0046] The DRAM cache management circuit 102 determines whether the write address 130 of the clean evicted data 132 is found in the DRAM cache indicator cache 134 (block 402). If the write address 130 is not present in the DRAM cache indicator cache 134, the DRAM cache management circuit 102 probabilistically replenishes the DRAM cache indicator cache 134 (e.g., by copying a master table entry 118(0)-118(M) from the master table 116 to the DRAM cache indicator cache 134) (block 404). If the DRAM cache indicator cache 134 is not replenished at block 404 (i.e., replenishment

was probabilistically determined not to occur), processing is complete (block 406). Otherwise, the DRAM cache management circuit 102 resumes processing at block 408.

[0047] If the DRAM cache management circuit 102 determines at decision block 402 that the write address 130 of the clean evicted data 132 is present in the DRAM cache indicator cache 134 (or if the DRAM cache indicator cache 134 is replenished at block 404), the DRAM cache management circuit 102 next determines whether the write address 130 of the clean evicted data 132 is present in the DRAM cache 104 (block 408). If the write address 130 is present in the DRAM cache 104, processing is complete (block 406). However, if the write address 130 of the clean evicted data 132 is not present in the DRAM cache 104, processing resumes at block 410 of Figure 4B.

[0048] Referring now to Figure 4B, the DRAM cache management circuit 102 next probabilistically writes the write address 130 and the clean evicted data 132 to the DRAM cache 104 (block 410). In some aspects, operations of block 410 for writing the write address 130 and the clean evicted data 132 to the DRAM cache 104 may include first randomly selecting a way 122(0)-122(Z) to be evicted from the DRAM cache 104 (block 412). The DRAM cache management circuit 102 reads a memory address of the selected way 122(0)-122(Z) from the DRAM cache 104 (block 414). The DRAM cache management circuit 102 then writes the write address 130 and the clean evicted data 132 to the selected way 122(0)-122(Z) in the DRAM cache 104 (block 416). The DRAM cache management circuit 102 updates the way number for the write address 130 in the DRAM cache indicator cache 134 to a way number of the selected way 122(0)-122(Z) (block 418). Processing then continues at block 420 of Figure 4C.

[0049] Turning to Figure 4C, further operations of block 410 for probabilistically writing the write address 130 and the clean evicted data 132 to the DRAM cache 104 include the DRAM cache management circuit 102 determining whether the memory address of the selected way 122(0)-122(Z) is present in the DRAM cache indicator cache 134 (block 420). If not, processing resumes at block 424 of Figure 4C. If the DRAM cache management circuit 102 determines at decision block 420 that the memory address of the selected way 122(0)-122(Z) is present in the DRAM cache indicator cache 134, the DRAM cache management circuit 102 resets the way number of the selected way 122(0)-122(Z) for the memory address in the DRAM cache indicator cache 134 (block 422).

[0050] If the DRAM cache management circuit 102 determines at decision block 420 that the memory address of the selected way 122(0)-122(Z) is not present in the

DRAM cache indicator cache 134, the DRAM cache management circuit 102 replenishes the DRAM cache indicator cache 134 (block 424). In some aspects, operations of block 424 for replenishing the DRAM cache indicator cache 134 include reading the master table entry 118(0)-118(M) of the selected way 122(0)-122(Z) corresponding to the memory address from the master table 116 in the system memory DRAM 108 (block 426). The DRAM cache management circuit 102 in some aspects may next write the way number of the selected way 122(0)-122(Z) for the memory address to the DRAM cache indicator cache 134 based on the master table entry 118(0)-118(M) (block 428). In some aspects, the DRAM cache management circuit 102 resets the way number of the selected way 122(0)-122(Z) corresponding to the memory address (block 430). The DRAM cache management circuit 102 then writes the way number to the master table 116 in the system memory DRAM 108 (without installing the master table entry 118(0)-118(M) in the DRAM cache indicator cache 134) (block 432).

[0051] Figures 5A-5C are provided to illustrate exemplary operations of the DRAM cache management circuit 102 of Figure 1 for performing a write operation resulting from an eviction of dirty data from the system cache 112 in a write-through mode. Elements of Figure 1 are referenced in describing Figures 5A-5C for the sake of clarity. In Figure 5A, operations begin with the DRAM cache management circuit 102 receiving the memory write request 128 comprising the write address 130 and the write data 132 (block 500). The write data 132 in the example of Figure 5A represents dirty (i.e., modified) data evicted from the system cache 112, and as a result is referred to herein as “dirty evicted data 132.”

[0052] The DRAM cache management circuit 102 determines whether the write address 130 of the dirty evicted data 132 is found in the DRAM cache indicator cache 134 (block 502). If the write address 130 is not present in the DRAM cache indicator cache 134, the DRAM cache management circuit 102 probabilistically replenishes the DRAM cache indicator cache 134 (by copying a master table entry 118(0)-118(M) from the master table 116 to the DRAM cache indicator cache 134, as a non-limiting example) (block 504). If the DRAM cache indicator cache 134 is replenished at block 504 (i.e., replenishment was probabilistically determined to occur), processing resumes at block 506. Otherwise, the DRAM cache management circuit 102 updates the DRAM cache indicator 120(0)-120(X) corresponding to the write address 130 in the master table 116 in the system memory DRAM 108 (e.g., by performing a read-modify-write

(RMW) operation on the master table entry 118(0)-118(M) for the DRAM cache indicator 120(0)-120(X)) (block 508). The DRAM cache management circuit 102 then writes the dirty evicted data 132 to the DRAM cache 104 (block 510). It is to be understood that, in some aspects, operations of block 508 for updating the DRAM cache indicator 120(0)-120(X) and operations of block 510 for writing the dirty evicted data 132 to the DRAM cache 104 may be carried out in parallel.

[0053] If the DRAM cache management circuit 102 determines at decision block 502 that the write address 130 of the dirty evicted data 132 is found in the DRAM cache indicator cache 134 (or if the DRAM cache indicator cache 134 is replenished at block 504), the DRAM cache management circuit 102 next determines whether the write address 130 of the dirty evicted data 132 is found in the DRAM cache 104 (block 506). If the write address 130 is not found in the DRAM cache 104, processing resumes at block 512 of Figure 5B. However, if the DRAM cache management circuit 102 determines at decision block 506 that the write address 130 is found in the DRAM cache 104, the DRAM cache management circuit 102 writes the dirty evicted data 132 to the DRAM cache 104 (e.g., by performing a no-evict-write to the DRAM cache 104) (block 514). The DRAM cache management circuit 102 then writes the dirty evicted data 132 to the system memory DRAM 108 (block 516).

[0054] Turning to Figure 5B, the DRAM cache management circuit 102 next probabilistically writes the write address 130 and the dirty evicted data 132 to the DRAM cache 104 (block 512). Some aspects may provide that operations of block 512 for writing the write address 130 and the dirty evicted data 132 to the DRAM cache 104 may include first randomly selecting a way 122(0)-122(Z) to be evicted from the DRAM cache 104 (block 518). A memory address of the selected way 122(0)-122(Z) is read from the DRAM cache 104 by the DRAM cache management circuit 102 (block 520). The DRAM cache management circuit 102 then writes the write address 130 and the dirty evicted data 132 to the selected way 122(0)-122(Z) in the DRAM cache 104 (block 522). The DRAM cache management circuit 102 updates the way number for the write address 130 in the DRAM cache indicator cache 134 to a way number of the selected way 122(0)-122(Z) (block 524). Processing then continues at block 526 of Figure 5C.

[0055] Referring now to Figure 5C, further operations of block 512 for probabilistically writing the write address 130 and the dirty evicted data 132 to the DRAM cache 104 include the DRAM cache management circuit 102 determining

whether a memory address of the selected way 122(0)-122(Z) is present in the DRAM cache indicator cache 134 (block 526). If not, processing resumes at block 528 of Figure 5C. If the DRAM cache management circuit 102 determines at decision block 526 that the memory address of the selected way 122(0)-122(Z) is present in the DRAM cache indicator cache 134, the DRAM cache management circuit 102 resets the way number of the selected way 122(0)-122(Z) for the memory address in the DRAM cache indicator cache 134 (block 530).

[0056] If the DRAM cache management circuit 102 determines at decision block 526 that the memory address of the selected way 122(0)-122(Z) is not present in the DRAM cache indicator cache 134, the DRAM cache management circuit 102 replenishes the DRAM cache indicator cache 134 (block 528). In some aspects, operations of block 528 for replenishing the DRAM cache indicator cache 134 include reading the master table entry 118(0)-118(M) of the selected way 122(0)-122(Z) corresponding to the memory address from the master table 116 in the system memory DRAM 108 (block 532). The DRAM cache management circuit 102 in some aspects may next write the way number of the selected way 122(0)-122(Z) for the memory address to the DRAM cache indicator cache 134 based on the master table entry 118(0)-118(M) (block 534). In some aspects, the DRAM cache management circuit 102 resets the way number of the selected way 122(0)-122(Z) corresponding to the memory address (block 536). The DRAM cache management circuit 102 then writes the way number to the master table 116 in the system memory DRAM 108 (without installing the master table entry 118(0)-118(M) in the DRAM cache indicator cache 134) (block 538).

[0057] To illustrate exemplary operations of the DRAM cache management circuit 102 of Figure 1 for performing a write operation resulting from an eviction of dirty data from the system cache 112 in a write-back mode, Figures 6A-6D are provided. For the sake of clarity, elements of Figure 1 are referenced in describing Figures 6A-6D. Operations in Figure 6A begin with the DRAM cache management circuit 102 receiving the memory write request 128 comprising the write address 130 and the write data 132 (block 600). As with Figure 5A, the write data 132 in the example of Figure 6A represents dirty (i.e., modified) data evicted from the system cache 112, and as a result is referred to herein as “dirty evicted data 132.”

[0058] The DRAM cache management circuit 102 determines whether the write address 130 of the dirty evicted data 132 is found in the DRAM cache indicator cache

134 (block 602). If the write address 130 is not present in the DRAM cache indicator cache 134, the DRAM cache management circuit 102 probabilistically replenishes the DRAM cache indicator cache 134 (e.g., by copying a master table entry 118(0)-118(M) from the master table 116 to the DRAM cache indicator cache 134) (block 604). If the DRAM cache indicator cache 134 is replenished at block 604 (i.e., replenishment was probabilistically determined to occur), processing resumes at block 606. Otherwise, the DRAM cache management circuit 102 updates the DRAM cache indicator 120(0)-120(X) corresponding to the write address 130 in the master table 116 in the system memory DRAM 108 (e.g., by performing a read-modify-write (RMW) operation on the master table entry 118(0)-118(M) for the DRAM cache indicator 120(0)-120(X)) (block 608). The DRAM cache management circuit 102 then writes the dirty evicted data 132 to the DRAM cache 104 (block 610). It is to be understood that, in some aspects, operations of block 608 for updating the DRAM cache indicator 120(0)-120(X) and operations of block 610 for writing the dirty evicted data 132 to the DRAM cache 104 may be carried out in parallel.

[0059] Some aspects of the DRAM cache management circuit 102 may next determine whether the DRAM cache indicator 120(0)-120(X) for the write address 130 from the master table 116 indicates that the write address 130 is in the DRAM cache 104 (block 612). If not, processing is complete (block 614). However, if the DRAM cache management circuit 102 determines at decision block 612 that the DRAM cache indicator 120(0)-120(X) for the write address 130 from the master table 116 indicates that the write address 130 is in the DRAM cache 104, the DRAM cache management circuit 102 writes the dirty evicted data 132 to the DRAM cache 104 (block 616).

[0060] Referring back to decision block 602, if the DRAM cache management circuit 102 determines that the write address 130 of the dirty evicted data 132 is found in the DRAM cache indicator cache 134 (or if the DRAM cache indicator cache 134 is replenished at block 604), the DRAM cache management circuit 102 next determines whether the write address 130 of the dirty evicted data 132 is found in the DRAM cache 104 (block 606). If the write address 130 is not found in the DRAM cache 104, processing resumes at block 618 of Figure 6B. However, if the DRAM cache management circuit 102 determines at decision block 606 that the write address 130 is found in the DRAM cache 104, the DRAM cache management circuit 102 writes the dirty evicted data 132 to the DRAM cache 104 (e.g., by performing a no-evict-write operation to the DRAM cache 104) (block 616).

[0061] Turning now to Figure 6B, the DRAM cache management circuit 102 next probabilistically writes the write address 130 and the dirty evicted data 132 to the DRAM cache 104 (block 618). According to some aspects, operations of block 618 for writing the write address 130 and the dirty evicted data 132 to the DRAM cache 104 may include first randomly selecting a way 122(0)-122(Z) to be evicted from the DRAM cache 104 (block 620). A memory address of the selected way 122(0)-122(Z) is read from the DRAM cache 104 by the DRAM cache management circuit 102 (block 622). The DRAM cache management circuit 102 then writes the write address 130 and the dirty evicted data 132 to the selected way 122(0)-122(Z) in the DRAM cache 104 (block 624). The DRAM cache management circuit 102 updates the way number for the write address 130 in the DRAM cache indicator cache 134 to a way number of the selected way 122(0)-122(Z) (block 626). The DRAM cache management circuit 102 also sets a dirty indicator 140(0)-140(C), 140'(0)-140'(C) for the write address 130 in the DRAM cache indicator cache 134 (block 628). Processing then continues at block 630 of Figure 6C.

[0062] In Figure 6C, further operations of block 618 for probabilistically writing the write address 130 and the dirty evicted data 132 to the DRAM cache 104 include the DRAM cache management circuit 102 determining whether a memory address of the selected way 122(0)-122(Z) is present in the DRAM cache indicator cache 134 (block 630). If not, processing resumes at block 632 in Figure 6D. If the DRAM cache management circuit 102 determines at decision block 630 that the memory address of the selected way 122(0)-122(Z) is present in the DRAM cache indicator cache 134, the DRAM cache management circuit 102 resets the way number and a dirty indicator 140(0)-140(C), 140'(0)-140'(C) of the selected way 122(0)-122(Z) for the memory address in the DRAM cache indicator cache 134 (block 634).

[0063] Referring now to Figure 6D, if the DRAM cache management circuit 102 determines at decision block 630 of Figure 6C that the memory address of the selected way 122(0)-122(Z) is not present in the DRAM cache indicator cache 134, the DRAM cache management circuit 102 replenishes the DRAM cache indicator cache 134 (block 632). In some aspects, operations of block 632 for replenishing the DRAM cache indicator cache 134 include reading the master table entry 118(0)-118(M) of the selected way 122(0)-122(Z) corresponding to the memory address from the master table 116 in the system memory DRAM 108 (block 634). The DRAM cache management circuit 102 in some aspects may next write the way number of the selected way 122(0)-

122(Z) for the memory address to the DRAM cache indicator cache 134 based on the master table entry 118(0)-118(M) (block 636). In some aspects, the DRAM cache management circuit 102 resets the way number of the selected way 122(0)-122(Z) corresponding to the memory address (block 638). The DRAM cache management circuit 102 then writes the way number to the master table 116 in the system memory DRAM 108 (without installing the master table entry 118(0)-118(M) in the DRAM cache indicator cache 134) (block 640). If the write address 130 and the dirty evicted data 132 were not probabilistically written to the DRAM cache 104 in block 618, the DRAM cache management circuit 102 writes the dirty evicted data 132 to the system memory DRAM 108 (block 642).

[0064] Providing scalable DRAM cache management using DRAM cache indicator caches according to aspects disclosed herein may be provided in or integrated into any processor-based device. Examples, without limitation, include a set top box, an entertainment unit, a navigation device, a communications device, a fixed location data unit, a mobile location data unit, a mobile phone, a cellular phone, a smart phone, a tablet, a phablet, a computer, a portable computer, a desktop computer, a personal digital assistant (PDA), a monitor, a computer monitor, a television, a tuner, a radio, a satellite radio, a music player, a digital music player, a portable music player, a digital video player, a video player, a digital video disc (DVD) player, a portable digital video player, and an automobile.

[0065] In this regard, Figure 7 illustrates an example of a processor-based system 700 that can employ the DRAM cache management circuit (DCMC) 102 illustrated in Figure 1. The processor-based system 700 includes one or more central processing units (CPUs) 702, each including one or more processors 704. The CPU(s) 702 may have cache memory 706 coupled to the processor(s) 704 for rapid access to temporarily stored data. The CPU(s) 702 is coupled to a system bus 708 and can intercouple master and slave devices included in the processor-based system 700. As is well known, the CPU(s) 702 communicates with these other devices by exchanging address, control, and data information over the system bus 708. For example, the CPU(s) 702 can communicate bus transaction requests to a memory controller 710 as an example of a slave device.

[0066] Other master and slave devices can be connected to the system bus 708. As illustrated in Figure 7, these devices can include a memory system 712, one or more input devices 714, one or more output devices 716, one or more network interface

devices 718, and one or more display controllers 720, as examples. The input device(s) 714 can include any type of input device, including but not limited to input keys, switches, voice processors, etc. The output device(s) 716 can include any type of output device, including, but not limited to, audio, video, other visual indicators, etc. The network interface device(s) 718 can be any devices configured to allow exchange of data to and from a network 722. The network 722 can be any type of network, including, but not limited to, a wired or wireless network, a private or public network, a local area network (LAN), a wireless local area network (WLAN), a wide area network (WAN), a BLUETOOTH™ network, and the Internet. The network interface device(s) 718 can be configured to support any type of communications protocol desired. The memory system 712 can include one or more memory units 724(0)-724(N).

[0067] The CPU(s) 702 may also be configured to access the display controller(s) 720 over the system bus 708 to control information sent to one or more displays 726. The display controller(s) 720 sends information to the display(s) 726 to be displayed via one or more video processors 728, which process the information to be displayed into a format suitable for the display(s) 726. The display(s) 726 can include any type of display, including, but not limited to, a cathode ray tube (CRT), a liquid crystal display (LCD), a plasma display, etc.

[0068] Those of skill in the art will further appreciate that the various illustrative logical blocks, modules, circuits, and algorithms described in connection with the aspects disclosed herein may be implemented as electronic hardware, instructions stored in memory or in another computer readable medium and executed by a processor or other processing device, or combinations of both. The master devices and slave devices described herein may be employed in any circuit, hardware component, integrated circuit (IC), or IC chip, as examples. Memory disclosed herein may be any type and size of memory and may be configured to store any type of information desired. To clearly illustrate this interchangeability, various illustrative components, blocks, modules, circuits, and steps have been described above generally in terms of their functionality. How such functionality is implemented depends upon the particular application, design choices, and/or design constraints imposed on the overall system. Skilled artisans may implement the described functionality in varying ways for each particular application, but such implementation decisions should not be interpreted as causing a departure from the scope of the present disclosure.

[0069] The various illustrative logical blocks, modules, and circuits described in connection with the aspects disclosed herein may be implemented or performed with a processor, a Digital Signal Processor (DSP), an Application Specific Integrated Circuit (ASIC), a Field Programmable Gate Array (FPGA) or other programmable logic device, discrete gate or transistor logic, discrete hardware components, or any combination thereof designed to perform the functions described herein. A processor may be a microprocessor, but in the alternative, the processor may be any conventional processor, controller, microcontroller, or state machine. A processor may also be implemented as a combination of computing devices (e.g., a combination of a DSP and a microprocessor, a plurality of microprocessors, one or more microprocessors in conjunction with a DSP core, or any other such configuration).

[0070] The aspects disclosed herein may be embodied in hardware and in instructions that are stored in hardware, and may reside, for example, in Random Access Memory (RAM), flash memory, Read Only Memory (ROM), Electrically Programmable ROM (EPROM), Electrically Erasable Programmable ROM (EEPROM), registers, a hard disk, a removable disk, a CD-ROM, or any other form of computer readable medium known in the art. An exemplary storage medium is coupled to the processor such that the processor can read information from, and write information to, the storage medium. In the alternative, the storage medium may be integral to the processor. The processor and the storage medium may reside in an ASIC. The ASIC may reside in a remote station. In the alternative, the processor and the storage medium may reside as discrete components in a remote station, base station, or server.

[0071] It is also noted that the operational steps described in any of the exemplary aspects herein are described to provide examples and discussion. The operations described may be performed in numerous different sequences other than the illustrated sequences. Furthermore, operations described in a single operational step may actually be performed in a number of different steps. Additionally, one or more operational steps discussed in the exemplary aspects may be combined. It is to be understood that the operational steps illustrated in the flowchart diagrams may be subject to numerous different modifications as will be readily apparent to one of skill in the art. Those of skill in the art will also understand that information and signals may be represented using any of a variety of different technologies and techniques. For example, data, instructions, commands, information, signals, bits, symbols, and chips that may be

referenced throughout the above description may be represented by voltages, currents, electromagnetic waves, magnetic fields or particles, optical fields or particles, or any combination thereof.

[0072] The previous description of the disclosure is provided to enable any person skilled in the art to make or use the disclosure. Various modifications to the disclosure will be readily apparent to those skilled in the art, and the generic principles defined herein may be applied to other variations without departing from the spirit or scope of the disclosure. Thus, the disclosure is not intended to be limited to the examples and designs described herein, but is to be accorded the widest scope consistent with the principles and novel features disclosed herein.

What is claimed is:

1. A dynamic random access memory (DRAM) cache management circuit, communicatively coupled to a DRAM cache that is part of a high-bandwidth memory and further communicatively coupled to a system memory DRAM;

the DRAM cache management circuit comprising a DRAM cache indicator cache configured to cache a plurality of DRAM cache indicators read from a master table in the system memory DRAM, the plurality of DRAM cache indicators indicating whether a corresponding memory line of the system memory DRAM is cached in the DRAM cache

the DRAM cache management circuit configured to:

receive a memory read request comprising a read address;

determine whether the read address is found in the DRAM cache indicator cache;

responsive to determining that the read address is not found in the DRAM cache indicator cache, read data at the read address in the system memory DRAM; and

responsive to determining that the read address is found in the DRAM cache indicator cache:

determine, based on the DRAM cache indicator cache, whether the read address is found in the DRAM cache;

responsive to determining that the read address is not found in the DRAM cache, read data at the read address in the system memory DRAM; and

responsive to determining that the read address is found in the DRAM cache, read data for the read address from the DRAM cache.

2. The DRAM cache management circuit of claim 1, configured to operate in a write-back mode, and further configured to, responsive to determining that the read address is found in the DRAM cache, determine whether the data for the read address in the DRAM cache is clean;

wherein the DRAM cache management circuit is configured to read the data for the read address from the DRAM cache further responsive to

determining that the data for the read address in the DRAM cache is not clean.

3. The DRAM cache management circuit of claim 2, further configured to, responsive to determining that the data for the read address in the DRAM cache is clean:
identify, based on a load balancing circuit of the DRAM cache management circuit, a preferred data source from among the DRAM cache and the system memory DRAM;
responsive to identifying the DRAM cache as the preferred data source, read data from the DRAM cache; and
responsive to identifying the system memory DRAM as the preferred data source, read data from the system memory DRAM.
4. The DRAM cache management circuit of claim 1, configured to operate in a write-through mode, and further configured to, responsive to determining that the read address is found in the DRAM cache:
identify, based on a load balancing circuit of the DRAM cache management circuit, a preferred data source from among the DRAM cache and the system memory DRAM; and
responsive to identifying the system memory DRAM as the preferred data source, read data from the system memory DRAM;
wherein the DRAM cache management circuit is configured to read the data for the read address from the DRAM cache further responsive to determining that the data for the read address in the DRAM cache is clean and identifying the DRAM cache as the preferred data source.
5. The DRAM cache management circuit of claim 1, wherein:
the DRAM cache management circuit is further coupled to a system cache; and
the DRAM cache management circuit is configured to receive the memory read request comprising the read address responsive to a miss on the system cache.

6. The DRAM cache management circuit of claim 1, configured to probabilistically replenish the DRAM cache indicator cache after reading the data at the read address in the system memory DRAM.
7. The DRAM cache management circuit of claim 1, configured to determine, based on the DRAM cache indicator cache, whether the read address is found in the DRAM cache by being configured to determine if a way number for the read address in the DRAM cache is non-zero.
8. The DRAM cache management circuit of claim 1, further configured to:
 - receive, from a system cache, a memory write request comprising a write address and write data comprising clean evicted data;
 - determine whether the write address is found in the DRAM cache; and
 - responsive to determining that the write address is not found in the DRAM cache, probabilistically write the write address and the clean evicted data to the DRAM cache.
9. The DRAM cache management circuit of claim 8, further configured to, prior to determining whether the write address is found in the DRAM cache:
 - determine whether the write address is found in the DRAM cache indicator cache; and
 - responsive to determining that the write address is not found in the DRAM cache indicator cache, probabilistically replenish the DRAM cache indicator cache;
 - wherein the DRAM cache management circuit is configured to determine whether the write address is found in the DRAM cache responsive to replenishing the DRAM cache indicator cache.
10. The DRAM cache management circuit of claim 8, configured to probabilistically write the write address and the clean evicted data to the DRAM cache by being configured to:
 - select a way to be evicted from the DRAM cache;
 - read a memory address of the selected way from the DRAM cache;

write the write address and the clean evicted data to the selected way in the DRAM cache;
update a way number for the write address in the DRAM cache indicator cache to a way number of the selected way;
determine whether the memory address of the selected way is present in the DRAM cache indicator cache; and
responsive to determining that the memory address of the selected way is present in the DRAM cache indicator cache, reset the way number of the selected way for the memory address in the DRAM cache indicator cache.

11. The DRAM cache management circuit of claim 10, further configured to, responsive to determining that the memory address of the selected way is not present in the DRAM cache indicator cache, replenish the DRAM cache indicator cache by being configured to:

read a master table entry of the selected way corresponding to the memory address; and
write the way number of the selected way for the memory address to the DRAM cache indicator cache based on the master table entry.

12. The DRAM cache management circuit of claim 10, further configured to, responsive to determining that the memory address of the selected way is not present in the DRAM cache indicator cache:

reset the way number of the selected way corresponding to the memory address;
and
write the way number to the master table.

13. The DRAM cache management circuit of claim 1, configured to operate in a write-through mode, and further configured to:

receive, from a system cache, a memory write request comprising a write address and write data comprising dirty evicted data;
determine whether the write address is found in the DRAM cache;
responsive to determining that the write address is not found in the DRAM cache, probabilistically write the write address and the dirty evicted data to the DRAM cache;

responsive to determining that the write address is found in the DRAM cache,
write the dirty evicted data to the DRAM cache; and
write the dirty evicted data to the system memory DRAM.

14. The DRAM cache management circuit of claim 13, further configured to, prior to determining whether the write address is found in the DRAM cache:

determine whether the write address is found in the DRAM cache indicator cache; and

responsive to determining that the write address is not found in the DRAM cache indicator cache, probabilistically replenish the DRAM cache indicator cache;

responsive to not replenishing the DRAM cache indicator cache:

update a DRAM cache indicator corresponding to the write address in the master table; and

write the dirty evicted data to the DRAM cache;

wherein the DRAM cache management circuit is configured to determine whether the write address is found in the DRAM cache responsive to replenishing the DRAM cache indicator cache.

15. The DRAM cache management circuit of claim 13, configured to probabilistically write the write address and the dirty evicted data to the DRAM cache by being configured to:

select a way to be evicted from the DRAM cache;

read a memory address of the selected way from the DRAM cache;

write the write address and the dirty evicted data to the selected way in the DRAM cache;

update the way number for the write address in the DRAM cache indicator cache to a way number of the selected way;

determine whether the memory address of the selected way is present in the DRAM cache indicator cache; and

responsive to determining that the memory address of the selected way is present in the DRAM cache indicator cache, reset the way number of the selected way for the memory address in the DRAM cache indicator cache.

16. The DRAM cache management circuit of claim 15, further configured to, responsive to determining that the memory address of the selected way is not present in the DRAM cache indicator cache, replenish the DRAM cache indicator cache by being configured to:

read a master table entry of the selected way corresponding to the memory address; and

write the way number of the selected way for the memory address to the DRAM cache indicator cache based on the master table entry.

17. The DRAM cache management circuit of claim 15, further configured to, responsive to determining that the memory address of the selected way is not present in the DRAM cache indicator cache:

reset the way number of the selected way corresponding to the memory address; and

write the way number to the master table.

18. The DRAM cache management circuit of claim 1, configured to operate in a write-back mode, and further configured to:

receive, from a system cache, a memory write request comprising a write address and write data comprising dirty evicted data;

determine whether the write address is found in the DRAM cache;

responsive to determining that the write address is not found in the DRAM cache, probabilistically write the write address and the dirty evicted data to the DRAM cache;

responsive to not writing the write address and the dirty evicted data to the DRAM cache, write the dirty evicted data to the system memory DRAM; and

responsive to determining that the write address is found in the DRAM cache, write the dirty evicted data to the DRAM cache.

19. The DRAM cache management circuit of claim 18, further configured to, prior to determining whether the write address is found in the DRAM cache:

determine whether the write address is found in the DRAM cache indicator cache; and

responsive to determining that the write address is not found in the DRAM cache indicator cache, probabilistically replenish the DRAM cache indicator cache;

responsive to not replenishing the DRAM cache indicator cache:

read a DRAM cache indicator for the write address from the master table;

write the dirty evicted data to the system memory DRAM; and

determine whether the DRAM cache indicator for the write address from the master table indicates that the write address is in the DRAM cache;

wherein the DRAM cache management circuit is configured to determine whether the write address is found in the DRAM cache responsive to replenishing the DRAM cache indicator cache.

20. The DRAM cache management circuit of claim 18, configured to probabilistically write the write address and the dirty evicted data to the DRAM cache by being configured to:

select a way to be evicted from the DRAM cache;

read a memory address of the selected way from the DRAM cache;

after reading the memory address of the selected way from the DRAM cache, write the write address and the dirty evicted data to the selected way in the DRAM cache;

update a way number for the write address in the DRAM cache indicator cache to a way number of the selected way;

set a dirty indicator for the write address in the DRAM cache indicator cache;

determine whether the memory address of the selected way is present in the DRAM cache indicator cache; and

responsive to determining that the memory address of the selected way is present in the DRAM cache indicator cache, reset the way number and the dirty indicator for the write address of the selected way in the DRAM cache indicator cache.

21. The DRAM cache management circuit of claim 20, further configured to, responsive to determining that the memory address of the selected way is not present in

the DRAM cache indicator cache, replenish the DRAM cache indicator cache by being configured to:

- read a master table entry of the selected way corresponding to the memory address; and
- write the way number of the selected way for the memory address to the DRAM cache indicator cache based on the master table entry.

22. The DRAM cache management circuit of claim 20, further configured to, responsive to determining that the memory address of the selected way is not present in the DRAM cache indicator cache:

- reset the way number of the selected way corresponding to the memory address;
- and
- write the way number to the master table.

23. The DRAM cache management circuit of claim 1 integrated into an integrated circuit (IC).

24. The DRAM cache management circuit of claim 1 integrated into a device selected from the group consisting of: a set top box; an entertainment unit; a navigation device; a communications device; a fixed location data unit; a mobile location data unit; a mobile phone; a cellular phone; a smart phone; a tablet; a phablet; a computer; a portable computer; a desktop computer; a personal digital assistant (PDA); a monitor; a computer monitor; a television; a tuner; a radio; a satellite radio; a music player; a digital music player; a portable music player; a digital video player; a video player; a digital video disc (DVD) player; a portable digital video player; and an automobile.

25. A method for providing scalable dynamic random access memory (DRAM) cache management, comprising:

- receiving, by a DRAM cache management circuit, a memory read request comprising a read address;
- determining whether the read address is found in a DRAM cache indicator cache of the DRAM cache management circuit;

responsive to determining that the read address is not found in the DRAM cache indicator cache, reading data at the read address in a system memory DRAM; and

responsive to determining that the read address is found in the DRAM cache indicator cache:

determining, based on the DRAM cache indicator cache, whether the read address is found in a DRAM cache that is part of a high-bandwidth memory;

responsive to determining that the read address is not found in the DRAM cache, reading data at the read address in the system memory DRAM; and

responsive to determining that the read address is found in the DRAM cache, reading data for the read address from the DRAM cache.

26. The method of claim 25, wherein the DRAM cache management circuit is configured to operate in a write-back mode, and further comprising, responsive to determining that the read address is found in the DRAM cache, determining whether the data for the read address in the DRAM cache is clean;

wherein reading the data for the read address from the DRAM cache is further responsive to determining that the data for the read address in the DRAM cache is not clean.

27. The method of claim 26, further comprising, responsive to determining that the data for the read address in the DRAM cache is clean:

identifying a preferred data source from among the DRAM cache and the system memory DRAM;

responsive to identifying the DRAM cache as the preferred data source, reading data from the DRAM cache; and

responsive to identifying the system memory DRAM as the preferred data source, reading data from the system memory DRAM.

28. The method of claim 25, wherein the DRAM cache management circuit is configured to operate in a write-through mode, and further comprising, responsive to determining that the read address is found in the DRAM cache:

identifying a preferred data source from among the DRAM cache and the system memory DRAM; and
responsive to identifying the system memory DRAM as the preferred data source, reading data from the system memory DRAM;
wherein reading the data for the read address from the DRAM cache is further responsive to determining that the data for the read address in the DRAM cache is clean and identifying the DRAM cache as the preferred data source.

29. The method of claim 25, wherein receiving the memory read request comprising the read address is responsive to a miss on a system cache.

30. The method of claim 25, further comprising probabilistically replenishing the DRAM cache indicator cache after reading the data at the read address in the system memory DRAM.

31. The method of claim 25, further comprising determining, based on the DRAM cache indicator cache, whether the read address is found in the DRAM cache by determining if a way number for the read address in the DRAM cache is non-zero.

32. The method of claim 25, further comprising:
receiving, from a system cache, a memory write request comprising a write address and write data comprising clean evicted data;
determining whether the write address is found in the DRAM cache; and
responsive to determining that the write address is not found in the DRAM cache, probabilistically writing the write address and the clean evicted data to the DRAM cache.

33. The method of claim 32, further comprising, prior to determining whether the write address is found in the DRAM cache:
determining whether the write address is found in the DRAM cache indicator cache; and

responsive to determining that the write address is not found in the DRAM cache indicator cache, probabilistically replenishing the DRAM cache indicator cache;

wherein determining whether the write address is found in the DRAM cache is responsive to replenishing the DRAM cache indicator cache.

34. The method of claim 32, comprising probabilistically writing the write address and the clean evicted data to the DRAM cache by:

selecting a way to be evicted from the DRAM cache;

reading a memory address of the selected way from the DRAM cache;

writing the write address and the clean evicted data to the selected way in the DRAM cache;

updating a way number for the write address in the DRAM cache indicator cache to a way number of the selected way;

determining whether the memory address of the selected way is present in the DRAM cache indicator cache; and

responsive to determining that the memory address of the selected way is present in the DRAM cache indicator cache, resetting the way number of the selected way for the memory address in the DRAM cache indicator cache.

35. The method of claim 34, further comprising, responsive to determining that the memory address of the selected way is not present in the DRAM cache indicator cache, replenishing the DRAM cache indicator cache by:

reading a master table entry of the selected way corresponding to the memory address from a master table in the system memory DRAM; and

writing the way number of the selected way for the memory address to the DRAM cache indicator cache based on the master table entry.

36. The method of claim 34, further comprising, responsive to determining that the memory address of the selected way is not present in the DRAM cache indicator cache:

resetting the way number of the selected way corresponding to the memory address; and

writing the way number to a master table in the system memory DRAM.

37. The method of claim 25, wherein the DRAM cache management circuit is configured to operate in a write-through mode, and further comprises:

- receiving, from a system cache, a memory write request comprising a write address and write data comprising dirty evicted data;
- determining whether the write address is found in the DRAM cache;
- responsive to determining that the write address is not found in the DRAM cache, probabilistically writing the write address and the dirty evicted data to the DRAM cache;
- responsive to determining that the write address is found in the DRAM cache, writing the dirty evicted data to the DRAM cache; and
- writing the dirty evicted data to the system memory DRAM.

38. The method of claim 37, further comprising, prior to determining whether the write address is found in the DRAM cache:

- determining whether the write address is found in the DRAM cache indicator cache; and
- responsive to determining that the write address is not found in the DRAM cache indicator cache, probabilistically replenishing the DRAM cache indicator cache;
- responsive to not replenishing the DRAM cache indicator cache:
 - updating a DRAM cache indicator corresponding to the write address in a master table in the system memory DRAM;
 - and
 - writing the dirty evicted data to the DRAM cache;

wherein determining whether the write address is found in the DRAM cache is responsive to replenishing the DRAM cache indicator cache.

39. The method of claim 37, wherein probabilistically writing the write address and the dirty evicted data to the DRAM cache comprises:

- selecting a way to be evicted from the DRAM cache;
- reading a memory address of the selected way from the DRAM cache;
- writing the write address and the dirty evicted data to the selected way in the DRAM cache;

updating a way number for the write address in the DRAM cache indicator cache to a way number of the selected way;
determining whether the memory address of the selected way is present in the DRAM cache indicator cache; and
responsive to determining that the memory address of the selected way is present in the DRAM cache indicator cache, resetting the way number of the selected way for the memory address in the DRAM cache indicator cache.

40. The method of claim 39, further comprising, responsive to determining that the memory address of the selected way is not present in the DRAM cache indicator cache, replenishing the DRAM cache indicator cache by:

reading a master table entry of the selected way corresponding to the memory address; and
writing the way number of the selected way for the memory address to the DRAM cache indicator cache based on the master table entry.

41. The method of claim 39, further comprising, responsive to determining that the memory address of the selected way is not present in the DRAM cache indicator cache:

resetting the way number of the selected way corresponding to the memory address; and
writing the way number to a master table in the system memory DRAM.

42. The method of claim 25, wherein the DRAM cache management circuit is configured to operate in a write-back mode, and further comprises:

receiving, from a system cache, a memory write request comprising a write address and write data comprising dirty evicted data;
determining whether the write address is found in the DRAM cache;
responsive to determining that the write address is not found in the DRAM cache, probabilistically writing the write address and the dirty evicted data to the DRAM cache;
responsive to not writing the write address and the dirty evicted data to the DRAM cache, writing the dirty evicted data to the system memory DRAM; and

responsive to determining that the write address is found in the DRAM cache,
writing the dirty evicted data to the DRAM cache.

43. The method of claim 42, further comprising, prior to determining whether the write address is found in the DRAM cache:

determining whether the write address is found in the DRAM cache indicator cache; and

responsive to determining that the write address is not found in the DRAM cache indicator cache, probabilistically replenishing the DRAM cache indicator cache;

responsive to not replenishing the DRAM cache indicator cache:

updating a DRAM cache indicator corresponding to the write address in a master table in the system memory DRAM;

writing the dirty evicted data to the system memory DRAM; and

determining whether the DRAM cache indicator for the write address from the master table indicates that the write address is in the DRAM cache;

wherein determining whether the write address is found in the DRAM cache is responsive to replenishing the DRAM cache indicator cache.

44. The method of claim 42, wherein probabilistically writing the write address and the dirty evicted data to the DRAM cache comprises:

selecting a way to be evicted from the DRAM cache;

reading a memory address of the selected way from the DRAM cache;

after reading the memory address of the selected way from the DRAM cache,
writing the write address and the dirty evicted data to the selected way in the DRAM cache;

updating a way number for the write address in the DRAM cache indicator cache to a way number of the selected way;

setting a dirty indicator for the write address in the DRAM cache indicator cache;

determining whether the memory address of the selected way is present in the DRAM cache indicator cache; and

responsive to determining that the memory address of the selected way is present in the DRAM cache indicator cache, resetting the way number and the dirty indicator of the selected way for the write address in the DRAM cache indicator cache.

45. The method of claim 44, further comprising, responsive to determining that the memory address of the selected way is not present in the DRAM cache indicator cache, replenishing the DRAM cache indicator cache by:

reading a master table entry of the selected way corresponding to the memory address; and

writing the way number of the selected way for the memory address to the DRAM cache indicator cache based on the master table entry.

46. The method of claim 44, further comprising, responsive to determining that the memory address of the selected way is not present in the DRAM cache indicator cache:

resetting the way number of the selected way corresponding to the memory address; and

writing the way number to a master table in the system memory DRAM.

47. A dynamic random access memory (DRAM) cache management circuit, comprising:

a means for receiving a memory read request comprising a read address;

a means for determining whether the read address is found in a DRAM cache indicator cache of the DRAM cache management circuit;

a means for reading data at the read address in a system memory DRAM, responsive to determining that the read address is not found in the DRAM cache indicator cache;

a means for determining, based on the DRAM cache indicator cache, whether the read address is found in a DRAM cache that is part of a high-bandwidth memory, responsive to determining that the read address is found in the DRAM cache indicator cache;

a means for reading data at the read address in the system memory DRAM, responsive to determining that the read address is not found in the DRAM cache; and

a means for reading data for the read address from the DRAM cache, responsive to determining that the read address is found in the DRAM cache.

1/15

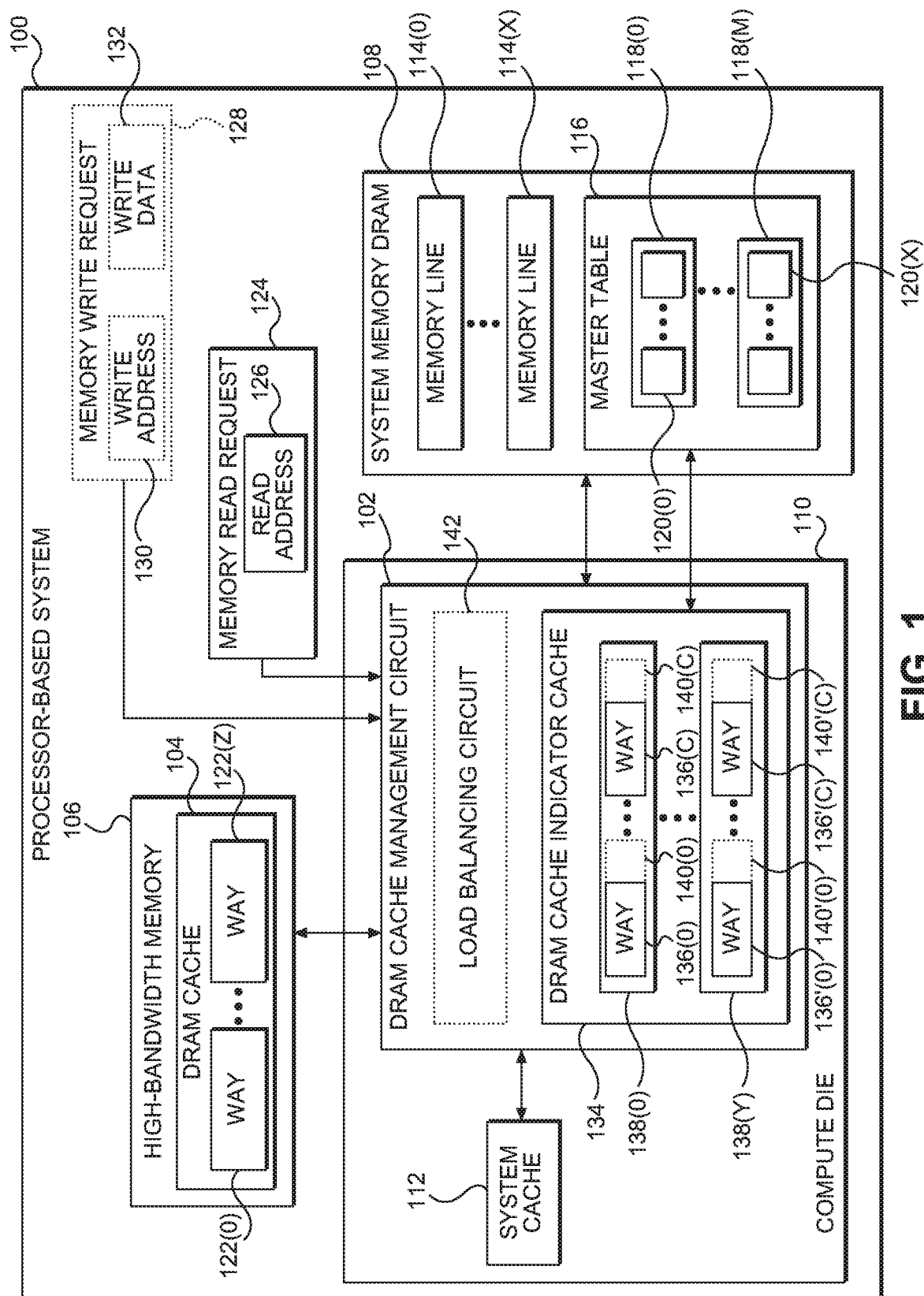
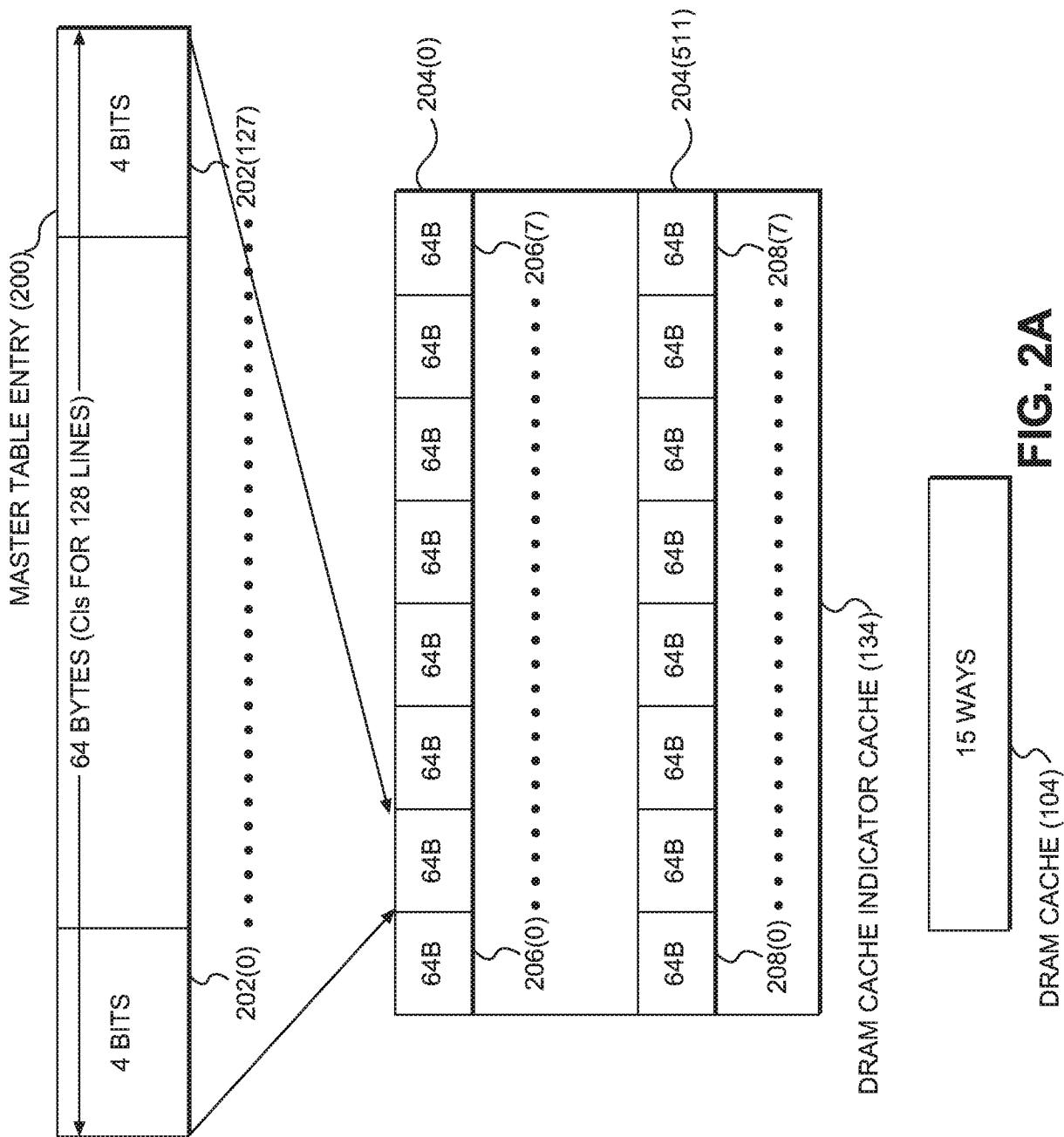
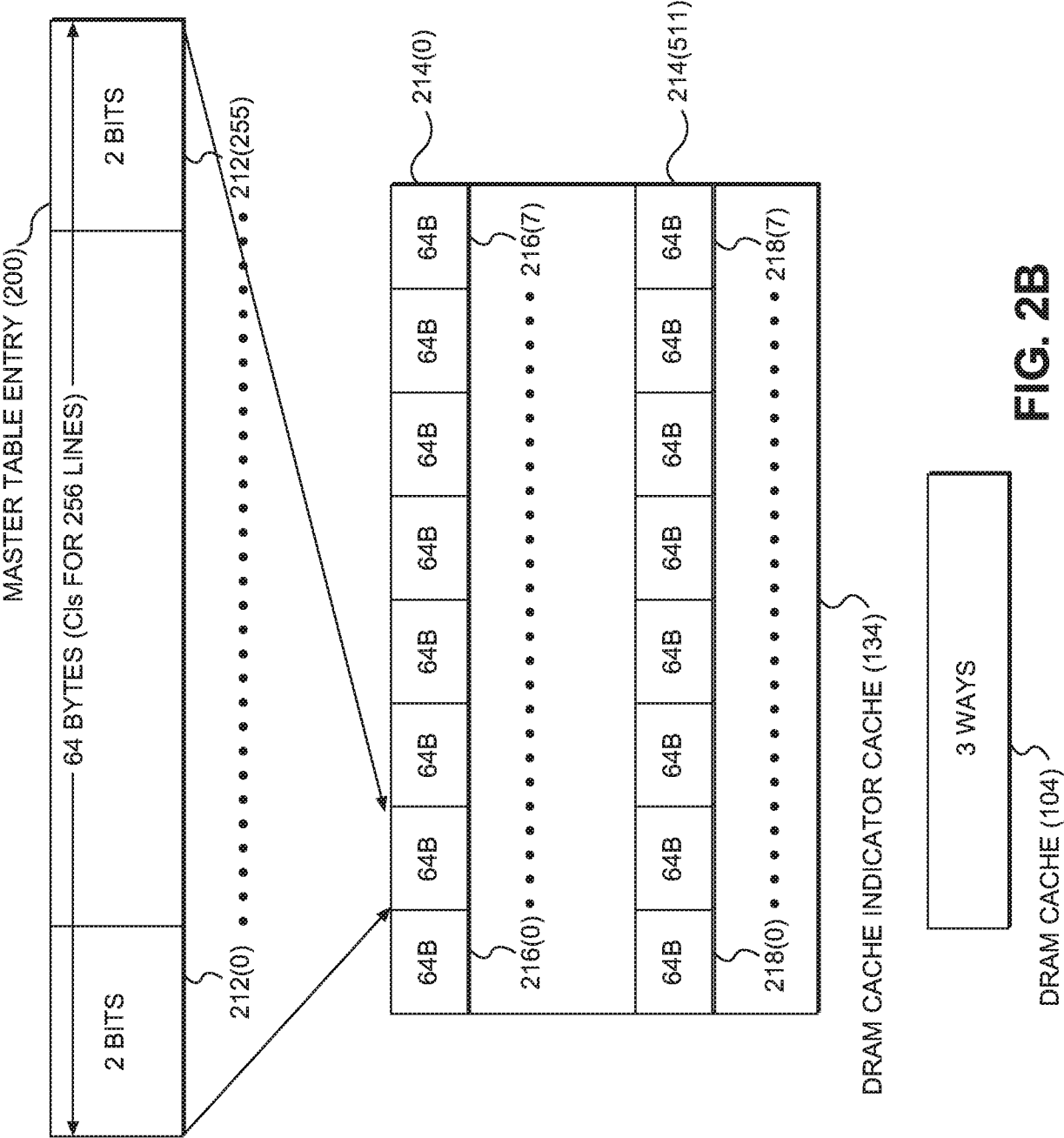
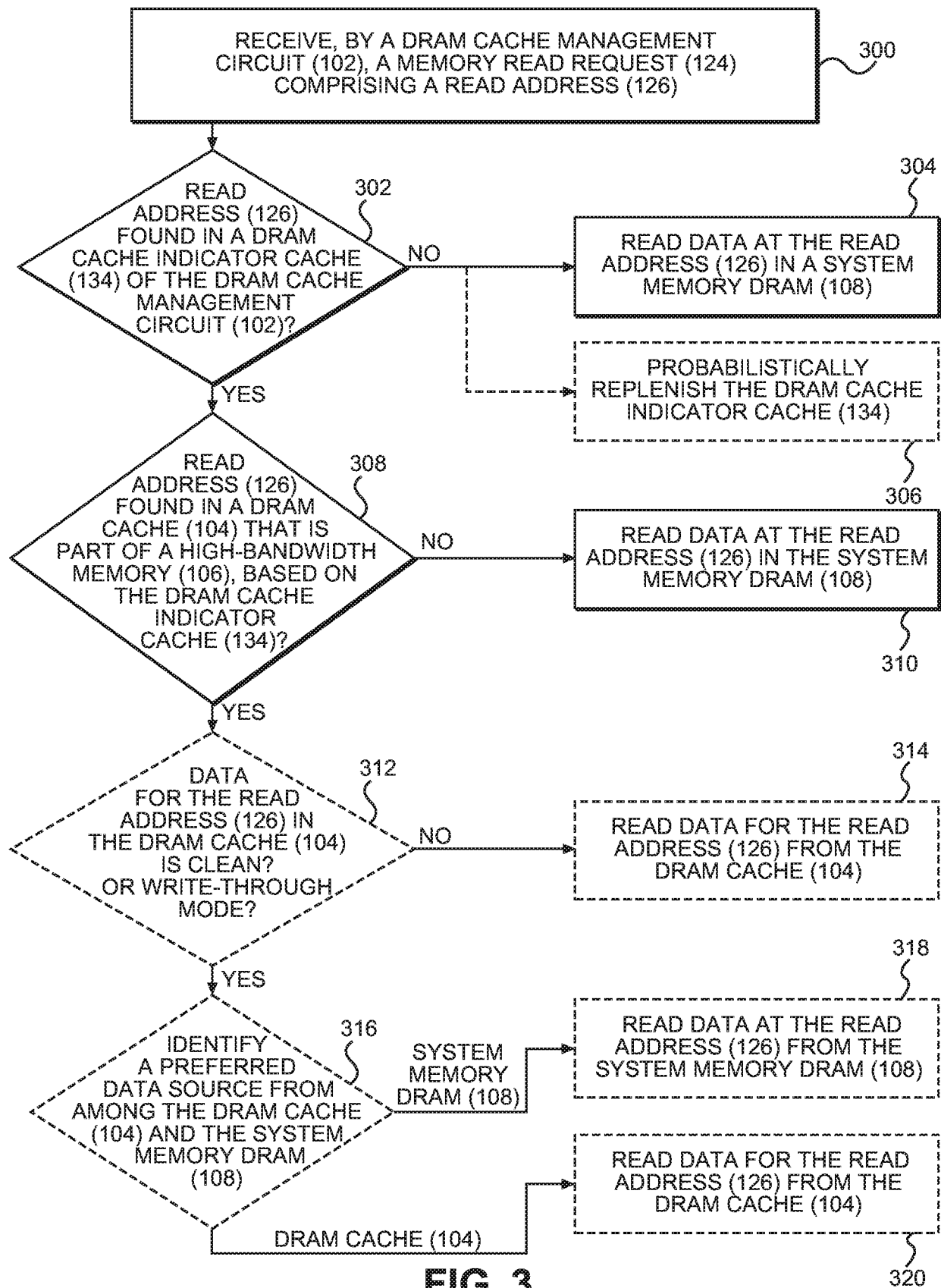


FIG. 1





4/15



5/15

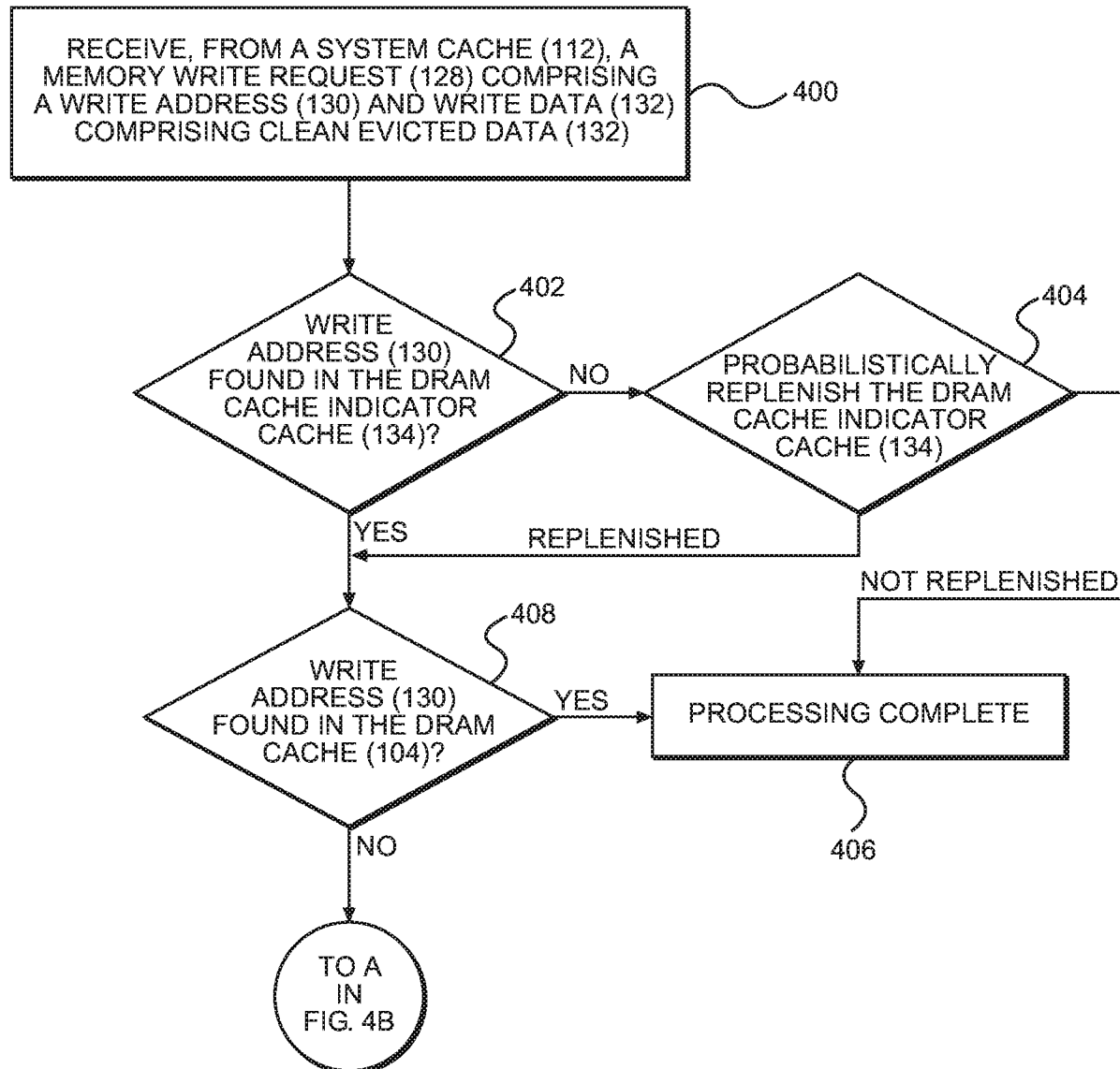
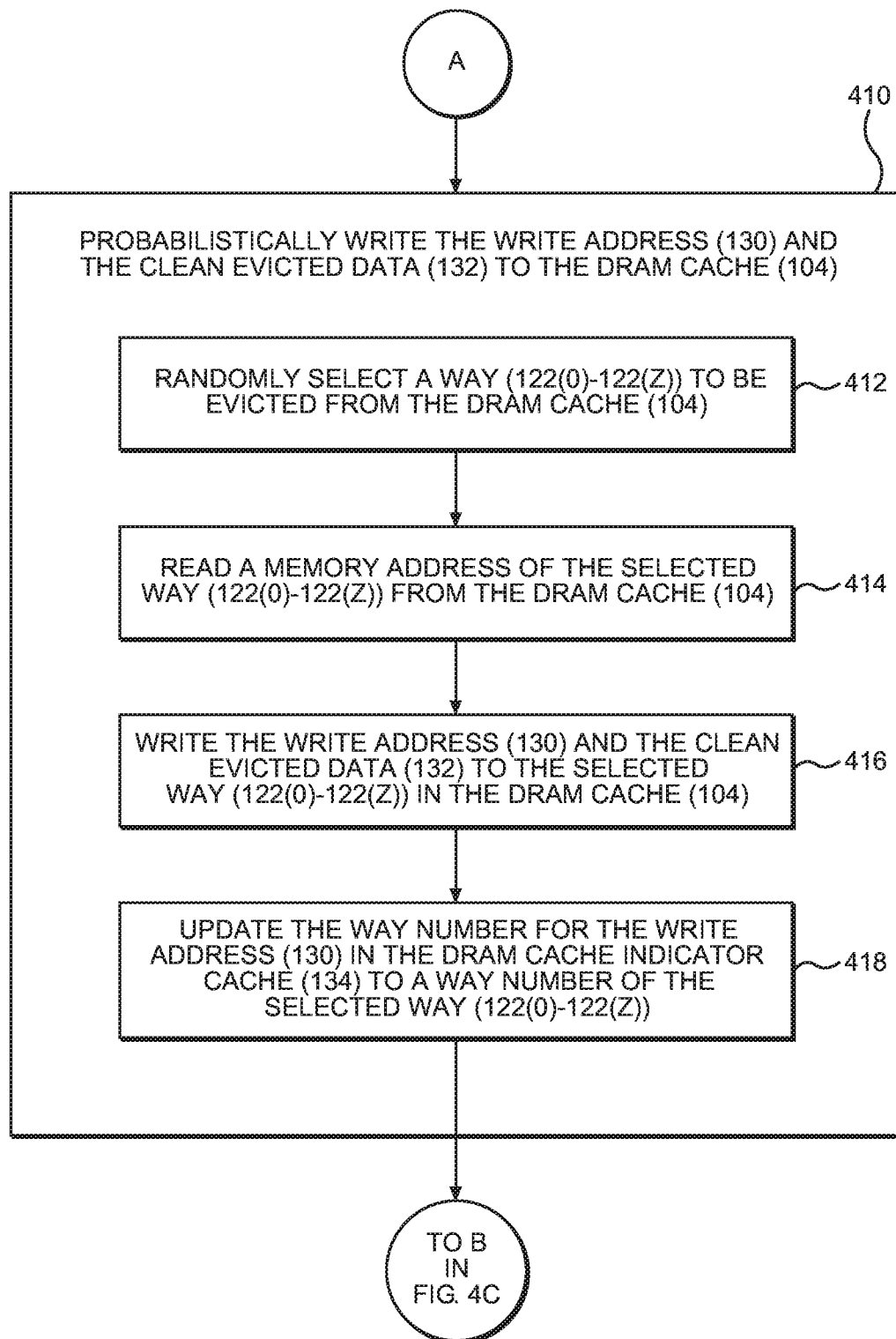


FIG. 4A

6/15

**FIG. 4B**

7/15

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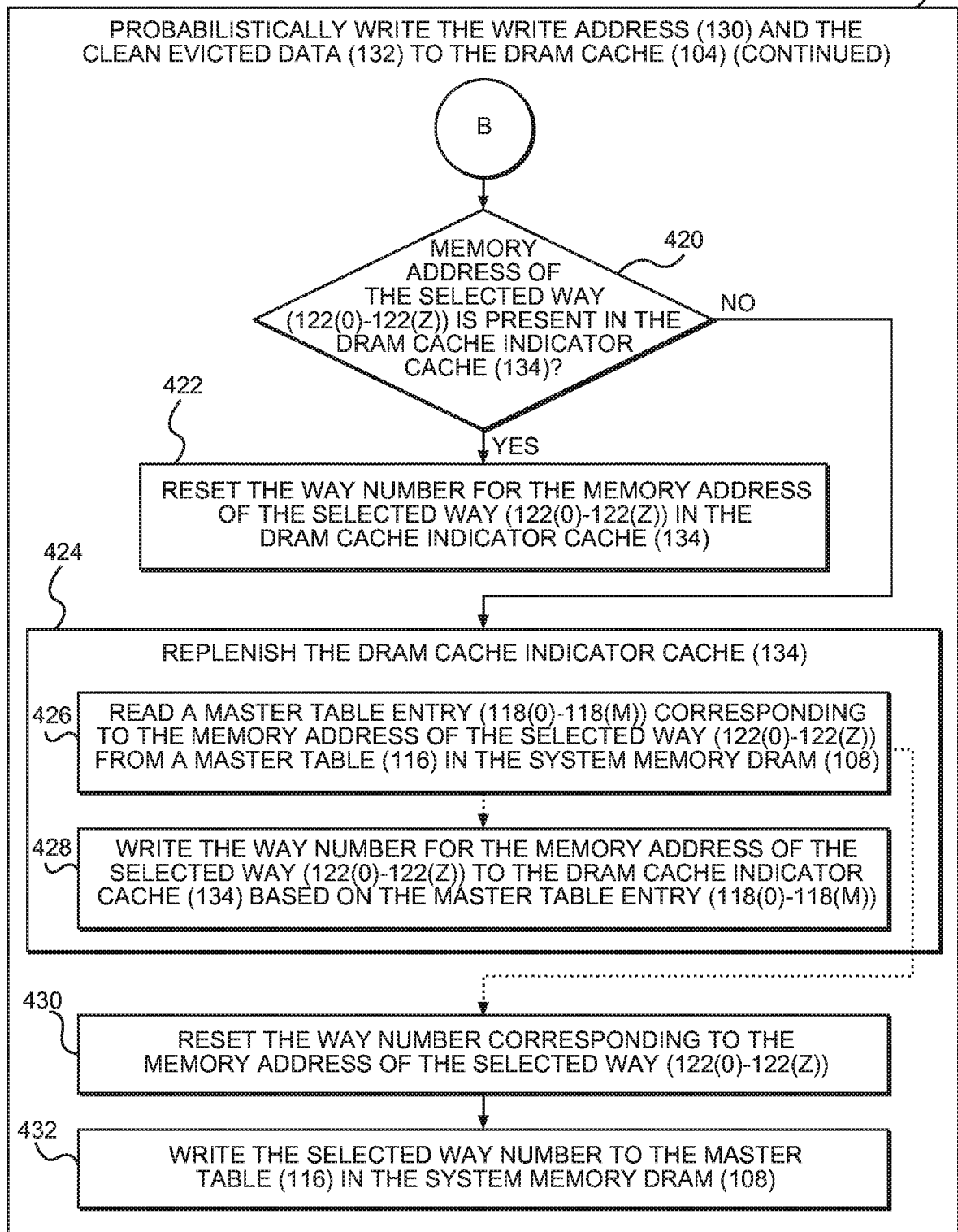


FIG. 4C

8/15

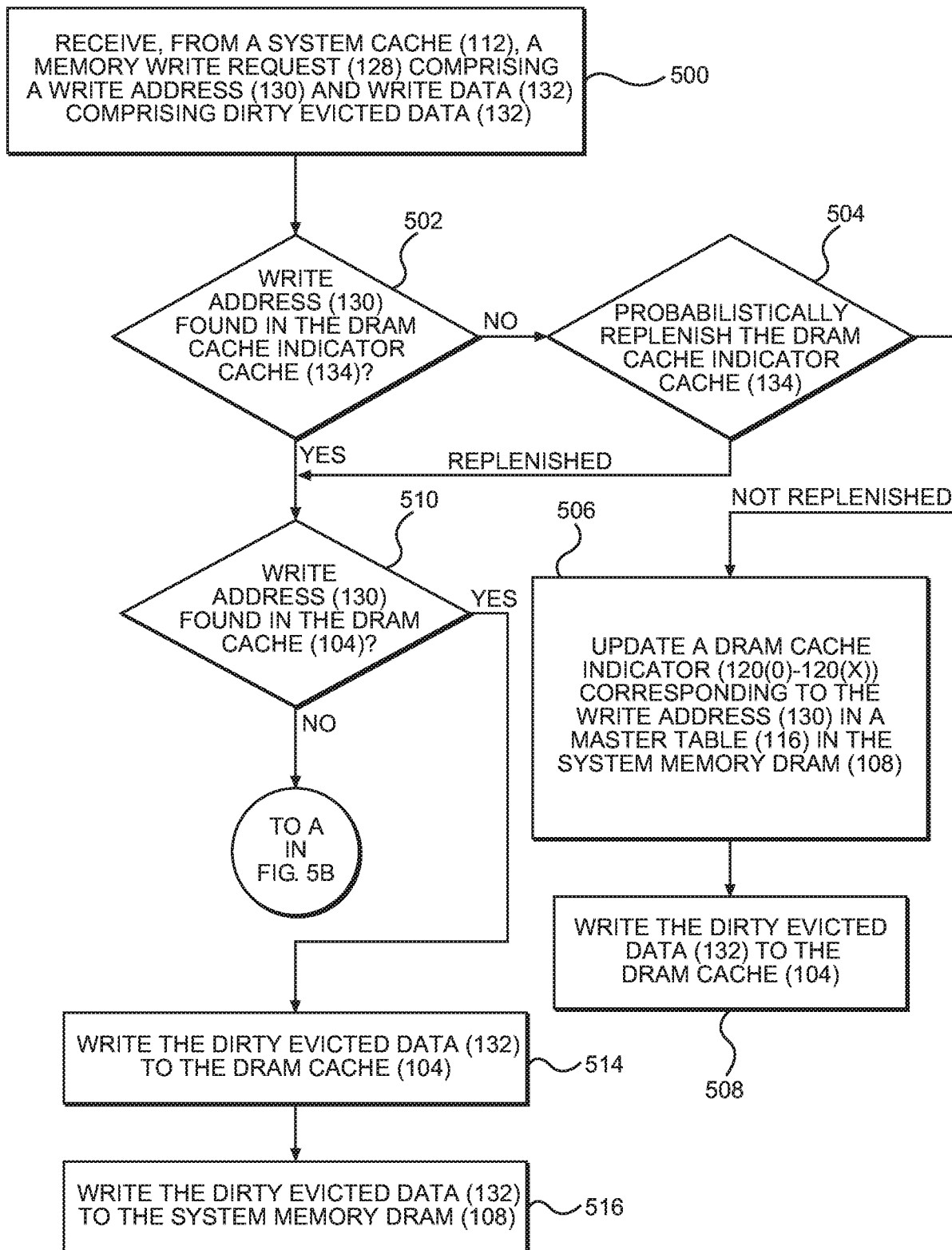
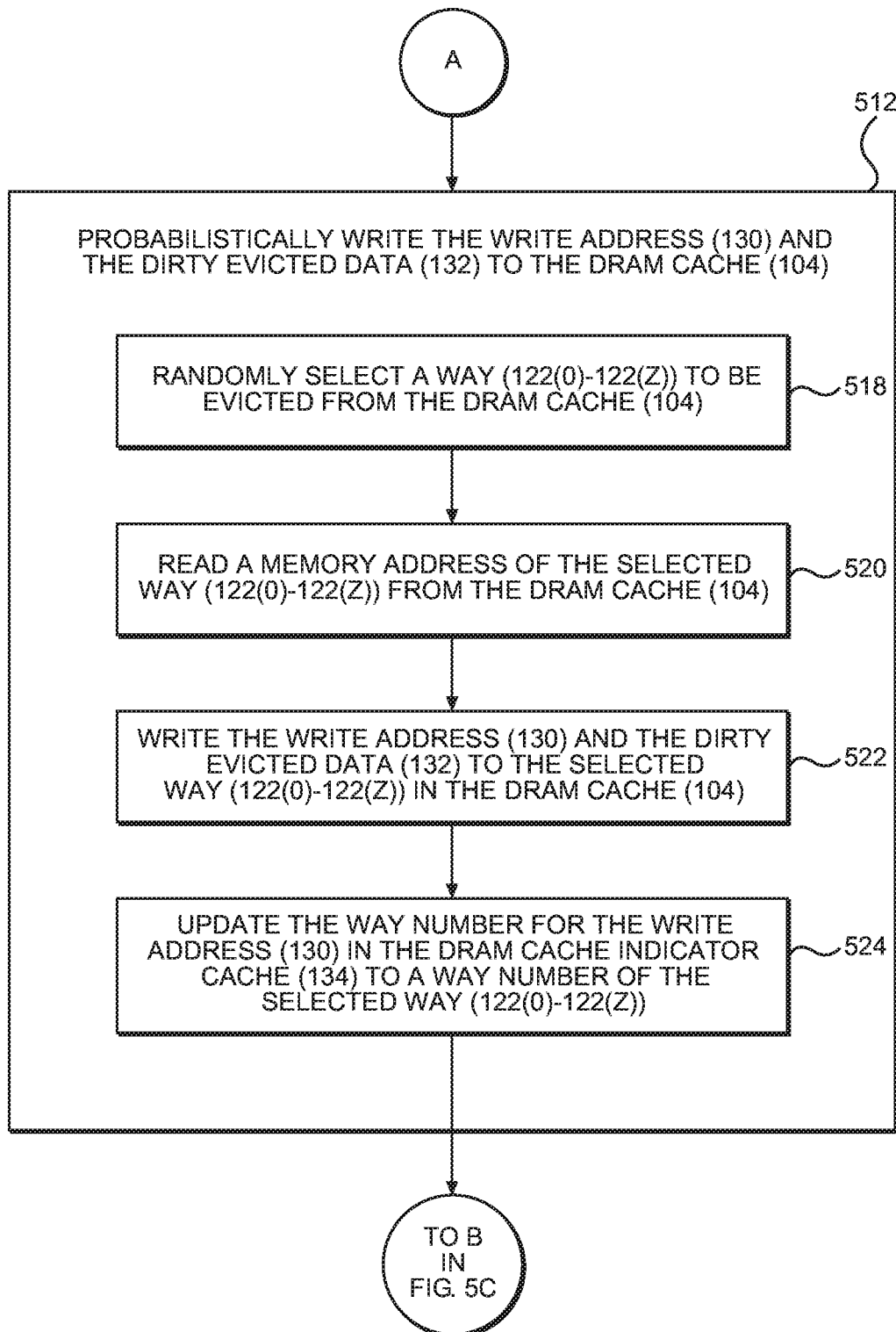


FIG. 5A

9/15

**FIG. 5B**

10/15

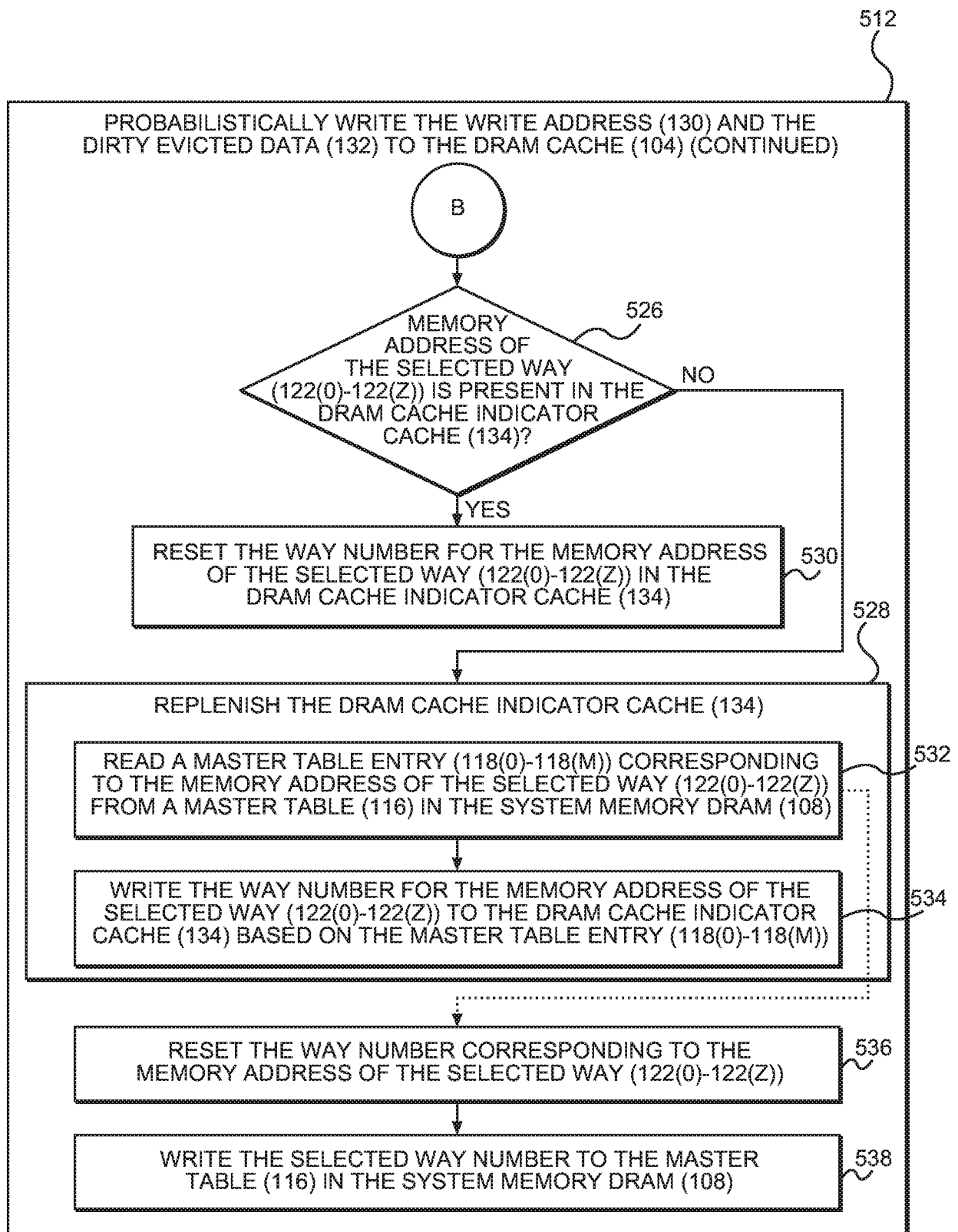
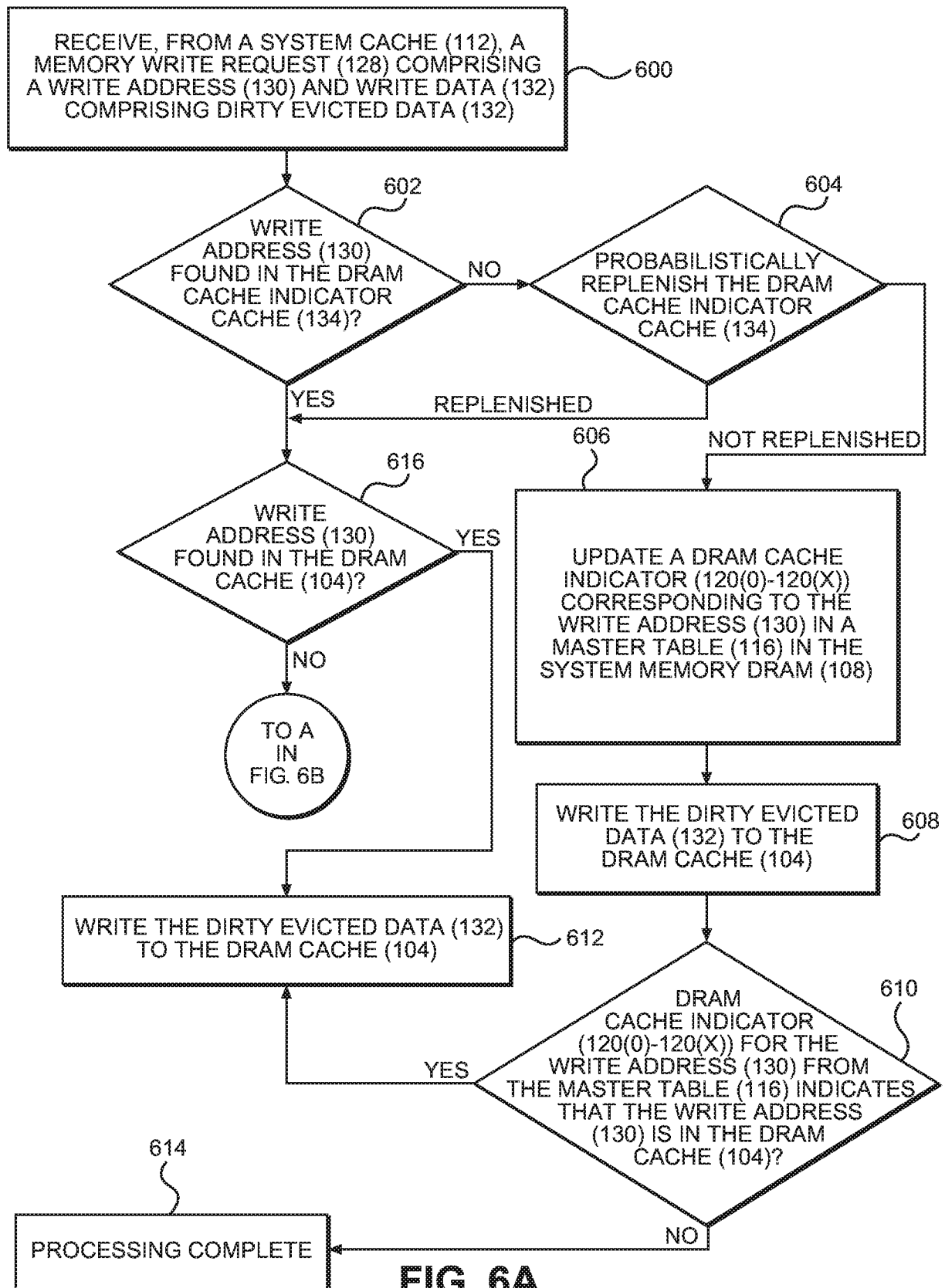
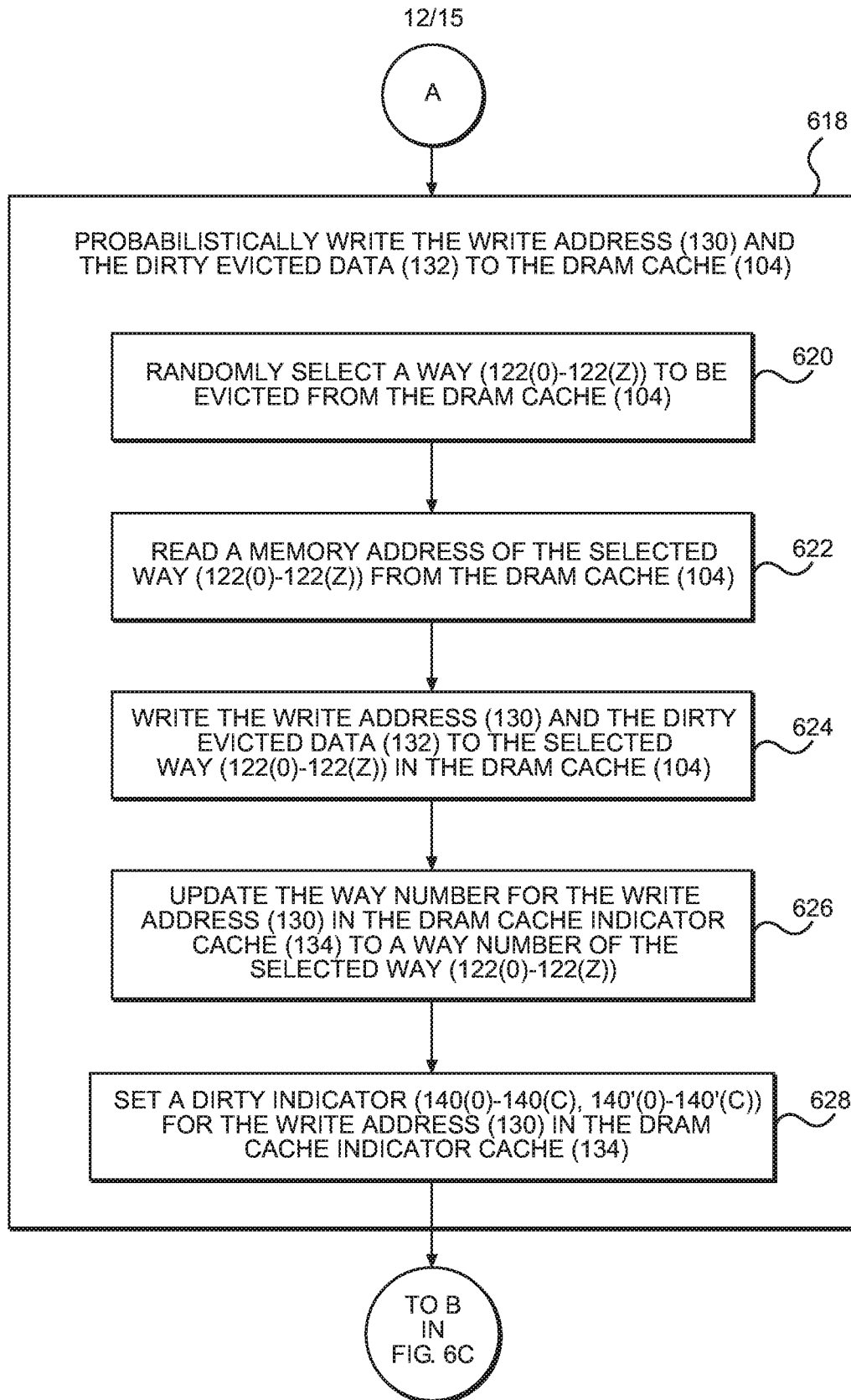


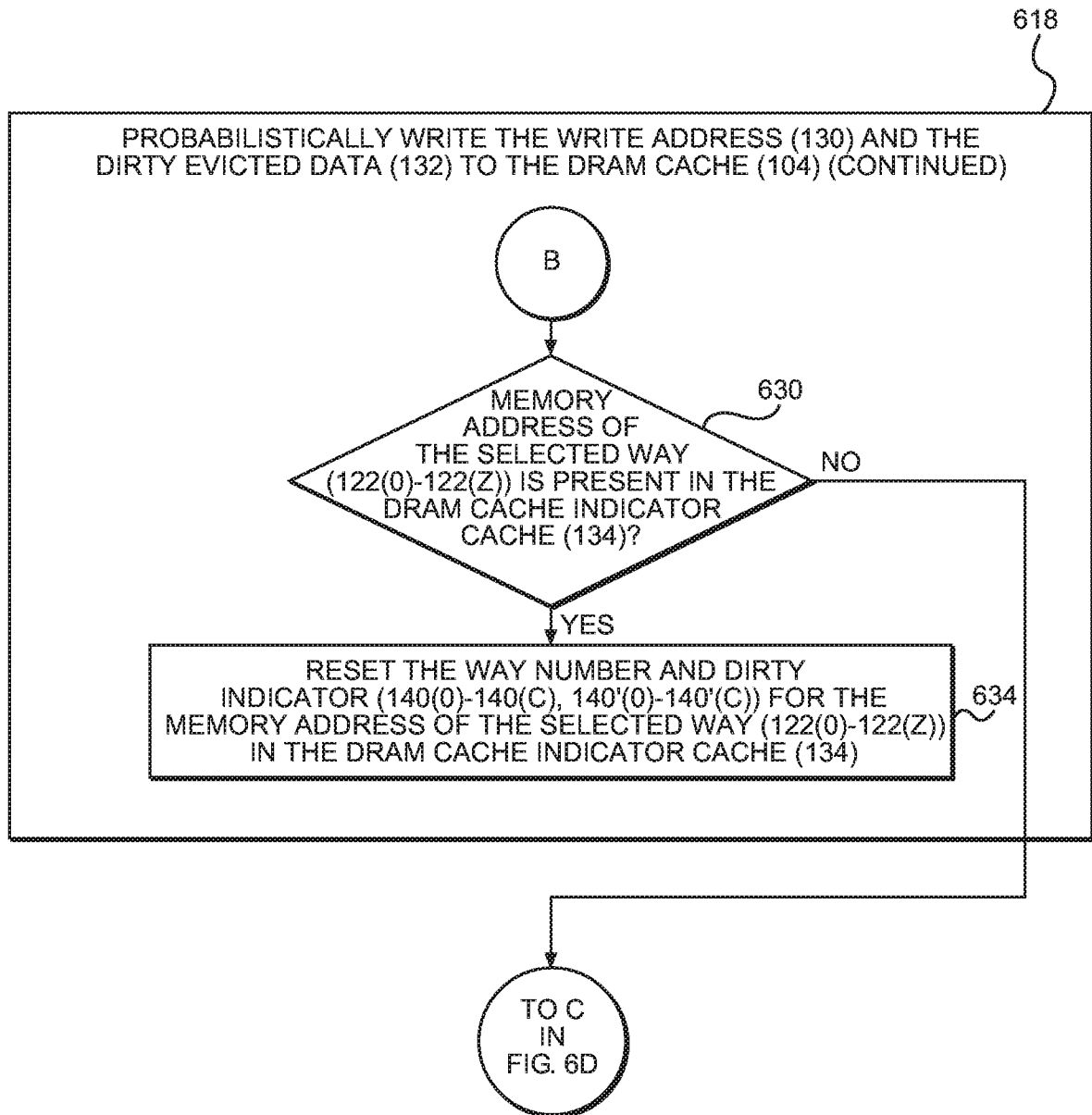
FIG. 5C

11/15



**FIG. 6B**

13/15

**FIG. 6C**

14/15

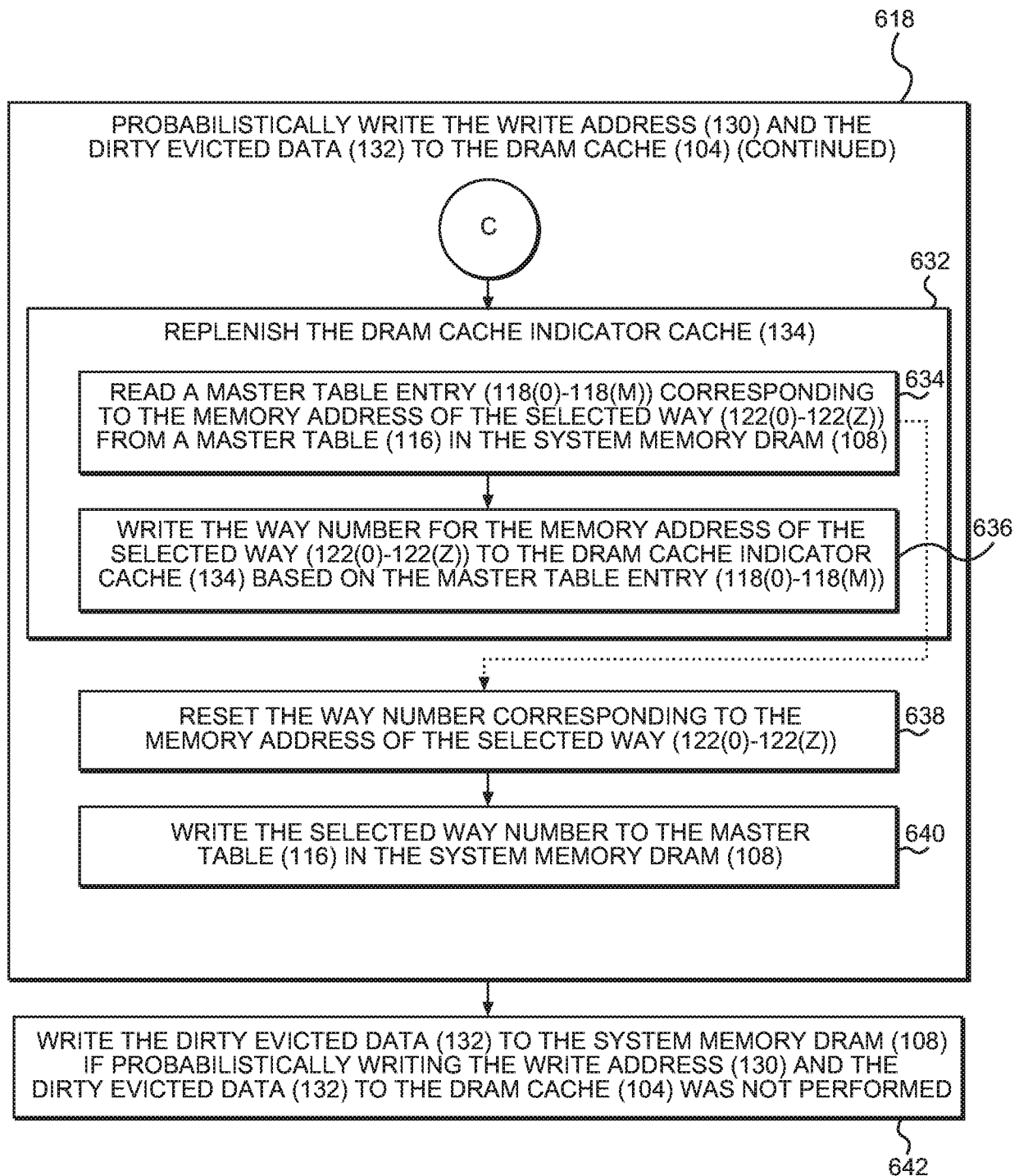


FIG. 6D

15/15

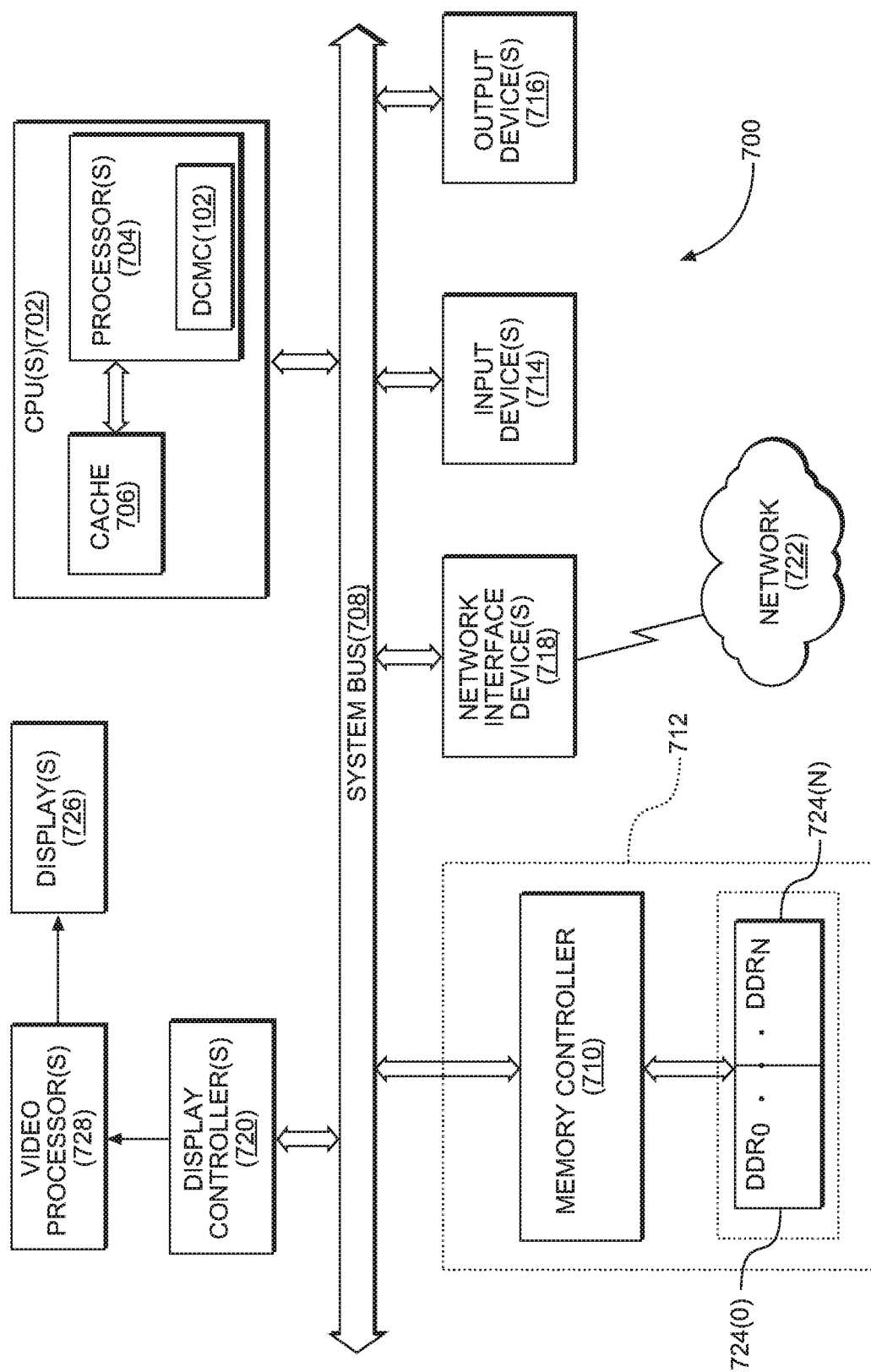


FIG. 7

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2017/016005A. CLASSIFICATION OF SUBJECT MATTER
INV. G06F12/0893
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G06F G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 2015/152857 A1 (EMPIRE TECHNOLOGY DEV LLC [US]) 8 October 2015 (2015-10-08) figure 1 paragraph [0022] paragraph [0076] -----	1-47



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents :

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

3 April 2017

Date of mailing of the international search report

21/04/2017

Name and mailing address of the ISA/

European Patent Office, P.B. 5818 Patentlaan 2
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Authorized officer

Filip, Liviu

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/US2017/016005

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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权利要求书10页 说明书16页 附图15页

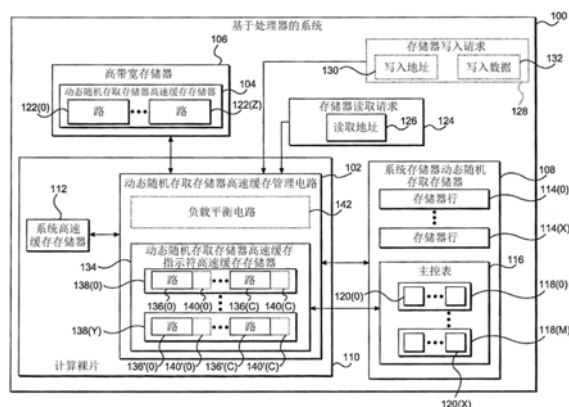
(54)发明名称

使用动态随机存取存储器(DRAM)高速缓存指示符高速缓存存储器以提供可扩展DRAM高速缓存管理

存储器DRAM而以优化方式执行存储器存取操作。

(57)摘要

本发明提供使用动态随机存取存储器DRAM高速缓存指示符高速缓存存储器以提供可扩展DRAM高速缓存管理。在一个方面中,提供DRAM高速缓存管理电路以管理对高带宽存储器中的DRAM高速缓存存储器的存取。所述DRAM高速缓存管理电路包括DRAM高速缓存指示符高速缓存存储器,其存储从系统存储器DRAM中的主控表读取并含有DRAM高速缓存指示符的主控表项。所述DRAM高速缓存指示符使得所述DRAM高速缓存管理电路能够确定所述系统存储器DRAM中的存储器行是否在高带宽存储器的所述DRAM高速缓存存储器中被高速缓存,且如果是,那么确定所述存储器行被存储在所述DRAM高速缓存存储器的哪一路中。基于所述DRAM高速缓存指示符高速缓存存储器,所述DRAM高速缓存管理电路可确定是否采用所述DRAM高速缓存存储器及/或所述系统



1. 一种动态随机存取存储器DRAM高速缓存管理电路,其以通信方式耦合到为高带宽存储器的部分的DRAM高速缓存存储器且进一步以通信方式耦合到系统存储器DRAM;

所述DRAM高速缓存管理电路包括DRAM高速缓存指示符高速缓存存储器,其经配置以高速缓存从所述系统存储器DRAM中的主控表读取的多个DRAM高速缓存指示符,所述多个DRAM高速缓存指示符指示所述系统存储器DRAM的对应存储器行是否在所述DRAM高速缓存存储器中被高速缓存;

所述DRAM高速缓存管理电路经配置以:

接收包括读取地址的存储器读取请求;

确定所述读取地址是否在所述DRAM高速缓存指示符高速缓存存储器中被发现;

响应于确定所述读取地址在所述DRAM高速缓存指示符高速缓存存储器中未被发现,读取在所述系统存储器DRAM中的所述读取地址处的数据;及

响应于确定所述读取地址在所述DRAM高速缓存指示符高速缓存存储器中被发现:

基于所述DRAM高速缓存指示符高速缓存存储器确定所述读取地址是否在所述DRAM高速缓存存储器中被发现;

响应于确定所述读取地址在所述DRAM高速缓存存储器中未被发现,读取在所述系统存储器DRAM中的所述读取地址处的数据;及

响应于确定所述读取地址在所述DRAM高速缓存存储器中被发现,从所述DRAM高速缓存存储器读取针对所述读取地址的数据。

2. 根据权利要求1所述的DRAM高速缓存管理电路,其经配置而在回写模式中操作,且经进一步配置以响应于确定所述读取地址在所述DRAM高速缓存存储器中被发现,确定所述DRAM高速缓存存储器中的针对所述读取地址的所述数据是否清洁;

其中所述DRAM高速缓存管理电路经配置以进一步响应于确定所述DRAM高速缓存存储器中的针对所述读取地址的所述数据并非清洁而从所述DRAM高速缓存存储器读取针对所述读取地址的所述数据。

3. 根据权利要求2所述的DRAM高速缓存管理电路,其经进一步配置以响应于确定所述DRAM高速缓存存储器中的针对所述读取地址的所述数据为清洁的:

基于所述DRAM高速缓存管理电路的负载平衡电路从所述DRAM高速缓存存储器及所述系统存储器DRAM当中识别优选数据源;

响应于将所述DRAM高速缓存存储器识别为所述优选数据源,从所述DRAM高速缓存存储器读取数据;及

响应于将所述系统存储器DRAM识别为所述优选数据源,从所述系统存储器DRAM读取数据。

4. 根据权利要求1所述的DRAM高速缓存管理电路,其经配置以在完全写入模式中操作,且经进一步配置以响应于确定所述读取地址在所述DRAM高速缓存存储器中被发现:

基于所述DRAM高速缓存管理电路的负载平衡电路从所述DRAM高速缓存存储器及所述系统存储器DRAM当中识别优选数据源;及

响应于将所述系统存储器DRAM识别为所述优选数据源,从所述系统存储器DRAM读取数据;

其中所述DRAM高速缓存管理电路经配置以进一步响应于确定所述DRAM高速缓存存储

器中的针对所述读取地址的所述数据为清洁的及将所述DRAM高速缓存存储器识别为所述优选数据源而从所述DRAM高速缓存存储器读取针对所述读取地址的所述数据。

5. 根据权利要求1所述的DRAM高速缓存管理电路, 其中:

所述DRAM高速缓存管理电路进一步耦合到系统高速缓存存储器; 及

所述DRAM高速缓存管理电路经配置以响应于对所述系统高速缓存存储器的未命中而接收包括所述读取地址的所述存储器读取请求。

6. 根据权利要求1所述的DRAM高速缓存管理电路, 其经配置以在读取所述系统存储器DRAM中的所述读取地址处的所述数据之后概率性地补充所述DRAM高速缓存指示符高速缓存存储器。

7. 根据权利要求1所述的DRAM高速缓存管理电路, 其经配置以基于所述DRAM高速缓存指示符高速缓存存储器通过经配置以确定所述DRAM高速缓存存储器中的针对所述读取地址的路编号是否为非零的而确定所述读取地址是否在所述DRAM高速缓存存储器中被发现。

8. 根据权利要求1所述的DRAM高速缓存管理电路, 其经进一步配置以:

从系统高速缓存存储器接收存储器写入请求, 所述存储器写入请求包括写入地址及包括清洁逐出的数据的写入数据;

确定所述写入地址是否在所述DRAM高速缓存存储器中被发现; 及

响应于确定所述写入地址在所述DRAM高速缓存存储器中未被发现, 将所述写入地址及所述清洁逐出的数据概率性地写入到所述DRAM高速缓存存储器。

9. 根据权利要求8所述的DRAM高速缓存管理电路, 其经进一步配置以在确定所述写入地址是否在所述DRAM高速缓存存储器中被发现之前:

确定所述写入地址是否在所述DRAM高速缓存指示符高速缓存存储器中被发现; 及

响应于确定所述写入地址在所述DRAM高速缓存指示符高速缓存存储器中未被发现, 概率性地补充所述DRAM高速缓存指示符高速缓存存储器;

其中所述DRAM高速缓存管理电路经配置以响应于补充所述DRAM高速缓存指示符高速缓存存储器而确定所述写入地址是否在所述DRAM高速缓存存储器中被发现。

10. 根据权利要求8所述的DRAM高速缓存管理电路, 其经配置以通过经配置以执行以下操作而将所述写入地址及所述清洁逐出的数据概率性地写入到所述DRAM高速缓存存储器:

选择待从所述DRAM高速缓存存储器逐出的路;

从所述DRAM高速缓存存储器读取所述所选择路的存储器地址;

将所述写入地址及所述清洁逐出的数据写入到所述DRAM高速缓存存储器中的所述所选择路;

将所述DRAM高速缓存指示符高速缓存存储器中的针对所述写入地址的路编号更新为所述所选择路的路编号;

确定所述所选择路的所述存储器地址是否存在于所述DRAM高速缓存指示符高速缓存存储器中; 及

响应于确定所述所选择路的所述存储器地址存在于所述DRAM高速缓存指示符高速缓存存储器中, 复位所述DRAM高速缓存指示符高速缓存存储器中的针对所述存储器地址的所述所选择路的所述路编号。

11. 根据权利要求10所述的DRAM高速缓存管理电路, 其经进一步配置以响应于确定所

述所选择路的所述存储器地址不存在于所述DRAM高速缓存指示符高速缓存存储器中,通过经配置以执行以下操作而补充所述DRAM高速缓存指示符高速缓存存储器:

读取对应于所述存储器地址的所述所选择路的主控表项;及

基于所述主控表项将针对所述存储器地址的所述所选择路的所述路编号写入到所述DRAM高速缓存指示符高速缓存存储器。

12. 根据权利要求10所述的DRAM高速缓存管理电路,其经进一步配置以响应于确定所述所选择路的所述存储器地址不存在于所述DRAM高速缓存指示符高速缓存存储器中:

复位对应于所述存储器地址的所述所选择路的所述路编号;及

写入所述路编号到所述主控表。

13. 根据权利要求1所述的DRAM高速缓存管理电路,其经配置以在完全写入模式中操作,且经进一步配置以:

从系统高速缓存存储器接收存储器写入请求,所述存储器写入请求包括写入地址及包括已变更逐出的数据的写入数据;

确定所述写入地址是否在所述DRAM高速缓存存储器中被发现;

响应于确定所述写入地址在所述DRAM高速缓存存储器中未被发现,将所述写入地址及所述已变更逐出的数据概率性地写入到所述DRAM高速缓存存储器;

响应于确定所述写入地址在所述DRAM高速缓存存储器中被发现,将所述已变更逐出的数据写入到所述DRAM高速缓存存储器;及

将所述已变更逐出的数据写入到所述系统存储器DRAM。

14. 根据权利要求13所述的DRAM高速缓存管理电路,其经进一步配置以在确定所述写入地址是否在所述DRAM高速缓存存储器中被发现之前:

确定所述写入地址是否在所述DRAM高速缓存指示符高速缓存存储器中被发现;及

响应于确定所述写入地址在所述DRAM高速缓存指示符高速缓存存储器中未被发现,概率性地补充所述DRAM高速缓存指示符高速缓存存储器;

响应于不补充所述DRAM高速缓存指示符高速缓存存储器:

更新所述主控表中的对应于所述写入地址的DRAM高速缓存指示符;及

将所述已变更逐出的数据写入到所述DRAM高速缓存存储器;

其中所述DRAM高速缓存管理电路经配置以响应于补充所述DRAM高速缓存指示符高速缓存存储器而确定所述写入地址是否在所述DRAM高速缓存存储器中被发现。

15. 根据权利要求13所述的DRAM高速缓存管理电路,其经配置以通过经配置以执行以下操作而将所述写入地址及所述已变更逐出的数据概率性地写入到所述DRAM高速缓存存储器:

选择待从所述DRAM高速缓存存储器逐出的路;

从所述DRAM高速缓存存储器读取所述所选择路的存储器地址;

将所述写入地址及所述已变更逐出的数据写入到所述DRAM高速缓存存储器中的所述所选择路;

将所述DRAM高速缓存指示符高速缓存存储器中的针对所述写入地址的所述路编号更新为所述所选择路的路编号;

确定所述所选择路的所述存储器地址是否存在于所述DRAM高速缓存指示符高速缓存

存储器中;及

响应于确定所述所选择路的所述存储器地址存在于所述DRAM高速缓存指示符高速缓存存储器中,复位所述DRAM高速缓存指示符高速缓存存储器中的针对所述存储器地址的所述所选择路的所述路编号。

16. 根据权利要求15所述的DRAM高速缓存管理电路,其经进一步配置以响应于确定所述所选择路的所述存储器地址不存在于所述DRAM高速缓存指示符高速缓存存储器中,通过经配置以执行以下操作而补充所述DRAM高速缓存指示符高速缓存存储器:

读取对应于所述存储器地址的所述所选择路的主控表项;及

基于所述主控表项将针对所述存储器地址的所述所选择路的所述路编号写入到所述DRAM高速缓存指示符高速缓存存储器。

17. 根据权利要求15所述的DRAM高速缓存管理电路,其经进一步配置以响应于确定所述所选择路的所述存储器地址不存在于所述DRAM高速缓存指示符高速缓存存储器中:

复位对应于所述存储器地址的所述所选择路的所述路编号;及

写入所述路编号到所述主控表。

18. 根据权利要求1所述的DRAM高速缓存管理电路,其经配置以在回写模式中操作,且经进一步配置以:

从系统高速缓存存储器接收存储器写入请求,所述存储器写入请求包括写入地址及包括已变更逐出的数据的写入数据;

确定所述写入地址是否在所述DRAM高速缓存存储器中被发现;

响应于确定所述写入地址在所述DRAM高速缓存存储器中未被发现,将所述写入地址及所述已变更逐出的数据概率性地写入到所述DRAM高速缓存存储器;

响应于未将所述写入地址及所述已变更逐出的数据写入到所述DRAM高速缓存存储器,将所述已变更逐出的数据写入到所述系统存储器DRAM;及

响应于确定所述写入地址在所述DRAM高速缓存存储器中被发现,将所述已变更逐出的数据写入到所述DRAM高速缓存存储器。

19. 根据权利要求18所述的DRAM高速缓存管理电路,其经进一步配置以在确定所述写入地址是否在所述DRAM高速缓存存储器中被发现之前:

确定所述写入地址是否在所述DRAM高速缓存指示符高速缓存存储器中被发现;及

响应于确定所述写入地址在所述DRAM高速缓存指示符高速缓存存储器中未被发现,概率性地补充所述DRAM高速缓存指示符高速缓存存储器;

响应于不补充所述DRAM高速缓存指示符高速缓存存储器:

从所述主控表读取针对所述写入地址的DRAM高速缓存指示符;

将所述已变更逐出的数据写入到所述系统存储器DRAM;及

确定来自所述主控表的针对所述写入地址的所述DRAM高速缓存指示符是否指示所述写入地址是在所述DRAM高速缓存存储器中;

其中所述DRAM高速缓存管理电路经配置以响应于补充所述DRAM高速缓存指示符高速缓存存储器而确定所述写入地址是否在所述DRAM高速缓存存储器中被发现。

20. 根据权利要求18所述的DRAM高速缓存管理电路,其经配置以通过经配置以执行以下操作而将所述写入地址及所述已变更逐出的数据概率性地写入到所述DRAM高速缓存存

储器：

选择待从所述DRAM高速缓存存储器逐出的路；

从所述DRAM高速缓存存储器读取所述所选择路的存储器地址；

在从所述DRAM高速缓存存储器读取所述所选择路的所述存储器地址之后，将所述写入地址及所述已变更逐出的数据写入到所述DRAM高速缓存存储器中的所述所选择路；

将所述DRAM高速缓存指示符高速缓存存储器中的针对所述写入地址的路编号更新为所述所选择路的路编号；

设定所述DRAM高速缓存指示符高速缓存存储器中的针对所述写入地址的已变更指示符；

确定所述所选择路的所述存储器地址是否存在于所述DRAM高速缓存指示符高速缓存存储器中；及

响应于确定所述所选择路的所述存储器地址存在于所述DRAM高速缓存指示符高速缓存存储器中，复位所述DRAM高速缓存指示符高速缓存存储器中针对所述所选择路的所述写入地址的所述路编号及所述已变更指示符。

21. 根据权利要求20所述的DRAM高速缓存管理电路，其经进一步配置以响应于确定所述所选择路的所述存储器地址不存在于所述DRAM高速缓存指示符高速缓存存储器中，通过经配置以执行以下操作而补充所述DRAM高速缓存指示符高速缓存存储器：

读取对应于所述存储器地址的所述所选择路的主控表项；及

基于所述主控表项将针对所述存储器地址的所述所选择路的所述路编号写入到所述DRAM高速缓存指示符高速缓存存储器。

22. 根据权利要求20所述的DRAM高速缓存管理电路，其经进一步配置以响应于确定所述所选择路的所述存储器地址不存在于所述DRAM高速缓存指示符高速缓存存储器中：

复位对应于所述存储器地址的所述所选择路的所述路编号；及

写入所述路编号到所述主控表。

23. 根据权利要求1所述的DRAM高速缓存管理电路，其集成到集成电路IC中。

24. 根据权利要求1所述的DRAM高速缓存管理电路，其集成到选自以下各者组成的群的装置中：机顶盒；娱乐单元；导航装置；通信装置；固定位置数据单元；移动位置数据单元；移动电话；蜂窝式电话；智能型电话；平板电脑；平板手机；计算机；便携式计算机；台式计算机；个人数字助理PDA；监视器；计算机监视器；电视；调谐器；无线电；卫星无线电；音乐播放器；数字音乐播放器；便携式音乐播放器；数字视频播放器；视频播放器；数字视频光盘DVD播放器；便携式数字视频播放器；及汽车。

25. 一种用于提供可扩展动态随机存取存储器DRAM高速缓存管理的方法，其包括：

通过DRAM高速缓存管理电路接收包括读取地址的存储器读取请求；

确定所述读取地址是否在所述DRAM高速缓存管理电路的DRAM高速缓存指示符高速缓存存储器中被发现；

响应于确定所述读取地址在所述DRAM高速缓存指示符高速缓存存储器中未被发现，读取在系统存储器DRAM中的所述读取地址处的数据；及

响应于确定所述读取地址在所述DRAM高速缓存指示符高速缓存存储器中被发现：

基于所述DRAM高速缓存指示符高速缓存存储器确定所述读取地址是否在为高带宽存

储器的部分的DRAM高速缓存存储器中被发现；

响应于确定所述读取地址在所述DRAM高速缓存存储器中未被发现，读取在所述系统存储器DRAM中的所述读取地址处的数据；及

响应于确定所述读取地址在所述DRAM高速缓存存储器中被发现，从所述DRAM高速缓存存储器读取针对所述读取地址的数据。

26. 根据权利要求25所述的方法，其中所述DRAM高速缓存管理电路经配置以在回写模式中操作，且所述方法进一步包括，响应于确定所述读取地址在所述DRAM高速缓存存储器中被发现，确定所述DRAM高速缓存存储器中的针对所述读取地址的所述数据是否为清洁的；

其中从所述DRAM高速缓存存储器读取针对所述读取地址的所述数据是进一步响应于确定所述DRAM高速缓存存储器中的针对所述读取地址的所述数据为不清洁的。

27. 根据权利要求26所述的方法，其进一步包括响应于确定所述DRAM高速缓存存储器中的针对所述读取地址的所述数据为清洁的：

从所述DRAM高速缓存存储器及所述系统存储器DRAM当中识别优选数据源；

响应于将所述DRAM高速缓存存储器识别为所述优选数据源，从所述DRAM高速缓存存储器读取数据；及

响应于将所述系统存储器DRAM识别为所述优选数据源，从所述系统存储器DRAM读取数据。

28. 根据权利要求25所述的方法，其中所述DRAM高速缓存管理电路经配置以在完全写入模式中操作，且其进一步包括响应于确定所述读取地址在所述DRAM高速缓存存储器中被发现：

从所述DRAM高速缓存存储器及所述系统存储器DRAM当中识别优选数据源；及

响应于将所述系统存储器DRAM识别为所述优选数据源，从所述系统存储器DRAM读取数据；

其中从所述DRAM高速缓存存储器读取针对所述读取地址的所述数据进一步是响应于确定所述DRAM高速缓存存储器中的针对所述读取地址的所述数据为清洁的及将所述DRAM高速缓存存储器识别为所述优选数据源。

29. 根据权利要求25所述的方法，其中接收包括所述读取地址的所述存储器读取请求是响应于对系统高速缓存存储器的未命中。

30. 根据权利要求25所述的方法，其进一步包括在读取所述系统存储器DRAM中的所述读取地址处的所述数据之后概率性地补充所述DRAM高速缓存指示符高速缓存存储器。

31. 根据权利要求25所述的方法，其进一步包括基于所述DRAM高速缓存指示符高速缓存存储器通过确定所述DRAM高速缓存存储器中的针对所述读取地址的路编号是否非零而确定所述读取地址是否在所述DRAM高速缓存存储器中被发现。

32. 根据权利要求25所述的方法，其进一步包括：

从系统高速缓存存储器接收存储器写入请求，所述存储器写入请求包括写入地址及包括清洁逐出的数据的写入数据；

确定所述写入地址是否在所述DRAM高速缓存存储器中被发现；及

响应于确定所述写入地址在所述DRAM高速缓存存储器中未被发现，将所述写入地址及

所述清洁逐出的数据概率性地写入到所述DRAM高速缓存存储器。

33. 根据权利要求32所述的方法,其进一步包括在确定所述写入地址是否在所述DRAM高速缓存存储器中被发现之前:

确定所述写入地址是否在所述DRAM高速缓存指示符高速缓存存储器中被发现;及

响应于确定所述写入地址未在所述DRAM高速缓存指示符高速缓存存储器中被发现,概率性地补充所述DRAM高速缓存指示符高速缓存存储器;

其中确定所述写入地址是否在所述DRAM高速缓存存储器中被发现是响应于补充所述DRAM高速缓存指示符高速缓存存储器。

34. 根据权利要求32所述的方法,其包括通过以下操作将所述写入地址及所述清洁逐出的数据概率性地写入到所述DRAM高速缓存存储器:

选择待从所述DRAM高速缓存存储器逐出的路;

从所述DRAM高速缓存存储器读取所述所选择路的存储器地址;

将所述写入地址及所述清洁逐出的数据写入到所述DRAM高速缓存存储器中的所述所选择路;

将所述DRAM高速缓存指示符高速缓存存储器中的针对所述写入地址的路编号更新为所述所选择路的路编号;

确定所述所选择路的所述存储器地址是否存在于所述DRAM高速缓存指示符高速缓存存储器中;及

响应于确定所述所选择路的所述存储器地址存在于所述DRAM高速缓存指示符高速缓存存储器中,复位所述DRAM高速缓存指示符高速缓存存储器中的针对所述存储器地址的所述所选择路的所述路编号。

35. 根据权利要求34所述的方法,其进一步包括响应于确定所述所选择路的所述存储器地址不存在于所述DRAM高速缓存指示符高速缓存存储器中,通过以下操作补充所述DRAM高速缓存指示符高速缓存存储器:

从所述系统存储器DRAM中的主控表读取对应于所述存储器地址的所述所选择路的主控表项;及

基于所述主控表项将针对所述存储器地址的所述所选择路的所述路编号写入到所述DRAM高速缓存指示符高速缓存存储器。

36. 根据权利要求34所述的方法,其进一步包括响应于确定所述所选择路的所述存储器地址不存在于所述DRAM高速缓存指示符高速缓存存储器中:

复位对应于所述存储器地址的所述所选择路的所述路编号;及

将所述路编号写入到所述系统存储器DRAM中的主控表。

37. 根据权利要求25所述的方法,其中所述DRAM高速缓存管理电路经配置以在完全写入模式中操作,且其进一步包括:

从系统高速缓存存储器接收存储器写入请求,所述存储器写入请求包括写入地址及包括已变更逐出的数据的写入数据;

确定所述写入地址是否在所述DRAM高速缓存存储器中被发现;

响应于确定所述写入地址在所述DRAM高速缓存存储器中未被发现,将所述写入地址及所述已变更逐出的数据概率性地写入到所述DRAM高速缓存存储器;

响应于确定所述写入地址在所述DRAM高速缓存存储器中被发现,将所述已变更逐出的数据写入到所述DRAM高速缓存存储器;及

将所述已变更逐出的数据写入到所述系统存储器DRAM。

38.根据权利要求37所述的方法,其进一步包括在确定所述写入地址是否在所述DRAM高速缓存存储器中被发现之前:

确定所述写入地址是否在所述DRAM高速缓存指示符高速缓存存储器中被发现;及

响应于确定所述写入地址在所述DRAM高速缓存指示符高速缓存存储器中未被发现,概率性地补充所述DRAM高速缓存指示符高速缓存存储器;

响应于不补充所述DRAM高速缓存指示符高速缓存存储器:

更新所述系统存储器DRAM中的主控表中的对应于所述写入地址的DRAM高速缓存指示符;及

将所述已变更逐出的数据写入到所述DRAM高速缓存存储器;

其中确定所述写入地址是否在所述DRAM高速缓存存储器中被发现是响应于补充所述DRAM高速缓存指示符高速缓存存储器。

39.根据权利要求37所述的方法,其中将所述写入地址及所述已变更逐出的数据概率性地写入到所述DRAM高速缓存存储器包括:

选择待从所述DRAM高速缓存存储器逐出的路;

从所述DRAM高速缓存存储器读取所述所选择路的存储器地址;

将所述写入地址及所述已变更逐出的数据写入到所述DRAM高速缓存存储器中的所述所选择路;

将所述DRAM高速缓存指示符高速缓存存储器中的针对所述写入地址的路编号更新为所述所选择路的路编号;

确定所述所选择路的所述存储器地址是否存在于所述DRAM高速缓存指示符高速缓存存储器中;及

响应于确定所述所选择路的所述存储器地址存在于所述DRAM高速缓存指示符高速缓存存储器中,复位所述DRAM高速缓存指示符高速缓存存储器中的针对所述存储器地址的所述所选择路的所述路编号。

40.根据权利要求39所述的方法,其进一步包括响应于确定所述所选择路的所述存储器地址不存在于所述DRAM高速缓存指示符高速缓存存储器中,通过以下操作补充所述DRAM高速缓存指示符高速缓存存储器:

读取对应于所述存储器地址的所述所选择路的主控表项;及

基于所述主控表项将针对所述存储器地址的所述所选择路的所述路编号写入到所述DRAM高速缓存指示符高速缓存存储器。

41.根据权利要求39所述的方法,其进一步包括响应于确定所述所选择路的所述存储器地址不存在于所述DRAM高速缓存指示符高速缓存存储器中:

复位对应于所述存储器地址的所述所选择路的所述路编号;及

将所述路编号写入到所述系统存储器DRAM中的主控表。

42.根据权利要求25所述的方法,其中所述DRAM高速缓存管理电路经配置以在回写模式中操作,且所述方法进一步包括:

从系统高速缓存存储器接收存储器写入请求,所述存储器写入请求包括写入地址及包括已变更逐出的数据的写入数据;

确定所述写入地址是否在所述DRAM高速缓存存储器中被发现;

响应于确定所述写入地址未在所述DRAM高速缓存存储器中被发现,将所述写入地址及所述已变更逐出的数据概率性地写入到所述DRAM高速缓存存储器;

响应于未将所述写入地址及所述已变更逐出的数据写入到所述DRAM高速缓存存储器,将所述已变更逐出的数据写入到所述系统存储器DRAM;及

响应于确定所述写入地址在所述DRAM高速缓存存储器中被发现,将所述已变更逐出的数据写入到所述DRAM高速缓存存储器。

43. 根据权利要求42所述的方法,其进一步包括在确定所述写入地址是否在所述DRAM高速缓存存储器中被发现之前:

确定所述写入地址是否在所述DRAM高速缓存指示符高速缓存存储器中被发现;及

响应于确定所述写入地址在所述DRAM高速缓存指示符高速缓存存储器中未被发现,概率性地补充所述DRAM高速缓存指示符高速缓存存储器;

响应于不补充所述DRAM高速缓存指示符高速缓存存储器:

更新所述系统存储器DRAM中的主控表中的对应于所述写入地址的DRAM高速缓存指示符;

将所述已变更逐出的数据写入到所述系统存储器DRAM;及

确定来自所述主控表的针对所述写入地址的所述DRAM高速缓存指示符是否指示所述写入地址是在所述DRAM高速缓存存储器中;

其中确定所述写入地址是否在所述DRAM高速缓存存储器中被发现是响应于补充所述DRAM高速缓存指示符高速缓存存储器。

44. 根据权利要求42所述的方法,其中将所述写入地址及所述已变更逐出的数据概率性地写入到所述DRAM高速缓存存储器包括:

选择待从所述DRAM高速缓存存储器逐出的路;

从所述DRAM高速缓存存储器读取所述所选择路的存储器地址;

在从所述DRAM高速缓存存储器读取所述所选择路的所述存储器地址之后,将所述写入地址及所述已变更逐出的数据写入到所述DRAM高速缓存存储器中的所述所选择路;

将所述DRAM高速缓存指示符高速缓存存储器中的针对所述写入地址的路编号更新为所述所选择路的路编号;

设定所述DRAM高速缓存指示符高速缓存存储器中的针对所述写入地址的已变更指示符;

确定所述所选择路的所述存储器地址是否存在于所述DRAM高速缓存指示符高速缓存存储器中;及

响应于确定所述所选择路的所述存储器地址存在于所述DRAM高速缓存指示符高速缓存存储器中,复位所述DRAM高速缓存指示符高速缓存存储器中针对所述写入地址的所述所选择路的所述路编号及所述已变更指示符。

45. 根据权利要求44所述的方法,其进一步包括响应于确定所述所选择路的所述存储器地址不存在于所述DRAM高速缓存指示符高速缓存存储器中,通过以下操作补充所述DRAM

高速缓存指示符高速缓存存储器：

读取对应于所述存储器地址的所述所选择路的主控表项；及

基于所述主控表项将针对所述存储器地址的所述所选择路的所述路编号写入到所述DRAM高速缓存指示符高速缓存存储器。

46. 根据权利要求44所述的方法，其进一步包括响应于确定所述所选择路的所述存储器地址不存在于所述DRAM高速缓存指示符高速缓存存储器中：

复位对应于所述存储器地址的所述所选择路的所述路编号；及

将所述路编号写入到所述系统存储器DRAM中的主控表。

47. 一种动态随机存取存储器DRAM高速缓存管理电路，其包括：

用于接收包括读取地址的存储器读取请求的装置；

用于确定所述读取地址是否在所述DRAM高速缓存管理电路的DRAM高速缓存指示符高速缓存存储器中被发现的装置；

用于响应于确定所述读取地址在所述DRAM高速缓存指示符高速缓存存储器中未被发现而读取在系统存储器DRAM中的所述读取地址处的数据的装置；

用于响应于确定所述读取地址在所述DRAM高速缓存指示符高速缓存存储器中被发现而基于所述DRAM高速缓存指示符高速缓存存储器确定所述读取地址是否在为高带宽存储器的部分的DRAM高速缓存存储器中被发现的装置；

用于响应于确定所述读取地址在所述DRAM高速缓存存储器中未被发现而读取在所述系统存储器DRAM中的所述读取地址处的数据的装置；及

用于响应于确定所述读取地址在所述DRAM高速缓存存储器中被发现而从所述DRAM高速缓存存储器读取针对所述读取地址的数据的装置。

使用动态随机存取存储器 (DRAM) 高速缓存指示符高速缓存存储器以提供可扩展DRAM高速缓存管理

[0001] 优先权要求

[0002] 本申请案要求2016年2月22日申请且题为“使用动态随机存取存储器 (DRAM) 高速缓存指示符高速缓存存储器以提供可扩展DRAM高速缓存管理 (PROVIDING SCALABLE DYNAMIC RANDOM ACCESS MEMORY (DRAM) CACHE MANAGEMENT USING DRAM CACHE INDICATOR CACHES)”的第62/298,088号美国临时专利申请案的优先权,所述申请案的内容以全文引用的方式并入本文中。

[0003] 本申请案要求2016年8月4日申请且题为“使用动态随机存取存储器 (DRAM) 高速缓存指示符高速缓存存储器以提供可扩展DRAM高速缓存管理 (ROVIDING SCALABLE DYNAMIC RANDOM ACCESS MEMORY (DRAM) CACHE MANAGEMENT USING DRAM CACHE INDICATOR CACHES)”的第15/228,320号美国专利申请案的优先权,所述专利申请案内容以全文引用方式并入本文中。

技术领域

[0004] 本发明的技术大体上涉及动态随机存取存储器 (DRAM) 管理,且详细来说涉及DRAM高速缓存存储器的管理。

背景技术

[0005] 由经垂直互连的多个堆叠裸片构成的裸片堆叠集成电路 (IC) 的出现已使得能够开发裸片堆叠式动态随机存取存储器 (DRAM)。裸片堆叠式DRAM可用于实施本文中称为“高带宽存储器”的存储器。高带宽存储器提供比常规系统存储器DRAM更大的带宽,同时提供类似存取时延。在一些实施方案中,高带宽存储器也可作为“附近”存储器,或相较于其它系统存储器DRAM更接近于存储器接口物理地定位的存储器。高带宽存储器可用于实施DRAM高速缓存存储器以存储先前从系统存储器DRAM读取且从较高级高速缓存存储器 (例如作为非限制性实例的3阶 (L3) 高速缓存存储器) 逐出的经频繁存取的数据。提供高带宽存储器中的DRAM高速缓存存储器可减少系统存储器DRAM上的存储器争用,且因此实际上增加整体存储器带宽。

[0006] 然而,高带宽存储器中的DRAM高速缓存存储器的管理可造成挑战。DRAM高速缓存存储器大小相较于系统存储器DRAM小数个数量级。因此,因为DRAM高速缓存存储器可仅仅存储系统存储器DRAM中的数据子集,所以DRAM高速缓存存储器的有效使用取决于待存储的存储器地址的智能型选择。因此,DRAM高速缓存管理机构应能够确定哪些存储器地址应选择性地安装在DRAM高速缓存存储器中,且应进一步能够确定存储器地址何时应安装在DRAM高速缓存存储器中及/或从DRAM高速缓存存储器中逐出。对于DRAM高速缓存管理机构来说,也可需要最小化对DRAM高速缓存存储器的存取时延的影响,且相对于DRAM高速缓存存储器大小及/或系统存储器DRAM大小可扩展。

[0007] 类似于可管理常规高速缓存存储器的方式,DRAM高速缓存管理的一些方法利用用

于存储对应于经高速缓存存储器地址的标签的高速缓存存储器。根据一种此类方法,与DRAM高速缓存存储器相关联的所有标签存储于计算裸片上与高带宽存储器分离的静态随机存取存储器(SRAM)中。然而,此方法可并非可充分扩展DRAM高速缓存存储器大小,这是由于较大DRAM高速缓存存储器大小可能需要较大区域用于非所需及/或太大以致不能存储于SRAM中的标签。另一方法涉及将标签定位于DRAM高速缓存存储器自身内而非定位于计算裸片上的SRAM内,及使用命中/未命中预测器以确定给定存储器地址是否存储于DRAM高速缓存存储器内。虽然此后一种方法最小化计算裸片中的SRAM的使用量,但任何不正确预测将导致数据从系统存储器DRAM读取。举例来说,如果命中/未命中预测器不正确地预测存储器地址定位于DRAM高速缓存存储器中,那么时延惩罚是由在从系统存储器DRAM读取存储器地址之前对DRAM高速缓存存储器的不必要读取而引发。相反,如果命中/未命中预测器不正确地预测存储器地址并不定位于DRAM高速缓存存储器中,那么避免对系统存储器DRAM的不必要读取的机会可能被浪费。不必要额外读取引发额外存取时延,其可抵消由使用DRAM高速缓存存储器产生的任何性能改进。

[0008] 因此,需要提供可扩展的DRAM高速缓存管理以改进存储器带宽同时最小化SRAM消耗及时延惩罚。

发明内容

[0009] 详细描述中公开的方面包含使用动态随机存取存储器(DRAM)高速缓存指示符高速缓存存储器提供可扩展DRAM高速缓存管理。在一些方面中,提供DRAM高速缓存管理电路以管理对高带宽存储器中的DRAM高速缓存存储器的存取。DRAM高速缓存管理电路包括DRAM高速缓存指示符高速缓存存储器,所述DRAM高速缓存指示符高速缓存存储器用以高速缓存主控表项,所述主控表项含有DRAM高速缓存指示符且从系统存储器DRAM中的主控表予以读取。DRAM高速缓存指示符使得DRAM高速缓存管理电路能够确定系统存储器DRAM中的存储器行是否在DRAM高速缓存存储器中被高速缓存(即,使用高带宽存储器实施),且如果是,那么确定存储器行存储在DRAM高速缓存存储器的哪一路。基于DRAM高速缓存指示符高速缓存存储器,DRAM高速缓存管理电路可确定存储器操作是否可使用DRAM高速缓存存储器及/或使用系统存储器DRAM而执行。DRAM高速缓存管理电路的一些方面可进一步提供负载平衡电路。在数据可从DRAM高速缓存存储器或系统存储器DRAM读取的情形中,DRAM高速缓存管理电路可使用负载平衡电路来选择读取数据所自的适当源。

[0010] DRAM高速缓存管理电路的其它方面可经配置以在完全写入模式或回写中操作。在后一方面中,DRAM高速缓存指示符高速缓存存储器可为存储于其中的每一存储器行提供已变更位。在一些方面中,DRAM高速缓存存储器及/或DRAM高速缓存指示符高速缓存存储器可基于概率性确定而由DRAM高速缓存管理电路来补充。举例来说,DRAM高速缓存管理电路可经配置而以随机间隔补充DRAM高速缓存存储器及/或DRAM高速缓存指示符高速缓存存储器,以使得仅一个百分比的经随机选择的数据被写入到DRAM高速缓存存储器及/或DRAM高速缓存指示符高速缓存存储器。

[0011] 在另一方面中,提供一种DRAM高速缓存管理电路。DRAM高速缓存管理电路以通信方式耦合到为高带宽存储器的部分的DRAM高速缓存存储器,且进一步以通信方式耦合到系统存储器DRAM。DRAM高速缓存管理电路包括经配置以高速缓存从系统存储器DRAM中的主控

表读取的多个DRAM高速缓存指示符的DRAM高速缓存指示符高速缓存存储器。所述多个DRAM高速缓存指示符指示系统存储器DRAM的对应存储器行是否在DRAM高速缓存存储器中被高速缓存。DRAM高速缓存管理电路经配置以接收包括读取地址的存储器读取请求。DRAM高速缓存管理电路经进一步配置以确定读取地址是否是在DRAM高速缓存指示符高速缓存存储器中被发现。DRAM高速缓存管理电路也经配置以响应于确定读取地址在DRAM高速缓存指示符高速缓存存储器中未被发现,读取在系统存储器DRAM中的读取地址处的数据。DRAM高速缓存管理电路另外经配置以响应于确定读取地址在DRAM高速缓存指示符高速缓存存储器中被发现,基于DRAM高速缓存指示符高速缓存存储器而确定读取地址是否在DRAM高速缓存存储器中被发现。DRAM高速缓存管理电路经进一步配置以响应于确定读取地址在DRAM高速缓存存储器中未被发现,读取在系统存储器DRAM中的读取地址处的数据。DRAM高速缓存管理电路也经配置以响应于确定读取地址在DRAM高速缓存存储器中被发现,从DRAM高速缓存存储器读取针对读取地址的数据。

[0012] 在另一方面中,提供一种用于提供可扩展DRAM高速缓存管理的方法。所述方法包括通过DRAM高速缓存管理电路接收包括读取地址的存储器读取请求。所述方法进一步包括确定读取地址是否在DRAM高速缓存管理电路的DRAM高速缓存指示符高速缓存存储器中被发现。所述方法也包括响应于确定读取地址在DRAM高速缓存指示符高速缓存存储器中未被发现,读取在系统存储器DRAM中的读取地址处的数据。所述方法另外包括响应于确定读取地址在DRAM高速缓存指示符高速缓存存储器中被发现,基于DRAM高速缓存指示符高速缓存存储器确定读取地址是否在为高带宽存储器的部分的DRAM高速缓存存储器中被发现。所述方法也包括响应于确定读取地址在DRAM高速缓存存储器中未被发现,读取在系统存储器DRAM中的读取地址处的数据。所述方法另外包括响应于确定读取地址在DRAM高速缓存存储器中被发现,从DRAM高速缓存存储器读取针对读取地址的数据。

[0013] 在另一方面中,提供一种DRAM高速缓存管理电路。DRAM高速缓存管理电路包括用于接收包括读取地址的存储器读取请求的装置。DRAM高速缓存管理电路进一步包括用于确定读取地址是否在DRAM高速缓存管理电路的DRAM高速缓存指示符高速缓存存储器中被发现的装置。DRAM高速缓存管理电路也包括用于响应于确定读取地址在DRAM高速缓存指示符高速缓存存储器中未被发现而读取在系统存储器DRAM中的读取地址处的数据的装置。DRAM高速缓存管理电路另外包括用于响应于确定读取地址在DRAM高速缓存指示符高速缓存存储器中被发现而基于DRAM高速缓存指示符高速缓存存储器确定读取地址是否在为高带宽存储器的部分的DRAM高速缓存存储器中被发现的装置。DRAM高速缓存管理电路进一步包括用于响应于确定读取地址在DRAM高速缓存存储器中未被发现而读取在系统存储器DRAM中的读取地址处的数据的装置。DRAM高速缓存管理电路也包括用于响应于确定读取地址在DRAM高速缓存存储器中被发现而从DRAM高速缓存存储器读取针对读取地址的数据的装置。

[0014] 在另一方面中,提供一种上面存储有计算机可执行指令的非暂时性计算机可读媒体。当通过处理器执行时,所述计算机可执行指令使得所述处理器接收包括读取地址的存储器读取请求。所述计算机可执行指令进一步使得处理器确定读取地址是否在DRAM高速缓存管理电路的DRAM高速缓存指示符高速缓存存储器中被发现。所述计算机可执行指令也使得处理器响应于确定读取地址在DRAM高速缓存指示符高速缓存存储器中未被发现而读取在系统存储器DRAM中的读取地址处的数据。所述计算机可执行指令另外使得处理器响应于

确定读取地址在DRAM高速缓存指示符高速缓存存储器中被发现而基于DRAM高速缓存指示符高速缓存存储器确定读取地址是否在为高带宽存储器的部分的DRAM高速缓存存储器中被发现。所述计算机可执行指令进一步使得处理器响应于确定读取地址未在DRAM高速缓存存储器中被发现而读取在系统存储器DRAM中的读取地址处的数据。所述计算机可执行指令也使得处理器响应于确定读取地址在DRAM高速缓存存储器中被发现而从DRAM高速缓存存储器读取针对读取地址的数据。

附图说明

[0015] 图1为基于处理器的系统的框图,所述基于处理器的系统包含提供动态随机存取存储器 (DRAM) 高速缓存存储器的高带宽存储器,及用于使用DRAM高速缓存指示符高速缓存存储器以提供可扩展DRAM高速缓存管理的示范性DRAM高速缓存管理电路;

[0016] 图2A到2B为说明用于可由图1的DRAM高速缓存管理电路管理的两个示范性DRAM高速缓存存储器的示范性主控表项及DRAM高速缓存指示符高速缓存内容的框图;

[0017] 图3为说明用于使用图1的DRAM高速缓存指示符高速缓存存储器及DRAM高速缓存存储器来执行读取操作的图1的DRAM高速缓存管理电路的示范性操作的流程图;

[0018] 图4A到4C为说明用于在完全写入模式或回写模式中执行由“清洁”(即,未经修改)数据从3阶 (L3) 高速缓存存储器逐出产生的写入操作的图1的DRAM高速缓存管理电路的示范性操作的流程图;

[0019] 图5A到5C为说明用于在完全写入模式中执行由“已变更”(即,经修改)数据从L3高速缓存存储器逐出产生的写入操作的图1的DRAM高速缓存管理电路的示范性操作的流程图;

[0020] 图6A到6D为说明用于在回写模式中执行由已变更数据从L3高速缓存存储器逐出产生的写入操作的图1的DRAM高速缓存管理电路的示范性操作的流程图;且

[0021] 图7为可包含图1的DRAM高速缓存管理电路的示范性基于处理器的系统的框图。

具体实施方式

[0022] 现在参考图式,描述本发明的若干示范性方面。词语“示范性”在本文中用以意谓“充当实例、例项或说明”。不必将本文中描述为“示范性”的任何方面解译为优选或优于其它方面。

[0023] 详细描述中公开的方面包含使用动态随机存取存储器 (DRAM) 高速缓存指示符高速缓存存储器提供可扩展DRAM高速缓存管理。如本文中所描述,DRAM高速缓存管理方案在由DRAM高速缓存管理方案利用的资源的大小相对独立于被管理的DRAM高速缓存存储器的容量的意义上为“可扩展的”。因此,就此来说,图1为示范性基于处理器的系统100的框图,所述基于处理器的系统100提供用于管理为高带宽存储器106的部分的DRAM高速缓存存储器104的DRAM高速缓存管理电路102。基于处理器的系统100包含系统存储器DRAM 108,其在一些方面中可包括一或多个双行存储器模块 (DIMM) (未图示)。基于处理器的系统100进一步提供计算裸片110,系统高速缓存存储器112(作为非限制性实例例如3阶 (L3) 高速缓存存储器) 定位于所述计算裸片上。基于处理器的系统100可涵盖已知数字逻辑元件、半导体电路、处理核心及/或存储器结构以及其它元件或其组合中的任一者。本文中所描述的方面并

不约束于元件的任何特定布置,且所公开技术可易于扩展到半导体裸片或封装上的各种结构及布局。应理解,基于处理器的系统100的一些方面可包含除图1中所说明的那些元件以外的元件。

[0024] 为改进存储器带宽,基于处理器的系统100的高带宽存储器106内的DRAM高速缓存存储器104可用于高速缓存先前从系统存储器DRAM 108内的存储器行114 (0) 到114 (X) 读取及/或从系统高速缓存存储器112逐出的存储器地址 (未图示) 及数据 (未图示)。作为非限制性实例,一些方面可规定仅仅在从系统存储器DRAM 108读取数据后才可在DRAM高速缓存存储器104中高速缓存数据,而在一些方面中数据可仅仅在从系统高速缓存存储器112逐出时才在DRAM高速缓存存储器104中被高速缓存。根据一些方面,对于由处理器载入及来自系统高速缓存存储器112的已变更逐出所触发的读取,在从系统存储器DRAM 108读取数据后可在DRAM高速缓存存储器104中高速缓存数据。

[0025] 高带宽存储器106内的DRAM高速缓存存储器104可独立于系统存储器DRAM 108及与系统存储器DRAM 108并行地存取。因此,存储器带宽可通过同时从DRAM高速缓存存储器104及系统存储器DRAM 108两者读取而有效增加。在一些方面中,DRAM高速缓存存储器104可实施随机替换策略以确定DRAM高速缓存存储器104内的逐出的候选者。

[0026] 存储在系统存储器DRAM 108中的主控表116用以跟踪系统存储器DRAM 108的哪些存储器行114 (0) 到114 (X) 存储于DRAM高速缓存存储器104中。应理解,如本文中所使用,系统存储器DRAM 108的“存储器行”指系统存储器DRAM 108的具有等于系统高速缓存存储器112的高速缓存行 (未图示) 的长度的长度的一部分。主控表116含有用于存储针对系统存储器DRAM 108的存储器行114 (0) 到114 (X) 中的每一者的DRAM高速缓存指示符120 (0) 到120 (X) 的主控表项118 (0) 到118 (M)。一些方面可规定,主控表项118 (0) 到118 (M) 中的每一者的大小对应于底层存储器的存储器存取粒度。作为非限制性实例,对于64个字节的存储器存取粒度,主控表项118 (0) 到118 (M) 中的每一者同样包括64个字节。因此,在DRAM高速缓存指示符120 (0) 到120 (X) 中的每一者包括四 (4) 个位的方面中,主控表116的64字节主控表项118 (0) 到118 (M) 中的每一者可存储针对系统存储器DRAM 108的128个存储器行114 (0) 到114 (X) 的DRAM高速缓存指示符120 (0) 到120 (X)。

[0027] 在一些方面中,主控表116中的DRAM高速缓存指示符120 (0) 到120 (X) 中的每一者不仅指示系统存储器DRAM 108的对应存储器行114 (0) 到114 (X) 是否存储于高带宽存储器106的DRAM高速缓存存储器104中,而且指示对应存储器行114 (0) 到114 (X) 存储于DRAM高速缓存存储器104的哪一路122 (0) 到122 (Z) 中。举例来说,在一些方面中,DRAM高速缓存指示符120 (0) 到120 (X) 中的每一者包括四 (4) 个位,且DRAM高速缓存存储器104可提供15个路122 (0) 到122 (14) (即, 2^4-1)。具有零 (0) 值的DRAM高速缓存指示符120 (0) 到120 (X) 指示系统存储器DRAM 108的对应存储器行114 (0) 到114 (X) 不存储于DRAM高速缓存存储器104中。具有大于零 (0) 的值N的DRAM高速缓存指示符120 (0) 到120 (X) 指示系统存储器DRAM 108的对应存储器行114 (0) 到114 (X) 于路122 (N-1) 中存储于DRAM高速缓存存储器104中,其中 $0 \leq N-1 \leq Z$ 。

[0028] 应理解,在一些方面中,主控表116的主控表项118 (0) 到118 (M) 可根据由DRAM高速缓存存储器104提供的路122 (0) 到122 (Z) 的数目提供大于或小于四个 (4) 位的DRAM高速缓存指示符120 (0) 到120 (X)。作为非限制性实例,对于每一DRAM高速缓存指示符120 (0) 到120

(X) 中的位的编号Q, DRAM高速缓存存储器104可提供某数目个路122 (0) 到122 (Z), 其中 $Z = 2^Q - 1$ 。因此, 包括两 (2) 个位的DRAM高速缓存指示符120 (0) 到120 (X) 对应于经组织成三 (3) 路122 (0) 到122 (2) 的DRAM高速缓存存储器104, 而包括三 (3) 位的DRAM高速缓存指示符120 (0) 到120 (X) 对应于提供七 (7) 路122 (0) 到122 (6) 的DRAM高速缓存存储器104。下文关于图2A及2B更详细地论述DRAM高速缓存指示符120 (0) 到120 (X) 及DRAM高速缓存存储器104的不同配置。

[0029] 因为主控表116的主控表项118 (0) 到118 (M) 存储针对系统存储器DRAM 108中的每一存储器行114 (0) 到114 (X) 的DRAM高速缓存指示符120 (0) 到120 (X), 所以主控表116的大小随着系统存储器DRAM 108的大小增加而增加。举例来说, 在主控表116内的DRAM高速缓存指示符120 (0) 到120 (X) 各自为四 (4) 位的方面中, 主控表116的总大小为系统存储器DRAM 108的大小的0.4%。因此, 存取用于每一存储器操作的主控表116可引发可补偿使用DRAM高速缓存存储器104的性能益处的时延惩罚。因此, 需要提供可扩展机构以用于管理对DRAM高速缓存存储器104的存取以改进存储器带宽同时最小化时延惩罚。

[0030] 就此来说, DRAM高速缓存管理电路102经提供以管理对DRAM高速缓存存储器104的存取。DRAM高速缓存管理电路102定位于计算裸片110上, 且以通信方式耦合到高带宽存储器106及系统存储器DRAM 108。也可由系统高速缓存存储器112从DRAM高速缓存管理电路102进行读取, 并由系统高速缓存存储器112对DRAM高速缓存管理电路102进行写入。如下文更详细地论述, DRAM高速缓存管理电路102可响应于接收到包括读取地址126的存储器读取请求124而执行存储器读取操作, 所述读取地址指定检索数据所自的存储器地址。在一些方面中, DRAM高速缓存管理电路102可响应于接收到存储器写入请求128而进一步执行存储器写入操作, 所述存储器写入请求包括写入数据132将写入到的写入地址130。

[0031] 为减少可由对主控表116的存取引起的存取时延, DRAM高速缓存管理电路102提供DRAM高速缓存指示符高速缓存存储器134。DRAM高速缓存指示符高速缓存存储器134由DRAM高速缓存管理电路102使用以在DRAM高速缓存指示符高速缓存行138 (0) 到138 (Y) 的路136 (0) 到136 (C)、136' (0) 到136' (C) 内高速缓存经频繁存取的主控表项118 (0) 到118 (M) (及存储于其中的DRAM高速缓存指示符120 (0) 到120 (X))。在一些方面中, DRAM高速缓存指示符高速缓存存储器134的路136 (0) 到136 (C)、136' (0) 到136' (C) 中的每一者的大小对应于主控表116中的主控表项118 (0) 到118 (M) 的大小。一些方面可规定DRAM高速缓存指示符高速缓存存储器134的路136 (0) 到136 (C)、136' (0) 到136' (C) 中的每一者的大小可大于主控表116中的主控表项118 (0) 到118 (M) 的大小。作为非限制性实例, DRAM高速缓存指示符高速缓存存储器134的路136 (0) 到136 (C)、136' (0) 到136' (C) 可包含已变更指示符140 (0) 到140 (C)、140' (0) 到140' (C), 其每一路136 (0) 到136 (C)、136' (0) 到136' (C) 添加一 (1) 个位。因此, 在路136 (0) 到136 (C)、136' (0) 到136' (C) 在每一DRAM高速缓存指示符120 (0) 到120 (X) 四 (4) 个位的情况下大小为64个字节的方面中, 可需要总共128个额外位以提供已变更指示符140 (0) 到140 (C)、140' (0) 到140' (C)。

[0032] DRAM高速缓存管理电路102的一些方面可进一步提供负载平衡电路142以改进存储器带宽并减少存储器存取争用。在可从系统存储器DRAM 108或DRAM高速缓存存储器104读取经请求存储器地址的情形中, 负载平衡电路142识别读取存储器地址所自的最适当源。举例来说, 在一些方面中, 负载平衡电路142可监视从DRAM高速缓存存储器104及系统存储

器DRAM 108的读取的时延,并可选择最近具有较好平均时延的源。以此方式,负载平衡电路142可在系统存储器DRAM 108与DRAM高速缓存存储器104之间分配存储器存取以优化系统资源的使用。

[0033] 在一些方面中,DRAM高速缓存管理电路102可经实施为“完全写入”高速缓存管理系统。在完全写入实施方案中,从系统高速缓存存储器112逐出的已变更(即,经修改)数据通过DRAM高速缓存管理电路102写入到高带宽存储器106的DRAM高速缓存存储器104及系统存储器DRAM 108两者。因此,DRAM高速缓存存储器104内的数据及系统存储器DRAM 108内的数据始终经同步。因为在完全写入实施方案中的DRAM高速缓存存储器104及系统存储器DRAM 108两者被确保含有正确数据,所以DRAM高速缓存管理电路102的负载平衡电路142可自由地负载平衡DRAM高速缓存存储器104与系统存储器DRAM 108之间的存储器读取操作。然而,DRAM高速缓存管理电路102的完全写入实施方案可不导致系统存储器DRAM 108的减少的写入带宽,此是由于对DRAM高速缓存存储器104的每一写入将对应于对系统存储器DRAM 108的写入。

[0034] DRAM高速缓存管理电路102的一些方面可经实施为“回写”高速缓存管理系统,其中DRAM高速缓存管理电路102的DRAM高速缓存指示符高速缓存存储器134包含用于其中的每一路136 (0) 到136 (C)、136' (0) 到136' (C) 的已变更指示符140 (0) 到140 (C)、140' (0) 到140' (C)。已变更指示符140 (0) 到140 (C)、140' (0) 到140' (C) 中的每一者指示存储于对应于DRAM高速缓存指示符高速缓存存储器134内的路136 (0) 到136 (C)、136' (0) 到136' (C) 的DRAM高速缓存存储器104中的数据是否为已变更(即,数据是否被写入到DRAM高速缓存存储器104但并未写入到系统存储器DRAM 108)。如果数据并非为已变更的,那么数据可从DRAM高速缓存存储器104或系统存储器DRAM 108读取,如由DRAM高速缓存管理电路102的负载平衡电路142所确定。然而,如果已变更指示符140 (0) 到140 (C)、140' (0) 到140' (C) 指示存储于DRAM高速缓存存储器104中的数据为已变更的,那么负载平衡为不可能的,此是由于DRAM高速缓存存储器104为经修改数据的唯一源。因此,DRAM高速缓存管理电路102从DRAM高速缓存存储器104读取已变更数据。

[0035] DRAM高速缓存管理电路102的回写实施方案可减少系统存储器DRAM 108的存储器写入带宽消耗,但DRAM高速缓存管理电路102最终必须将从DRAM高速缓存存储器104逐出的已变更数据回写到系统存储器DRAM 108。在DRAM高速缓存管理电路102的回写实施方案的一些方面中,当DRAM高速缓存指示符高速缓存行138 (0) 到138 (Y) 从DRAM高速缓存指示符高速缓存存储器134逐出时,DRAM高速缓存管理电路102经配置以将DRAM高速缓存存储器104中的对应于经逐出DRAM高速缓存指示符高速缓存行138 (0) 到138 (Y) 的所有已变更数据复制到系统存储器DRAM 108。

[0036] DRAM高速缓存管理电路102的一些方面可根据通过DRAM高速缓存管理电路102进行的对应概率确定通过执行一些操作(例如,作为非限制性实例,涉及对系统存储器DRAM 108及/或DRAM高速缓存存储器104的存储器存取的操作)而进一步改进存储器带宽。每一概率确定可用于调谐对应操作的频率,且可为无状态的(即,与先前概率确定的结果不相关)。举例来说,根据DRAM高速缓存管理电路102的一些方面,由系统高速缓存存储器112逐出的数据可基于概率确定而写入到DRAM高速缓存存储器104,以使得通过系统高速缓存存储器112逐出的仅仅一个百分比经随机选择数据写入到DRAM高速缓存存储器104。类似地,DRAM

高速缓存管理电路102的一些方面可经配置以基于概率确定补充DRAM高速缓存指示符高速缓存存储器134 (例如,通过将读取数据的主控表项118 (0) 到118 (M) 从主控表116复制到DRAM高速缓存指示符高速缓存存储器134)。因此,应理解,本文中描述为“概率性地”发生的每一操作在给定例项中可能执行或可能不执行,且进一步理解其给定概率操作的发生或缺少可通过DRAM高速缓存管理电路102进一步触发额外操作。

[0037] 为说明图1的DRAM高速缓存存储器104的一些实施方案的示范性主控表项118 (0) 到118 (M) 及DRAM高速缓存指示符120 (0) 到120 (X) 内容,提供图2A到2B。图2A说明包括15路的DRAM高速缓存存储器104的实施方案,而图2B说明包括三 (3) 路的DRAM高速缓存存储器104的实施方案。为清楚起见,在描述图2A及2B时参考图1的元件。

[0038] 在图2A中,说明具有64个字节的的大小的示范性主控表项200 (其可对应于图1的主控表项118 (0) 到118 (M) 中的一者)。主控表项200包含DRAM高速缓存指示符202 (0) 到202 (127) (对应于图1的DRAM高速缓存指示符120 (0) 到120 (X)), 其每一者大小为四 (4) 个位。因此,主控表项200存储针对系统存储器DRAM 108的128个存储器行114 (0) 到114 (X) 的DRAM高速缓存指示符202 (0) 到202 (127)。为了高速缓存DRAM高速缓存指示符202 (0) 到202 (127), DRAM高速缓存指示符高速缓存存储器134提供DRAM高速缓存指示符高速缓存行204 (0) 到204 (511) (对应于图1的DRAM高速缓存指示符高速缓存行138 (0) 到138 (Y))。DRAM高速缓存指示符高速缓存行204 (0) 到204 (511) 中的每一者由八 (8) 路 (例如,分别为DRAM高速缓存指示符高速缓存行204 (0)、204 (511) 的路206 (0) 到206 (7)、208 (0) 到208 (7)) 构成。路206 (0) 到206 (7)、208 (0) 到208 (7) 中的每一者对应于图1的路136 (0) 到136 (C)、136' (0) 到136' (C), 且可存储一 (1) 个主控表项,例如主控表项200。

[0039] 现参看图2B,展示具有64字节的主控表项210。在图2B的实例中,主控表项210包含DRAM高速缓存指示符212 (0) 到212 (255), 其每一者大小为两个 (2) 位。因此,主控表项210存储针对系统存储器DRAM 108的256个存储器行的DRAM高速缓存指示符212 (0) 到212 (255)。在此实例中的DRAM高速缓存指示符高速缓存存储器134提供DRAM高速缓存指示符高速缓存行214 (0) 到214 (511) 以高速缓存DRAM高速缓存指示符212 (0) 到212 (255)。DRAM高速缓存指示符高速缓存行214 (0) 到214 (511) 中的每一者由八 (8) 路 (例如,分别为DRAM高速缓存指示符高速缓存行214 (0)、214 (511) 的路216 (0) 到216 (7)、218 (0) 到218 (7)) 构成。路216 (0) 到216 (7)、218 (0) 到218 (7) 中的每一者可存储一 (1) 个主控表项,例如主控表项210。

[0040] 图3为说明用于使用图1的DRAM高速缓存指示符高速缓存存储器134及DRAM高速缓存存储器104来执行读取操作的图1的DRAM高速缓存管理电路102的示范性操作的流程图。为清楚起见,在描述图3时参考图1的元件。在图3中,操作以DRAM高速缓存管理电路102接收包括读取地址126的存储器读取请求124 (例如,由于系统高速缓存存储器112上的未命中) 开始 (块300)。因此,DRAM高速缓存管理电路102可在本文中称为“用于接收包括读取地址的存储器读取请求的装置”。DRAM高速缓存管理电路102确定读取地址126是否在DRAM高速缓存管理电路102的DRAM高速缓存指示符高速缓存存储器134中被发现 (块302)。DRAM高速缓存管理电路102因此可在本文中称为“用于确定读取地址是否在DRAM高速缓存管理电路的DRAM高速缓存指示符高速缓存存储器中被发现的装置”。

[0041] 如果存储器读取请求124的读取地址126在DRAM高速缓存指示符高速缓存存储器134中未被发现,那么DRAM高速缓存管理电路102读取在系统存储器DRAM 108中的读取地址

126处的数据(块304)。就此来说,DRAM高速缓存管理电路102可在本文中称为“用于响应于确定读取地址在DRAM高速缓存指示符高速缓存存储器中未被发现而读取在系统存储器DRAM中的读取地址处的数据的装置”。与对读取地址126处的数据进行读取并行地,DRAM高速缓存管理电路102的一些方面可概率性地补充DRAM高速缓存指示符高速缓存存储器134(块306)。通过补充DRAM高速缓存指示符高速缓存存储器134,后续读取(其可在空间上邻近于读取数据)将引起DRAM高速缓存指示符高速缓存存储器134命中的似然度可得以增加。

[0042] 作为非限制性实例,在一些方面中,概率性地补充DRAM高速缓存指示符高速缓存存储器134可包含将所读取数据的主控表项118(0)到118(M)从主控表116复制到DRAM高速缓存指示符高速缓存存储器134。一些方面可规定,用于补充DRAM高速缓存指示符高速缓存存储器134的块306的操作可包含从系统存储器DRAM 108中的主控表116跨越读取地址126读取主控表项118(0)到118(M)。主控表项118(0)到118(M)接着安装于DRAM高速缓存指示符高速缓存存储器134中。如果主控表项118(0)到118(M)的安装使得路136(0)到136(C)、136'(0)到136'(C)中的一者从DRAM高速缓存指示符高速缓存存储器134逐出,那么经逐出路136(0)到136(C)、136'(0)到136'(C)的内容(不具有可能存在的任何已变更指示符140(0)到140(C)、140'(0)到140'(C))经写入到系统存储器DRAM 108中的主控表116。在DRAM高速缓存管理电路102经配置以在回写模式中操作的方面中,由经逐出路136(0)到136(C)、136'(0)到136'(C)指示的任何已变更DRAM高速缓存行也从DRAM高速缓存存储器104复制到系统存储器DRAM 108。

[0043] 如果DRAM高速缓存管理电路102在决定块302处确定读取地址126在DRAM高速缓存指示符高速缓存存储器134中被发现,那么DRAM高速缓存管理电路102接下来基于DRAM高速缓存指示符高速缓存存储器134确定读取地址126是否在为高带宽存储器的部分的DRAM高速缓存存储器104中被发现(块308)。因此,DRAM高速缓存管理电路102可在本文中称为“用于响应于确定读取地址在DRAM高速缓存指示符高速缓存存储器中被发现而基于DRAM高速缓存指示符高速缓存存储器确定读取地址是否在为高带宽存储器的部分的DRAM高速缓存存储器中被发现的装置”。在一些方面中,确定读取地址126是否在DRAM高速缓存存储器104中被发现可包含确定DRAM高速缓存指示符高速缓存存储器134中的用于读取地址126的路编号是否为非零。如果是,那么读取地址126是在DRAM高速缓存存储器104中。否则,如果DRAM高速缓存指示符高速缓存存储器134中的用于读取地址126的路编号为零(0),那么读取地址126不在DRAM高速缓存存储器104中。

[0044] 如果读取地址126在DRAM高速缓存存储器104中未被发现,那么DRAM高速缓存管理电路102读取在系统存储器DRAM 108中的读取地址126处的数据(块310)。DRAM高速缓存管理电路102因此可在本文中称为“用于响应于确定读取地址在DRAM高速缓存存储器中未被发现而读取在系统存储器DRAM中的读取地址处的数据的装置”。然而,如果DRAM高速缓存管理电路102在决定块308处确定读取地址126在DRAM高速缓存存储器104中被发现,那么DRAM高速缓存管理电路102在一些方面中确定DRAM高速缓存存储器104中的针对读取地址126的数据是否清洁(或替代地,DRAM高速缓存管理电路102是否经配置以在完全写入模式中操作)(块312)。如果DRAM高速缓存存储器104中的数据不清洁及/或DRAM高速缓存管理电路102并非在完全写入模式中操作,那么经请求数据可仅仅从DRAM高速缓存存储器104被安全地读取。因此,DRAM高速缓存管理电路102从DRAM高速缓存存储器104读取针对读取地址126

的数据(块314)。就此来说,DRAM高速缓存管理电路102可在本文中称为“用于响应于确定读取地址在DRAM高速缓存存储器中被发现而从DRAM高速缓存存储器读取针对读取地址的数据的装置”。

[0045] 如果DRAM高速缓存管理电路102在决定块312处确定DRAM高速缓存存储器104中的数据为清洁的及/或DRAM高速缓存管理电路102在完全写入模式中操作,那么经请求数据可从系统存储器DRAM 108或DRAM高速缓存存储器104被安全地读取。因此,作为非限制性实例,DRAM高速缓存管理电路102的负载平衡电路142基于负载平衡准则(例如带宽及时延)从DRAM高速缓存存储器104及系统存储器DRAM 108当中识别优选数据源(块316)。如果负载平衡电路142确定系统存储器DRAM 108为优选数据源,那么读取地址126处的数据可从系统存储器DRAM 108读取(块318)。类似地,如果负载平衡电路142确定DRAM高速缓存存储器104为优选数据源,那么针对读取地址126的数据可从DRAM高速缓存存储器104读取(块320)。

[0046] 为了说明图1的DRAM高速缓存管理电路102的用于在完全写入模式中或在回写模式中执行由清洁(即,未经修改)数据从系统高速缓存存储器112的逐出引起的写入操作的示范性操作,提供图4A到4C。为清楚起见,在描述图4A到4C时参考图1的元件。图4A中的操作以DRAM高速缓存管理电路102接收包括写入地址130及写入数据132的存储器写入请求128(块400)开始。在此实例中,写入数据132表示从系统高速缓存存储器112逐出的清洁(即,未经修改)数据,且因此在本文中称为“清洁逐出的数据132”。

[0047] DRAM高速缓存管理电路102确定清洁逐出的数据132的写入地址130是否在DRAM高速缓存指示符高速缓存存储器134中被发现(块402)。如果写入地址130不存在于DRAM高速缓存指示符高速缓存存储器134中,那么DRAM高速缓存管理电路102概率性地补充DRAM高速缓存指示符高速缓存存储器134(例如,通过将主控表项118(O)到118(M)从主控表116复制到DRAM高速缓存指示符高速缓存存储器134)(块404)。如果DRAM高速缓存指示符高速缓存存储器134在块404处不予以补充(即,补充经概率性地确定为不发生),那么处理完成(块406)。否则,DRAM高速缓存管理电路102在块408处恢复处理。

[0048] 如果DRAM高速缓存管理电路102在决定块402处确定清洁逐出的数据132的写入地址130存在于DRAM高速缓存指示符高速缓存存储器134中(或如果在块404处补充DRAM高速缓存指示符高速缓存存储器134),那么DRAM高速缓存管理电路102接下来确定清洁逐出的数据132的写入地址130存在于DRAM高速缓存存储器104中(块408)。如果写入地址130存在于DRAM高速缓存存储器104中,那么处理完成(块406)。然而,如果清洁逐出的数据132的写入地址130不存在于DRAM高速缓存存储器104中,那么处理在图4B的块410处恢复。

[0049] 现参看图4B,DRAM高速缓存管理电路102接下来将写入地址130及清洁逐出的数据132概率性地写入到DRAM高速缓存存储器104(块410)。在一些方面中,用于将写入地址130及清洁逐出的数据132写入到DRAM高速缓存存储器104的块410的操作可包含首先随机地选择待从DRAM高速缓存存储器104逐出的路122(O)到122(Z)(块412)。DRAM高速缓存管理电路102从DRAM高速缓存存储器104读取所选择路122(O)到122(Z)的存储器地址(块414)。DRAM高速缓存管理电路102接着将写入地址130及清洁逐出的数据132写入到DRAM高速缓存存储器104中的所选择路122(O)到122(Z)(块416)。DRAM高速缓存管理电路102将DRAM高速缓存指示符高速缓存存储器134中的用于写入地址130的路编号更新为所选择路122(O)到122(Z)的路编号(块418)。处理接着在图4C的块420处继续。

[0050] 转到图4C,用于将写入地址130及清洁逐出的数据132概率性地写入到DRAM高速缓存存储器104的块410的其它操作包含DRAM高速缓存管理电路102确定所选择路122 (0) 到122 (Z) 的存储器地址是否存在于DRAM高速缓存指示符高速缓存存储器134中(块420)。如果不存在,那么处理在图4C的块424处恢复。如果DRAM高速缓存管理电路102在决定块420处确定所选择路122 (0) 到122 (Z) 的存储器地址存在于DRAM高速缓存指示符高速缓存存储器134中,那么DRAM高速缓存管理电路102复位DRAM高速缓存指示符高速缓存存储器134中的针对存储器地址的所选择路122 (0) 到122 (Z) 的路编号(块422)。

[0051] 如果DRAM高速缓存管理电路102在决定块420处确定所选择路122 (0) 到122 (Z) 的存储器地址不存在于DRAM高速缓存指示符高速缓存存储器134中,那么DRAM高速缓存管理电路102补充DRAM高速缓存指示符高速缓存存储器134(块424)。在一些方面中,用于补充DRAM高速缓存指示符高速缓存存储器134的块424的操作包含从系统存储器DRAM 108中的主控表116读取对应于存储器地址的所选择路122 (0) 到122 (Z) 的主控表项118 (0) 到118 (M) (块426)。DRAM高速缓存管理电路102在一些方面中可接下来基于主控表项118 (0) 到118 (M) 将针对存储器地址的所选择路122 (0) 到122 (Z) 的路编号写入到DRAM高速缓存指示符高速缓存存储器134(块428)。在一些方面中,DRAM高速缓存管理电路102复位对应于存储器地址的所选择路122 (0) 到122 (Z) 的路编号(块430)。DRAM高速缓存管理电路102接着将路编号写入到系统存储器DRAM 108中的主控表116(而不需将主控表项118 (0) 到118 (M) 安装于DRAM高速缓存指示符高速缓存存储器134中)(块432)。

[0052] 图5A到5C经提供以说明用于在完全写入模式中执行由已变更数据从系统高速缓存存储器112逐出引起的写入操作的图1的DRAM高速缓存管理电路102的示范性操作。为清楚起见,在描述图5A到5C时参考图1的元件。在图5A中,操作以DRAM高速缓存管理电路102接收包括写入地址130及写入数据132的存储器写入请求128(块500)开始。图5A的实例中的写入数据132表示从系统高速缓存存储器112逐出的已变更(即,经修改)数据,且因此在本文中称为“已变更逐出的数据132”。

[0053] DRAM高速缓存管理电路102确定已变更逐出的数据132的写入地址130是否在DRAM高速缓存指示符高速缓存存储器134中被发现(块502)。如果写入地址130不存在于DRAM高速缓存指示符高速缓存存储器134中,那么DRAM高速缓存管理电路102概率性地补充DRAM高速缓存指示符高速缓存存储器134(作为非限制性实例,通过将主控表项118 (0) 到118 (M) 从主控表116复制到DRAM高速缓存指示符高速缓存存储器134)(块504)。如果DRAM高速缓存指示符高速缓存存储器134在块504处予以补充(即,补充经概率性地确定为发生),那么处理在块506处恢复。否则,DRAM高速缓存管理电路102在系统存储器DRAM 108中的主控表116中更新对应于写入地址130的DRAM高速缓存指示符120 (0) 到120 (X) (例如,通过对针对DRAM高速缓存指示符120 (0) 到120 (X) 的主控表项118 (0) 到118 (M) 执行读取-修改-写入(RMW)操作)(块508)。DRAM高速缓存管理电路102接着将已变更逐出的数据132写入到DRAM高速缓存存储器104(块510)。应理解,在一些方面中,用于更新DRAM高速缓存指示符120 (0) 到120 (X) 的块508的操作及用于将已变更逐出的数据132写入到DRAM高速缓存存储器104的块510的操作可经并行进行。

[0054] 如果DRAM高速缓存管理电路102在决定块502处确定已变更逐出的数据132的写入地址130在DRAM高速缓存指示符高速缓存存储器134中被发现(或如果在块504处补充DRAM

高速缓存指示符高速缓存存储器134),那么DRAM高速缓存管理电路102接下来确定已变更逐出的数据132的写入地址130是否在DRAM高速缓存存储器104中被发现(块506)。如果写入地址130未在DRAM高速缓存存储器104中被发现,那么处理在图5B的块512处恢复。然而,如果DRAM高速缓存管理电路102在决定块506处确定写入地址130在DRAM高速缓存存储器104中被发现,那么DRAM高速缓存管理电路102将已变更逐出的数据132写入到DRAM高速缓存存储器104(例如,通过对DRAM高速缓存存储器104执行非-逐出-写入)(块514)。DRAM高速缓存管理电路102接着将已变更逐出的数据132写入到系统存储器DRAM 108(块516)。

[0055] 转到图5B,DRAM高速缓存管理电路102接下来将写入地址130及已变更逐出的数据132概率性地写入到DRAM高速缓存存储器104(块512)。一些方面可规定用于将写入地址130及已变更逐出的数据132写入到DRAM高速缓存存储器104的块512的操作可包含首先随机地选择待从DRAM高速缓存存储器104逐出的路122(0)到122(Z)(块518)。通过DRAM高速缓存管理电路102从DRAM高速缓存存储器104读取所选择路122(0)到122(Z)的存储器地址(块520)。DRAM高速缓存管理电路102接着将写入地址130及已变更逐出的数据132写入到DRAM高速缓存存储器104中的所选择路122(0)到122(Z)(块522)。DRAM高速缓存管理电路102将DRAM高速缓存指示符高速缓存存储器134中的用于写入地址130的路编号更新为所选择路122(0)到122(Z)的路编号(块524)。处理接着在图5C的块526处继续。

[0056] 现参看图5C,用于将写入地址130及已变更逐出的数据132概率性地写入到DRAM高速缓存存储器104的块512的其它操作包含DRAM高速缓存管理电路102确定所选择路122(0)到122(Z)的存储器地址是否存在于DRAM高速缓存指示符高速缓存存储器134中(块526)。如果不存在,那么处理在图5C的块528处恢复。如果DRAM高速缓存管理电路102在决定块526处确定所选择路122(0)到122(Z)的存储器地址存在于DRAM高速缓存指示符高速缓存存储器134中,那么DRAM高速缓存管理电路102复位DRAM高速缓存指示符高速缓存存储器134中的针对存储器地址的所选择路122(0)到122(Z)的路编号(块530)。

[0057] 如果DRAM高速缓存管理电路102在决定块526处确定所选择路122(0)到122(Z)的存储器地址不存在于DRAM高速缓存指示符高速缓存存储器134中,那么DRAM高速缓存管理电路102补充DRAM高速缓存指示符高速缓存存储器134(块528)。在一些方面中,用于补充DRAM高速缓存指示符高速缓存存储器134的块528的操作包含从系统存储器DRAM 108中的主控表116读取对应于存储器地址的所选择路122(0)到122(Z)的主控表项118(0)到118(M)(块532)。DRAM高速缓存管理电路102在一些方面中可接下来基于主控表项118(0)到118(M)将针对存储器地址的所选择路122(0)到122(Z)的路编号写入到DRAM高速缓存指示符高速缓存存储器134(块534)。在一些方面中,DRAM高速缓存管理电路102复位对应于存储器地址的所选择路122(0)到122(Z)的路编号(块536)。DRAM高速缓存管理电路102接着将路编号写入到系统存储器DRAM 108中的主控表116(而不需将主控表项118(0)到118(M)安装于DRAM高速缓存指示符高速缓存存储器134中)(块538)。

[0058] 为了说明用于在回写模式中执行由已变更数据从系统高速缓存存储器112的逐出引起的写入操作的图1的DRAM高速缓存管理电路102的示范性操作,提供图6A到6D。为清楚起见,在描述图6A到6D时参考图1的元件。图6A中的操作以DRAM高速缓存管理电路102接收包括写入地址130及写入数据132的存储器写入请求128(块600)开始。如同图5A一般,图6A的实例中的写入数据132表示从系统高速缓存存储器112逐出的已变更(即,经修改)数据,

且因此在本文中称为“已变更逐出的数据132”。

[0059] DRAM高速缓存管理电路102确定已变更逐出的数据132的写入地址130是否在DRAM高速缓存指示符高速缓存存储器134中被发现(块602)。如果写入地址130不存在于DRAM高速缓存指示符高速缓存存储器134中,那么DRAM高速缓存管理电路102概率性地补充DRAM高速缓存指示符高速缓存存储器134(例如,通过将主控表项118(0)到118(M)从主控表116复制到DRAM高速缓存指示符高速缓存存储器134)(块604)。如果DRAM高速缓存指示符高速缓存存储器134在块604处予以补充(即,补充经概率性地确定为发生),那么处理在块606处恢复。否则,DRAM高速缓存管理电路102在系统存储器DRAM 108中的主控表116中更新对应于写入地址130的DRAM高速缓存指示符120(0)到120(X)(例如,通过对针对DRAM高速缓存指示符120(0)到120(X)的主控表项118(0)到118(M)执行读取-修改-写入(RMW)操作)(块608)。DRAM高速缓存管理电路102接着将已变更逐出的数据132写入到DRAM高速缓存存储器104(块610)。应理解,在一些方面中,用于更新DRAM高速缓存指示符120(0)到120(X)的块608的操作及用于将已变更逐出的数据132写入到DRAM高速缓存存储器104的块610的操作可并行地进行。

[0060] DRAM高速缓存管理电路102的一些方面可接下来确定来自主控表116的针对写入地址130的DRAM高速缓存指示符120(0)到120(X)是否指示写入地址130是在DRAM高速缓存存储器104中(块612)。如果否,那么处理完成(块614)。然而,如果DRAM高速缓存管理电路102在决定块612处确定来自主控表116的针对写入地址130的DRAM高速缓存指示符120(0)到120(X)指示写入地址130是在DRAM高速缓存存储器104中,那么DRAM高速缓存管理电路102将已变更逐出的数据132写入到DRAM高速缓存存储器104(块616)。

[0061] 返回参看决定块602,如果DRAM高速缓存管理电路102确定已变更逐出的数据132的写入地址130在DRAM高速缓存指示符高速缓存存储器134中被发现(或如果在块604处补充DRAM高速缓存指示符高速缓存存储器134),那么DRAM高速缓存管理电路102接下来确定已变更逐出的数据132的写入地址130是否在DRAM高速缓存存储器104中被发现(块606)。如果写入地址130未在DRAM高速缓存存储器104中被发现,那么处理在图6B的块618处恢复。然而,如果DRAM高速缓存管理电路102在决定块606处确定写入地址130在DRAM高速缓存存储器104中被发现,那么DRAM高速缓存管理电路102将已变更逐出的数据132写入到DRAM高速缓存存储器104(例如,通过对DRAM高速缓存存储器104执行非-逐出-写入操作)(块616)。

[0062] 现转而参看图6B,DRAM高速缓存管理电路102接下来将写入地址130及已变更逐出的数据132概率性地写入到DRAM高速缓存存储器104(块618)。根据一些方面,用于将写入地址130及已变更逐出的数据132写入到DRAM高速缓存存储器104的块618的操作可包含首先随机地选择待从DRAM高速缓存存储器104逐出的路122(0)到122(Z)(块620)。通过DRAM高速缓存管理电路102从DRAM高速缓存存储器104读取所选择路122(0)到122(Z)的存储器地址(块622)。DRAM高速缓存管理电路102接着将写入地址130及已变更逐出的数据132写入到DRAM高速缓存存储器104中的所选择路122(0)到122(Z)(块624)。DRAM高速缓存管理电路102将DRAM高速缓存指示符高速缓存存储器134中的用于写入地址130的路编号更新为所选择路122(0)到122(Z)的路编号(块626)。DRAM高速缓存管理电路102也设定DRAM高速缓存指示符高速缓存存储器134中的针对写入地址130的已变更指示符140(0)到140(C)、140'(0)到140'(C)(块628)。处理接着在图6C的块630处继续。

[0063] 在图6C中,用于将写入地址130及已变更逐出的数据132概率性地写入到DRAM高速缓存存储器104的块618的其它操作包含DRAM高速缓存管理电路102确定所选择路122 (0) 到122 (Z) 的存储器地址是否存在于DRAM高速缓存指示符高速缓存存储器134中(块630)。如果否,那么处理在图6D中的块632处恢复。如果DRAM高速缓存管理电路102在决定块630处确定所选择路122 (0) 到122 (Z) 的存储器地址存在于DRAM高速缓存指示符高速缓存存储器134中,那么DRAM高速缓存管理电路102复位DRAM高速缓存指示符高速缓存存储器134中的针对存储器地址的所选择路122 (0) 到122 (Z) 的路编号及已变更指示符140 (0) 到140 (C)、140' (0) 到140' (C) (块634)。

[0064] 现参看图6D,如果DRAM高速缓存管理电路102在图6C的决定块630处确定所选择路122 (0) 到122 (Z) 的存储器地址不存在于DRAM高速缓存指示符高速缓存存储器134中,那么DRAM高速缓存管理电路102补充DRAM高速缓存指示符高速缓存存储器134(块632)。在一些方面中,用于补充DRAM高速缓存指示符高速缓存存储器134的块632的操作包含从系统存储器DRAM 108中的主控表116读取对应于存储器地址的所选择路122 (0) 到122 (Z) 的主控表项118 (0) 到118 (M) (块634)。DRAM高速缓存管理电路102在一些方面中可接下来基于主控表项118 (0) 到118 (M) 将针对存储器地址的所选择路122 (0) 到122 (Z) 的路编号写入到DRAM高速缓存指示符高速缓存存储器134(块636)。在一些方面中,DRAM高速缓存管理电路102复位对应于存储器地址的所选择路122 (0) 到122 (Z) 的路编号(块638)。DRAM高速缓存管理电路102接着将路编号写入到系统存储器DRAM 108中的主控表116(而不需将主控表项118 (0) 到118 (M) 安装于DRAM高速缓存指示符高速缓存存储器134中)(块640)。如果在块618中写入地址130及已变更逐出的数据132并未概率性地写入到DRAM高速缓存存储器104,那么DRAM高速缓存管理电路102将已变更逐出的数据132写入到系统存储器DRAM 108(块642)。

[0065] 根据本文所公开的方面使用DRAM高速缓存指示符高速缓存存储器以提供可扩展DRAM高速缓存管理可在任一基于处理器的装置中提供或集成于任一基于处理器的装置中。实例包含(但不限于)机顶盒、娱乐单元、导航装置、通信装置、固定位置数据单元、移动位置数据单元、移动电话、蜂窝式电话、智能型手机、平板计算机、平板手机、计算机、便携式计算机、台式计算机、个人数字助理(PDA)、监视器、计算机监视器、电视、调谐器、无线电、卫星无线电、音乐播放器、数字音乐播放器、便携式音乐播放器、数字视频播放器、视频播放器、数字视频光盘(DVD)播放器、便携式数字视频播放器及汽车。

[0066] 就此来说,图7说明可采用图1中所说明的DRAM高速缓存管理电路(DCMC) 102的基于处理器的系统700的实例。基于处理器的系统700包含一或多个中央处理单元(CPU) 702,每一中央处理单元702包含一或多个处理器704。一或多个CPU 702可具有耦合到一或多个处理器704以用于快速存取暂时存储的数据的高速缓存存储器706。一或多个CPU 702耦合到系统总线708且可将包含于基于处理器的系统700中的主控装置与从属装置相互耦合。如所熟知,一或多个CPU 702通过经由系统总线708交换地址、控制及数据信息而与此些其它装置通信。举例来说,一或多个CPU 702可将总线异动请求传达到作为从属装置的实例的存储器控制器710。

[0067] 其它主控装置及从属装置可连接到系统总线708。作为实例,如图7中所说明,此些装置可包含存储器系统712、一或多个输入装置714、一或多个输出装置716、一或多个网络接口装置718及一或多个显示器控制器720。输入装置714可包含任何类型的输入装置,包含

(但不限于)输入按键、开关、语音处理器等。输出装置716可包含任何类型的输出装置,包含(但不限于)音频、视频、其它视觉指示器等。网络接口装置718可为经配置以允许到及从网络722的数据交换的任何装置。网络722可为任何类型的网络,包含(但不限于)有线或无线网络、私用或公用网络、局域网(LAN)、无线局域网(WLAN)、广域网(WAN)、BLUETOOTH™网络及因特网。网络接口装置718可经配置以支持任何类型的所要通信协议。存储器系统712可包含一或多个存储器单元724(O)到724(N)。

[0068] CPU 702也可经配置以经由系统总线708存取显示器控制器720以控制发送到一或多个显示器726的信息。显示器控制器720将信息发送到待经由一或多个视频处理器728显示的显示器726,所述视频处理器将待显示的信息处理成适合于显示器726的格式。显示器726可包含任何类型的显示器,包含(但不限于)阴极射线管(CRT)、液晶显示器(LCD)、等离子体显示器等。

[0069] 所属领域的一般技术人员将进一步了解,结合本文所公开的方面所描述的各种说明性逻辑块、模块、电路及算法可实施为电子硬件、存储于存储器中或另一计算机可读媒体中且由处理器或其它处理装置执行的指令,或此两者的组合。作为实例,本文中所描述的主控装置及从属装置可用于任何电路、硬件组件、集成电路(IC)或IC芯片中。本文中所公开的存储器可为任何类型及大小的存储器,且可经配置以存储任何类型的所要信息。为了清楚地说明此可互换性,上文已大体上在功能性方面描述了各种说明性组件、块、模块、电路及步骤。如何实施此功能性视特定应用、设计选择及/或强加于整个系统的设计约束而定。对于每一特定应用来说,所属领域的一般技术人员可以变化的方式实施所描述的功能性,但不应将所述实施决策解译为导致脱离本发明的范围。

[0070] 结合本文中所公开的方面而描述的各种说明性逻辑块、模块及电路可通过以下各者来实施或执行:处理器、数字信号处理器(DSP)、专用集成电路(ASIC)、现场可编程门阵列(FPGA)或其它可编程逻辑装置、离散闸或晶体管逻辑、离散硬件组件或其经设计以执行本文中所描述的功能的任何组合。处理器可为微处理器,但在替代方案中,处理器可为任何常规的处理器、控制器、微控制器或状态机。处理器也可实施为计算装置的组合(例如,DSP与微处理器的组合、多个微处理器、结合DSP核心的一或多个微处理器,或任何其它此配置)。

[0071] 本文中所公开的方面可以硬件及存储于硬件中的指令体现,且可驻存于(例如)随机存取存储器(RAM)、快闪存储器、只读存储器(ROM)、电可编程ROM(EPROM)、电可擦除可编程ROM(EEPROM)、寄存器、硬盘、抽取式磁盘、CD-ROM或所属领域中已知的任何其它形式的计算机可读媒体中。示范性存储媒体耦合到处理器,使得处理器可从存储媒体读取信息且将信息写入到存储媒体。在替代方案中,存储媒体可集成到处理器。处理器及存储媒体可驻存于ASIC中。所述ASIC可驻存于远程台中。在替代方案中,处理器及存储媒体可作为离散组件而驻存于远程台、基站或服务器中。

[0072] 也应注意,描述于本文中的示范性方面中的任一者中的操作步骤经描述以提供实例及论述。可以除了所说明的序列以外的众多不同序列来执行所描述的操作。此外,描述于单一操作步骤中的操作可实际上以数个不同步骤执行。另外,可组合示范性方面中所论述的一或多个操作步骤。应理解,如所属领域的一般技术人员将显而易见,流程图中所说明的操作步骤可经受众多不同修改。所属领域的一般技术人员也将理解,可使用各种不同技术及技法中的任一者表示信息及信号。举例来说,贯穿以上描述可能参考的数据、指令、命令、

信息、信号、位、符号及码片可由电压、电流、电磁波、磁场或磁性粒子、光场或光学粒子或其任何组合来表示。

[0073] 提供本发明的先前描述以使得任何所属领域的一般技术人员能够制造或使用本发明。对本发明的各种修改对于所属领域的一般技术人员来说将易于为显而易见的,且本文中所定义的一般原理可在不背离本发明的精神或范围的情况下应用于其它变化。因此,本发明并不打算限于本文中所描述的实例及设计,而是应符合与本文中所公开的原理及新颖特征相一致的最广泛范围。

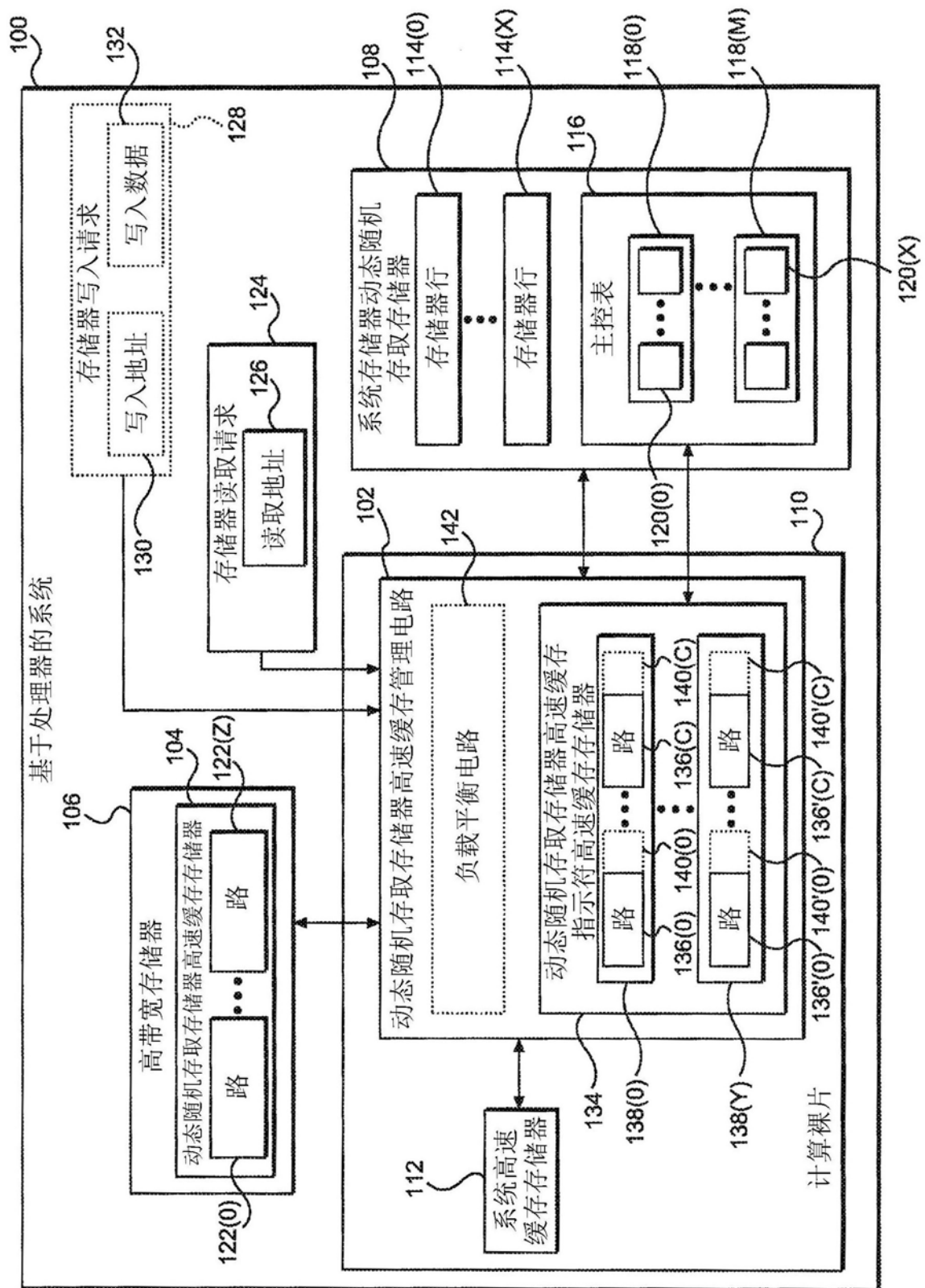


图1

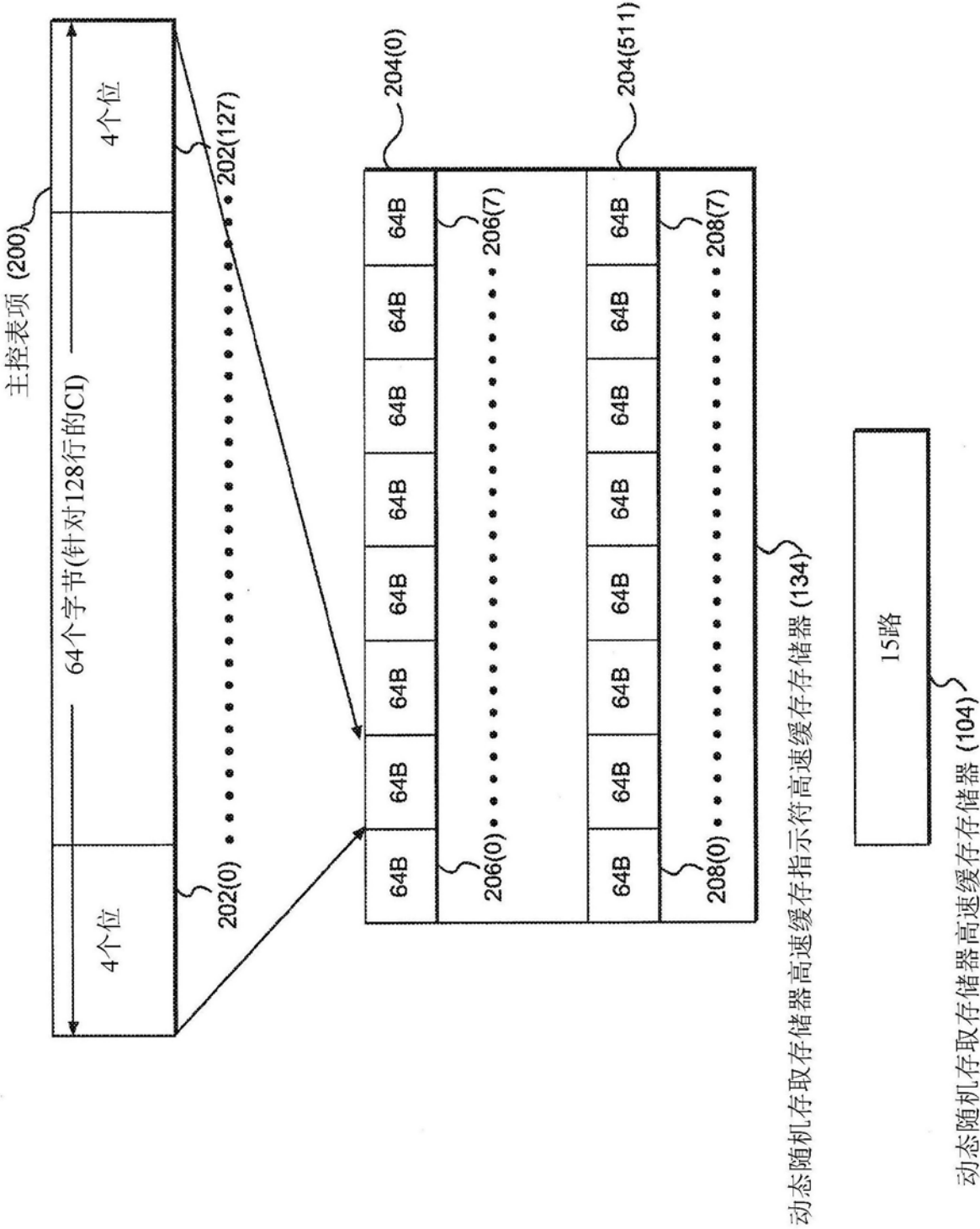


图2A

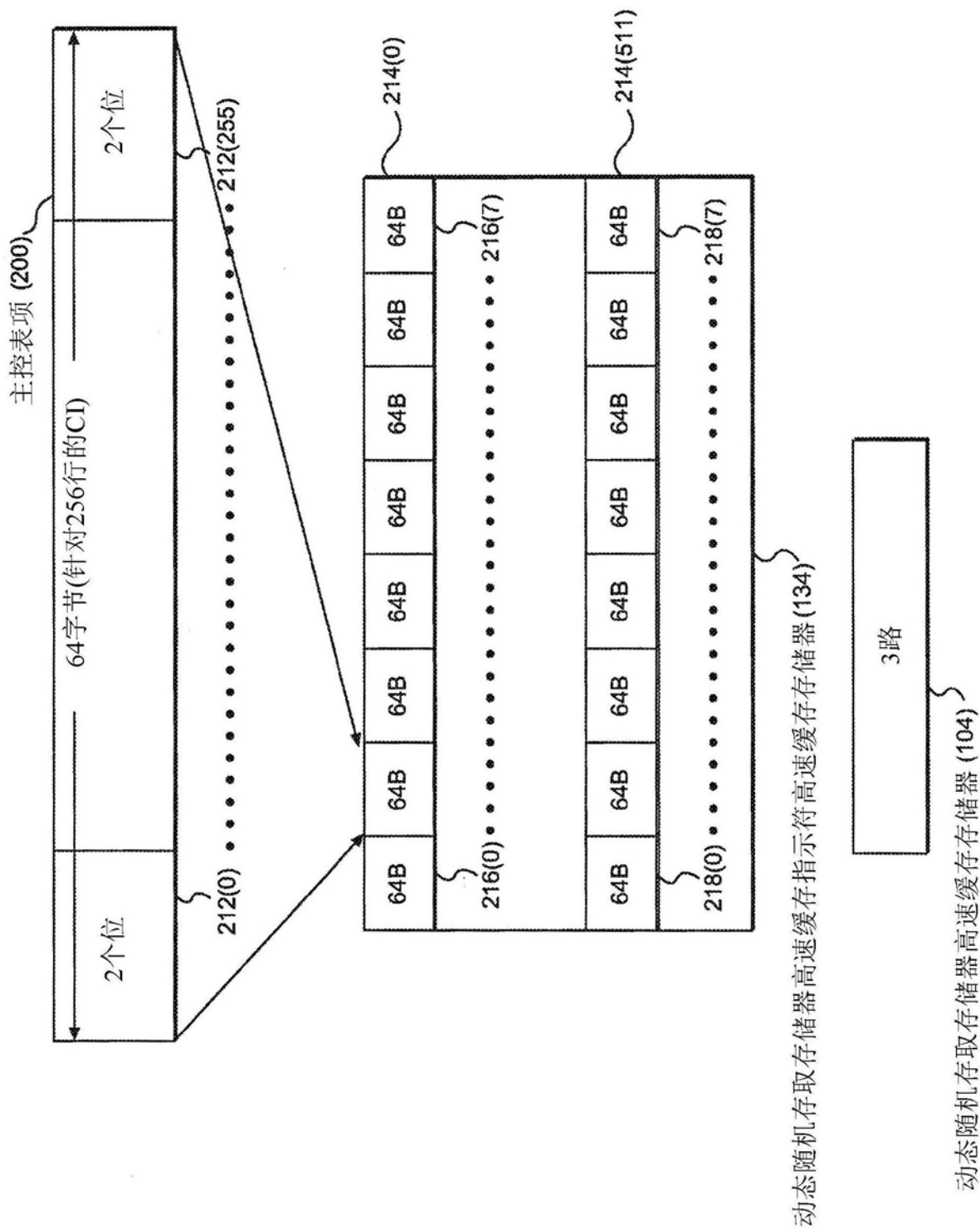


图2B

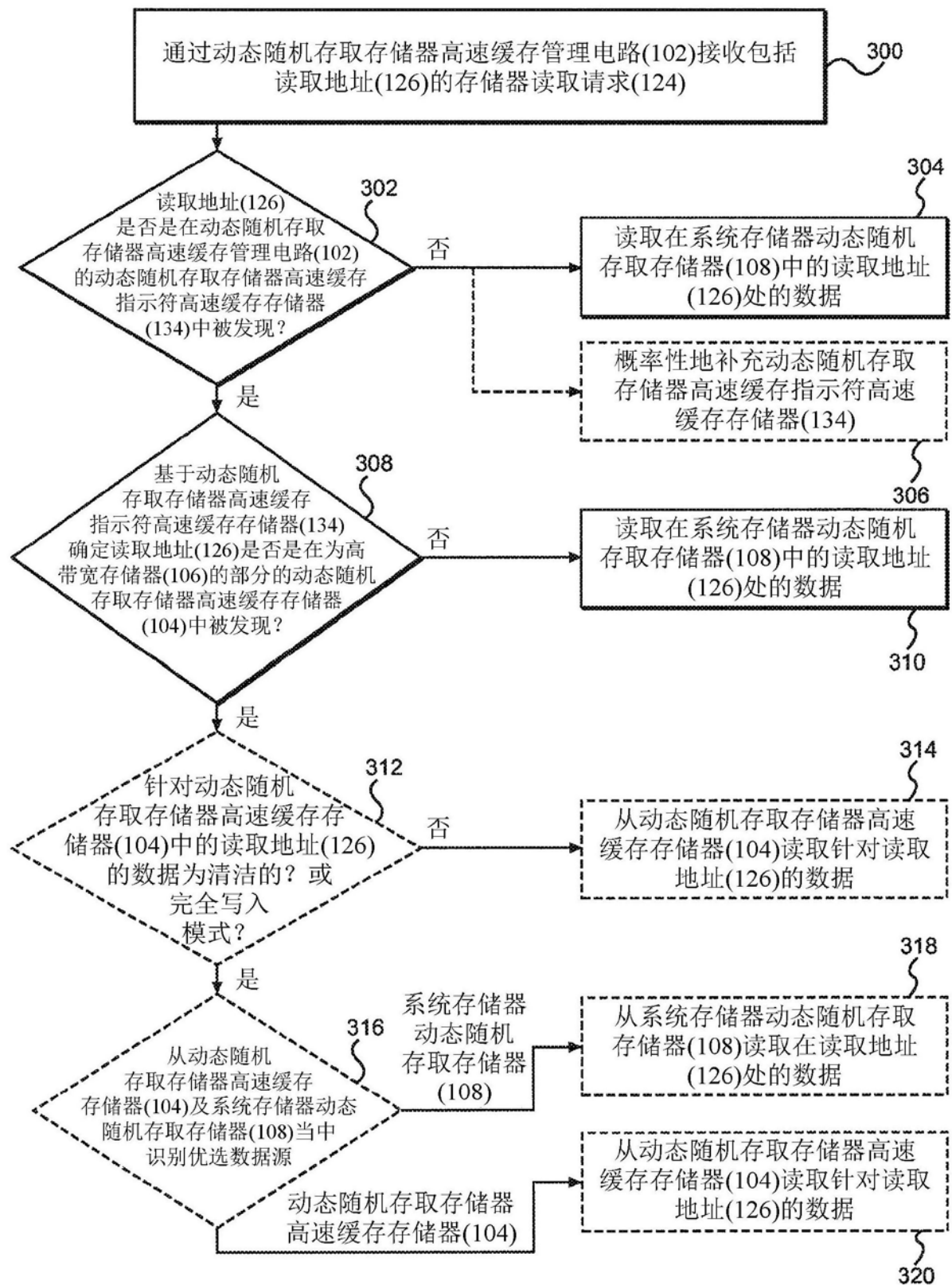


图3

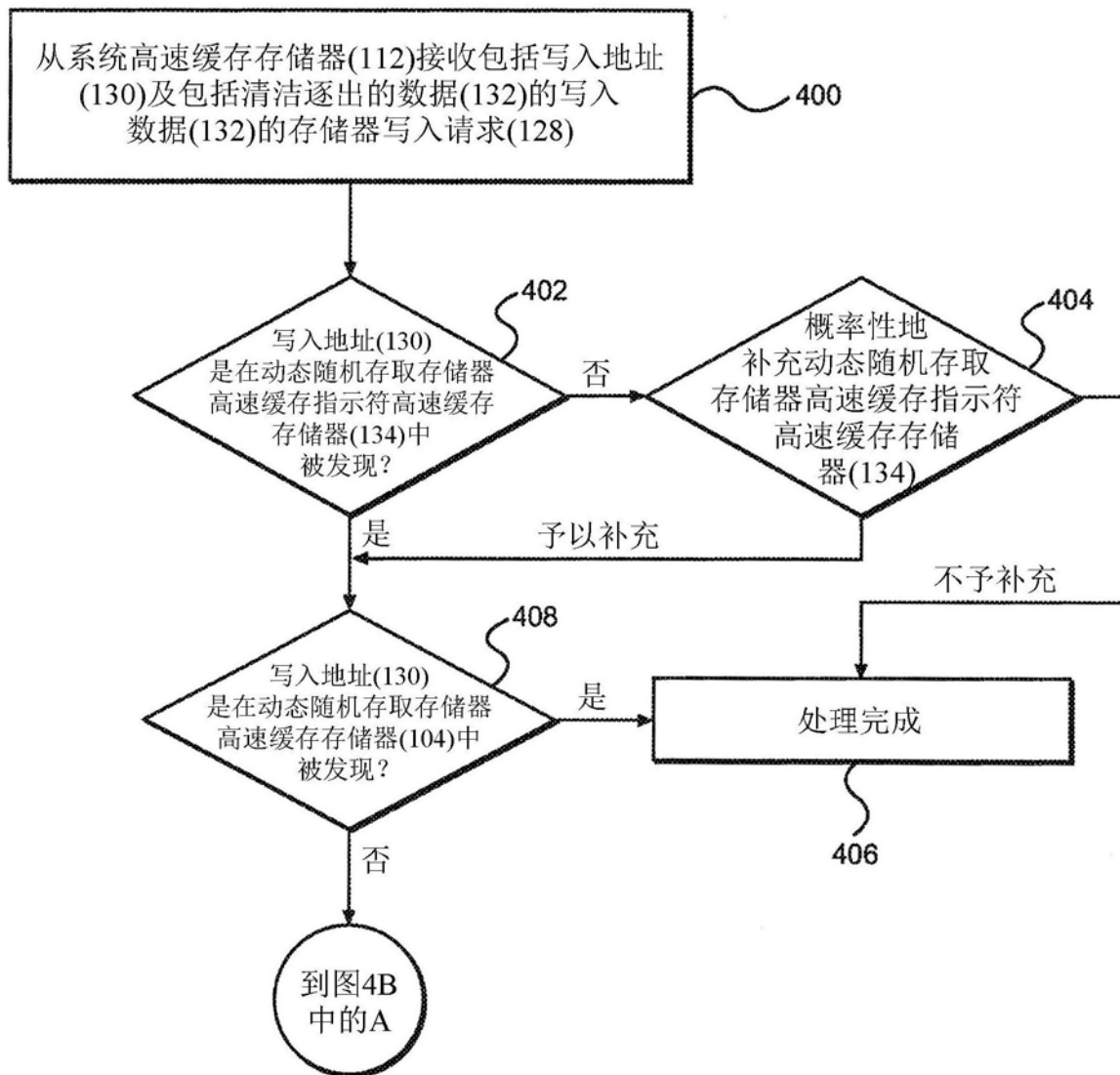


图4A

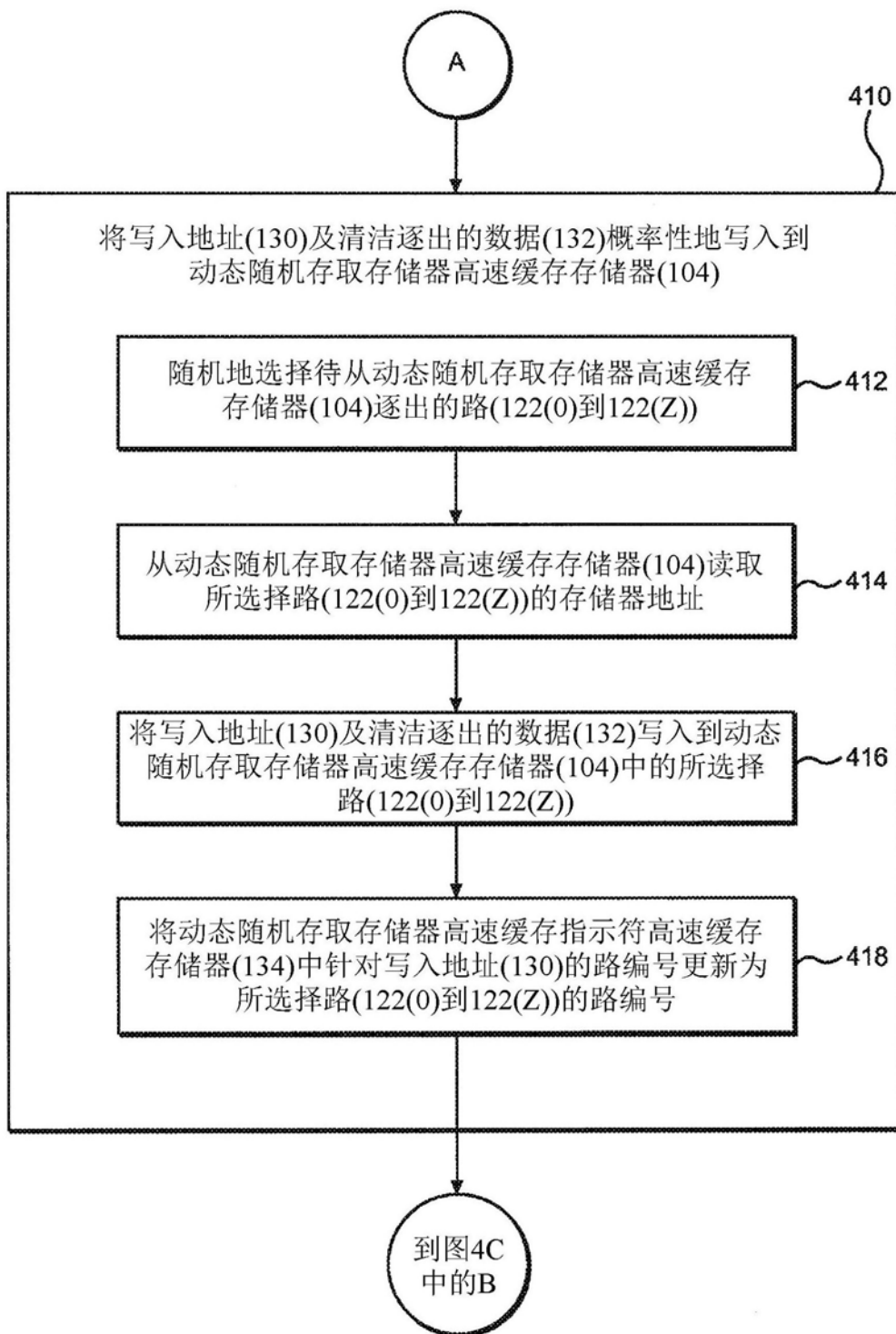


图4B

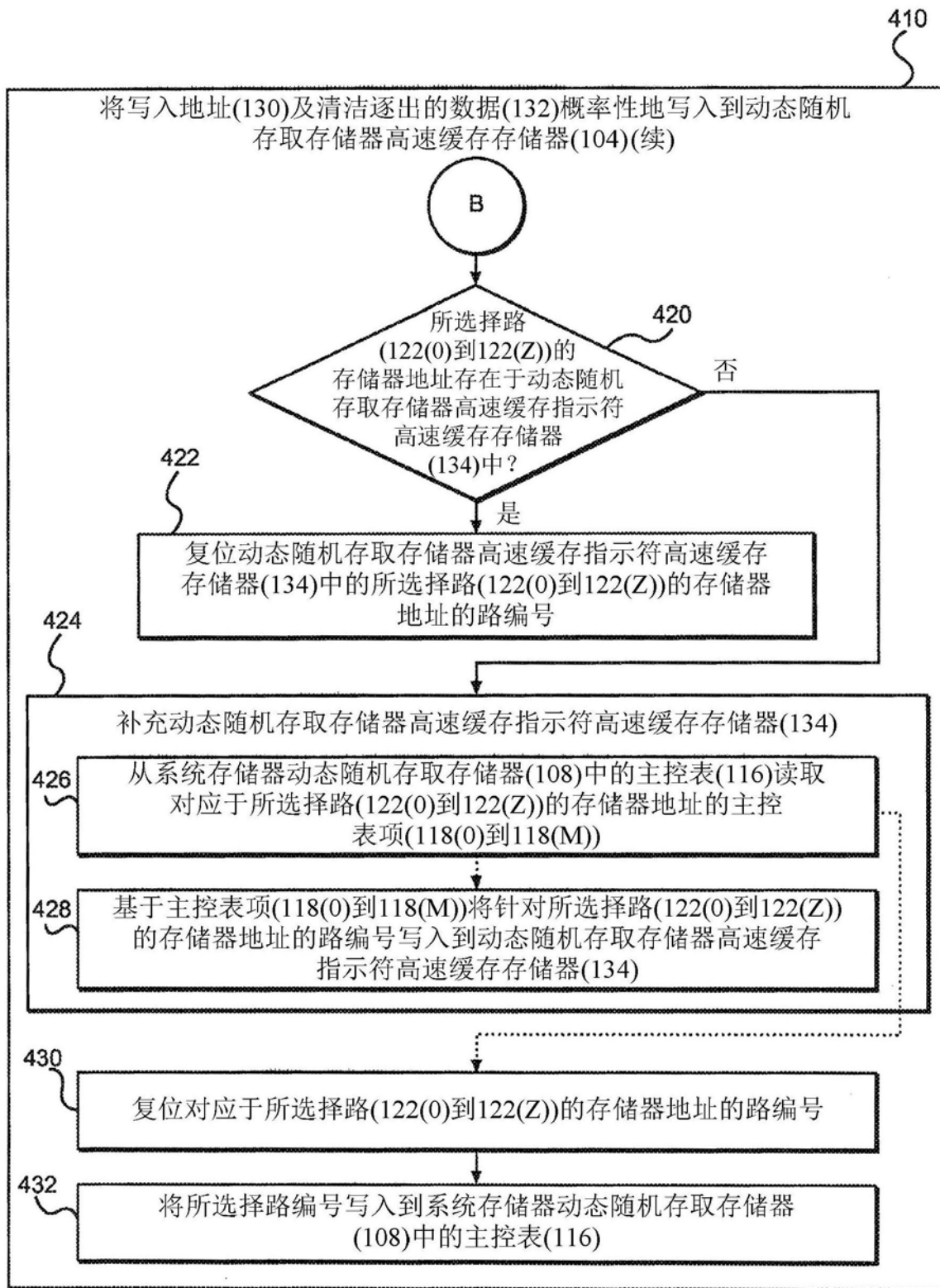


图4C

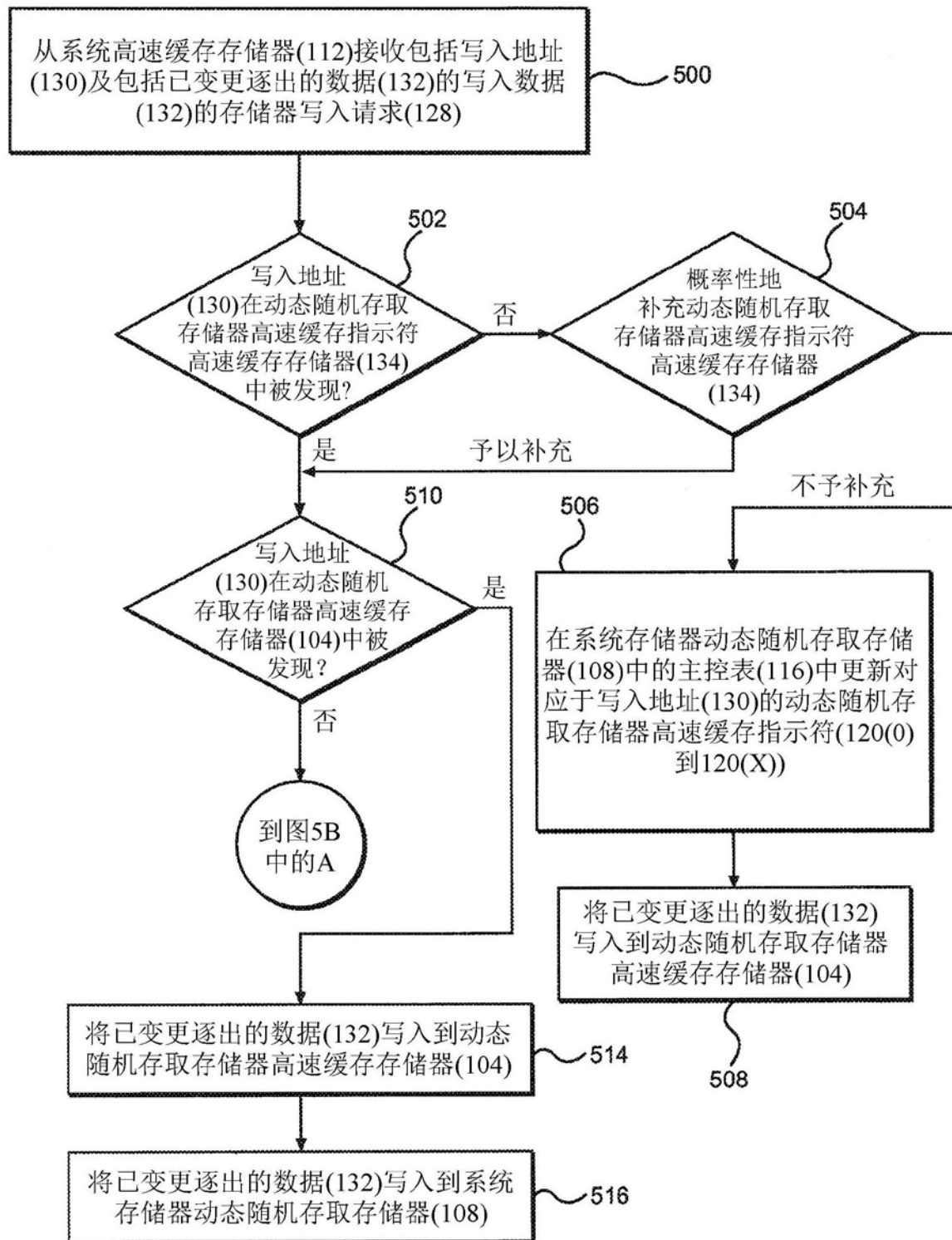


图5A

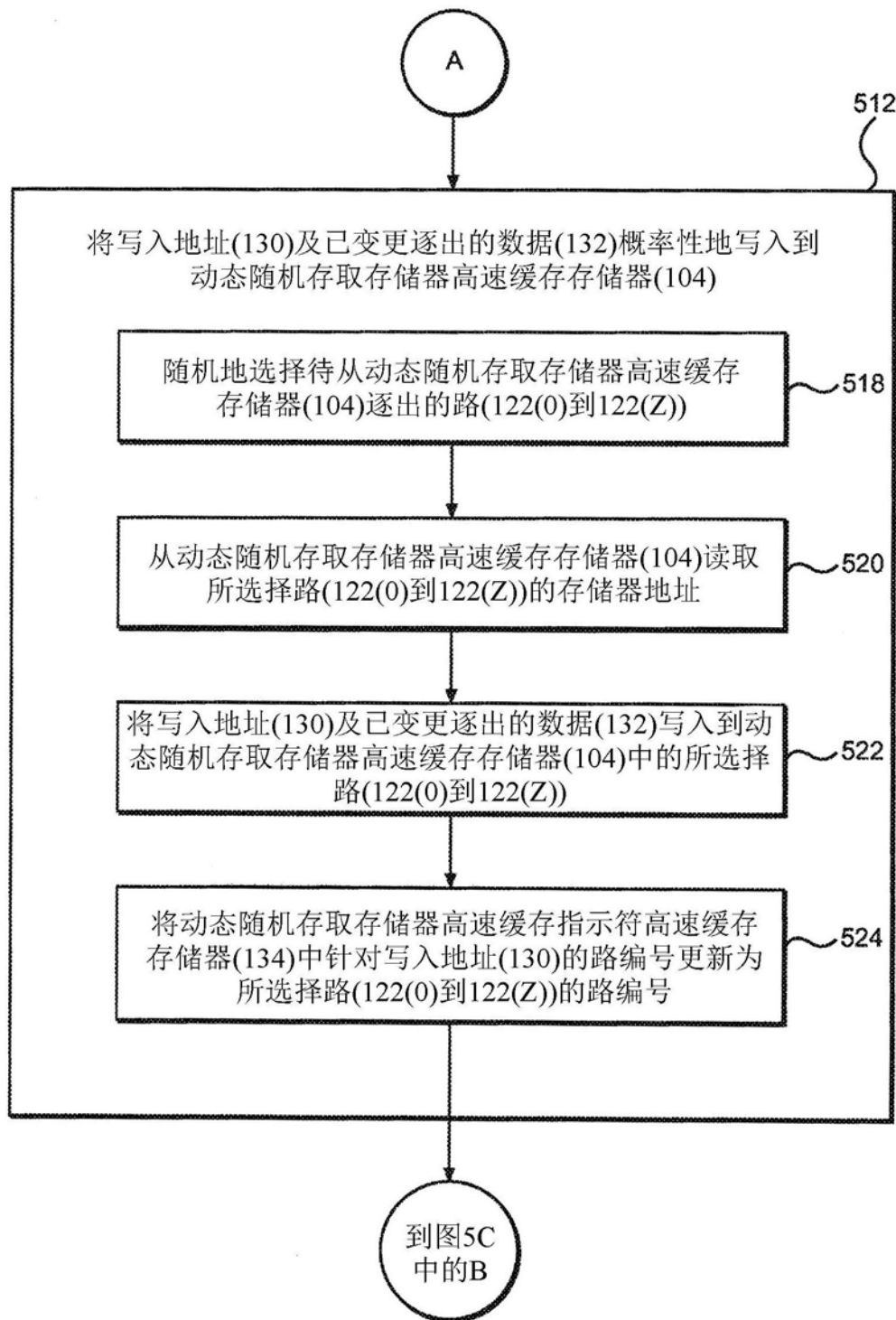


图5B

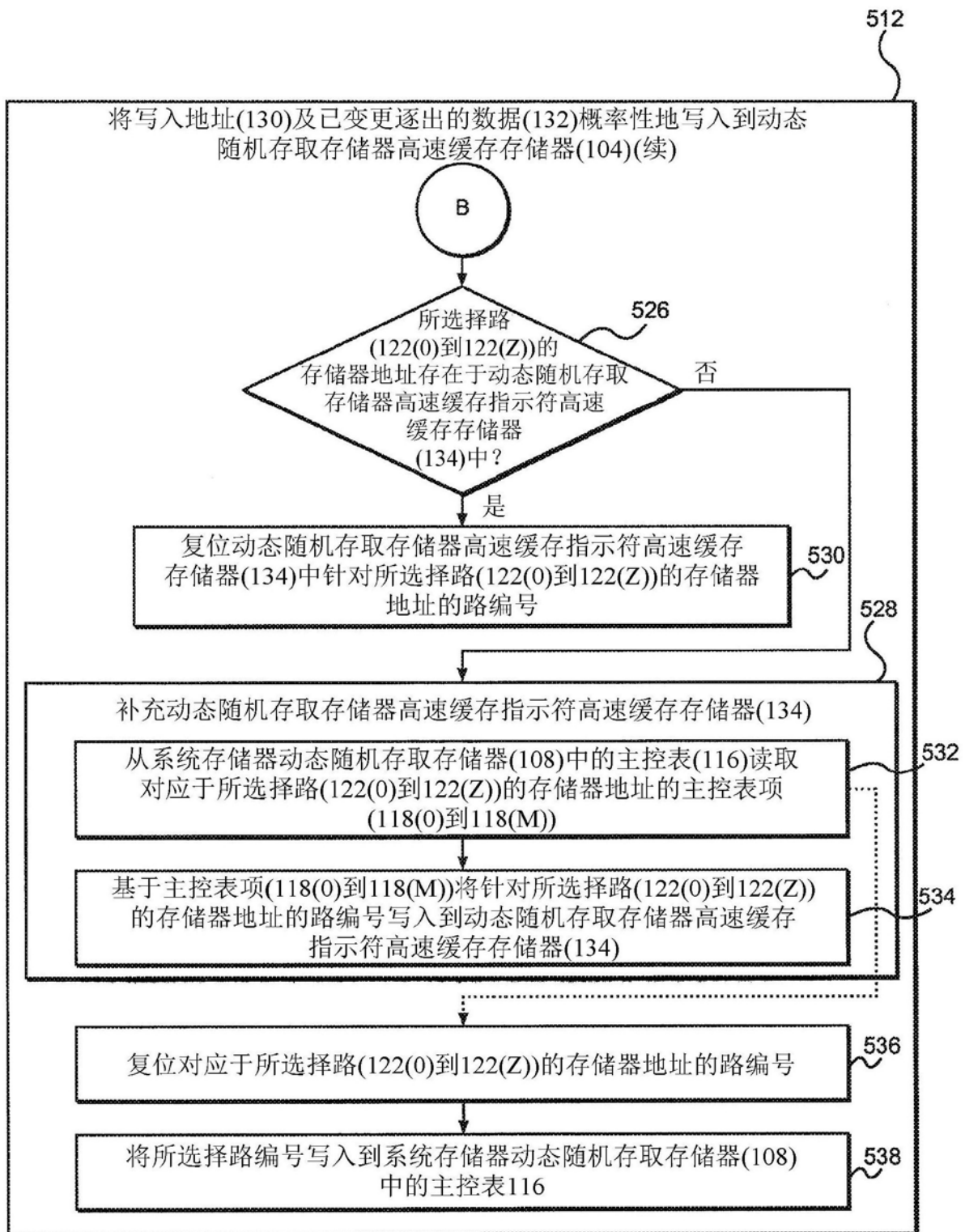


图5C

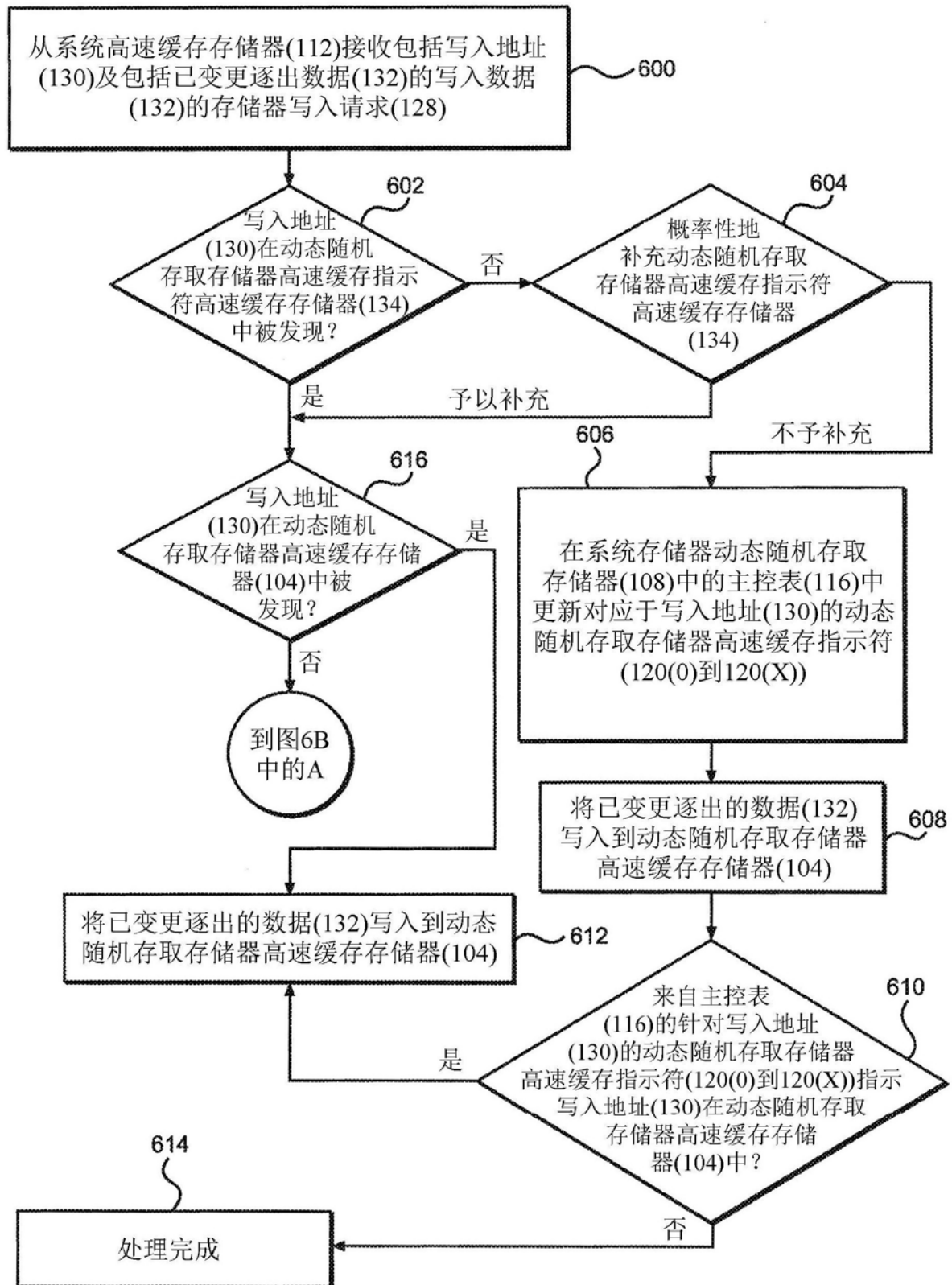


图6A

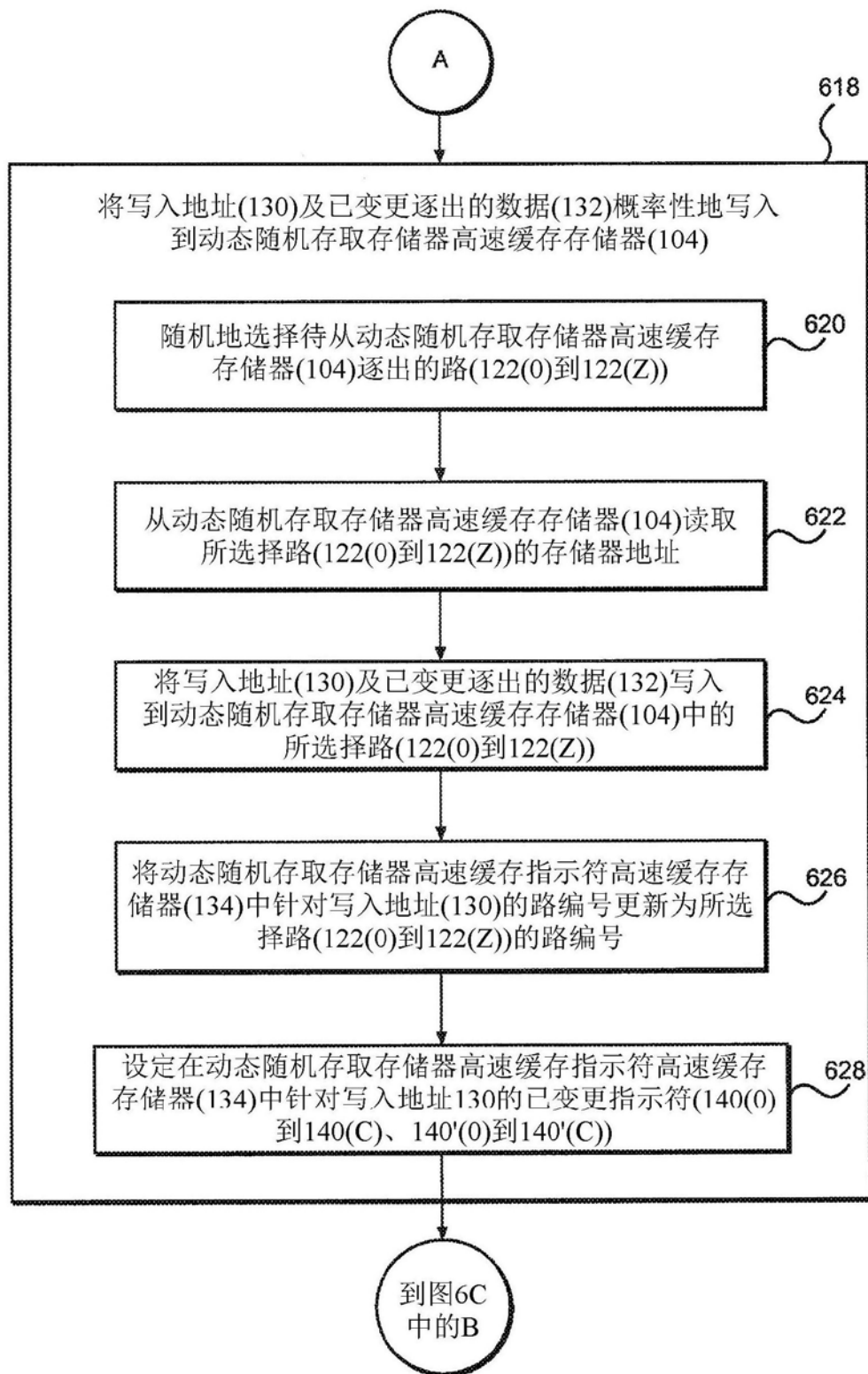


图6B

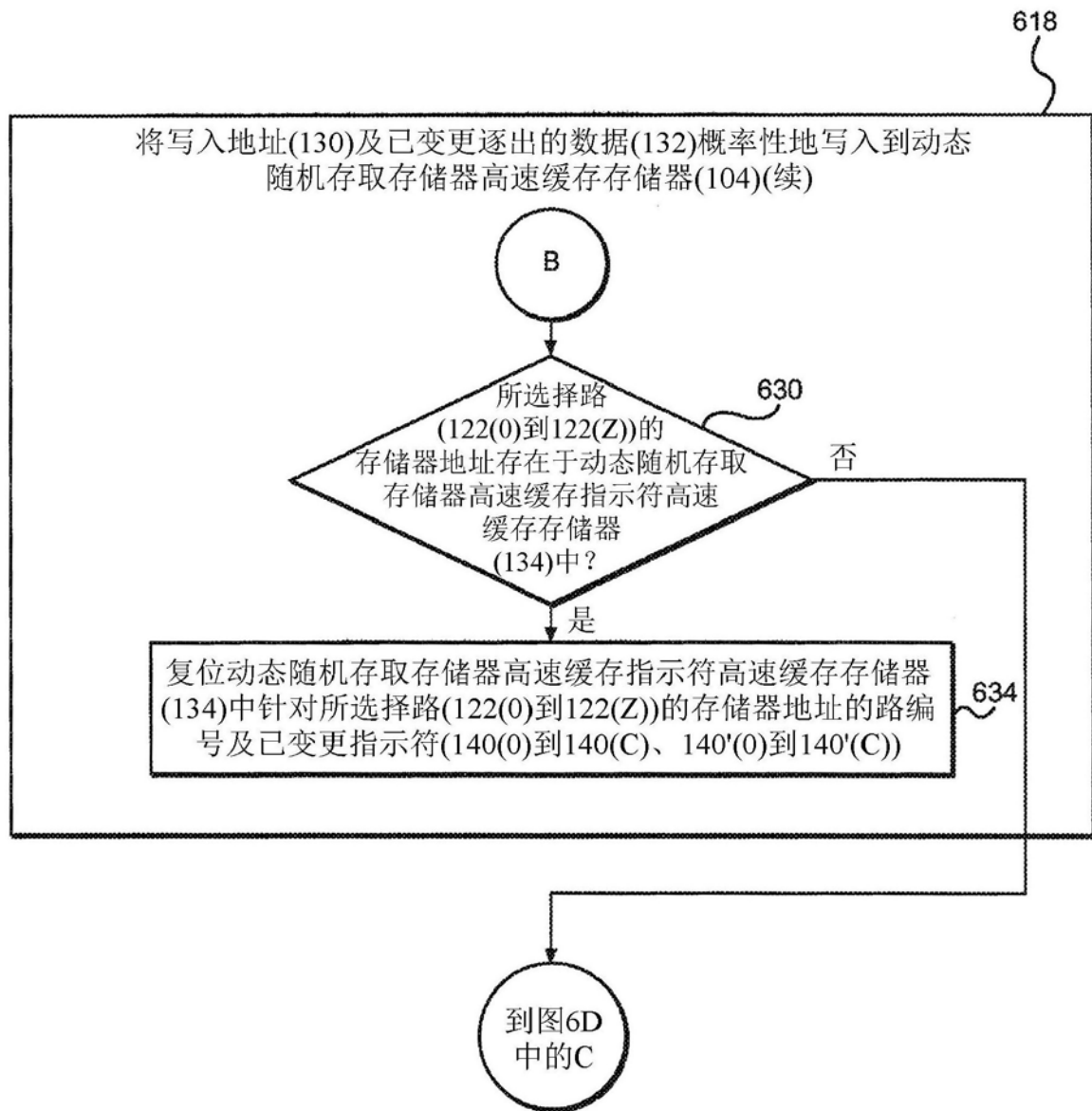


图6C

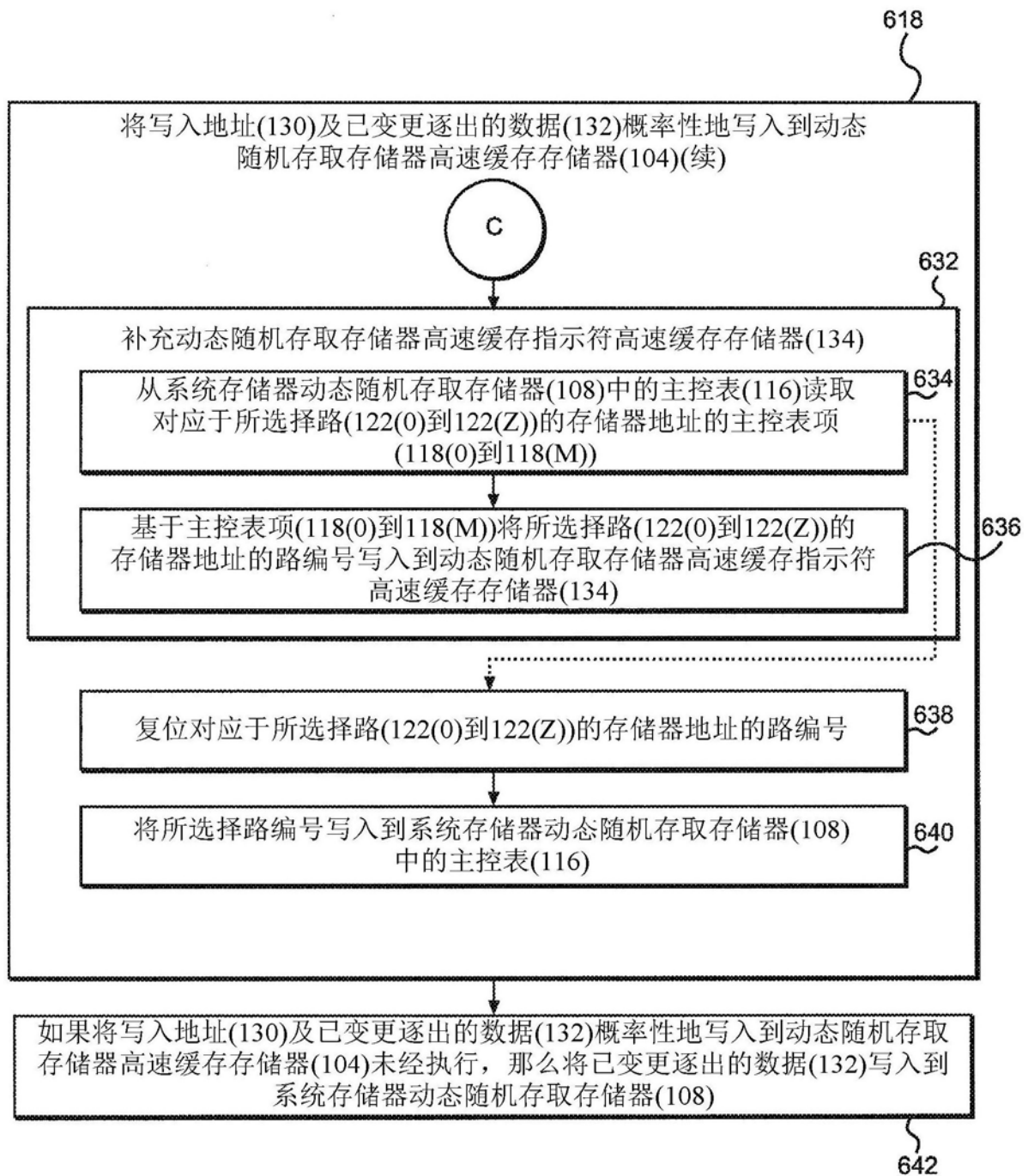


图6D

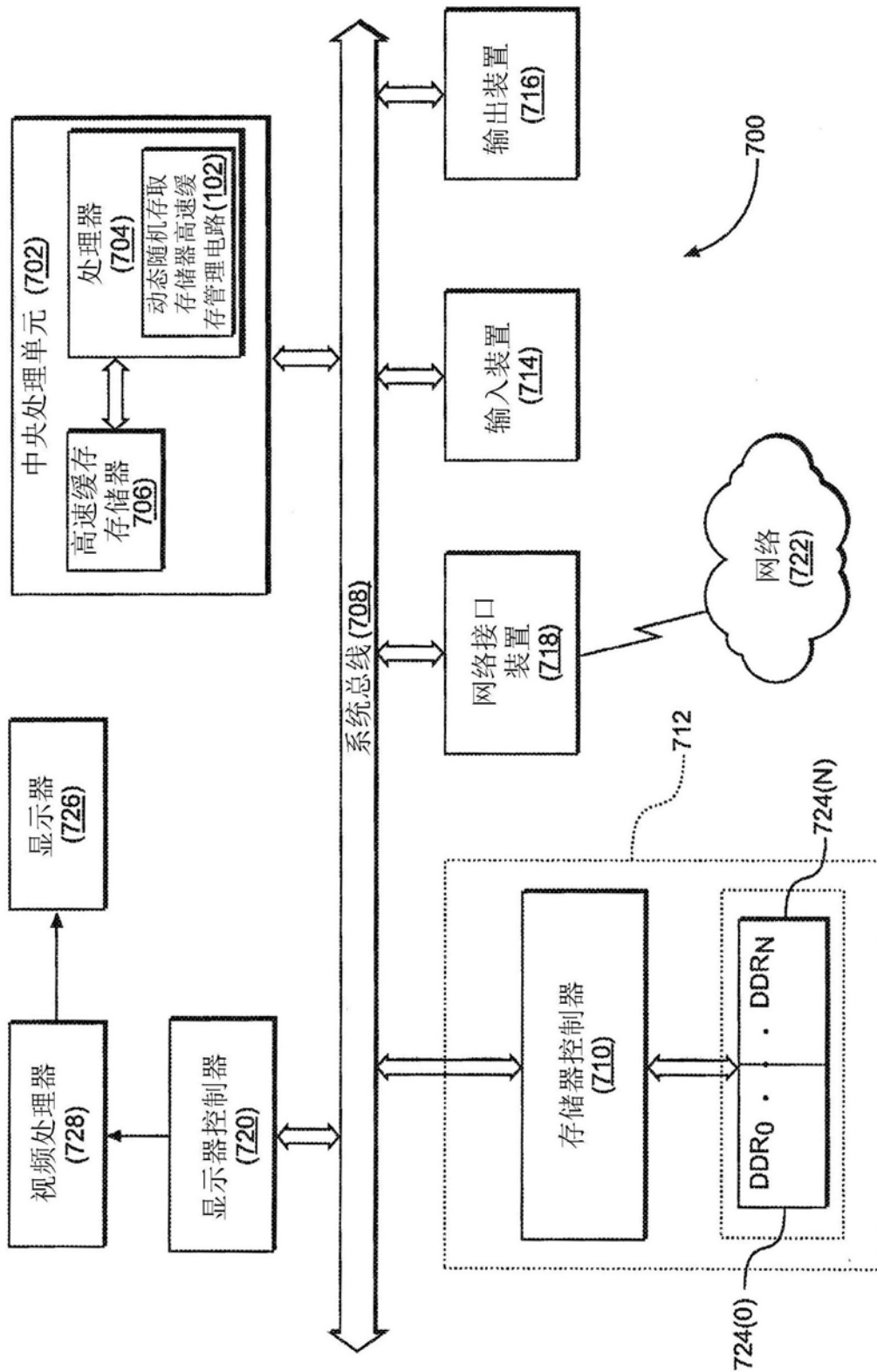


图7