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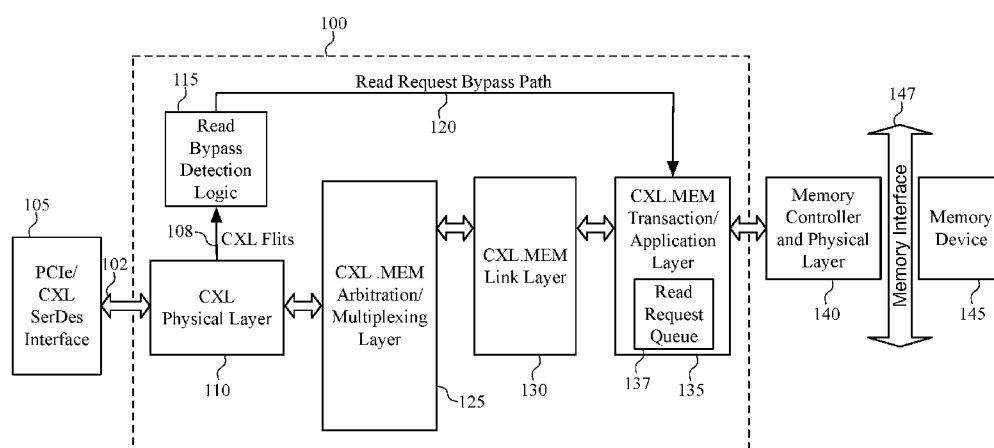


FIG. 1

(57) **Abstract:** System and method for analyzing CXL flits at read bypass detection logic (115) to identify bypass memory read requests (108) and transmitting the identified bypass memory read requests (108) over a read request bypass path (120) directly to a transaction/application layer (135) of the CXL memory controller (100), wherein the read request bypass path (120) does not include an arbitration/multiplexing layer (125) and a link layer (130) of the CXL memory controller (100), thereby reducing the latency inherent in a CXL memory controller (100).

SYSTEM AND METHOD FOR BYPASS MEMORY READ REQUEST DETECTION

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] The present application claims priority to United States Provisional Patent Application Serial No. 63/195,455 filed on June 1, 2021 and United States Non-Provisional Patent Application Serial No. 17/741,282 filed on May 10, 2022, the contents of each of which are incorporated by reference herein in their entirety.

BACKGROUND OF THE INVENTION

[0002] Compute Express Link (CXL) is based on the Peripheral Component Interconnect Express (PCIe) Gen5 link infrastructure to provide an open interconnect standard for enabling efficient, coherent memory access between a host, such as a CPU, and a device, such as a hardware accelerator or a memory expansion device that is handling an intensive workload.

[0003] One of the primary benefits of CXL is that it allows various CPUs to access various types of memory using the same method, thereby allowing the various CPUs to utilize the same memory pool of devices. The read latency associated with memory access is critical for host CPU performance and as such, it is highly advantageous to reduce the read latency associated with CXL attached devices, such as double data rate (DDR) memory controllers.

[0004] Accordingly, what is needed in the art is a system and method that improves the read latency of CXL attached memory controllers.

SUMMARY OF THE INVENTION

[0005] In various examples, the present provides a system and method that improves the read latency of CXL attached memory controllers.

[0006] In one example, a method is provided for bypass memory read request detection, which includes, receiving a plurality of data packets at a physical layer of a CXL memory controller,

deriving a plurality Compute Express Link (CXL) flow control units (flits) from the plurality of data packets received at a physical layer of a CXL memory controller, transmitting each of the received plurality of CXL flits to read bypass detection logic of the CXL memory controller and analyzing each of the plurality of CXL flits at the read bypass detection logic to identify a bypass memory read request from the plurality of CXL flits. In a particular example, analyzing each of the plurality of CXL flits at the read bypass detection logic of the CXL memory includes detecting a master to subordinate (M2S) request having a memory read operation code in the CXL flit to identify the bypass memory read request. The method further includes, transmitting the bypass memory read request over a read request bypass path directly to a transaction/application layer of the CXL memory controller, wherein the read request bypass path does not include an arbitration/multiplexing layer and a link layer of the CXL memory controller. When a read request queue of the CXL memory controller is empty, the method continues by, generating a memory read command on an interface of a memory device attached to the CXL memory controller in response to the bypass memory read request received at the transaction/application layer of the CXL memory controller, receiving read data from the memory device at the transaction/application layer in response to the memory read command and, when there is a link layer memory read request at the transaction/application layer that matches the bypass memory read request that generated the memory read command, the method concludes by forwarding the read data received at the transaction/application layer to the link layer of the CXL memory controller.

[0007] In an additional example, when there is not a link layer memory read request at the transaction/application layer that matches the bypass memory read request that generated the memory read command, the method continues by discarding the read data received at the transaction/application layer. Additionally, when the read request queue of the CXL memory controller is not empty, the method continues by not generating the memory read command on the interface of the memory device attached to the CXL memory controller and discarding the bypass memory read request. A memory read command will also not be generated on the memory device interface, and the bypass memory read request will be discarded, if an address space of the bypass memory read request is not valid.

[0008] In a particular example, the memory device attached to the CXL memory controller is a Double Data Rate (DDR) memory device.

[0009] In an additional example, a compute express link (CXL) memory controller is provided which includes read bypass detection logic to receive a plurality of CXL flits from a CXL physical layer of a CXL memory controller and to analyze each of the received plurality of CXL flits to identify a bypass memory read request from the plurality of CXL flits. In a particular example, the CXL memory controller analyzes each of the plurality of CXL flits by detecting a master to subordinate (M2S) request having a memory read operation code in the CXL flit to identify the bypass memory read request. The CXL memory controller further includes a read request bypass path, which includes the read bypass detection logic and connects the CXL physical layer to a transaction/application layer of the CXL memory controller, the read request bypass path bypassing an arbitration/multiplexing layer of the CXL memory controller and a link layer of the CXL memory controller. The transaction/application layer generates a memory read command on an interface of a memory device associated with the CXL memory controller in response to the bypass memory read request received at the transaction/application layer when a read request queue is empty, receives read data from the memory device in response to the memory read command and forwards the read data received at the transaction/application layer to the link layer when there is a link layer memory read request at the transaction/application layer that matches the bypass memory read request that generated the memory read command.

[0010] In an additional example, the CXL memory controller discards the read data received at the transaction/application layer when there is not a link layer memory read request at the transaction/application layer that matches the bypass memory read request that generated the memory read command. Additionally, the CXL memory controller does not generate the memory read command on the interface of the memory device when the read request queue is not empty and discards the bypass memory read request. The CXL memory controller also discards the bypass memory read request and does not generate the memory read command on the memory device interface when an address space of the bypass memory read request is not valid.

[0011] Accordingly, these various examples provide an improved system and method for reducing read latency for CXL attached memory controllers.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] The accompanying drawings, which are incorporated in and form a part of this specification, illustrate various examples and, together with the Detailed Description of the Invention, serve to explain principles discussed below. The drawings referred to in this brief description should not be understood as being drawn to scale unless specifically noted.

[0013] FIG. 1 is a block diagram illustrating an example CXL memory controller including read bypass detection logic.

[0014] FIG. 2 is a table illustrating CXL.cache/CXL.mem Flit Header Definition in accordance with the CXL 2.0 Specification.

[0015] FIG. 3 is a table illustrating Slot Format Field Encoding in accordance with the CXL 2.0 Specification.

[0016] FIG. 4 is a table illustrating H2D/M2S Slot Formats in accordance with the CXL 2.0 Specification.

[0017] FIG. 5A is a flow diagram illustrating an example method for reducing read latency in a CXL memory controller.

[0018] FIG. 5B is a continuation of the flow diagram of FIG. 5A illustrating an example method for reducing read latency in a CXL memory controller.

[0019] FIG. 6A is a flow diagram illustrating an example method for reducing read latency in a CXL memory controller and for selectively discarding bypass memory read requests.

[0020] FIG. 6B is a continuation of the flow diagram of FIG. 6A illustrating an example method for reducing read latency in a CXL memory controller and for selectively discarding bypass memory read requests.

[0021] FIG. 7 is a flow diagram illustrating an example method for reducing read latency

in a CXL memory controller and for selectively discarding link layer memory read requests.

[0022] FIG. 8A is a flow diagram illustrating an example method for reducing read latency in a CXL memory controller and for matching link layer memory read requests to bypass memory read requests.

[0023] FIG. 8B is a continuation of the flow diagram of the 8A illustrating an example method for reducing read latency in a CXL memory controller and for matching link layer memory read requests to bypass memory read requests.

DETAILED DESCRIPTION OF THE INVENTION

[0024] Reference will now be made in detail to various examples, which are illustrated in the accompanying drawings. While various examples are discussed herein, it will be understood that they are not intended to be limiting. On the contrary, the presented examples are intended to cover alternatives, modifications, and equivalents, which may be included within the spirit and scope of the various examples as defined by the appended claims. Furthermore, in this Detailed Description of the Invention, numerous specific details are set forth in order to provide a thorough understanding. However, examples may be practiced without one or more of these specific details. In other instances, well known methods, procedures, components, and circuits have not been described in detail as not to unnecessarily obscure aspects of the described examples.

[0025] It will be understood that, although the terms first, second, third, without limitation, may be used herein to describe various elements, components, regions, layers, and/or sections, these elements, components, regions, layers, and/or sections should not be limited by these terms. These terms are only used to distinguish one element, component, region, layer, or section from another region, layer, or section. Thus, a first element, component, region, layer, or section discussed below could be termed a second element, component, region, layer, or section.

[0026] Unless otherwise defined, all terms (including technical and scientific terms) used herein have the same meaning as commonly understood by one of ordinary skill in the art. It will be further understood that terms, such as those defined in commonly used dictionaries, should be interpreted as having a meaning that is consistent with their meaning in the context of the relevant

art and will not be interpreted in an idealized or overly formal sense unless expressly so defined herein.

[0027] CXL has been developed as a standard to provide an improved, high-speed CPU-to-device and CPU-to-memory interconnect that will accelerate next-generation data center performance and emerging computing applications, such as artificial intelligence, machine learning and other applications. CXL maintains memory coherency between the CPU memory space and the memory space of attached devices, which provides for resource sharing, thereby enabling high performance, reduced complexity and lower overall system costs.

[0028] CXL supports a set of protocols that include input/output (I/O) semantics (CXL.io), which are similar to PCIe I/O semantics, caching protocol semantics (CXL.cache), and memory access semantics (CXL.mem). The CXL.io protocol is equivalent to PCIe transport over the CXL protocol and CXL.mem is a memory access protocol that supports device-attached memory to provide a transactional interface between the CPU and the memory device. In some applications, the CXL protocols may be built upon the well-established and widely adopted PCIe infrastructure (e.g., PCIe 5.0), thereby leveraging the PCIe physical interface and enhancing the protocol with CXL to provide memory coherency between a CPU memory and an accelerator device memory.

[0029] With reference to FIG. 1, a compute express link (CXL) memory controller 100 includes, read bypass detection logic 115 to receive a plurality of CXL flits 108 from a CXL physical layer 110 of the CXL memory controller 100. The CXL flits 108 may be derived from data packets received over a PCIe/CXL serializer/deserializer (SerDes) interface 105 from a CPU or other host device.

[0030] CXL flits (flow control units) are link layer data packets formatted for use over interconnected links, such as PCIe-based or CXL-based links. In a particular example, CXL flits are known to be comprised of 528 bits, which includes 64 bytes of data followed by 2 bytes of cyclic redundancy check (CRC) to check the integrity of the data bytes. In accordance with the CXL protocol, a CXL flit begins after the protocol identification (ProtID) field. The ProtID field

is used by the CXL.mem arbitration/multiplexing layer 125 to direct the CXL flit to the CXL.mem link layer 130.

[0031] With reference to FIG. 2, a CXL.cache/CXL.mem flit includes a header that carries a Type bit 200 and Slot n information, which is used to determine if the flit is a protocol flit and if it may comprise a M2S Req (Master to Subordinate request). With reference to FIG. 3 and FIG. 4, if Slot 0 has a field value of 3'b101 300, it indicates that the flit is H5 format 400 and is carrying a CXL.mem Req.

[0032] The M2S Req itself is only 87 bits. Adding header bytes of 4 bytes plus Protocol ID of 2 bytes, means that it is necessary to collect a total of 135 bits (48 bits + 87 bits) to be able to detect a memory read request in the CXL flit.

[0033] In standard operation of a CXL controller, that does not implement the read bypass path 120 of the present examples, which however has other elements which are found in CXL memory controller 100, CXL flits received at a physical layer of the CXL memory controller 110 that are carrying a memory read request (CXL.mem Req.) are transmitted to a CXL.mem arbitration/multiplexing layer 125 and the CXL.mem arbitration/multiplexing layer 125 then transmits the CXL flits to the CXL.mem link layer 130. The CXL.mem link layer 130 checks each of CXL flits to verify that they are not all-data flits (i.e., do not contain a header) and that CRC for the CXL flit is correct. If the CXL flit passes these verifications, the CXL.mem link layer 130 then transmits the read request to a CXL.mem transaction/application layer 135. The CXL.mem transaction/application layer 135 then generates a read command and forwards the read command to a memory controller and physical layer 140. The memory controller and physical layer 140 then generates a memory read command on the memory interface device 147. The memory controller and physical layer 140 also generates an activate command on the memory interface 147, if the memory device 145 page is not already open, which allows the CPU host to access the memory device 145 through the memory interface 147, as controlled by the CXL memory controller 100. In this standard implementation, undesirable latency exists in the read data path between the CXL physical layer 110 and the CXL.mem transaction/application layer 135.

[0034] As shown in FIG. 1 a read request bypass path 120, including read bypass detection logic 115, connecting the CXL physical layer 110 to the transaction/application layer 135 is implemented in the CXL memory controller 100. As shown, the read request bypass path bypasses the CXL.mem arbitration/multiplexing layer 125 of the CXL memory controller 100 and the link layer 130 of the CXL memory controller 100. The read bypass detection logic 115 receives a plurality of CXL flits 108 from the CXL physical layer 110 and analyzes each of the received plurality of CXL flits 108 to identify a bypass memory read request from the plurality of CXL flits 108. Detecting a master to subordinate (M2S) request having a memory read operation code in the CXL flit 108 identifies the bypass memory read request of the CXL flit 108. Read bypass detection logic 115, upon detection of a bypass memory read request from the plurality of CXL flits 108, forwards the bypass memory read request over the read request bypass path 120 directly to CXL.mem transaction/application layer 135.

[0035] The physical layer 110 of the CXL memory controller 100 receives a plurality of data packets 102 from the PCIe/CXL SerDes Interface 105, derives the plurality of CXL flits 108 and transmits the plurality of CXL flits 108 both to the read bypass detection logic 115 and to the CXL.mem arbitration/multiplexing layer 125 of the CXL memory controller 100. As described above, the CXL.mem arbitration/multiplexing layer 125 identifies one or more link layer memory read requests from the plurality of CXL flits and transmits the one or more link layer memory read requests to the CXL.mem link layer 130. The CXL.mem link layer 130 performs a cyclic redundancy check (CRC) on each of the one or more link layer memory read requests, transmits the link layer memory read requests that pass the CRC to the CXL.mem transaction/application layer 135 of the CXL memory controller 100 and discards the link layer memory read requests that fail the CRC.

[0036] Upon receiving a bypass memory read request from the read bypass detection logic 115, the CXL.mem transaction/application layer 135 of the CXL memory controller 100 forwards a read command to the memory controller and physical layer 140. The memory controller and physical layer 140 then generates a memory read command and a memory activate command on the memory interface 147 of a memory device 145 associated with the CXL memory controller

100 in response to the bypass memory read request received at the transaction/application layer 135 over read request bypass path 135 when a read request queue 137 is empty. The CXL.mem transaction/application layer 135 then receives read data from the memory device 145 over the memory interface 147 as controlled by the memory controller and physical layer 140 in response to the memory read command. The CXL.mem transaction/application layer 135 forwards the read data received at the CXL.mem transaction/application layer 135 to the CXL.mem link layer 130 when there is a link layer memory read request at the CXL.mem transaction/application layer 135 that matches the bypass memory read request that generated the memory read command. In a particular example, the memory controller and physical layer 140 may be a DDR memory controller and physical layer, the memory interface 147 may be a DDR interface and the memory device 145 may be a DDR device.

[0037] The CXL.mem transaction/application layer 135 does not generate the memory read command in response to the bypass memory read request when the read request queue 137 is not empty and discards the bypass memory read request. The CXL specification defines M2S Req/MemSpecReq request, which can be used to issue speculative reads to memory devices. Memory speculative reads may be issued in order to initiate a memory access before the CXL memory controller 100 has resolved any coherence issues in the memory device 145 in order to reduce latency. However, the read data can only be returned from the memory device 145 in response to the speculative read if a matching MemRd request has been received at the CXL.mem transaction/memory layer 135 of the CXL memory controller 100. In operation, upon receiving a bypass memory read request at the CXL.mem transaction/application layer 135, the CXL.mem transaction/application layer 135 does not consume a request buffer entry. The request buffer entry is needed for the link layer flow control and is expected to be consumed by the forthcoming link layer M2S request, i.e., the matching MemRd request received from the CXL.mem link layer 130. If the read request queue 137 is not empty, then, as indicated above, the transaction/application layer 135 discards the bypass memory read request. If the read request queue 137 is empty, then the bypass memory read command is forwarded directly to the memory controller and physical layer 140.

[0038] Additionally, the CXL.mem transaction/application layer 135 discards the read data received at the CXL.mem transaction/application layer in response to the bypass memory read request when there is not a link layer memory read request at the CXL.mem transaction/application layer 135 that matches the bypass memory read request. All bypass memory read requests received at the CXL.mem transaction/application layer 135 are expected to be shortly followed by an identical memory read request from the link layer 130. If the CXL.mem transaction/application layer 135 receives a memory read request from the link layer 130 and it matches a pending bypass memory read request at the CXL.mem transaction/application layer 135, then the CXL.mem transaction/application layer 135 discards the memory read request from the link layer 130 and recycles the link layer credit. As such, the CXL.mem transaction/application layer 135 forwards the read data from the memory device 145 to the link layer 130 only if a matching memory read request from the link layer 130 has been received at the CXL.mem transaction/application layer 135. If no matching memory read request from the link layer 130 has been received at the CXL.mem transaction/application layer 135, then either the read bypass detection logic 115 erroneously detected a bypass memory read request from an all-data flit, or the CXL.mem link layer 130 detected a CRC error, or another uncorrectable error occurred in the CXL.mem link layer 130. In these cases, the CXL.mem transaction/application layer 135 discards the read data associated with the bypass memory read request. This situation is considered a non-fatal condition and the CXL.mem transaction/application layer 135 generates a debug event in response.

[0039] It is possible that the bytes following the ProtID do not contain a .mem flit with a header slot and the flit will be considered an all-data flit. In an all-data flit, the data may be aliased such that the read bypass detection logic 115 detects a nonexistent bypass memory read request. In this case, when the bypass memory read request is forwarded to the CXL.mem transaction/application layer 135, the CXL.mem transaction/application layer 135 may process the bypass memory read request and issue the read command to the memory interface 147. The read data received in response to the false detection will be subsequently discarded by the CXL.mem transaction/application layer 135. However, the probability of a false detection of this type is

extremely rare, and therefore the impact to the bandwidth of the memory device 145 due to a false detection is negligible.

[0040] The CXL.mem transaction/application layer 135 also discards bypass memory read requests that do not fall within a valid address space of the memory device 145 and does not generate the memory read command on the memory device interface 147 when an address space of the bypass memory read request is not valid.

[0041] FIG. 5A and FIG. 5B illustrate a flow diagram 500 of a method for reducing read latency in a CXL memory controller, such as the CXL memory controller 100 of FIG. 1.

[0042] At operation 502, the method begins by receiving a plurality of data packets at a physical layer of a CXL memory controller. With reference to FIG. 1, a physical layer 110 of the CXL memory controller 100 may receive a plurality of data packets 102 from the PCIe/CXL SerDes interface 105.

[0043] At operation 505, the method continues by deriving a plurality of Compute Express Link (CXL) flow control units (flits) from the plurality of data packets received at the physical layer of a CXL memory controller. With reference to FIG. 1, the physical layer 110 of the CXL memory controller 100 may derive a plurality of flits 108 from the plurality of received data packets 102.

[0044] At operation 510, the method continues by transmitting each of the received plurality of CXL flits to read bypass detection logic of the CXL memory controller and at operation 515 by analyzing each of the plurality of CXL flits at the read bypass detection logic to identify a bypass memory read request from the plurality of CXL flits. With reference to FIG. 1, the plurality of CXL flits 108 may be received at the read bypass detection logic 115 of the CXL memory controller 100 and the read bypass detection logic 115 may analyze each of the plurality of CXL flits 108 at the read bypass detection logic 115 to identify a bypass memory read request from the plurality of CXL flits 108.

[0045] The method continues at operation 520 by transmitting the bypass memory read request over a read request bypass path directly to a transaction/application layer of the CXL

memory controller, wherein the read request bypass path does not include an arbitration/multiplexing layer and a link layer of the CXL memory controller. With reference to FIG. 1, the bypass memory read request may be transmitted over a read request bypass path 120 directly to the CXL.mem transaction/application layer 135 of the CXL memory controller 100, thereby bypassing the CXL.mem arbitration/multiplexing layer 125 and the CXL.mem link layer 130.

[0046] At operation 525, the method continues, when a read request queue of the CXL memory controller is empty, generating a memory read command on an interface of a memory device attached to the CXL memory controller in response to the bypass memory read request received at the transaction/application layer of the CXL memory controller. With reference to FIG. 1, when a read request queue 137 of the CXL memory controller 100 is empty, in response to the bypass memory read request a read command may be generated by the CXL.mem transaction/layer 135 and forwarded to the memory controller and physical layer 140. The memory controller and physical layer 140 may then generate a memory read command on the memory interface 147 of a memory device 145 in response to the bypass memory read request received at the CXL.mem transaction/application layer 135 of the CXL memory controller 100. The memory controller and physical layer 140 may also generate an activate command on the memory interface 147 prior to generating the memory read command on the memory interface, if the memory device page is not already open.

[0047] At operation 530, the method continues by receiving read data from the memory device at the transaction/application layer in response to the memory read command and the method concludes at operation 535, when there is a link layer memory read request at the transaction/application layer that matches the bypass memory read request that generated the memory read command, forwarding the read data received at the transaction/application layer to the link layer of the CXL memory controller. Optionally, if there is not a link layer memory read request at the transaction/application layer that matches the bypass memory read request that generated the memory read command, the read data received at the transaction/application layer is discarded. With reference to FIG. 1, read data received from the memory device 145 at the

CXL.mem transaction/application layer 135 in response to the memory read command is forwarded to the CXL.mem link layer 130 of the CXL memory controller 100 when there is a link layer memory read request at the CXL.mem transaction/application layer 135 that matches the bypass memory read request that generated the memory read command.

[0048] FIG. 6A and FIG. 6B are a set of flow diagrams 600 illustrating an example method for reducing read latency in a CXL memory controller and for selectively discarding bypass memory read requests.

[0049] At operation 605, the method begins by receiving a plurality of Compute Express Link (CXL) flow control units (flits) at a physical layer of a CXL memory controller. With reference to FIG. 1, a CXL physical layer 110 of the CXL memory controller 100 may receive a plurality of flits.

[0050] At operation 610, the method continues by transmitting each of the received plurality of CXL flits to read bypass detection logic of the CXL memory controller and at operation 615 by analyzing each of the plurality of CXL flits at the read bypass detection logic to identify a bypass memory read request from the plurality of CXL flits. With reference to FIG. 1, the plurality of CXL flits 108 may be received at the read bypass detection logic 115 of the CXL memory controller 100 and the read bypass detection logic 115 may analyze each of the plurality of CXL flits 108 at the read bypass detection logic to identify a bypass memory read request from the plurality of CXL flits 108.

[0051] The method continues at operation 620 by transmitting the bypass memory read request over a read request bypass path directly to a transaction/application layer of the CXL memory controller, wherein the read request bypass path does not include an arbitration/multiplexing layer and a link layer of the CXL memory controller. With reference to FIG. 1, the bypass memory read request may be transmitted over a read request bypass path 120 directly to the CXL.mem transaction/application layer 135 of the CXL memory controller 100, thereby bypassing the CXL.mem arbitration/multiplexing layer 125 and the CXL.mem link layer 130.

[0052] At operation 625, the method continues by determining if a read request queue of the CXL memory controller is empty. If it is determined that the read request queue of the CXL memory controller is empty at operation 625, then the method continues at operation 630. If it is determined that the read request queue of the CXL memory controller is not empty, then the method concludes at operation 635 by not generating a memory read command on the interface of the memory device attached to the CXL memory controller in response to the bypass memory read request and discarding the bypass memory read request. With reference to FIG. 1, the read request queue 137 may be determined to be empty or not empty by the CXL.mem transaction/application layer 135.

[0053] At operation 630, the method continues by determining if an address space of the bypass memory read request is valid. If the address space is determined to be valid, then the method continues at operation 645 of FIG. 6B. If it is determined that the address space of the bypass memory read request is not valid, the method concludes at operation 640 by discarding the bypass memory read request. With reference to FIG. 1, the transaction/application layer 135 may determine if the address space of the bypass memory read request is valid and if not, discard the bypass memory read request.

[0054] The method continues at operation 645 by generating a memory read command on an interface of a memory device attached to the CXL memory controller in response to the bypass memory read request received at the transaction/application layer of the CXL memory controller and at operation 650 by receiving read data from the memory device at the transaction layer in response to the memory read command. With reference to FIG. 1, a read command may be generated by the CXL.mem transaction/application layer 135 of the CXL memory controller 100 in response to receiving the bypass memory read request. The read command may then be forwarded to the memory controller and physical layer 140. The memory controller and physical layer 140 may then generate a memory read command on an interface 147 of a memory device 145. As such, a memory read command is generated on the interface of a memory device attached to the CXL memory controller in response to the bypass memory read request received at the transaction/application layer 135 of the CXL memory controller 100 and read data may be received

from the memory device 145.

[0055] At operation 655 it is determined if there is a link layer memory read request at the transaction/application layer that matches the bypass memory read request that generated the memory read command. If there is a matching link layer memory read request, then the method concludes at operation 660 by forwarding the read data received at the transaction/application layer to the link layer of the CXL memory controller 360. If there is not a matching link layer memory read request, then method concludes at operation 665 by discarding the read data received at the transaction/application layer. With reference to FIG. 1, if there is a memory read request from the CXL.mem link layer 130 that matches the bypass memory read request at the CXL.mem transaction/application layer 135, then the CXL.mem transaction/application layer 135 forwards the read data to the CXL.mem link layer 130. Alternatively, if there is not a matching link layer memory read request at the CXL.mem transaction/application layer 135, then the CXL.mem transaction/application 135 discards the read data from the memory device.

[0056] FIG. 7 is a flow diagram illustrating an example method 700 for reducing read latency in a CXL memory controller and for selectively discarding link layer memory read requests.

[0057] At operation 705, the method begins by transmitting the plurality of CXL flits received at the physical layer of the CXL memory controller to the arbitration/multiplexing layer of the CXL memory controller. With reference to FIG. 1, the CXL flits 108 received at the CXL physical layer 110 are transmitted to the CXL.mem arbitration/multiplexing layer 125.

[0058] The method continues at operation 710 by identifying, at the arbitration/multiplexing layer of the CXL memory controller, one or more link layer memory read requests from the plurality of CXL flits, at operation 715 by transmitting the identified one or more link layer memory read requests to the link layer of the CXL memory controller, at operation 720 by performing a cyclic redundancy check (CRC) on each of the identified and transmitted one or more link layer memory read requests, and at operation 725 by transmitting the link layer memory read requests that pass the CRC to the transaction/application layer of the CXL memory controller.

The method concludes at operation 730 by discarding the link layer memory read requests that fail the CRC. With reference to FIG. 1, the CXL.mem arbitration/multiplexing layer 135 may identify one or more link layer memory read requests from the CXL flits 108 and transmit the identified one or more link layer memory read request to the CXL.mem link layer 130. A CRC check may be performed on the identified one or more link layer memory read request and the link layer memory read request that fail the CRC may be discarded.

[0059] FIG. 8A and FIG. 8B are a set of flow diagrams 800 illustrating a method for reducing read latency in a CXL memory controller and for matching link layer memory read requests to bypass memory read requests, in accordance with an example of the present invention.

[0060] At operation 805, the method begins by receiving a plurality of Compute Express Link (CXL) flow control units (flits) at a physical layer of a CXL memory controller. With reference to FIG. 1, a CXL physical layer 110 of the CXL memory controller 100 may receive a plurality of flits 108.

[0061] At operation 810, the method continues by transmitting each of the received plurality of CXL flits to read bypass detection logic of the CXL memory controller and at operation 815 by analyzing each of the plurality of CXL flits at the read bypass detection logic to identify a bypass memory read request from the plurality of CXL flits. With reference to FIG. 1, the plurality of CXL flits 108 may be received at the read bypass detection logic 115 of the CXL memory controller 100 and the read bypass detection logic 115 may analyze each of the plurality of CXL flits 108 at the read bypass detection logic 115 to identify a bypass memory read request from the plurality of CXL flits 108.

[0062] The method continues at operation 820 by transmitting the bypass memory read request over a read request bypass path directly to a transaction/application layer of the CXL memory controller, wherein the read request bypass path does not include an arbitration/multiplexing layer and a link layer of the CXL memory controller. With reference to FIG. 1, the bypass memory read request may be transmitted over a read request bypass path 120 directly to the CXL.mem transaction/application layer 135 of the CXL memory controller 100,

thereby bypassing the CXL.mem arbitration/multiplexing layer 125 and the CXL.mem link layer 130.

[0063] At operation 825, the method continues, when a read request queue of the CXL memory controller is empty, generating a memory read command on an interface of a memory device attached to the CXL memory controller in response to the bypass memory read request received at the transaction/application layer of the CXL memory controller and when the read request queue of the CXL memory controller is not empty, discarding the bypass memory read request. With reference to FIG. 1, when a read request queue 137 of the CXL memory controller 100 is empty, a memory read command may be generated on an interface 147 of a memory device 145 in response to the bypass memory read request received at the transaction/application layer 135 of the CXL memory controller 100. Alternatively, when the read request queue 137 is not empty, the transaction/application layer 135 may discard the bypass memory read request before generating the memory read command on the interface 147 of the memory device 145.

[0064] At operation 830, the method continues by receiving read data from the memory device at the transaction/application layer in response to the memory read command and the method concludes at operation 835, when there is a link layer memory read request at the transaction/application layer that matches the bypass memory read request that generated the memory read command, forwarding the read data received at the transaction/application layer to the link layer of the CXL memory controller. Additionally, if there is not a link layer memory read request at the transaction/application layer that matches the bypass memory read request that generated the memory read command, the read data received at the transaction/application layer is discarded. With reference to FIG. 1, read data received from the memory device 145 at the CXL.mem transaction/application layer 135 in response to the memory read command is forwarded to the CXL.mem link layer 130 of the CXL memory controller 100 when there is a link layer memory read request at the CXL.mem transaction/application layer 135 that matches the bypass memory read request that generated the memory read command. Alternatively, the CXL.mem transaction/application 135 discards the read data when there is not a link layer memory read request at the transaction/application layer 135 that matches the bypass memory read request

that generated the memory read command.

[0065] In various examples, portions of the system of the present examples may be implemented in a Field Programmable Gate Array (FPGA) or Application Specific Integrated Circuit (ASIC). As would be appreciated by one skilled in the art, various functions of circuit elements may also be implemented as processing steps in a software program. Such software may be employed in, for example, a digital signal processor, a network processor, a microcontroller or general-purpose computer.

[0066] Unless specifically stated otherwise as apparent from the discussion, it is appreciated that throughout the description, discussions utilizing terms such as “receiving”, “determining”, “generating”, “limiting”, “sending”, “counting”, “classifying”, or the like, can refer to the action and processes of a computer system, or similar electronic computing device, that manipulates and transforms data represented as physical (electronic) quantities within the computer system’s registers and memories into other data similarly represented as physical quantities within the computer system memories or registers or other such information storage, transmission, or display devices.

[0067] The present examples may be embodied on various computing platforms that perform actions responsive to software-based instructions. The following provides an antecedent basis for the information technology that may be utilized to enable the present examples.

[0068] The method of the present examples may be stored on a computer readable medium which may be a computer readable signal medium or a computer readable storage medium. A computer readable storage medium may be, for example, but not limited to, an electronic, magnetic, optical, electromagnetic, infrared, or semiconductor system, apparatus, or device, or any suitable combination of the foregoing. More specific examples (a non-exhaustive list) of the computer readable storage medium would include the following: an electrical connection having one or more wires, a portable computer diskette, a hard disk, a random access memory (RAM), a read-only memory (ROM), an erasable programmable read-only memory (EPROM or Flash memory), an optical fiber, a portable compact disc read-only memory (CD-ROM), an optical

storage device, a magnetic storage device, or any suitable combination of the foregoing. In the context of this document, a computer readable storage medium may be any non-transitory, tangible medium that can contain, or store a program for use by or in connection with an instruction execution system, apparatus, or device.

[0069] A computer readable signal medium may include a propagated data signal with computer readable program code embodied therein, for example, in baseband or as part of a carrier wave. Such a propagated signal may take any of a variety of forms, including, but not limited to, electro-magnetic, optical, or any suitable combination thereof. A computer readable signal medium may be any computer readable medium that is not a computer readable storage medium and that can communicate, propagate, or transport a program for use by or in connection with an instruction execution system, apparatus, or device. However, as indicated above, due to circuit statutory subject matter restrictions, claims as a software product are those embodied in a non-transitory software medium such as a computer hard drive, flash-RAM, optical disk or the like.

[0070] Program code embodied on a computer readable medium may be transmitted using any appropriate medium, including but not limited to wireless, wire-line, optical fiber cable, radio frequency, etc., or any suitable combination of the foregoing. Computer program code for carrying out operations for aspects of the present example may be written in any combination of one or more programming languages, including an object-oriented programming language such as Java, C#, C++, Visual Basic or the like and conventional procedural programming languages, such as the “C” programming language or similar programming languages.

[0071] Aspects of the present examples are described below with reference to flowchart illustrations and/or block diagrams of methods, apparatus (systems) and computer program products. It will be understood that each block of the flowchart illustrations and/or block diagrams, and combinations of blocks in the flowchart illustrations and/or block diagrams, can be implemented by computer program instructions. These computer program instructions may be provided to a processor of a general-purpose computer, special purpose computer, or other programmable data processing apparatus to produce a machine, such that the instructions, which

execute via the processor of the computer or other programmable data processing apparatus, create means for implementing the functions/acts specified in the flowchart and/or block diagram block or blocks.

[0072] These computer program instructions may also be stored in a computer readable medium that can direct a computer, processor, or other programmable data processing apparatus, or other devices to function in a particular manner, such that the instructions stored in the computer readable medium produce an article of manufacture including instructions which implement the function/act specified in the flowchart and/or block diagram block or blocks.

[0073] The computer program instructions may also be loaded onto a computer, other programmable data processing apparatus, or other devices to cause a series of operational steps to be performed on the computer, other programmable apparatus or other devices to produce a computer implemented process such that the instructions which execute on the computer or other programmable apparatus provide processes for implementing the functions/acts specified in the flowchart and/or block diagram block or blocks.

[0074] Further, for purposes of discussing and understanding the examples, it is to be understood that various terms are used by those knowledgeable in the art to describe techniques and approaches. Furthermore, in the description, for purposes of explanation, numerous specific details are set forth in order to provide a thorough understanding. It will be evident, however, to one of ordinary skill in the art that the present examples may be practiced without these specific details. In some instances, well-known structures and devices are shown in block diagram form, rather than in detail. These examples are described in sufficient detail to enable those of ordinary skill in the art to practice the examples, and it is to be understood that other examples may be utilized, and that logical, mechanical, electrical, and other changes may be made without departing from the scope.

CLAIMS

What is claimed is:

1. A method for bypass memory read request detection, the method comprising:

receiving a plurality of data packets at a physical layer of a CXL memory controller;

deriving a plurality of Compute Express Link (CXL) flow control units (flits) from the plurality of data packets received at the physical layer of a CXL memory controller;

transmitting each of the received plurality of CXL flits to read bypass detection logic of the CXL memory controller;

analyzing each of the plurality of CXL flits at the read bypass detection logic to identify a bypass memory read request from the plurality of CXL flits;

transmitting the bypass memory read request over a read request bypass path directly to a transaction/application layer of the CXL memory controller, wherein the read request bypass path does not include an arbitration/multiplexing layer and a link layer of the CXL memory controller;

when a read request queue of the CXL memory controller is empty, generating a memory read command on an interface of a memory device attached to the CXL memory controller in response to the bypass memory read request received at the transaction/application layer of the CXL memory controller;

receiving read data from the memory device at the transaction/application layer in response to the memory read command; and

when there is a link layer memory read request at the transaction/application layer that matches the bypass memory read request that generated the memory read command, forwarding the read data received at the transaction/application layer to the link layer of the CXL memory controller.

2. The method of claim 1, comprising, when there is not a link layer memory read request at the transaction/application layer that matches the bypass memory read request that generated the memory read command, discarding the read data received at the transaction/application layer.
3. The method of claim 1, wherein analyzing each of the plurality of CXL flits at the read bypass detection logic of the CXL memory comprises detecting a master to subordinate (M2S) request having a memory read operation code in the CXL flit to identify the bypass memory read request.
4. The method of claim 1, comprising, when the read request queue of the CXL memory controller is not empty, not generating the memory read command on the interface of the memory device attached to the CXL memory controller and discarding the bypass memory read request.
5. The method of claim 1, comprising, discarding the link layer memory read request that matches the bypass memory read request that generated the memory read command.
6. The method of claim 1, comprising, discarding the bypass memory read request at the transaction/application layer and not generating the memory read command on the

memory device interface when an address space of the bypass memory read request is not valid.

7. The method of claim 1, comprising, transmitting an activate command on the memory device interface prior to generating the memory read command on the memory device interface.

8. The method of claim 1, comprising:

transmitting the plurality of CXL flits received at the physical layer of the CXL memory controller to the arbitration/multiplexing layer of the CXL memory controller;

identifying, at the arbitration/multiplexing layer of the CXL memory controller, one or more link layer memory read requests from the plurality of CXL flits;

transmitting the identified one or more link layer memory read requests to the link layer of the CXL memory controller;

performing a cyclic redundancy check (CRC) on each of the identified and transmitted one or more link layer memory read requests;

transmitting the link layer memory read requests that pass the CRC to the transaction/application layer of the CXL memory controller; and

discarding the link layer memory read requests that fail the CRC.

9. The method of claim 1, wherein the memory device attached to the CXL memory controller is a Double Data Rate (DDR) memory device.

10. A method for reading a memory device, the method comprising:

receiving a plurality of Compute Express Link (CXL) flow control units (flits) at a physical layer of a CXL memory controller;

transmitting each of the received plurality of CXL flits to read bypass detection logic of the CXL memory controller;

analyzing each of the received and transmitted plurality of CXL flits at the read bypass detection logic to identify a bypass memory read request from the plurality of CXL flits, wherein the bypass memory read request comprises an address space;

transmitting the bypass memory read request over a read request bypass path directly to a transaction/application layer of the CXL memory controller, wherein the read request bypass path does not include an arbitration/multiplexing layer and a link layer of the CXL memory controller;

discarding the bypass memory read request at the transaction/application layer when the address space of the bypass memory read request is not valid;

when a read request queue of the CXL memory controller is empty, generating a memory read command on an interface of a memory device attached to the CXL memory controller in response to the bypass memory read request received at the transaction/application layer of the CXL memory controller and when the read request queue of the CXL memory controller is not empty, discarding the bypass memory read request;

receiving read data from the memory device at the transaction/application layer in response to the memory read command; and

when there is a link layer memory read request at the transaction/application layer that matches the bypass memory read request that generated the memory read command, forwarding the read data received at the transaction/application layer to the link layer of the CXL memory controller and when there is not a link layer memory read request at the transaction/application layer that matches the bypass memory read request that generated the memory read command, discarding the read data received at the transaction/application layer.

11. The method of claim 10, comprising:

transmitting the plurality of CXL flits received at the physical layer of the CXL memory controller to the arbitration/multiplexing layer of the CXL memory controller;

identifying, at the arbitration/multiplexing layer of the CXL memory controller, one or more link layer memory read requests from the plurality of CXL flits;

transmitting the identified one or more link layer memory read requests to the link layer of the CXL memory controller; and

performing a cyclic redundancy check (CRC) on each of the one or more link layer memory read requests;

transmitting the link layer memory read requests that pass the CRC to the transaction/application layer of the CXL memory controller; and

discarding the link layer memory read requests that fail the CRC.

12. A compute express link (CXL) memory controller comprising:

read bypass detection logic to receive a plurality of CXL flits from a CXL physical layer of a CXL memory controller and to analyze each of the received plurality of CXL flits to identify a bypass memory read request from the plurality of CXL flits;

a read request bypass path comprising the read bypass detection logic, the read request bypass path connecting the CXL physical layer to a transaction/application layer of the CXL memory controller, the read request bypass path bypassing an arbitration/multiplexing layer of the CXL memory controller and a link layer of the CXL memory controller;

the transaction/application layer to:

generate a memory read command on an interface of a memory device associated with the CXL memory controller in response to the bypass memory read request received at the transaction/application layer when a read request queue is empty; receive read data from the memory device in response to the memory read command; and

forward the read data received at the transaction/application layer to the link layer when there is a link layer memory read request at the transaction/application layer that matches the bypass memory read request that generated the memory read command.

13. The CXL memory controller of claim 12, wherein the read bypass detection logic to analyze each of the plurality of CXL flits by detecting a master to subordinate (M2S) request having a memory read operation code in the CXL flit to identify the bypass memory read request.
14. The CXL memory controller of claim 12, wherein the transaction/application layer to discard the read data received at the transaction/application layer when there is not a link layer memory read request at the transaction/application layer that matches the bypass memory read request that generated the memory read command.
15. The CXL memory controller of claim 12, wherein the transaction/application layer to not generate the memory read command on the interface of the memory device when the read request queue is not empty and to discard the bypass memory read request.
16. The CXL memory controller of claim 12, wherein the transaction/application layer to discard the link layer memory read request that matches the bypass memory read request that generated the memory read command.
17. The CXL memory controller of claim 12, wherein the transaction/application layer to discard the bypass memory read request and to not generate the memory read command on the memory device interface when an address space of the bypass memory read request is not valid.

18. The CXL memory controller of claim 12, wherein the transaction/application layer to transmit an activate command on the memory device interface prior to generating the memory read command on the memory device interface.
19. The CXL memory controller of claim 12, comprising:
- the physical layer of the CXL memory controller to receive the plurality of CXL flits, to transmit the plurality of CXL flits to the read bypass detection logic and to transmit the plurality of CXL flits to the arbitration/multiplexing layer of the CXL memory controller;
 - the arbitration/multiplexing layer to identify one or more link layer memory read requests from the plurality of CXL flits and to transmit the one or more link layer memory read requests to the link layer; and
 - the link layer to perform a cyclic redundancy check (CRC) on each of the one or more link layer memory read requests, to transmit the link layer memory read requests that pass the CRC to the transaction/application layer of the CXL memory controller and to discard the link layer memory read requests that fail the CRC.
20. The CXL memory controller of claim 12, wherein the memory device is a Double Data Rate (DDR) memory device.

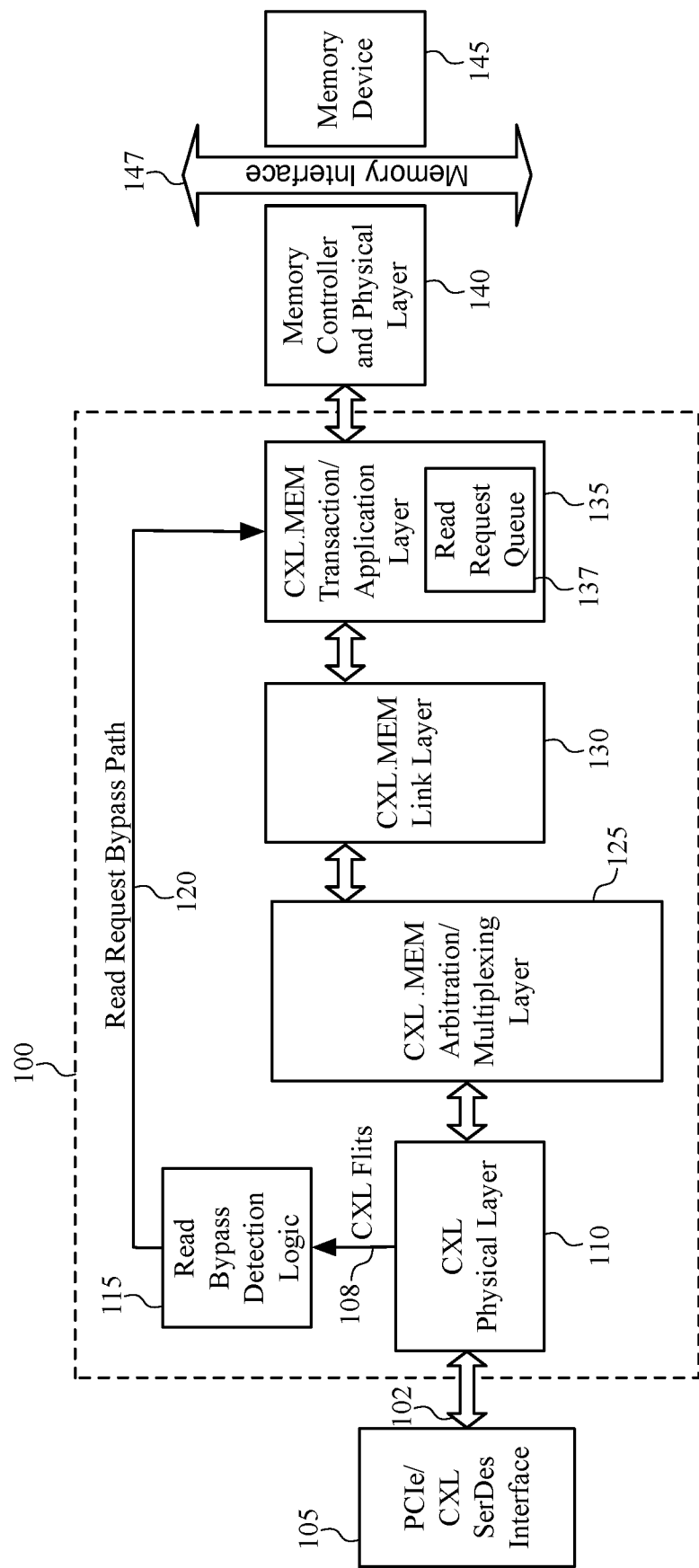


FIG. 1

CXL.cache/CXL.mem Flit Header Definition

200

Field Name	Brief Description	Size
Type	This field distinguishes between a Protocol or a Control Flit	1
Ak	This is an acknowledgment of 8 successful flit transfers Reserved for Retry, and Init control flits	1
BE	Byte Enable (Reserved for control flits)	1
Sz	Size (Reserved for control flits)	1
ReqCrd	Request Credit Return Reserved for Retry, and Init control flits	4
DataCrd	Data Credit Return Reserved for Retry, and Init control flits	4
RspCrd	Response Credit Return Reserved for Retry, and Init control flits	4
Slot 0	Slot 0 Format Type (Reserved for control flits)	3
Slot 1	Slot 1 Format Type (Reserved for control flits)	3
Slot 2	Slot 2 Format Type (Reserved for control flits)	3
Slot 3	Slot 3 Format Type (Reserved for control flits)	3
RSVD	Reserved	4
Total		32

FIG. 2

Slot Format Field Encoding

300

Slot Format Encoding	H2D/M2S		D2H/S2M	
	Slot 0	Slots 1,2 and 3	Slot 0	Slots 1, 2 and 3
000	H0	G0	H0	G0
001	H1	G1	H1	G1
010	H2	G2	H2	G2
011	H3	G3	H3	G3
100	H4	G4	H4	G4
101	H5	G5	H5	G5
110	H6	RSVD	H6	G6
111	RSVD	RSVD	RSVD	RSVD

FIG. 3

H2D/M2S Slot Formats

400

Format to Req Type Mapping	H2D/M2S	
	Type	Size
H0	CXL.cache Req + CXL.cache Resp	96
H1	CXL.cache Data Header + 2 CXL.cache Resp	88
H2	CXL.cache Req + CXL.cache Data Header	88
H3	4 CXL.cache Data Header	96
H4	CXL.mem Rwd Header	87
H5	CXL.mem Req Only	87
H6	MAC slot used for link integrity.	96
G0	CXL.cache/ CXL.mem Data Chunk	128
G1	4 CXL.cache Resp	128
G2	CXL.cache Req + CXL.cache Data Header + CXL.cache Resp	120
G3	4 CXL.cache Data Header + CXL.cache Resp	128
G4	CXL.mem Req + CXL.cache Data Header	111
G5	CXL.mem Rwd Header + CXL.cache Resp	119

FIG. 4

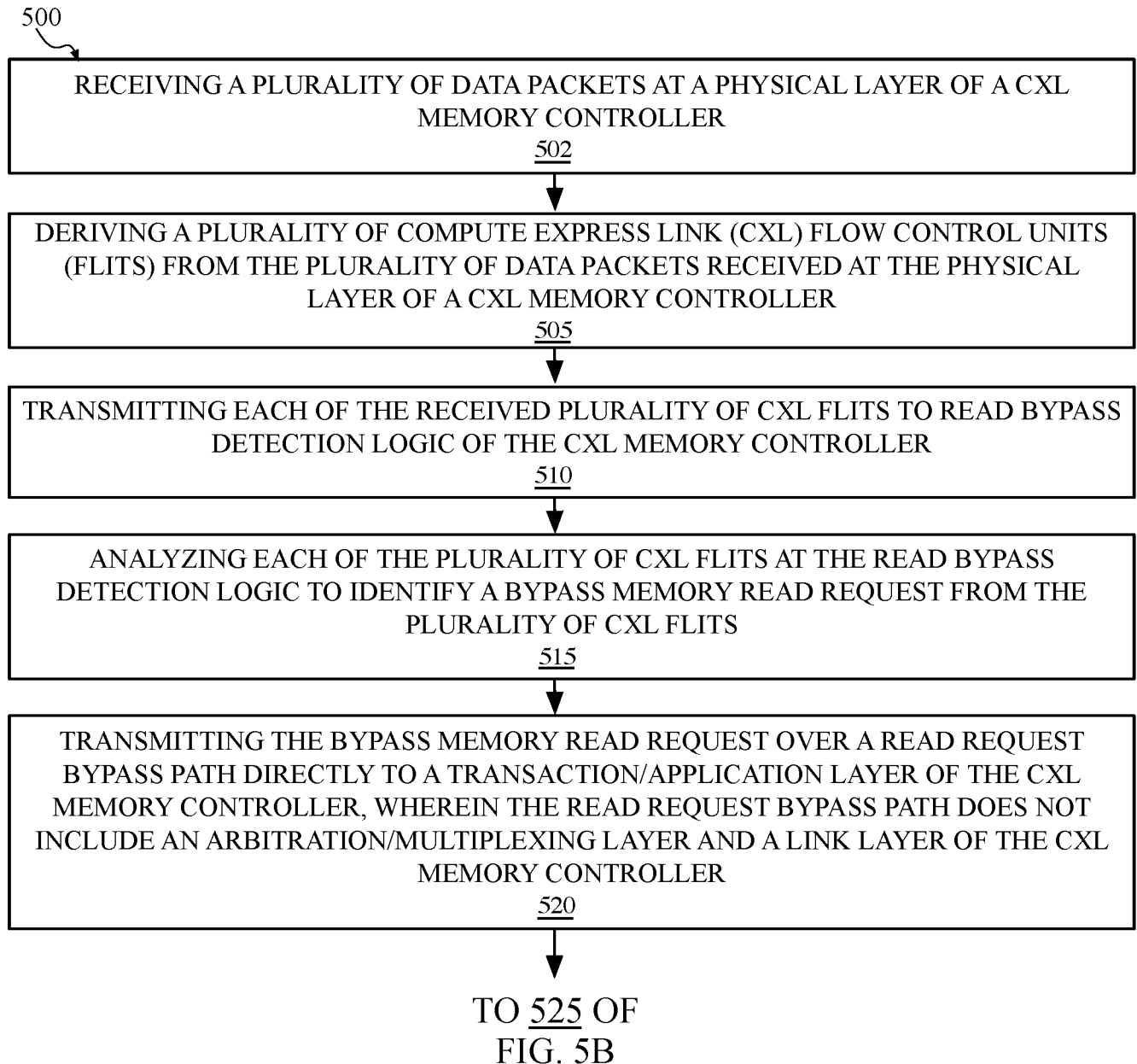


FIG. 5A

FROM 520
OF FIG. 5A



WHEN A READ REQUEST QUEUE OF THE CXL MEMORY CONTROLLER IS EMPTY, GENERATING A MEMORY READ COMMAND ON AN INTERFACE OF A MEMORY DEVICE ATTACHED TO THE CXL MEMORY CONTROLLER IN RESPONSE TO THE BYPASS MEMORY READ REQUEST RECEIVED AT THE TRANSACTION/APPLICATION LAYER OF THE CXL MEMORY CONTROLLER (OPT. GENERATING AN ACTIVATE COMMAND ON THE MEMORY DEVICE INTERFACE PRIOR TO GENERATING THE MEMORY READ COMMAND ON THE MEMORY DEVICE INTERFACE)

525



RECEIVING READ DATA FROM THE MEMORY DEVICE AT THE TRANSACTION/APPLICATION LAYER IN RESPONSE TO THE MEMORY READ COMMAND

530



WHEN THERE IS A LINK LAYER MEMORY READ REQUEST AT THE TRANSACTION/APPLICATION LAYER THAT MATCHES THE BYPASS MEMORY READ REQUEST THAT GENERATED THE MEMORY READ COMMAND, FORWARDING THE READ DATA RECEIVED AT THE TRANSACTION/APPLICATION LAYER TO THE LINK LAYER OF THE CXL MEMORY CONTROLLER (OPT. DISCARDING THE LINK LAYER MEMORY READ REQUEST THAT MATCHES THE BYPASS MEMORY READ REQUEST THAT GENERATED THE MEMORY READ COMMAND)

535

FIG. 5B

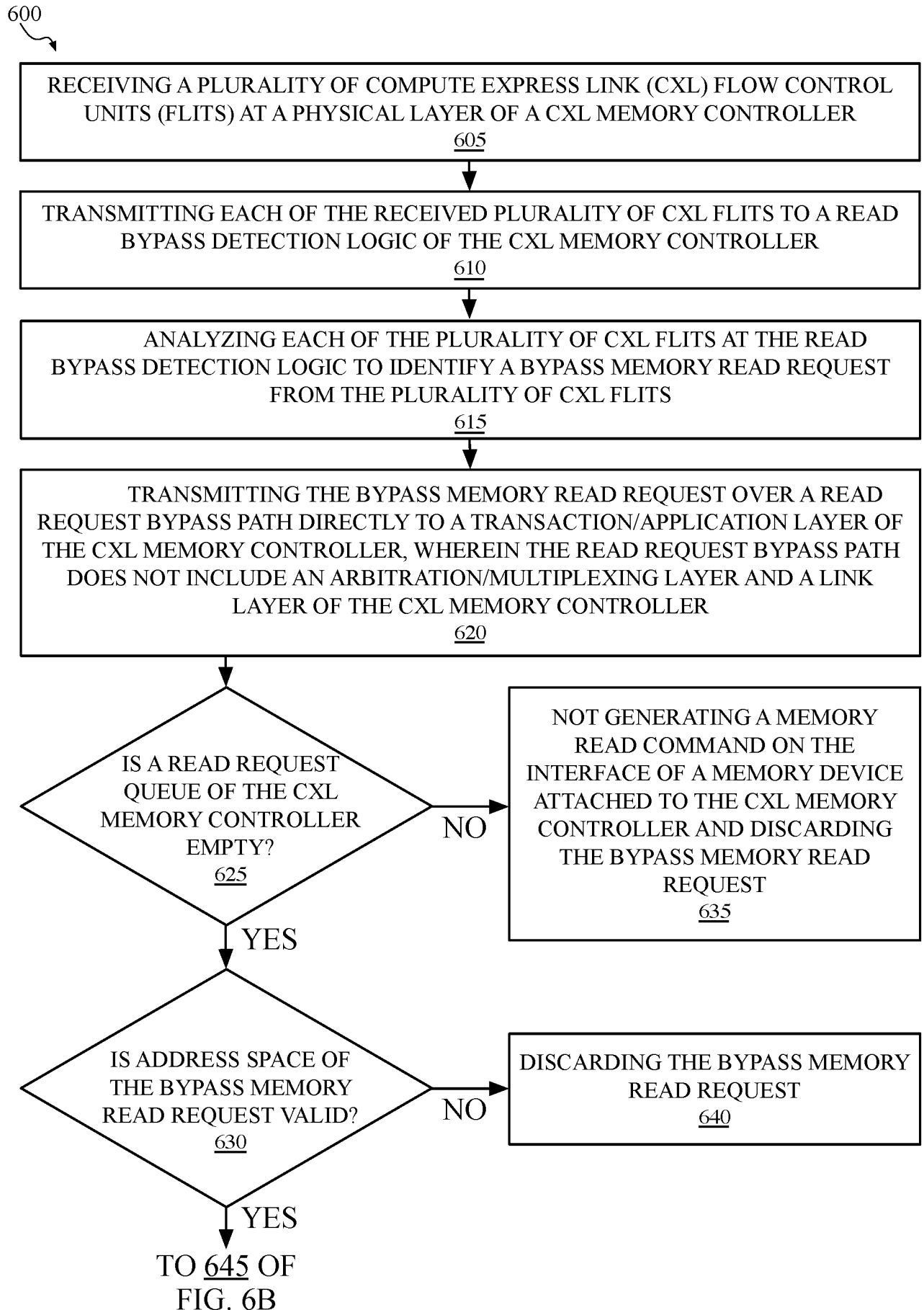


FIG. 6A

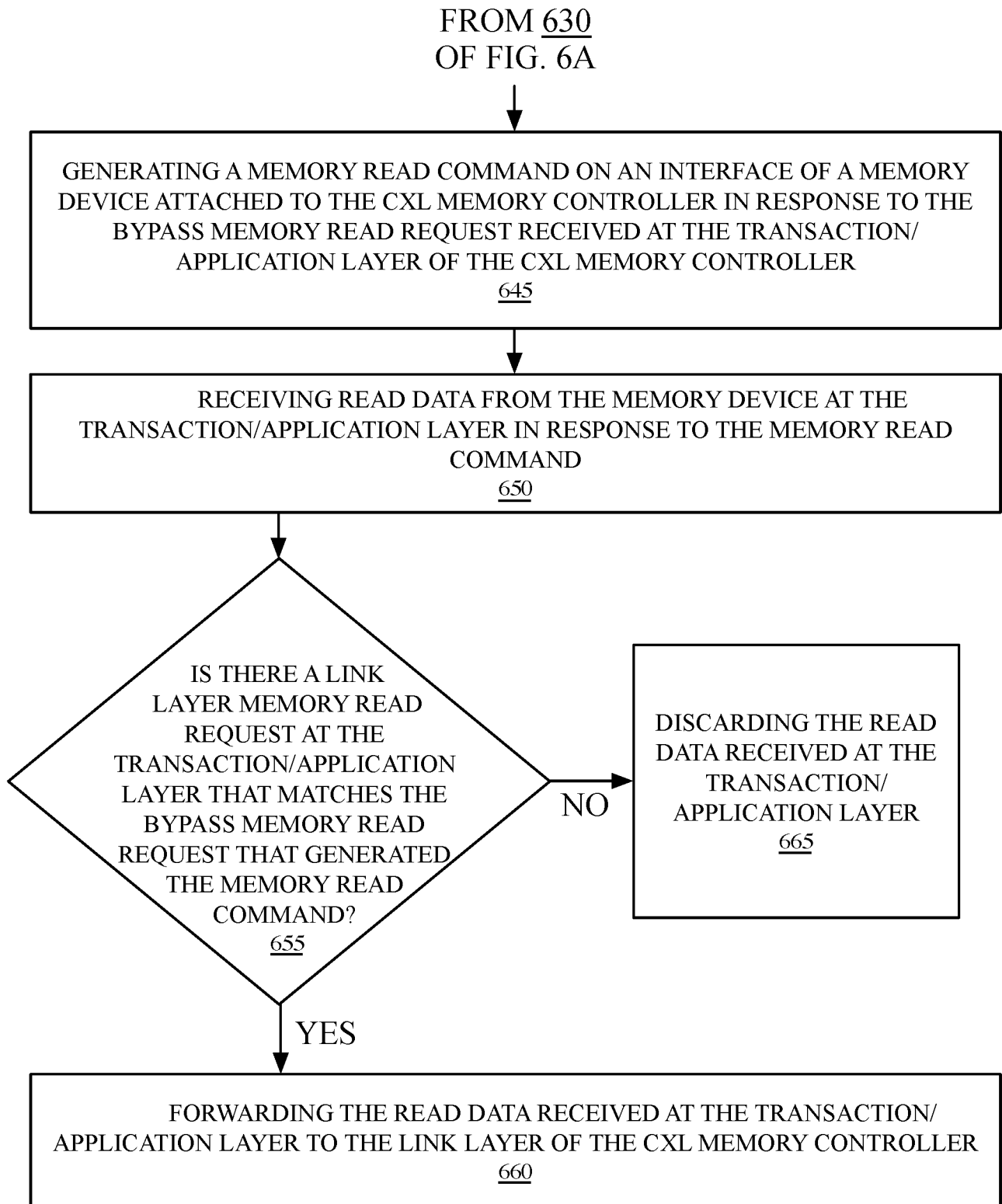


FIG. 6B

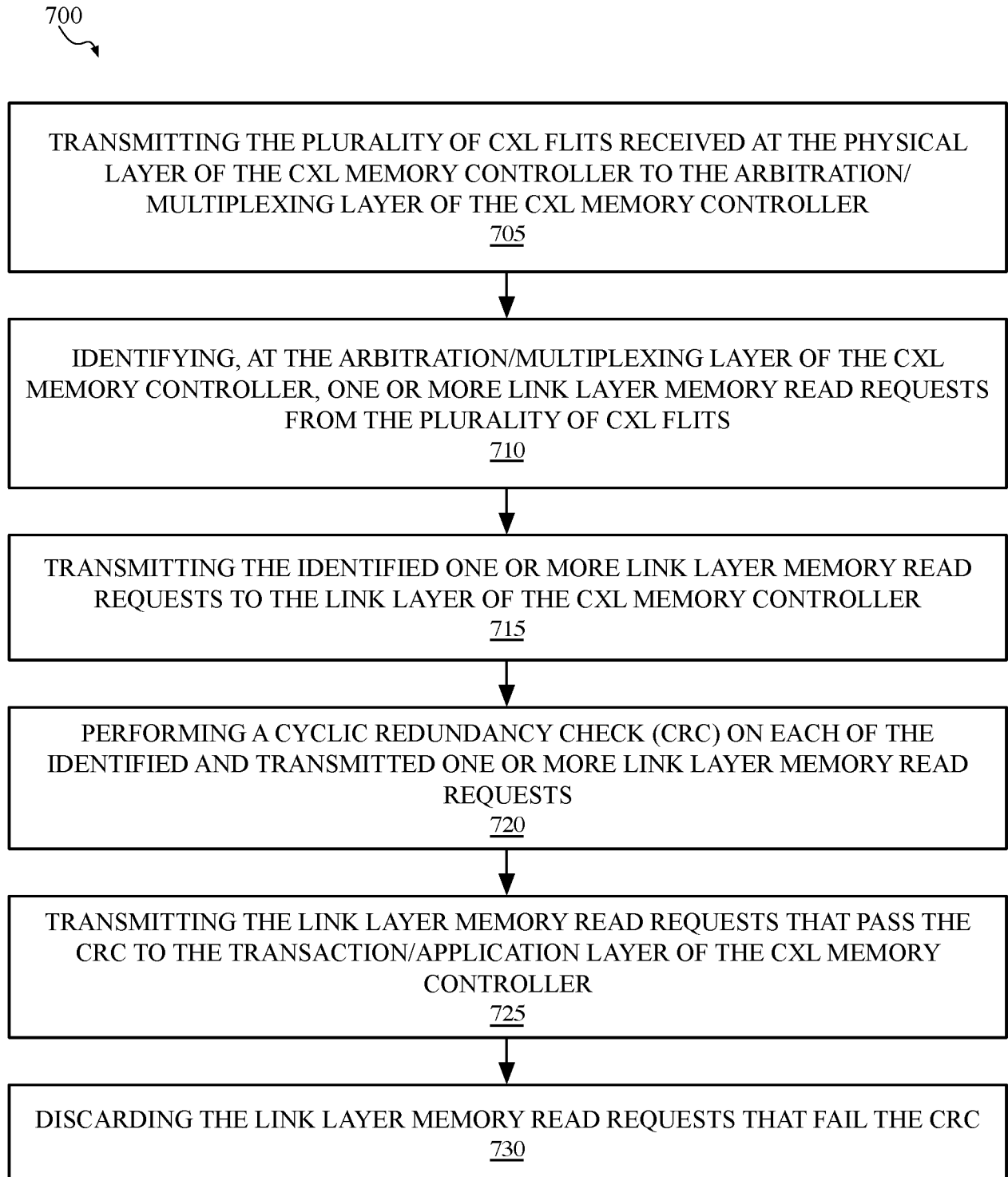
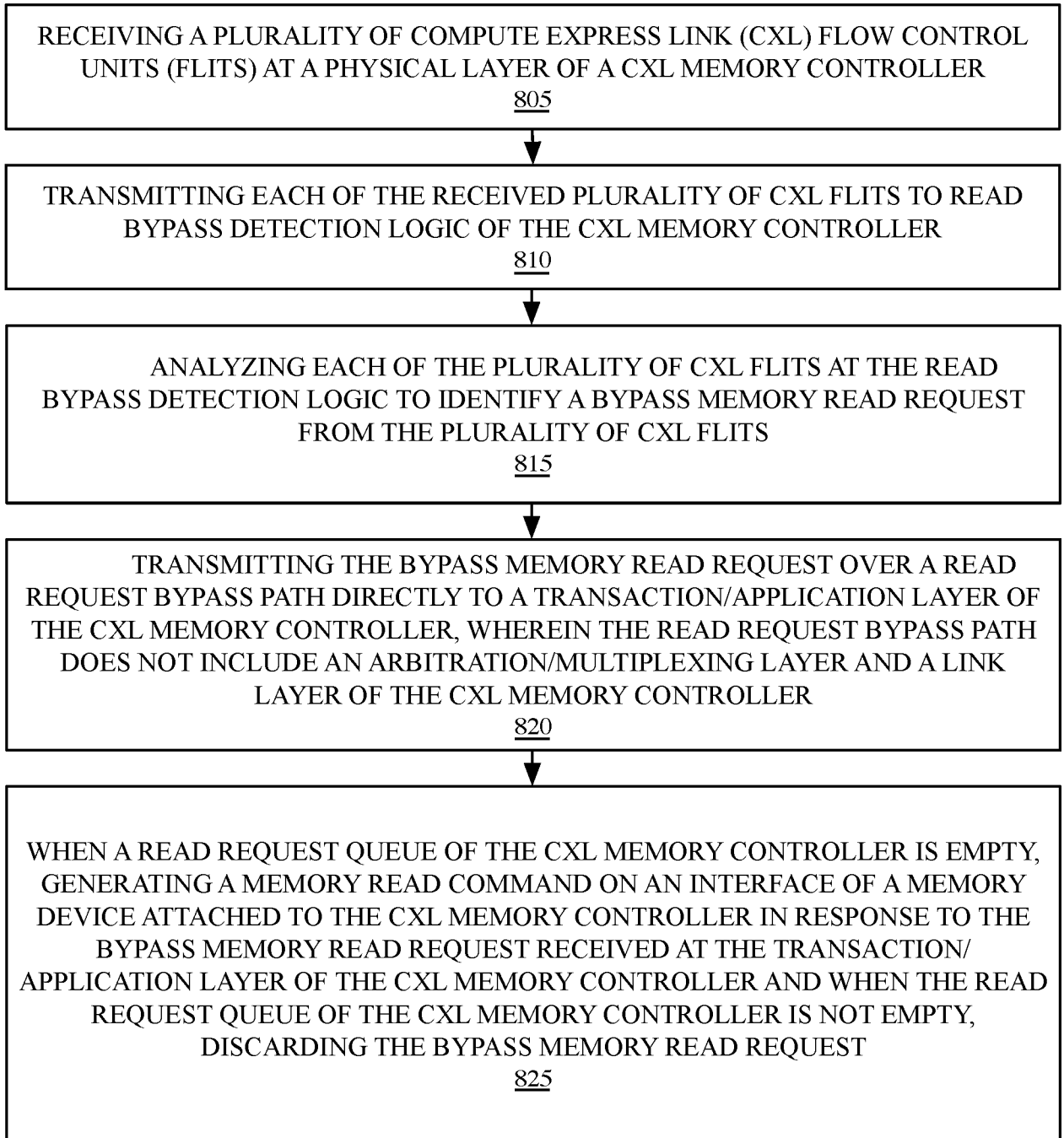


FIG. 7

800


TO 830 OF
FIG. 8B

FIG. 8A

FROM 825
OF FIG. 8A



RECEIVING READ DATA FROM THE MEMORY DEVICE AT THE
TRANSACTION/APPLICATION LAYER IN RESPONSE TO THE MEMORY READ
COMMAND

830



WHEN THERE IS A LINK LAYER MEMORY READ REQUEST AT THE
TRANSACTION/APPLICATION LAYER THAT MATCHES THE BYPASS MEMORY
READ REQUEST THAT GENERATED THE MEMORY READ COMMAND,
FORWARDING THE READ DATA RECEIVED AT THE TRANSACTION/APPLICATION
LAYER TO THE LINK LAYER OF THE CXL MEMORY CONTROLLER AND WHEN
THERE IS NOT A LINK LAYER MEMORY READ REQUEST AT THE TRANSACTION/
APPLICATION LAYER THAT MATCHES THE BYPASS MEMORY READ REQUEST
THAT GENERATED THE MEMORY READ COMMAND, DISCARDING THE READ
DATA RECEIVED AT THE TRANSACTION/APPLICATION LAYER

835

FIG. 8B

INTERNATIONAL SEARCH REPORT

International application No

PCT/US2022/028767

A. CLASSIFICATION OF SUBJECT MATTER**INV. G06F13/16****ADD.**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2003/140202 A1 (LABERGE PAUL A [US]) 24 July 2003 (2003-07-24) figures 2,3 paragraph [0020] - paragraph [0024] -----	1-20
A	US 2020/328879 A1 (MAKARAM RAGHUNANDAN [US] ET AL) 15 October 2020 (2020-10-15) figure 5 paragraph [0053] paragraph [0060] -----	1-20



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance;; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance;; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

18 August 2022

Date of mailing of the international search report

25/08/2022

Name and mailing address of the ISA/

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/US2022/028767

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2003140202 A1	24-07-2003	NONE	

US 2020328879 A1	15-10-2020	CN 112398656 A	23-02-2021
		EP 3779762 A1	17-02-2021
		US 2020328879 A1	15-10-2020
