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[54] MULTIPLE POTENTIOMETER TIMER FOR ELEVATOR CONTROLS

[72] Inventors: **James H. Stichweh**, Princeton, Ind.; **Stephen A. Hornung**, Augustine, France; **Paul Duckwall, III**, Louisville, Ky.

[73] Assignee: **Armor Elevator Company, Inc.**, Milwaukee, Wis.

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[58] **Field of Search** 307/301, 293, 246

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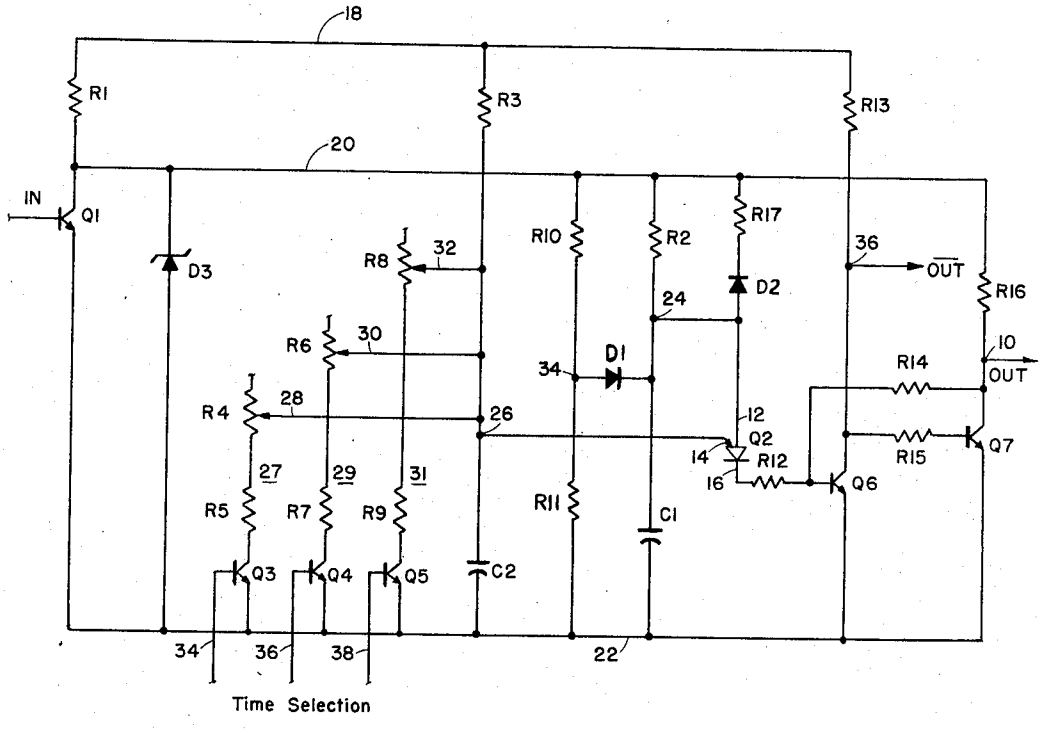
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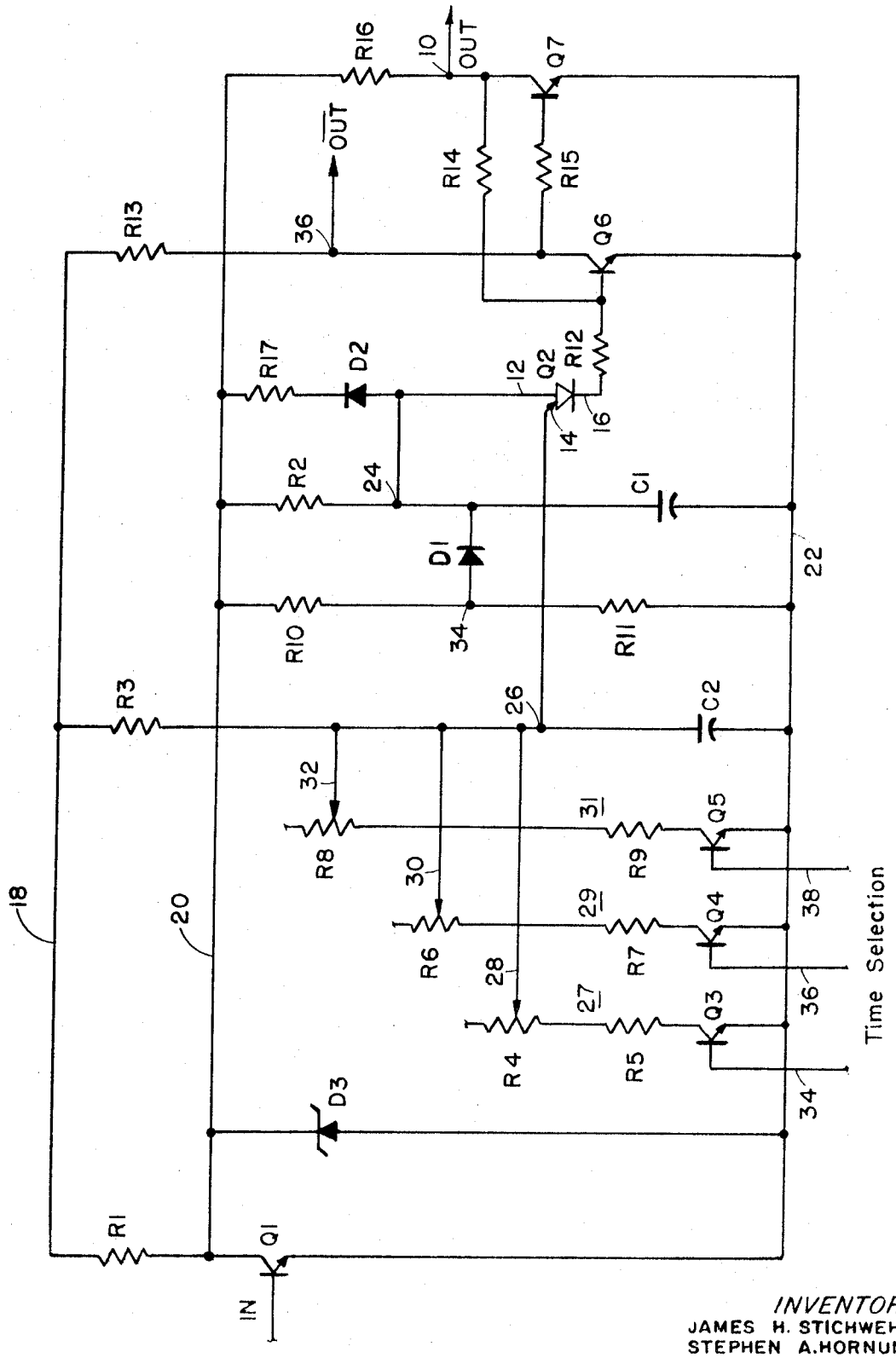
Primary Examiner—Donald D. Forrer
Assistant Examiner—R. C. Woodbridge
Attorney—Sandoe, Hopgood and Calimafde

[57] **ABSTRACT**

A timer circuit produces an output signal at a predetermined time following the application of an input signal. The input signal actuates a timing circuit which, at a specified time thereafter, causes a switching device to be actuated, which in turn produces the output signal. One or more of a plurality of control means are selectively insertable into the timing circuit, thereby to select one of a plurality of available time intervals between the input and output signals.

11 Claims, 1 Drawing Figure





INVENTORS
JAMES H. STICHWEH
STEPHEN A. HORNUNG
PAUL DUCKWALL III

by Sandoe, Hopgood & Calimafde
ATTORNEYS

MULTIPLE POTENTIOMETER TIMER FOR ELEVATOR CONTROLS

The present invention relates to timer circuits, and particularly to a timer circuit capable of producing an output signal at a selected one of several available time intervals following the application of an input signal to the circuit.

Timer circuits for producing an output signal at a predetermined interval following the application of an input or control signal find widespread use in control systems in applications in which an operation is to be initiated at a specified time after the occurrence of a control or actuating operation. A typical application of a timer circuit is in an elevator control system in which it is desired to close the elevator door a predetermined interval after the operation of a control switch, relay or the like. When an elevator car is stopped at a given floor, it is usually desired to maintain the door open for a specified interval to allow a number of passengers to freely enter and leave the elevator at that floor. Upon the completion of that time period, the door is closed to permit the elevator to be transported to a different floor. The time interval during which the door is kept open is predetermined for optimum operation of the elevator, and is preferably maintained at or near the desired time interval over repeated operations of the door control system.

In many uses of timer circuits, it may be desired to have the same circuit operate to produce an output signal at more than just a single preset time interval after the application of the input signal. That is, for various operating conditions of the system of which the timer circuit is a part, it is often desirable and useful that the timer circuit produce a preset but different time interval for each of a number of specified system conditions. For example, in the elevator control system discussed above, there may be several distinct operating conditions for which the door is maintained open for different time intervals, each interval corresponding to the optimum operation of the elevator for the particular operating condition. Thus, for example, when the elevator stops at a floor when a car and a hall call are both registered, it is desirable to provide a longer interval during which the door is maintained open than for the condition in which the elevator car stops only for a hall call or a car call. Furthermore, if the elevator door is caused to reopen by the engagement therewith of a passenger such as by means of a photoelectric device, safety-edge device or "Door Open" button, it is desired that the door thereafter remain open for a relatively shorter time. In addition, if an elevator is parked at a given floor and its doors are then opened in response to a hall call, it is usually desirable to provide a relatively longer time interval for the door to remain open.

For simplicity and compactness of the elevator control system, it would be clearly advantageous to utilize only a single timer circuit for producing each of the desired time intervals for the various anticipated system operating conditions.

There are several criteria for judging the performance of such timer circuits. Among the most significant of these are accuracy and repeatability of operation; that is, the time interval between the actuating input signal and the output signal should remain substantially constant for each operation of the timer circuit. For a timer circuit having a plurality of available delays between its input and output signals, each of these available delays should have similar characteristics of precision and repeatability. Other factors to be considered in the design of a timer circuit of the type described are the availability of a relatively short delay time if desired, and the prevention of an erroneous output signal at all times.

Various attempts and approaches have been made in the design of timer circuits of the type described, but each of these circuits has been deficient in not satisfactorily meeting one or more of the desired criteria set forth above. Specifically, it has heretofore been found difficult to achieve the desired features of accuracy and repeatability of timer operation over long periods of usage, particularly in timer circuits having provisions for providing a plurality of different time delays.

It is an object of the present invention to provide a timer circuit which can be selectively conditioned to produce one of a plurality of available time delays between an input and an output signal.

It is a further object of the present invention to provide a timer circuit of the type described in which the available time settings may each be adjusted with considerable precision.

It is another object of the present invention to provide a timer circuit of the type described in which the time delay provided between the input and output signal remains substantially constant over many operations of the circuit.

It is a general object of the present invention to provide a timer circuit having more than one available time delay which can be selected according to one or more anticipated operating conditions, which circuit operates in a more precise and reliable manner than has heretofore been obtainable in circuits of this type.

The timer circuit of the present invention comprises an input switching device which receives the input signal. Upon receipt of an input signal, the input switching device causes a timing circuit to be energized. When the timing circuit reaches a specified level, a second switching device is caused to be actuated, which in turn is effective to produce an output signal at a predetermined time interval following the initial application of the input signal to the input switching device. In accord with the present invention, one or more of a plurality of control means are selectively operatively connected into the timing circuit, thereby to selectively vary the interval between the input and output signals in accord with the selected control means.

As herein described, the second switching device may comprise a unijunction transistor of the type having an anode and a gate terminal. That transistor is actuated, i.e., rendered conductive, when the voltage level at the anode exceeds the voltage level at the gate. The timing circuit comprises a charging capacitor connected to the anode terminal and means including the selected control means are connected to the gate terminal to apply a preset voltage level thereat corresponding to which, if any, of the control means has been selectively connected into the timing circuit. Additional switching means may be provided in operative association with each of the control means, and suitable control signals derived from an external source are applied to these additional switching means to actuate one or more of the latter, thereby to selectively connect one or more of the control means to the timing circuit.

To the accomplishment of the above and to such other objects as may hereinafter appear, the present invention relates to a timer circuit having selectively adjustable delay control means as defined in the appended claims and as described in the following specification taken in conjunction with the accompanying drawing, in which

the single FIGURE is a schematic circuit diagram of the timer circuit of the present invention.

The timer circuit shown in the FIGURE receives an input signal at a first switching means here shown as an NPN transistor Q1, and produces an output signal at an output terminal **10** at a predetermined time interval thereafter. The output signal is produced upon the actuation of a second switching means here shown in the form of a programmable unijunction transistor Q2 which is caused to be conductive at that predetermined time after the input signal is applied to the transistor Q1. In accord with the present invention, the time delay between the input and output signals may be one of a plurality of preset intervals according to the operation of delay control means which are selectively operatively connected to transistor Q2 in accord with the desired operation of the circuit.

Transistor Q2 is preferably a programmable unijunction transistor (PUT) having an anode terminal **12**, a gate terminal **14** and a cathode terminal **16**. The transistor is caused to conduct whenever the voltage at the anode terminal **12** exceeds the voltage level at the gate terminal **14**.

The input signal is applied to the base of transistor Q1. The collector of that transistor is connected through a resistor R1 to a voltage supply line 18 and by a line 20 to a timing-charging circuit which comprises a resistor R2 connected in series with a capacitor C1 between line 20 and ground at line 22. A junction point 24 is defined between resistor R2 and capacitor C1 which in turn is directly connected to the anode terminal 12 of unijunction transistor Q2. A resistor R3 is connected in series with a capacitor C2 between lines 18 and 22 and a junction point 26, defined between these components, is connected directly to the gate terminal 14 of unijunction transistor Q2.

The potential at which capacitor C2 is charged, to wit, the potential at point 26, is that potential level which is applied at the gate terminal of the unijunction transistor Q2. Similarly, the potential applied to the anode terminal of unijunction transistor Q2 corresponds to the charging potential of capacitor C1 which appears at junction point 24.

In the presence of an input signal at its base, transistor Q1 is normally biased by suitable means (not shown) to a conducting state so that the charging circuit of resistor R2 and capacitor C1 is normally bypassed through the then conducting collector-emitter circuit of transistor Q1, and the potential at point 24 is substantially zero. When an input signal is removed from to the base of transistor Q1, that transistor is cut off or rendered non-conductive and current then begins to flow through resistor R2 and capacitor C1 causing the potential at point 24 to rise in a known manner. When that potential reaches a predetermined level with respect to potential at point 26, unijunction transistor Q2 is rendered conductive, causing capacitor C1 to discharge through the anode-cathode circuit of unijunction transistor Q2, which discharge in turn is effective to produce the output signal at terminal 10 having the desired time delay with respect to the input signal.

The time at which unijunction transistor Q2 is rendered conductive after the application of the input signal to the base of transistor Q1 is determined by two factors; the preset potential at the gate terminal of unijunction transistor Q2 which in turn is determined by the potential across capacitor C2; and the time required to charge the potential at point 24 to a value exceeding the potential level at point 26. The latter is, of course, determined in a known manner by the proper selection of the component values of resistor R2 and capacitor C1.

In accord with the present invention, control means are provided to selectively adjust the preset value at the gate terminal of unijunction transistor Q2 so that the time interval between the application of the input signal to the base of transistor Q1 and the onset of conductivity of unijunction transistor Q2 may be adjusted to satisfy desired system operating conditions. To this end, a plurality of control elements, here shown as a plurality of pairs of resistors, are selectively connected in parallel between point 26 and ground at line 22. The preset potential level at point 26 and thus at the gate of unijunction transistor Q2 is determined by which, if any, of these control means is operatively connected into the circuit. As herein shown, there are three such control means, one of which, generally designated 27, comprises a potentiometer R4 connected in series with a resistor R5 and the collector-emitter circuit of an NPN transistor Q3 to ground. A wiper arm 28 of potentiometer R4 is connect to point 26. Similarly, a second control means, generally designated 29, comprises a potentiometer R6 connected in series with a resistor R7 and the collector-emitter circuit of an NPN transistor Q4 to ground, the wiper arm 30 of potentiometer R6 being connected to point 26. A third control means, generally designated 31, comprises a potentiometer R8 connected in series with resistor R9 and the collector-emitter circuit of an NPN transistor Q5 to ground, the wiper arm 32 of potentiometer R8 also being connected to point 26. The determination of which of the series-connected control means 27, 29 and 31 is to be operatively connected into the timer circuit at point 26 is made by controlling the state of conductivity of the transistors Q3, Q4 and Q5. This in turn is determined by the nature of the control signals applied to the bases of these transistors at terminals 34, 36 and 38, respectively, which control signals are received from an external source (not shown) in the system of which the timer is a part.

The potentiometers R4, R6 and R8 are initially preset to establish a predetermined voltage at point 26, so that whenever their associated switching transistor Q3, Q4 or Q5, respectively, is rendered conductive by the application thereto of an appropriate control signal, unijunction transistor Q2 is caused to be conductive at a predetermined time interval following the application of the input signal to transistor Q1, corresponding to the time interval desired for that control signal.

Resistors R10 and R11 are connected in series between lines 20 and 22 and define a junction point 34 therebetween. A diode D1 is connected between point 34 and point 24. Resistors R10, R11 and diode D1 serve to increase the rate at which capacitor C1 may be charged, thus making it possible for the potential at the anode of unijunction transistor Q2 to reach a level capable of rendering that transistor conductive at a quicker rate. This enables the timer circuit of the present invention to operate at a relatively short minimum time interval when desired.

The cathode terminal 16 of unijunction transistor Q2 is connected through a resistor R12 to the base of a normally "off" or non-conducting NPN transistor Q6. The emitter of transistor Q6 is connected to ground and the collector of that transistor is connected through a resistor R12 to the supply line 18. The base of transistor Q6 is biased by a resistor R14 connected between output terminal 10 and that base, and the collector of transistor Q6 is connected through a resistor R15 to the base of a normally conducting output PNP transistor Q7, the emitter of which is connected to ground. The collector of transistor Q7 is connected to output terminal 10 and through a resistor R16 to line 20. When unijunction transistor Q2 is rendered conductive, transistor Q6 is also rendered conductive, which in turn causes transistor Q7 to be rendered non-conductive. This causes a high level signal to appear at the collector of transistor Q7 and thus at the output terminal 10. It will be noted that the inverse of the output signal may be derived at a point 36 defined at the collector of transistor Q6.

The occasion may arise when the input signal is applied to the base of transistor Q1 prior to the triggering of unijunction transistor Q2. When this occurs, it is desired to provide a discharge path for capacitor C1 without producing an erroneous output signal at terminal 10. If the discharge path for capacitor C1 for this condition would solely be through the unijunction transistor Q2, resistor R12 and transistor Q6, there is a possibility that this discharge current would cause transistor Q6 to be temporarily rendered conductive which in turn would cause transistor Q7 to be turned off which, as described above, would momentarily produce an output signal at terminal 10 at a time when such a signal is not desired. To prevent this from occurring, a secondary, relatively low impedance discharge path is provided for capacitor C1, that path comprising a diode D2 connected in series with a resistor R17 between point 24 and line 20. Thus, when the input signal is applied to the base of transistor Q1, rendering that transistor once again conductive, capacitor C1 is discharged through that low impedance path to effectively prevent the possible erroneous conduction of transistor Q6 and the resulting production of an erroneous output signal at output terminal 10.

This danger of producing an erroneous output signal is further minimized by connecting resistor R3 to voltage supply line 18 rather than to the collector of transistor Q1, thus making the preset gate potential of unijunction transistor Q2 substantially independent of the conduction state of the input transistor Q1.

In the event that the power supply at line 18 is an unregulated one, it may be desired to provide means to maintain a constant potential between lines 20 and 22. To this end, a Zener diode D3 may be connected between these lines and across the collector and emitter of transistor Q1. The constant

potential ensured by the provision of diode D3 is required to obtain the proper time interval between the input and output signals by establishing the proper accurate voltage levels at the gate and anode terminals of unijunction transistor Q2.

For increased reliability and repeatability of circuit operation, it has been found desirable to utilize a programmable unijunction transistor (PUT) as the second switching transistor Q2 rather than the more conventional type unijunction transistor (UJT). A transistor of this type is the D13T1 manufactured by the General Electric Company.

The circuit of the present invention may thus be used to advantage in any situation wherein one of a number of preset time intervals between two signals is desired. One such application would be in an elevator control system in which several different time intervals are desired for operating the elevator doors depending upon the operating conditions of the elevator. For example, for the condition in which the elevator stops at a floor when both a car and a hall call are registered, it is then desirable to provide a longer door-open time than when the elevator car has stopped for only a hall call or a car call. Moreover, if the elevator door is caused to reopen by a safety device upon the engagement with the leading edge of the elevator door by a passenger, such as by means of a photoelectric device, safety edge, or door-open button, a still shorter time for the door to remain open is desired. In addition, if the elevator is parked at a floor and its door is then opened in response to a hall call, it is then usually desired that the door-open time be relatively long. These conditions are established by suitable elevator control circuitry (not shown herein), which produces, upon the appropriate operating condition of the elevator, a control signal which is applied at either terminal **34**, **36** or **38**, to respectively render their associated transistor Q3, Q4 or Q5 conductive, thereby completing the circuit between their associated control means **27**, **29** or **31** and ground. This reduces the voltage level at point **26** and thus at the gate of unijunction transistor Q2 by a predetermined amount, to in turn lower the time interval between the application of the input signal to transistor Q2 and the production of the output signal at terminal **10**. The input signal applied to the base of transistor Q1 when the present circuit is in use in an elevator control system of this type would be defined by the elevator actuating signal, and the output signal would be defined by the door-closing signal. As a result, the elevator door is caused to close at whichever time is desired after the appropriate actuating signal for each of the situations described above is produced in the elevator control system.

While the application of the timer circuit of the present invention has been herein disclosed for use in an elevator control system, it will be apparent that many other applications of that circuit may be made to equal advantage when variable time intervals between input and output signals are desired for system operation depending upon the nature of an external input control signal or signals applied to the circuit. Furthermore, while only three control means are here shown as being selectively operatively connectable into the circuit, it is apparent that more (or less) of these control means, each having an associated switching device to connect them into the circuit at the desired time, may be provided to further increase the flexibility of the circuit by providing a greater number of possible time intervals between the input and output signals.

Thus, while only a single embodiment of the present invention has been herein disclosed, it will be apparent that variations may be made thereto without departure from the spirit and scope of the present invention.

We claim:

1. A timing circuit for producing an output signal a predetermined time after the appearance of an input signal, said circuit comprising a first switching means connected for receiving said input signal, a second switching means having first and second inputs and an output for providing said output signal, a timing means connected to said first switching means and to said first input of said second switching means and effective a predetermined time after the actuation of said first switching means to actuate said second switching means, and a plurality of control means selectively connected to said second input for preconditioning said second switching means for actuation by said timing means to provide one of a plurality of predetermined timing intervals.

2. The circuit of claim 1, wherein said second switching means includes a unijunction transistor having a gate input connected to said control means and an anode input connected to said timing means.

3. The circuit of claim 1, and including a power source means for providing electrical power, said timing means including a first capacitance means selectively connected to be charged by said source means and further connected to said first input, said first switching means responsive to said input signal for effectively connecting said first capacitance means to said source means for initiating a timing sequence.

4. The circuit of claim 3, and including a connecting means for selectively connecting said plurality of control means to said second input for providing said output signal at a selected one of a plurality of pre-established timing intervals in response to said input signal and to the selective operation of said connecting means.

5. The timing circuit of claim 1, including

a power source means for providing electrical power, and wherein said timing means is operatively connected to said source means for providing a voltage varying with time to said first input in response to the operation of said first switching means.

6. The circuit of claim 5, wherein said first switching means operatively connects said source means to a ground potential and to said timing means and provides current to said timing means in response to said input signal.

7. The circuit of claim 1, wherein said control means includes a voltage divider circuit having first and second impedance means serially connected forming a juncture point therebetween, said juncture point connected to said second input of said second switching means, said second impedance means including a plurality of impedance elements operatively parallel connected for providing a plurality of preset voltages to second input of said second switching means.

8. The circuit of claim 7, wherein said second impedance means includes a capacitor and first, second and third resistive elements operatively parallel connected by first, second and third control switches, respectively, for selecting one of a plurality of preset voltages for said juncture point.

9. The circuit of claim 1, wherein said timing means includes a serially connected resistor and capacitor having a first juncture point therebetween connected to said first input of said second switching means for selectively providing a voltage varying with time.

10. The circuit of claim 9, wherein said timing means further includes a pair of serially connected resistors forming a second juncture point therebetween, and a diode connected to said first and second juncture points for conducting current to said capacitor.

11. The circuit of claim 9, and including a serially connected diode and second resistor parallel connected with said first resistor for selectively allowing said capacitor to discharge.

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