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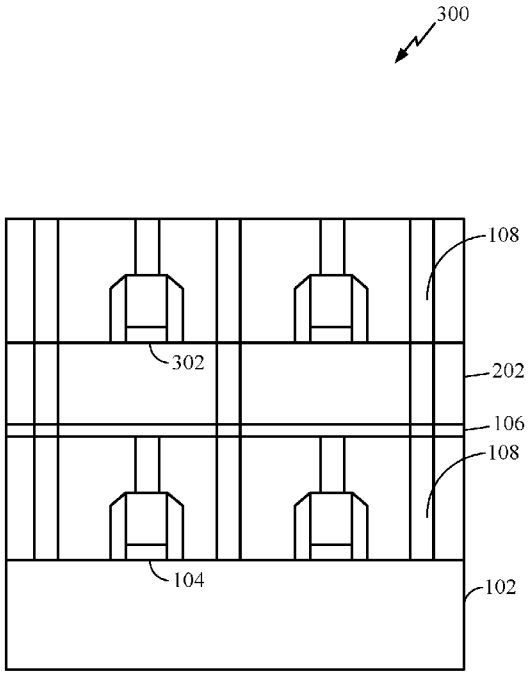
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[Continued on next page]

(54) Title: HETEROGENEOUS CHANNEL MATERIAL INTEGRATION INTO WAFER

(57) Abstract: Methods for integrating heterogeneous channel material into a semiconductor device, and semiconductor devices that integrate heterogeneous channel material. A method for fabricating a semiconductor device includes processing a first substrate of a first material at a first thermal budget to fabricate a p-type device. The method further includes coupling a second substrate of a second material to the first substrate. The method also includes processing the second substrate to fabricate an n-type device at a second thermal budget that is less than the first thermal budget. The p-type device and the n-type device may cooperate to form a complementary device.

FIG. 3



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— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

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HETEROGENEOUS CHANNEL MATERIAL INTEGRATION INTO WAFER

BACKGROUND

Field

[0001] Aspects of the present disclosure relate to semiconductor devices, and more particularly to heterogeneous channel material integration for materials that have different thermal budgets.

Background

[0002] Semiconductor chip level bonded devices are used in several consumer and commercial applications. Semiconductor devices are often made from a single type of material. Semiconductor devices may also be made of different types of material grown onto a substrate based on lattice matching and compatible crystalline structures. Semiconductor devices manufactured from compound materials (i.e., where the semiconductor structure is more than one material), such as III-V materials, are typically grown on gallium arsenide or other compound semiconductor substrates. These devices are difficult to integrate with electronic devices fabricated on silicon because of lattice mismatches between the crystalline structures of silicon and compound semiconductor materials.

SUMMARY

[0003] A method for fabricating a device in accordance with one aspect of the present disclosure includes processing a first substrate of a first material at a first thermal budget to fabricate a p-type device. Such a method further includes coupling a second substrate of a second material to the first substrate. The method also includes processing the second substrate to fabricate an n-type device at a second thermal budget that is less than the first thermal budget. The p-type device and the n-type device may cooperate to form a complementary device.

[0004] A semiconductor device in accordance with another aspect of the present disclosure includes a first substrate of a first material having a first thermal budget. The first substrate may include a p-type device. Such a device also includes a second substrate of a second material having a second thermal budget that is coupled to the first

substrate. The second substrate may include an n-type device. The p-type device and the n-type device may cooperate to form a complementary device.

[0005] Another semiconductor device in accordance with one aspect of the present disclosure includes a first means for conducting a first charge carrier type in a first substrate of a first material having a first thermal budget. Such a device also includes a second means for conducting a second charge carrier type in a second substrate. The second substrate may be of a second material having a second thermal budget and coupled to the first substrate. The first means and the second means may cooperate to form a complementary device.

[0006] This has outlined, rather broadly, the features and technical advantages of the present disclosure in order that the detailed description that follows may be better understood. Additional features and advantages of the disclosure will be described below. It should be appreciated by those skilled in the art that this disclosure may be readily utilized as a basis for modifying or designing other structures for carrying out the same purposes of the present disclosure. It should also be realized by those skilled in the art that such equivalent constructions do not depart from the teachings of the disclosure as set forth in the appended claims. The novel features, which are believed to be characteristic of the disclosure, both as to its organization and method of operation, together with further objects and advantages, will be better understood from the following description when considered in connection with the accompanying figures. It is to be expressly understood, however, that each of the figures is provided for the purpose of illustration and description only and is not intended as a definition of the limits of the present disclosure.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] For a more complete understanding of the present disclosure, reference is now made to the following description taken in conjunction with the accompanying drawings.

[0008] FIGURE 1 illustrates a side view of a semiconductor device in an aspect of the present disclosure.

[0009] FIGURE 2 illustrates coupling a compound semiconductor substrate to a different material system semiconductor device in an aspect of the present disclosure.

[0010] FIGURE 3 illustrates a side view of a compound semiconductor device formed on the different material system semiconductor device in an aspect of the present disclosure.

[0011] FIGURE 4 is a process flow diagram illustrating a method of making a resonator according to an aspect of the present disclosure.

[0012] FIGURE 5 is a block diagram showing an exemplary wireless communication system in which a configuration of the disclosure may be advantageously employed.

[0013] FIGURE 6 is a block diagram illustrating a design workstation used for circuit, layout, and logic design of a semiconductor component according to one configuration.

DETAILED DESCRIPTION

[0014] The detailed description set forth below, in connection with the appended drawings, is intended as a description of various configurations and is not intended to represent the only configurations in which the concepts described herein may be practiced. The detailed description includes specific details for the purpose of providing a thorough understanding of the various concepts. It will be apparent to those skilled in the art, however, that these concepts may be practiced without these specific details. In some instances, well-known structures and components are shown in block diagram form in order to avoid obscuring such concepts. As described herein, the use of the term "and/or" is intended to represent an "inclusive OR", and the use of the term "or" is intended to represent an "exclusive OR".

[0015] A high mobility conduction channel is desirable for high performance transistors. Such transistors are often made using III-V materials. The narrow energy bandgap of III-V materials, however, may not provide leakage current below 1 nA/μm. For low-power devices, silicon channels are desired because silicon channels can prevent low leakage currents, however, these devices may have lower performance than III-V devices.

[0016] Heterogeneous channel integration of a III-V channel into a semiconductor wafer, (e.g., silicon), or integration of III-V devices with other semiconductor material systems into the same wafer is difficult. Complicated epitaxial growth processes due to dissimilar materials, and thermal and mechanical stresses, complicate heterogeneous material integration. Integrating a separate semiconductor material system with III-V devices into a single wafer is even more difficult due to the thermal budget of some material systems (e.g., silicon >1000 C) and the thermal budget limitation of III-V materials (<700 C).

[0017] An aspect of the present disclosure processes different semiconductor material systems, (e.g., Si and III-V) devices in different levels or "tiers." One aspect of the present disclosure allows for silicon processing and III-V processing within the same circuit without affecting prior structural process steps.

[0018] FIGURE 1 illustrates a side view of a semiconductor device in an aspect of the present disclosure. A wafer 100 comprises a first substrate 102, a semiconductor device 104, an interface layer 106, and an interconnect 108. The wafer 100 may comprise many integrated circuits, which are produced by dicing, cleaving, or cutting the wafer 100 into pieces. As such, FIGURE 1 may illustrate the wafer 100 or a semiconductor chip that is a portion of the wafer 100.

[0019] One aspect of the present disclosure uses a semiconductor (e.g., silicon (Si)) substrate as the first substrate 102. Further, the semiconductor device 104, which may be formed on (or in) the first substrate 102, may be a metal-oxide-semiconductor field-effect transistor (MOSFET). The semiconductor device 104 may also be a tunneling field-effect transistor (TFET). The wafer 100 is processed to create the semiconductor device 104 and to create the interconnect 108. The first substrate 102 is processed until the semiconductor device 104 and interconnects have reached a certain point in the processing. That point may be at any desired time, but may be up to the local interconnection layer (e.g., middle of line (MOL)) or the first conductive layer (e.g., metal one (M1)).

[0020] The interface layer 106 is then coupled to the last processed portion of the first substrate 102. The interface layer 106 may be an amorphous layer, such as silicon dioxide (SiO_2), a crystalline layer, or any other layer or material that aids in the bonding

or coupling of another material to the wafer 100 and also provides electrical isolation of the devices on substrate 102 from the subsequently processed devices.

[0021] FIGURE 2 illustrates coupling of a compound semiconductor substrate to a semiconductor (e.g., silicon) device in an aspect of the present disclosure. A coupled structure 200 shows that a second substrate 202 is coupled to the interface layer 106 of the wafer 100. The coupling of the second substrate 202 may be a bonding or "smart cut" process to couple the second substrate 202 to the wafer 100. The coupling may also be an oxide-oxide process. The coupling of the second substrate 202 may also be performed using annealing, plasma welding, or other forms of coupling the second substrate 202 to the wafer 100.

[0022] The second substrate 202 may be a III-V material, a II-VI material, or another material that has a different thermal budget than the first substrate 102. For example, and not by way of limitation, the first substrate 102 may be a silicon substrate that has a thermal budget of greater than 1000 degrees Centigrade. The second substrate 202 may be a III-V substrate (e.g., a gallium arsenide (GaAs) substrate) that has a thermal budget of less than 700 degrees Centigrade. This reduced thermal budget is specified because the crystalline bonds and/or covalent bonding of the compound III-V materials break down at the higher temperatures used for semiconductor processing.

[0023] The difference in thermal budget between the first substrate 102 and the second substrate 202 may be great enough to allow for processing of the second substrate 202 without substantial effect on the prior processing performed on the first substrate 102. The second substrate 202 may be coupled directly to the interface layer 106, or may be coupled to another layer of the first substrate 102. Further, additional steps (e.g., thinning the second substrate 202), may be performed prior to or after coupling the second substrate to the wafer 100.

[0024] FIGURE 3 illustrates a side view of a compound semiconductor device 300 formed on a semiconductor device in an aspect of the present disclosure. The compound semiconductor device 300 includes a semiconductor device 302 formed on (or in) the second substrate 202. The second substrate 202 may be further processed to extend the interconnect 108 through the second substrate 202 and through additional processing layers coupled to the second substrate 202. In the case of III-V processing,

which is performed at less than 700 degrees Centigrade, the semiconductor device 104, which may be a MOSFET, is substantially unchanged in electrical performance after forming the semiconductor device 302.

[0025] In an aspect of the present disclosure, the semiconductor device 302 may also be a MOSFET and/or a TFET device. In this configuration, the semiconductor device 104 and the semiconductor device 302 use different charge carriers in their respective channels. The semiconductor device 104 and the semiconductor device 302 may then be combined to create a complementary metal-oxide-semiconductor (CMOS) device.

[0026] A high mobility conduction channel is desirable for high performance transistors. Depending on a dopant density of the semiconductor device 104 when fabricated in silicon, electron mobility varies between 90 and 1500 cm^2/V-s, and hole mobility varies between 50 and 450 cm^2/V-s. In III-V materials, such as gallium arsenide, electron mobility is ~8500 cm^2/V-s, and hole mobility is relatively constant at ~400 cm^2/V-s.

[0027] A complementary device, in accordance with one aspect of the present disclosure, may use a p-type carrier in the semiconductor device 104 and an n-type device in the semiconductor device 302 to provide increased carrier mobility. Further, because the processing of the semiconductor device 302 can be tailored for single charge carrier devices, the narrow energy bandgap of III-V materials used in the second substrate 202 may be designed to assist in containing leakage current for values below 1 nA/μm. Alternatively, the semiconductor device 302 may be used in applications where leakage current would not degrade the overall circuit function. The use of the second substrate 202 may increase the performance of the compound semiconductor device 300 over a similar circuit made only from a single substrate material.

[0028] For example, and not by way of limitation, the semiconductor device 104 may be a p-type device (a PMOS device), and the semiconductor device 302 may be an n-type device (an NMOS device). The semiconductor device 104 and the semiconductor device 302 may then be coupled together to create a complementary device (CMOS). The processing of the semiconductor device 104, and/or the selection of the material used for the first substrate 102, may then be improved or even optimized for a specific charge carrier in the channel in the semiconductor device 104. Similarly, the processing

of the semiconductor device 302, and/or the selection of the material for the second substrate 202 may then be improved or even optimized for a specific charge carrier in the channel in the semiconductor device 302. The present disclosure allows for tailoring of the channel characteristics through the use of the first substrate 102 and the second substrate 202. Further, the present disclosure allows for selection of the channel charge carriers and device performance and maintains the performance of the semiconductor device 104 while processing the semiconductor device 302.

[0029] In the case of III-V materials, the III-V process to create the semiconductor device 302 uses temperatures that have a negligible influence on the processing steps used to create the semiconductor device 104. Thus, creating the semiconductor device 302 has a negligible impact on the semiconductor device 104.

[0030] The semiconductor device 104 may also be assigned to a particular use, while the semiconductor device 302 may be assigned to a different use, within an aspect of the present disclosure. For example, the semiconductor device 104 may be used for a low power portion of an overall circuit where the compound semiconductor device 300 is employed, such as a modem. The semiconductor device 302, in such an aspect of the present disclosure, may be used as a high performance portion of the circuit such as a central processing unit (CPU).

[0031] FIGURE 4 is a process flow diagram illustrating a method 400 of making an integrated device according to an aspect of the present disclosure. At block 402, a first substrate of a first material is processed at a first thermal budget to fabricate a p-type device. At block 404, a second substrate of a second material is coupled to the first substrate. At block 406, the second substrate is processed to fabricate an n-type device at a second thermal budget that is lower than the first thermal budget. In one configuration, the p-type device and the n-type device cooperate to form a complementary device. For example, the semiconductor device 104 may be a p-type device (a PMOS device), and the semiconductor device 302 may be an n-type device (an NMOS device). The semiconductor device 104 and the semiconductor device 302 may then be coupled together to create a complementary device (CMOS), as shown in FIGURE 3.

[0032] A compound device, in accordance with an aspect of the present disclosure, includes a first means for conducting a first charge carrier type in a first substrate of a first material having a first thermal budget. In one aspect of the disclosure, the first means may be the semiconductor device 104 and/or other structures configured to perform the functions recited by the first means. The compound semiconductor device also includes a second means for conducting a second charge carrier type in a second substrate of a second material having a second thermal budget coupled to the first substrate. The first means and the second means may cooperate to form a complementary device. In one aspect of the present disclosure, the second means may be the semiconductor device 302, and/or other structures configured to perform the functions recited by the second means. In another aspect, the aforementioned means may be any module or any apparatus configured to perform the functions recited by the aforementioned means.

[0033] FIGURE 5 is a block diagram showing an exemplary wireless communication system 500 in which an aspect of the disclosure may be advantageously employed. For purposes of illustration, FIGURE 6 shows three remote units 520, 530, and 550 and two base stations 540. It will be recognized that wireless communication systems may have many more remote units and base stations. Remote units 520, 530, and 550 include IC devices 525A, 525C, and 525B that include the disclosed devices. It will be recognized that other devices may also include the disclosed heterogeneous channel materials, such as the base stations, switching devices, and network equipment. FIGURE 5 shows forward link signals 580 from the two base stations 540 to the remote units 520, 530, and 550 and reverse link signals 590 from the remote units 520, 530, and 550 to the two base stations 540.

[0034] In FIGURE 5, remote unit 520 is shown as a mobile telephone, remote unit 530 is shown as a portable computer, and remote unit 550 is shown as a fixed location remote unit in a wireless local loop system. For example, the remote units may be mobile phones, hand-held personal communication systems (PCS) units, portable data units such as personal data assistants, GPS enabled devices, navigation devices, set top boxes, music players, video players, entertainment units, fixed location data units such as meter reading equipment, or other devices that store or retrieve data or computer instructions, or combinations thereof. Although FIGURE 5 illustrates remote units

according to the aspects of the disclosure, the disclosure is not limited to these exemplary illustrated units. Aspects of the disclosure may be suitably employed in many devices, which include the disclosed devices.

[0035] FIGURE 6 is a block diagram illustrating a design workstation used for circuit, layout, and logic design of a semiconductor component, such as the devices disclosed above. A design workstation 600 includes a hard disk 601 containing operating system software, support files, and design software such as Cadence or OrCAD. The design workstation 600 also includes a display 602 to facilitate design of a circuit 610 or a semiconductor component 612 such as a device having heterogeneous channel materials. A storage medium 604 is provided for tangibly storing the design of the circuit 610 or the semiconductor component 612. The design of the circuit 610 or the semiconductor component 612 may be stored on the storage medium 604 in a file format such as GDSII or GERBER. The storage medium 604 may be a CD-ROM, DVD, hard disk, flash memory, or other appropriate device. Furthermore, the design workstation 600 includes a drive apparatus 603 for accepting input from or writing output to the storage medium 604.

[0036] Data recorded on the storage medium 604 may specify logic circuit configurations, pattern data for photolithography masks, or mask pattern data for serial write tools such as electron beam lithography. The data may further include logic verification data such as timing diagrams or net circuits associated with logic simulations. Providing data on the storage medium 604 facilitates the design of the circuit 610 or the semiconductor component 612 by decreasing the number of processes for designing semiconductor wafers.

[0037] Those of skill would further appreciate that the various illustrative logical blocks, modules, circuits, and algorithm steps described in connection with the disclosure herein may be implemented as electronic hardware, computer software, or combinations of both. To clearly illustrate this interchangeability of hardware and software, various illustrative components, blocks, modules, circuits, and steps have been described above generally in terms of their functionality. Whether such functionality is implemented as hardware or software depends upon the particular application and design constraints imposed on the overall system. Skilled artisans may implement the

described functionality in varying ways for each particular application, but such implementation decisions should not be interpreted as causing a departure from the scope of the present disclosure.

[0038] The various illustrative logical blocks, modules, and circuits described in connection with the disclosure herein may be implemented or performed with a general-purpose processor, a digital signal processor (DSP), an application specific integrated circuit (ASIC), a field programmable gate array (FPGA) or other programmable logic device, discrete gate or transistor logic, discrete hardware components, or any combination thereof designed to perform the functions described herein. A general-purpose processor may be a microprocessor, but in the alternative, the processor may be any conventional processor, controller, microcontroller, or state machine. A processor may also be implemented as a combination of computing devices, e.g., a combination of a DSP and a microprocessor, multiple microprocessors, one or more microprocessors in conjunction with a DSP core, or any other such configuration.

[0039] The steps of a method or algorithm described in connection with the disclosure may be embodied directly in hardware, in a software module executed by a processor, or in a combination of the two. A software module may reside in RAM, flash memory, ROM, EPROM, EEPROM, registers, hard disk, a removable disk, a CD-ROM, or any other form of storage medium known in the art. An exemplary storage medium is coupled to the processor such that the processor can read information from, and write information to, the storage medium. In the alternative, the storage medium may be integral to the processor. The processor and the storage medium may reside in an ASIC. The ASIC may reside in a user terminal. In the alternative, the processor and the storage medium may reside as discrete components in a user terminal.

[0040] In one or more exemplary designs, the functions described may be implemented in hardware, software, firmware, or any combination thereof. If implemented in software, the functions may be stored on or transmitted over as one or more instructions or code on a computer-readable medium. Computer-readable media includes both computer storage media and communication media including any medium that facilitates transfer of a computer program from one place to another. A storage media may be any available media that can be accessed by a general purpose or special

purpose computer. By way of example, and not limitation, such computer-readable media can include RAM, ROM, EEPROM, CD-ROM or other optical disk storage, magnetic disk storage or other magnetic storage devices, or any other medium that can be used to carry or store specified program code means in the form of instructions or data structures and that can be accessed by a general-purpose or special-purpose computer, or a general-purpose or special-purpose processor. Also, any connection is properly termed a computer-readable medium. For example, if the software is transmitted from a website, server, or other remote source using a coaxial cable, fiber optic cable, twisted pair, digital subscriber line (DSL), or wireless technologies such as infrared, radio, and microwave, then the coaxial cable, fiber optic cable, twisted pair, DSL, or wireless technologies such as infrared, radio, and microwave are included in the definition of medium. Disk and disc, as used herein, includes compact disc (CD), laser disc, optical disc, digital versatile disc (DVD), floppy disk and Blu-ray disc where disks usually reproduce data magnetically, while discs reproduce data optically with lasers. Combinations of the above should also be included within the scope of computer-readable media.

[0041] The previous description of the disclosure is provided to enable any person skilled in the art to make or use the disclosure. Various modifications to the disclosure will be readily apparent to those skilled in the art, and the generic principles defined herein may be applied to other variations without departing from the spirit or scope of the disclosure. Thus, the disclosure is not intended to be limited to the examples and designs described herein but is to be accorded the widest scope consistent with the principles and novel features disclosed herein.

CLAIMS

WHAT IS CLAIMED IS:

1. A method for fabricating a semiconductor device, comprising:

processing a first substrate of a first material at a first thermal budget to fabricate a p-type device;

coupling a second substrate of a second material to the first substrate; and

processing the second substrate to fabricate an n-type device at a second thermal budget that is less than the first thermal budget, in which the p-type device and the n-type device cooperate to form a complementary device.

2. The method of claim 1, further comprising:

fabricating an additional layer on the first substrate; and

coupling the second substrate to the additional layer.

3. The method of claim 1, in which the first substrate is a silicon substrate.

4. The method of claim 1, in which the first thermal budget is greater than 1000 degrees centigrade.

5. The method of claim 1, in which processing the second substrate at the second thermal budget substantially retains performance of the p-type device.

6. The method of claim 1, in which the second substrate is a III-V substrate.

7. The method of claim 1, in which the second thermal budget is less than 700 degrees centigrade.

8. The method of claim 1, further comprising electrically coupling the p-type device of the first substrate and the n-type device of the second substrate, in which the second substrate is on the first substrate.

9. The method of claim 1, in which the semiconductor device is integrated into a mobile phone, a set top box, a music player, a video player, an entertainment unit,

a navigation device, a computer, a hand-held personal communication systems (PCS) unit, a portable data unit, and/or a fixed location data unit.

10. A method for fabricating a semiconductor device, comprising:

the step of processing a first substrate, of a first material, at a first thermal budget to fabricate a p-type device;

the step of coupling a second substrate comprising a second material to the first substrate; and

the step of processing the second substrate to fabricate an n-type device at a second thermal budget that is lower than the first thermal budget, in which the p-type device and the n-type device cooperate to form a complementary device.

11. The method of claim 10, further comprising:

the step of fabricating an additional layer on the first substrate; and

the step of coupling the second substrate to the additional layer.

12. The method of claim 10, in which the first substrate is a silicon substrate.

13. The method of claim 10, in which the first thermal budget is greater than 1000 degrees centigrade.

14. The method of claim 10, in which the step of processing the second substrate at the second thermal budget substantially retains performance of the p-type device.

15. The method of claim 10, in which the second substrate is a III-V substrate.

16. The method of claim 10, in which the second thermal budget is less than 700 degrees centigrade.

17. The method of claim 10, further comprising the step of electrically coupling the p-type device of the first substrate and the n-type device of the second substrate in which the second substrate is on the first substrate.

18. The method of claim 10, in which the semiconductor device is integrated into a mobile phone, a set top box, a music player, a video player, an entertainment unit, a navigation device, a computer, a hand-held personal communication systems (PCS) unit, a portable data unit, and/or a fixed location data unit.

19. A semiconductor device, comprising:

a first substrate of a first material having a first thermal budget, the first substrate comprising a p-type device; and

a second substrate of a second material having a second thermal budget coupled to the first substrate, the second substrate comprising an n-type device, in which the p-type device and the n-type device cooperate to form a complementary device.

20. The semiconductor device of claim 19, in which the second substrate is on the first substrate and the p-type device of the first substrate is electrically coupled to the n-type device of the second substrate.

21. The semiconductor device of claim 19, further comprising an additional layer on the first substrate and coupled to the second substrate.

22. The semiconductor device of claim 19, in which the first substrate is a silicon substrate and the second substrate is a III-V substrate.

23. The semiconductor device of claim 19, in which the first thermal budget is greater than 1000 degrees centigrade and the second thermal budget is less than 700 degrees centigrade.

24. The semiconductor device of claim 19, integrated into a mobile phone, a set top box, a music player, a video player, an entertainment unit, a navigation device, a

computer, a hand-held personal communication systems (PCS) unit, a portable data unit, and/or a fixed location data unit.

25. A semiconductor device, comprising:

first means for conducting a first charge carrier type in a first substrate of a first material having a first thermal budget; and

second means for conducting a second charge carrier type in a second substrate of a second material having a second thermal budget coupled to the first substrate, in which the first means and the second means cooperate to form a complementary device.

26. The semiconductor device of claim 25, in which the second substrate is on the first substrate and the first means of the first substrate is electrically coupled to the second means of the second substrate.

27. The semiconductor device of claim 25, further comprising an additional layer on the first substrate and coupled to the second substrate.

28. The semiconductor device of claim 25, in which the first substrate is a silicon substrate and the second substrate is a III-V substrate.

29. The semiconductor device of claim 25, in which the first thermal budget is greater than 1000 degrees centigrade and the second thermal budget is less than 700 degrees centigrade.

30. The semiconductor device of claim 25, integrated into a mobile phone, a set top box, a music player, a video player, an entertainment unit, a navigation device, a computer, a hand-held personal communication systems (PCS) unit, a portable data unit, and/or a fixed location data unit.

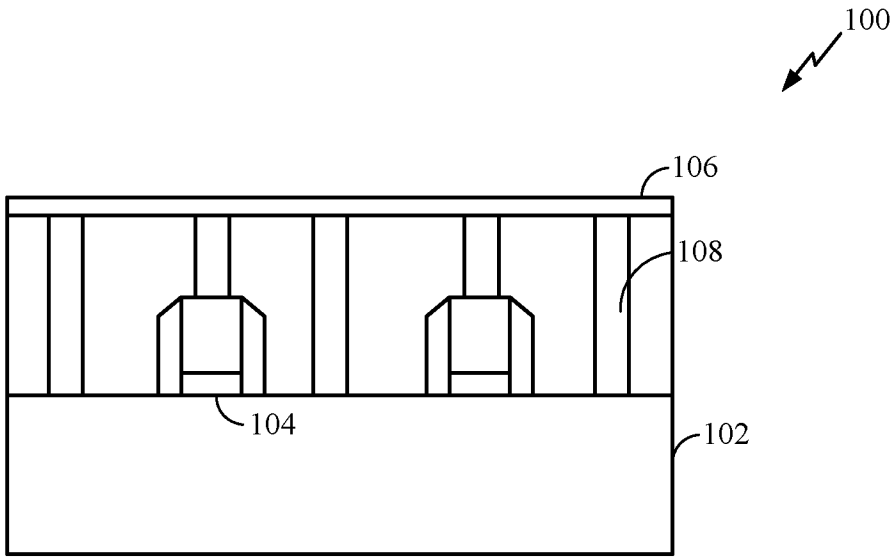


FIG. 1

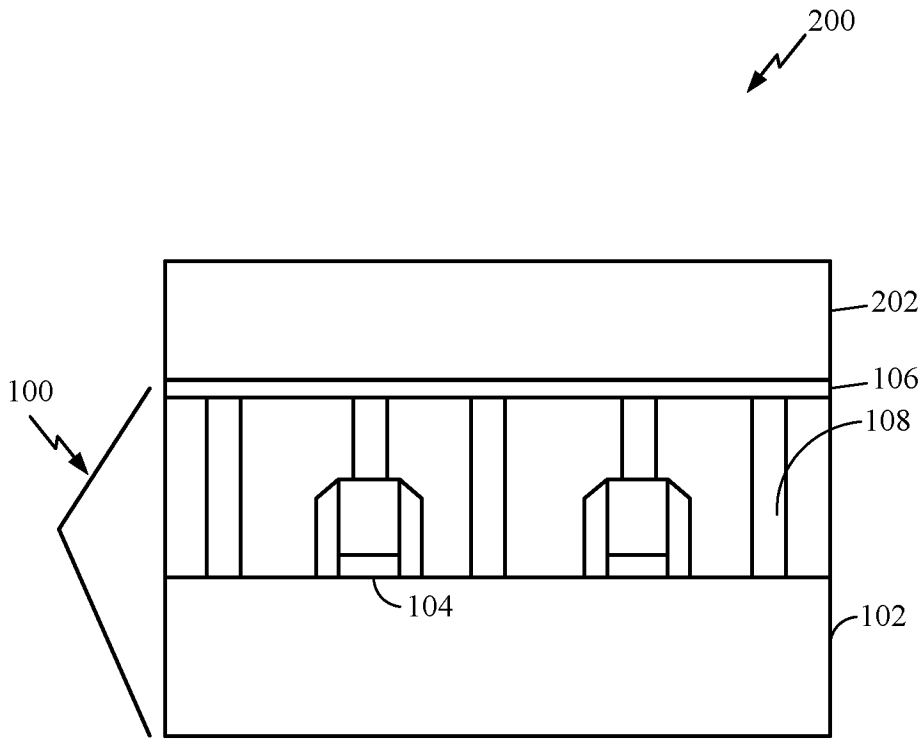


FIG. 2

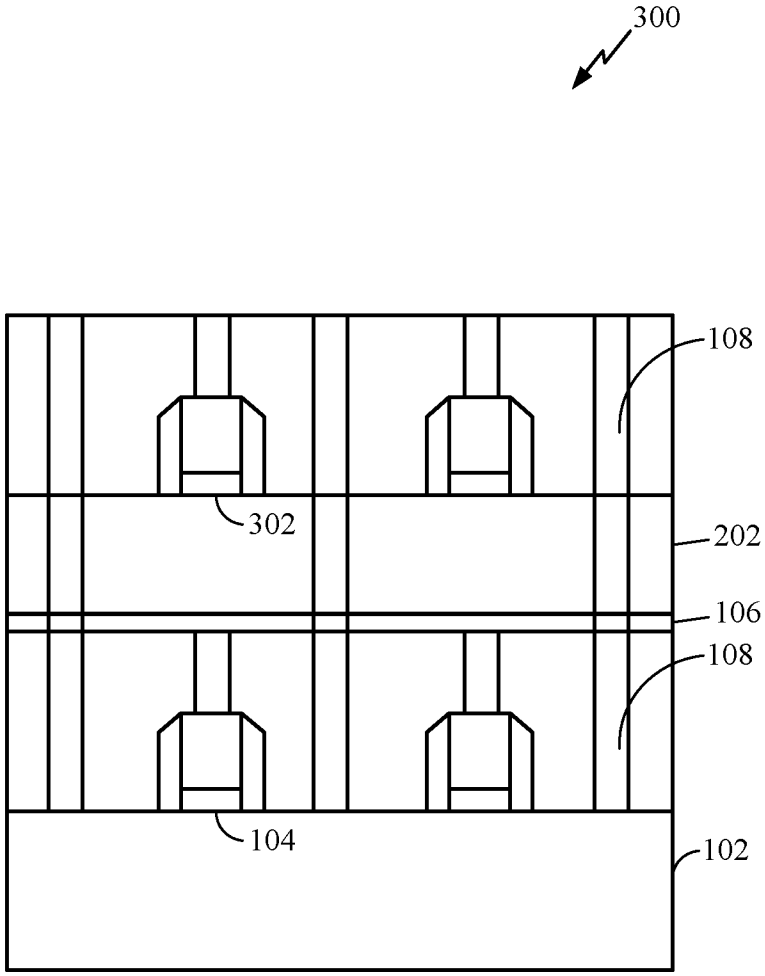


FIG. 3

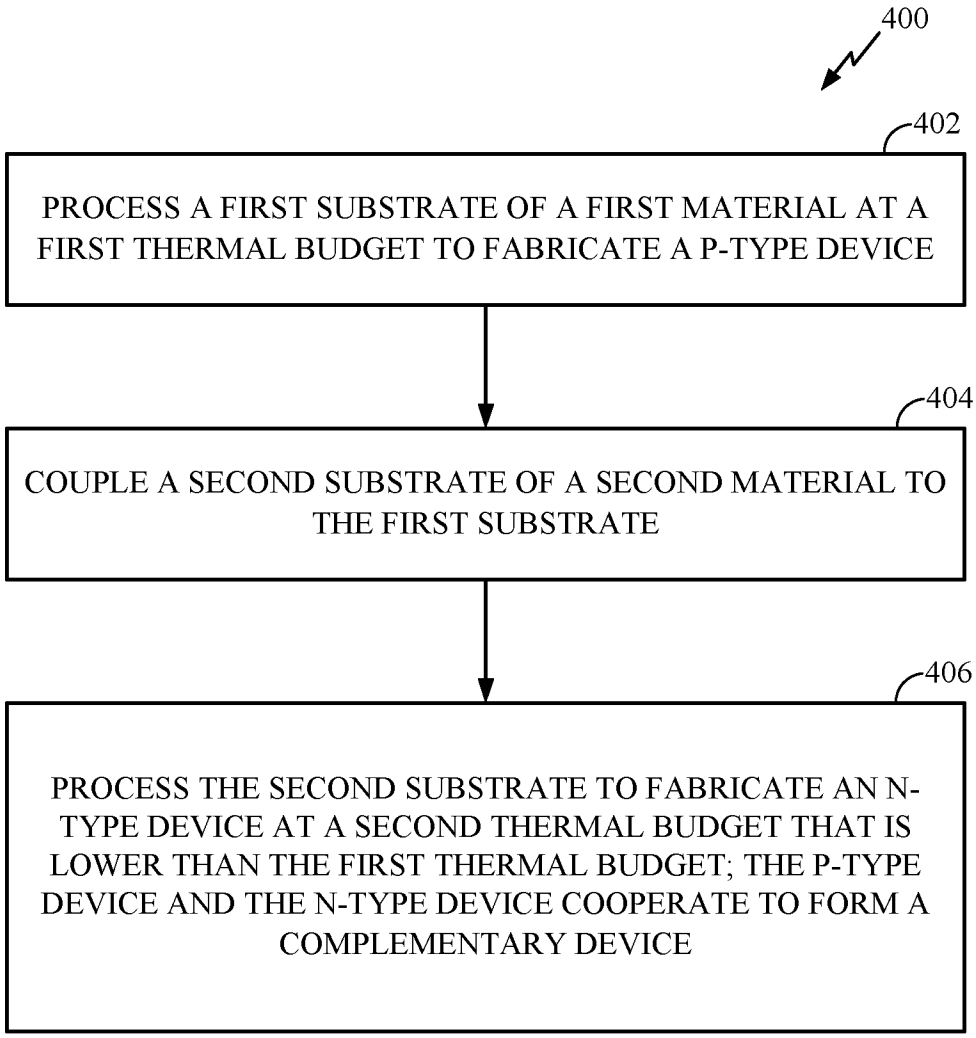

400
402
PROCESS A FIRST SUBSTRATE OF A FIRST MATERIAL AT A FIRST THERMAL BUDGET TO FABRICATE A P-TYPE DEVICE
404
COUPLE A SECOND SUBSTRATE OF A SECOND MATERIAL TO THE FIRST SUBSTRATE
406
PROCESS THE SECOND SUBSTRATE TO FABRICATE AN N-TYPE DEVICE AT A SECOND THERMAL BUDGET THAT IS LOWER THAN THE FIRST THERMAL BUDGET; THE P-TYPE DEVICE AND THE N-TYPE DEVICE COOPERATE TO FORM A COMPLEMENTARY DEVICE

FIG. 4

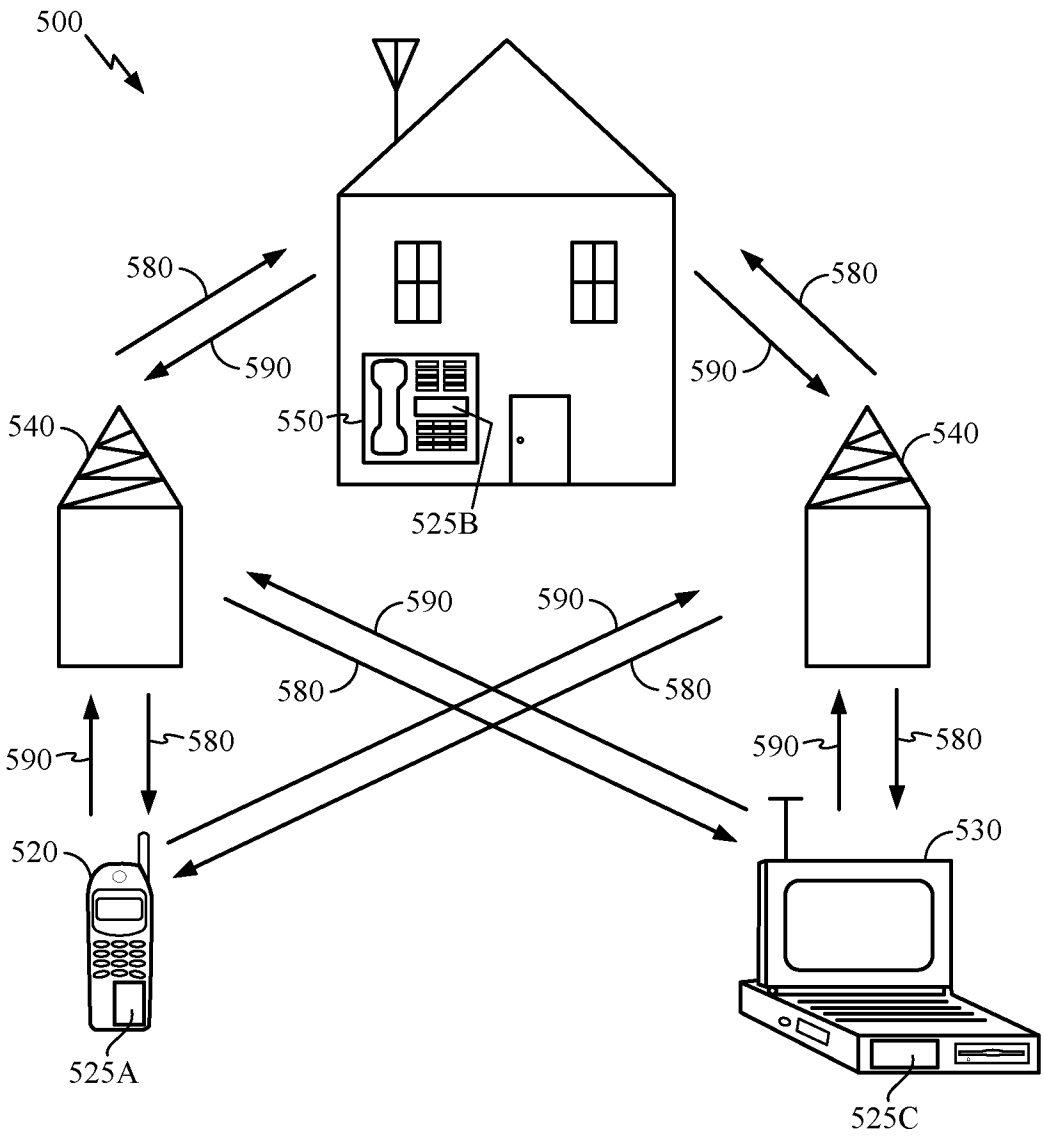

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525B
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525A
525C

FIG. 5

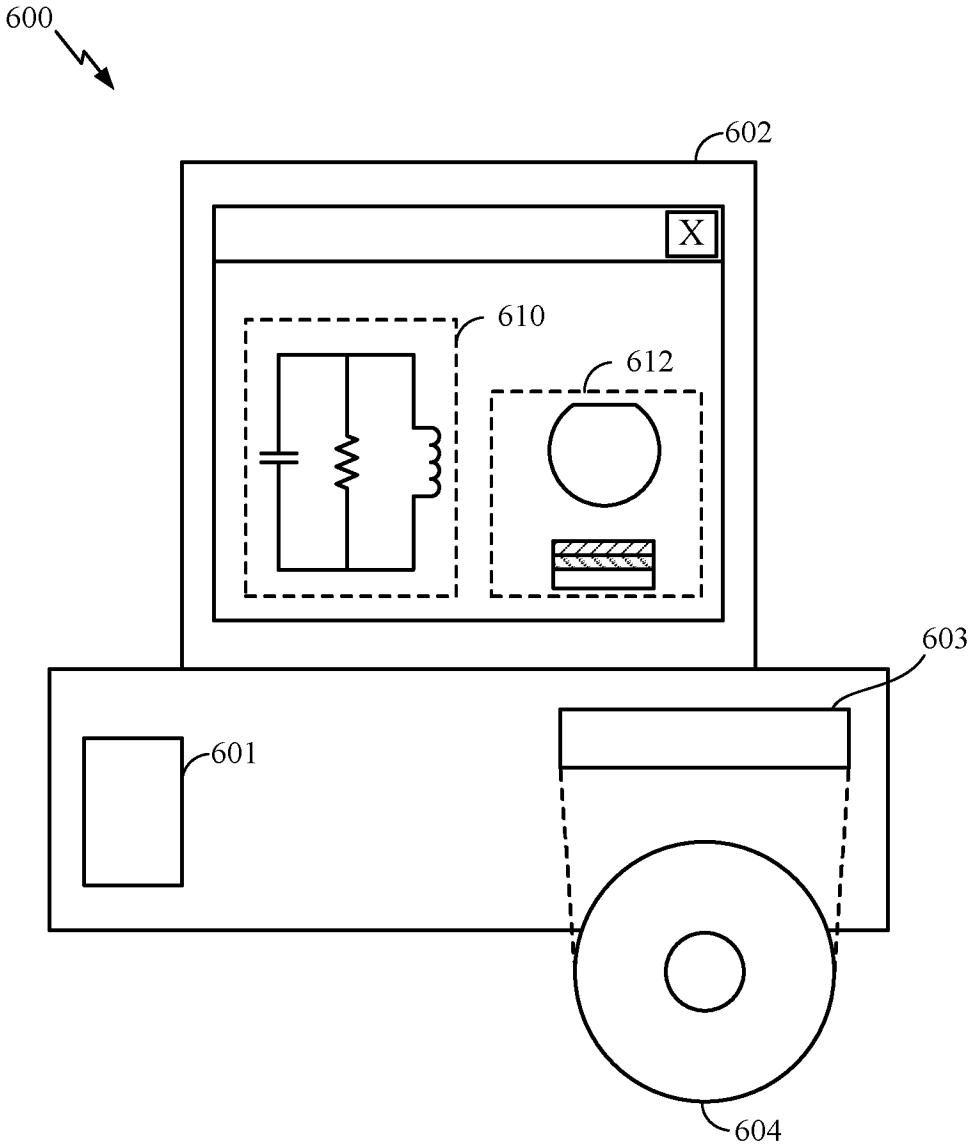


FIG. 6

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2014/053897

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L21/8258 H01L21/822 H01L27/06 H01L27/092 H01L21/762
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, INSPEC, IBM-TDB, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2013/082235 A1 (GU SHIQUN [US] ET AL) 4 April 2013 (2013-04-04)	1-3, 5-12, 14-22, 24-28,30
Y	abstract; claims; figures 5A,5C paragraphs [0006], [0028], [0032], [0033], [0039]	23,29
X	EP 1 104 028 A2 (LUCENT TECHNOLOGIES INC [US]) 30 May 2001 (2001-05-30)	1,4,5,9, 10,13, 14,18, 19,24, 25,30
Y	abstract; claims; figures 1,2D,2F paragraphs [0012], [0020], [0030], [0035]	23,29

-/--

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
5 December 2014	15/12/2014

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Wirner, Christoph

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2014/053897

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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Y	abstract; figures paragraph [0046] - paragraph [0059]	23,29

X	US 5 606 186 A (NODA MINORU [JP]) 25 February 1997 (1997-02-25)	19-22, 24-28,30
Y	abstract; claims; figure 1 column 4, line 51 - column 5, line 3	23,29

X	EP 2 521 168 A1 (IMEC [BE]) 7 November 2012 (2012-11-07)	19,22, 24,25, 28,30
Y	abstract; claims; figure 1F paragraph [0036] - paragraph [0037]	23,29

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Y	abstract; claims; figure 1	23,29
X,P	-& US 2014/091392 A1 (TAKADA TOMOYUKI [JP] ET AL) 3 April 2014 (2014-04-03) abstract; claims; figure 1 paragraph [0010]	19,22, 25,28

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
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