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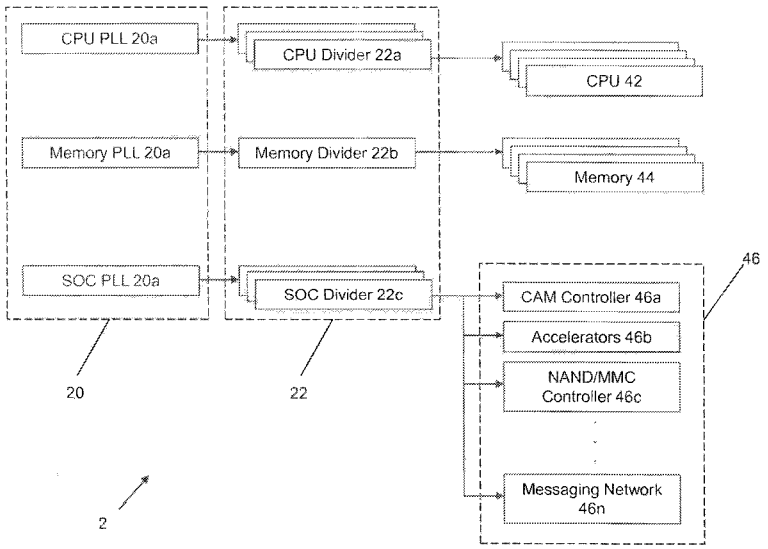
(54) **Title**: IMPROVED MULTI-PART CLOCK MANAGEMENT

Fig. 1



(57) **Abstract**: An improved approach is described for implementing a clock management system. A multi-part phase locked loop circuit is provided to handle the different clock needs of the circuit, where each of the phase locked loops within the multi-part phase locked loop circuit may feed a clock output to one or more divider circuits. The divider circuits may be dedicated to specific components. For example, a SoC PLL may generate a clock output to a SoC divider that is dedicated to providing a clock to content address memory (CAM) components. This approach allows the clock management system to efficiently generate clock signals with variable levels of frequencies, even for complicated circuits having many different functional portions and components.

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IMPROVED MULTI-PART CLOCK MANAGEMENT

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] The present disclosure relates to clock management systems.

Background Art

[0002] Clock synthesis circuits are used to generate clock signals. Typically, the clock signals provide timing for operation of a circuit. In some applications, multiple timing references or clocks, which operate at different frequencies, are required. For example, some communication standards require operation of transmitter and receiver circuits at pre-determined clock frequencies. If a circuit supports multiple timing references, then multiple clock synthesis circuits are used.

[0003] Some circuit applications require a variable frequency clock. In general, a variable frequency clock is a clock that may change its frequency over time or for different purposes. There are many reasons why it is important to be able to vary the clock frequency that is used for timing in a computing system. For example, it is often important to vary the clock frequency in a computer system because of an interface between different controllers and components in the system.

[0004] A complicated circuit may require many different variances to the clock frequency for different portions of the circuit. The different required clock frequencies may span a very large and disparate range of different frequencies. In addition, the different clock frequencies may need to be directed to many different parts of the circuit.

BRIEF SUMMARY OF THE INVENTION

[0005] An improved approach is described for implementing a clock management system. According to some embodiments, a multi-part phase locked loop circuit is provided to handle the different clock needs of the circuit. The multi-part phase locked loop circuit includes a first PLL (phase locked loop) for processor components, a second

PLL for memory components, and a third PLL for SoC components. Each of the phase locked loops within the multi-part phase locked loop circuit may feed a clock output to one or more divider circuits. The divider circuits may be dedicated to specific components. For example, the SoC PLL may generate a clock output to a SoC divider that is dedicated to providing a clock to content address memory (CAM) components. This approach allows the clock management system to efficiently generate clock signals with variable levels of frequencies, even for complicated circuits having many different functional portions and components.

[0006] Other and additional objects, features, and advantages of the invention are described in the detailed description, figures, and claims.

BRIEF DESCRIPTION OF THE DRAWINGS/FIGURES

[0007] Fig. 1 illustrates a clock management system having a multi-part PLL.

[0008] Fig. 2 illustrates an example system in which a multi-part PLL may be employed to generate clock signals.

[0009] Fig. 3 shows a diagram of a multi-part PLL circuit.

[0010] Fig. 4 shows a diagram of a divider circuit to receive a clock output from a multi-part PLL circuit.

[0011] Fig. 5 shows a diagram of an alternate divider circuit to receive a clock output from a multi-part PLL circuit.

DETAILED DESCRIPTION OF THE INVENTION

[0012] Embodiments will now be described in detail with respect to the drawings, which are provided as illustrative examples so as to enable those skilled in the art to practice the invention. Notably, the figures and examples below are not meant to limit the scope of the present disclosure to a single embodiment, but other embodiments are possible by way of interchange of some or all of described or illustrated embodiments. Whenever convenient, the same reference numbers will be used throughout the drawings to refer to the same or like parts. Where certain elements of the these embodiments can be partially or fully implemented using these known components, only those portions of known components that are necessary for understanding of the embodiment will be described,

and details descriptions of other portions of such known components will be omitted so as to not obscure the description of the invention. In the present specification, an embodiment showing a singular component should not be considered to be limiting; rather, the scope is intended to encompass other embodiments including a plurality of the same components, and vice versa, unless explicitly stated otherwise. Further, the present disclosure encompasses present and future known equivalents to the components referred to by way of illustration.

[0013] Some embodiments are directed to an improved approach for implementing a clock management system. In a complicated system having many different components and subsystems, it is likely that the different system portions will need to have clock frequencies that differ from one another. As an example, consider a modern multiprocessing system that has multiple processors, multiple memory components (e.g., DRAMs), and multiple specialized subsystems on the chips/system, where these components or subsystems may have clock requirements that greatly differ from one another.

[0014] A multi-part phase locked loop circuit is provided to handle the different clock needs of the circuit, where each of the phase locked loops within the multi-part phase locked loop circuit may feed a clock output to one or more divider circuits. The divider circuits may be dedicated to specific components. For example, a SoC PLL may generate a clock output to a SoC divider that is dedicated to providing a clock to content address memory (CAM) components. This approach allows the clock management system to efficiently generate clock signals with variable levels of frequencies, even for complicated circuits having many different functional portions and components, and therefore different clock needs for the different portions of the system.

[0015] Fig. 1 illustrates a high level diagram of a clock management circuit 2 according to some embodiments. The clock management circuit 2 is operable to generate clock signals that are utilized by multiple disparate portions or multiple categories of subsystems within a larger electronic system or chip. Clock management circuit 2 includes a multi-part phase locked loop circuit 20 that feeds clock outputs to a multi-part divider circuit 22.

[0016] Multi-part phase locked loop circuit 20 includes multiples PLLs that are specific to the different types of components and subsystems in the circuit which will require a

clock signal. For example, phase locked loop circuit 20 may include a CPU PLL 20a that generates a clock output to be used by CPUs, processors, and/or processor cores. The phase locked loop circuit 20 may also include a memory PLL 20b for generating a clock output to be used by memory components, such as DRAM memory components. In addition, the phase locked loop 20 may include a SoC PLL 20c that generates a clock output to be used by various subsystems, engines, controllers, engines, and other system components, e.g., which are implemented as system on chips (SoCs). While only three PLLs 20a, 20b, and 20c are shown in this example (which correspond to clock signals for certain specific components types), it is noted that different embodiments may be implemented which include additional PLLs and/or additional combinations of PLLs to generate clock outputs for other types or combinations of system components.

[0017] Some or all of the outputs from the multi-part phase locked loop circuit 20 may be provided to a multi-part divider circuit 22 to provide a frequency scaled clock from the PLLs 20a, 20b, and 20c to multiple downstream components. One or more CPU dividers 22a are used to provide CPU clock signal(s) from the CPU PLL 20a to be consumed by CPUs, processors, and/or processor cores 42. In a multiprocessor or multi-core processor system, there will be multiple CPU dividers 22a to provide clocks to the multiple CPUs, processors, and/or processor cores 42. A memory divider 22b is used to provide a frequency scaled clock from the memory PLL 20b to be consumed by memory components 44.

[0018] A SoC divider 22c is used to provide a frequency scaled clock to downstream components 46, such as subsystems, engines, accelerators, and/or controllers. Examples of such downstream SoC components 46 include, for example, CAM controllers 46a, accelerators 46b, NAND/MMC controllers 46c, and a messaging network 46n. Other examples of such components not shown in the figure include Flash interfaces, compression engines, a GPU, data transfer engines, RAID engines, encryption engines, security acceleration engines, network acceleration engines, and/or RSA/ECC engines. In this way, the system 2 can provide a dedicated divider circuit to specific components/component types, e.g., where a SoC PLL generates a clock output to a SoC divider that is dedicated to CAM devices.

[0019] The multi-part phase locked loop circuit of the present disclosure can be used in any type of system that requires and consumes multiple disparate clock frequencies in the

different parts of the system. Fig. 2 depicts an example processing system 100E that may utilize the clock management circuit 2 of Fig. 1 to generate clock signals for the different components within the system 100E. The processing system 100E has three bidirectional communication rings (each depicted as a bold-line oval), a plurality of CPUs (e.g. Core-0, Core-1, etc), a plurality of accelerators (e.g. Network Acceleration Engine, POE, Interlaken-LAI) to perform a set of operations, and a plurality of IO blocks (e.g. ICI , general purpose I/O 1E06, etc). The three rings can be used for referring to and/or moving packets within the context of an on-chip network.

[0020] As shown, each instance of the plurality of CPUs (e.g. Core-0, Core-1, etc) comprises its respective level two cache (e.g. the respective L2 cache, as shown), and comprises its respective level one cache for instructions (e.g. the respective L1-I cache) and its respective level one cache for data (e.g. the respective L1-D cache). Each of the CPUs has a virtual CPU (e.g. $1E04_0$,...$1E04_3$) depicted as an oval within a core.

[0021] In some embodiments, the Memory Distributed Interconnect 1E32 (MDI) comprises a memory interconnect ring, the messaging network 1E42 comprises a messaging ring, and the I/O distributed interconnect 1E42 (IODI) comprises an IO interconnect ring. Also shown is a packet ordering engine (POE) to distribute packets in a particular order to a networking output. In this embodiment, the POE connects to the network acceleration engine (shown as, Network Accel Engine).

[0022] In the embodiment shown, the processing system 100E includes an L3 cache to connect to the MDI ring (e.g. an example of a memory interconnect ring 132). The interconnect serves to connect memory elements to other memory elements, possibly using a message station or direct memory access logic. For example, in some embodiments, an instance of a CPU (e.g. Core-0) includes one or more cache memories local to the CPU, and the local cache can be connected to the Memory Distributed Interconnect 1E32 ring. A memory interconnect ring 1E32 can be configured to any width, including any width of any interconnected memory, or even multiples of widths of any interconnected memory, or even fractions of the width of any interconnected memory.

[0023] The processing system 100E depicts an I/O distributed interconnect 1E42 (an example of an IO interconnect ring 142), which I/O distributed interconnect 1E42 serves

to connect IO blocks (e.g. PCI-E, POE, etc) and accelerators (e.g. security engines) to each other, and to the fast messaging network (as shown).

[0024] The accelerators can be located and configured to perform any specific operation. In some cases, one or more accelerators can be configured to perform such a specific operation autonomously (e.g. without intra-operation intervention by a CPU) and, in some cases, one or more accelerators can be configured to perform operations under programmatic control, which programmatic control can be implemented in any combination of configuration registers and sequencing units (e.g. a finite state machine, a micro-sequencer, etc). The Interlaken LA / PCI-E (104) may be a single module or two separate modules. The Interlaken LA of 104 may be individually enabled or disabled while the PCI-E is always enabled in some embodiments. The Interlaken LA / PCI-E (104) interacts with a number of devices, including for example, a CAM devices 102 (also referred to as a "knowledge based processor" or "KBP"), a host, and peripherals and I/O. The clock management system described above may be used to generate a clock that is consumed by CAM device 102.

[0025] Further details regarding an exemplary processing system that may be used to implement the system of Fig. 2 is described in United States Patent Application No. 13/107,809 filed May 13, 2011, entitled "IMPLEMENTING INTEGRATED NETWORKING FUNCTIONS AT WIRE SPEED", which is hereby expressly incorporated by reference in its entirety.

[0026] Fig. 3 shows a diagram of an example multi-part phase locked loop circuit 300. Multi-part phase locked loop circuit 300 includes a CPU PLL 302, a memory PLL 304, and a SoC PLL 306.

[0027] The CPU PLL 302 operates to provide a clock output on line 314 to a CPU divider (shown in Fig. 4). The output clock signal generated by the CPU PLL 302 is used by downstream CPU(s), processor(s), and/or processor core(s).

[0028] In some embodiments the ratio of the output frequency of the CPU PLL 302 with respect to the input frequency is determined by reference and feedback divider levels according to Equation 1:

Equation 1: $Frequency_{out} = [(Frequency_{in} / R) \times (F+1) \times 4] / 2$

[0029] The input value on line 308 allows for a specified frequency input value (e.g., a user specified value) to be provided (e.g., at the boot-up time of the circuit), which is used

to control the divider of the feedback loop 310, and which corresponds to the "F" value of Equation 1. The reference clock signal is provided on line 332, which is the "$Frequency_{in}$" value of Equation 1. Line 330 provides another input value that may be specified to be applied at boot-up time, which is applied to the reference divider 334 and which corresponds to the "R" value of Equation 1. The CPU PLL outputs a lock signal on line 313, which is sent to a status register 312.

[0030] The memory PLL 304 operates to provide an output clock signal on line 316 to a memory divider. The clock output generated by the memory PLL 304 is used by downstream memory components, after being suitably divided by a divider circuit (shown in Fig. 5).

[0031] The ratio of the output frequency of the memory PLL 304 with respect to the input frequency is determined by reference and feedback divider levels according to the Equation 1 that was provided above. The reference clock is provided on line 342, which corresponds to the "$Frequency_{in}$" value of Equation 1. Line 346 from the control register portion 344 provides an input value corresponding to the "R" value of Equation 1, which is applied to the reference divider 340. The input value on line 348 from the control register 344 corresponds to the "F" value in Equation 1, and is applied to the frequency divider 320 to implement a feedback loop.

[0032] A reset signal may be applied to the memory PLL on line 338. The reset signal value is provided from the control register portion 336. In the reset state, the PLL is powered down and the output to the divider circuit is forced low. The memory PLL 304 outputs a lock signal on line 318, which is sent to the status register 312.

[0033] The SoC PLL 306 operates to provide a clock output on line 326 to a SoC divider. The output clock signal generated by the SoC PLL 306 is used by downstream subsystems, engines, accelerators, and/or controllers, such as a CAM controller, NAND controller, MMC controller, messaging network, Flash interface, compression engine, GPU, data transfer engine, RAID engine, encryption engine, security acceleration engine, network acceleration engine, and/or RSA/ECC engine.

[0034] As with the other PLLs, the ratio of the output frequency of the SoC PLL 306 with respect to the input frequency is determined by reference and feedback divider levels according to Equation 1. The reference clock is provided on line 355, which corresponds to the "$Frequency_{in}$" value of Equation 1. Line 351 from the control register portion 344

provides an input value corresponding to the "R" value of Equation 1, which is applied to the reference divider 358. The input value on line 350 from the control register 344 corresponds to the "F" value in Equation 1, and is applied to the frequency divider 322 to implement a feedback loop.

[0035] A reset signal may be applied to the SoC PLL on line 362. The reset signal value is provided from the control register portion 360. In the reset state, the PLL is powered down and the output to the divider circuit is forced low. The SoC PLL 306 outputs a lock signal on line 324, which is sent to the status register 312.

[0036] Fig. 4 shows a schematic of an example CPU divider circuit 400. In some embodiments, each core of a multi-core processor (such as the system shown in Fig. 2) corresponds to its own dedicated CPU divider 400. This enables independent clock control for each individual core. While the circuit shown in Fig. 4 is for a single core, the registers may be shared among the multiple cores with different bit fields in the registers controlling the dividers for all the cores.

[0037] The CPU divider 400 includes a dynamic frequency selection divider (DFS) 402, which allows for dynamic frequency clocking that enables the circuit to dynamically operate at different frequencies depending on the instruction being executed. A gray-code counter 404 is employed to dynamically control the frequency generated by the divider 402. The divider values can be incremented or decremented using the gray-code counter 404. This allows the device to employ a high divider value at power-up, to start up with a low clock frequency, and then decrement the divider 402 until the frequency has ramped up to the operating frequency. The divider value is provided by register 412, the increment value is provided by register 414, and the decrement value is provided by register 416.

[0038] The phase delay block 406 is used to impose phase delays for the CPU clock. In some embodiments, when the PLL circuit is used in an 8-core system there are four phase relationships between the eight core clocks, where the basic unit of phase change is 90 degrees. The phase delay block 406 is controlled an input from control register 410. This allows for the rising and falling edges of the clocks to be adjusted to reduce noise in the overall system.

[0039] Various types of input clocks 426 may be provided to the divider circuit 400 through mux 424. For example, a test clock may be provided that is output from circuit 400 as the core clock 428. The test clock is sent on line 432 through mux 408 to bypass

the divider 402. Mux 408 is controlled to perform this bypass based on a bypass control signal from the register 422.

[0040] A core PLL output clock is the clock that is provided from CPU 302 (of Fig. 3). This is the output clock 428 that is used to drive the cores in normal operation, when suitably divided by divider 402 and phase adjusted by block 406. In this mode, the control signal from register 422 is used to control mux 408 to pass the output from block 406 instead of line 432 as the clock signal on line 428.

[0041] An oscillator clock may be used as a reference clock for the system. This type of clock is used if the entire system is to be run on the same clock, e.g., if the entire circuit is to be run in a scan or test mode. This type of clock would also travel through line 432 to bypass the divider 402 and phase delay block 406.

[0042] The divider 402 can be disabled or reset. When disabled or reset, the divider output is set low. The "reset" control signal is provided from control register 418. The "disable" control signal is provide from control register 420.

[0043] Fig. 5 shows a schematic of an example divider circuit 500 that can be used to implement either the memory divider or the SoC divider. In some embodiments, there are multiple SoC divider circuits that each are dedicated to a specific downstream SoC component, which enables independent clock control for each SoC component. For example, one of the divider circuits 500 can be dedicated to CAM devices in the overall processing system. However, a single divider 500 can be implemented to handle multiple memory components of the same type, e.g., to handle multiple DRAM memory components.

[0044] Like the divider circuit shown in Fig. 4, the divider circuit 500 of Fig. 5 includes a dynamic frequency selection divider (DFS) 502 which allows for dynamic frequency clocking that enables the circuit to dynamically operate at different frequencies. While the register functions are similar, a different set of control registers are used in the circuit of Fig. 5 as compared to those used in the circuit of Fig. 4. One difference is that a phase delay register is not needed for the circuit of Fig. 4. This because the clocking frequencies needed for the SoC and memory clocks are relatively less prone to noise as compared to the core clocks, and therefore will not need the phase delays that may be needed for the core clocks.

[0045] A gray-code counter 504 is employed to dynamically control the frequency generated by the divider 502 in circuit 500. As before, the divider values can be incremented or decremented using the gray-code counter 504, which allows the device to employ a high divider value at power-up, to start up with a low clock frequency, and then decrement the divider 502 until the frequency has ramped up to the operating frequency. The divider value is provided by register 512, the increment value is provided by register 514, and the decrement value is provided by register 516.

[0046] Input clocks 526 may be provided to the divider circuit 500 through mux 524. The input clock from the previous PLL stage is also provided on line 530 through mux 524. When the circuit 500 is used as a memory divider, the clock is provided from the memory PLL 304. When the circuit 500 is used as a SoC divider, the clock is provided from the SoC PLL 304. These are the clocks that drive the normal operation of memory and SoCs from the divider circuit 500. In this mode, a control signal from register 522 is used to control mux 508 to output a clock signal 528 from the divider 502.

[0047] The circuit 500 may also be used in a bypass mode, where mux 408 is controlled by a bypass signal from the register 422 to send the signal on line 432 through mux 508 to bypass the divider 502. For example, a test clock or oscillator clock may be provided as inputs 526 on line 532 through mux 524 which bypasses the divider 502 in the bypass mode.

[0048] The divider 502 can be disabled or reset. When disabled or reset, the divider output is set low. The "reset" control signal is provided from control register 518. The "disable" control signal is provide from control register 520.

[0049] Therefore, what has been described is an improved approach for implementing a clock management system. The multi-part phase locked loop circuit of the disclosure is provided to handle the different clock needs of the circuit, where each of the phase locked loops within the multi-part phase locked loop circuit may feed a clock output to one or more divider circuits. The divider circuits may be dedicated to specific components. For example, a SoC PLL may generate a clock output to a SoC divider that is dedicated to providing a clock to content address memory (CAM) components. This approach allows the clock management system to efficiently generate clock signals with variable levels of frequencies, even for complicated circuits having many different functional portions and components, and therefore different clock needs for the different portions of the system.

[0050] While various embodiments have been described above, it should be understood that they have been presented by way of example only, and not limitation. Thus, the breadth and scope of a preferred embodiment should not be limited by any of the above-described exemplary embodiments, but should be defined only in accordance with the following claims and their equivalents.

WHAT IS CLAIMED IS:

1. A system, comprising:

a plurality of processor cores;

a memory component;

a content addressable memory;

a first phase locked loop circuit to output a first clock output for the plurality of processor cores;

a second phase locked loop circuit to output a second clock output for the memory component;

a third phase locked loop circuit to output a third clock for the content addressable memory;

a plurality of first divider circuits coupled to the first phase locked loop circuit to frequency scale the first clock output for consumption by the plurality of processor cores, in which each processor core from the plurality of processor cores is associated with a dedicated first divider circuit;

a second divider circuit coupled to the second phase locked loop circuit to frequency scale the second clock output for consumption by the memory component; and

a plurality of third divider circuits coupled to the third phase locked loop circuit to frequency scale the third clock output, in which the content addressable memory is associated with a dedicated third divider circuit.

2. The system of claim 1 in which the third phase locked loop circuit and the plurality of third divider circuits are to provide the third clock output to SoC components.

3. The system of claim 2 in which the plurality of third divider circuits is to provide the third clock output to a SoC component corresponding to a controller for the content addressable memory.

4. The system of claim 2 in which the SoC components comprise a NAND controller, a MMC controller, a messaging network, a Flash interface, a compression engine, a GPU, data transfer engine, a RAID engine, an encryption engine, a security acceleration engine, a network acceleration engine, or a RSA/ECC engine.

5. The system of claim 2 in which an individual SoC component or component type corresponds to a dedicated divider circuit.

6. The system of claim 1 in which the first, second, or third divider circuits are implemented as dynamic frequency selection dividers.

7. The system of claim 6 further comprising a counter to control the dynamic frequency selection divider.

8. The system of claim 7 in which the counter is a gray-code counter.

9. The system of claim 1 in which the plurality of first divider circuits further comprises a phase delay block to impose a phase delay output.

10. A method for implementing clock management, comprising:

generating a first clock output with a first phase locked loop circuit;

generating a second clock output with a second phase locked loop circuit;

generating a third clock output with a third phase locked loop circuit;

utilizing a plurality of first divider circuits coupled to the first phase locked loop circuit to frequency scale the first clock output for consumption by a plurality of processor cores, in which each processor core from the plurality of processor cores is associated with a dedicated first divider circuit;

utilizing a second divider circuit coupled to the second phase locked loop circuit to frequency scale the second clock output for consumption by a memory component; and

utilizing a plurality of third divider circuits coupled to the third phase locked loop circuit to frequency scale the third clock output for consumption by a content addressable memory, in which the content addressable memory is associated with a dedicated third divider circuit.

11. The method of claim 10 in which the third phase locked loop circuit and the plurality of third divider circuit provide the third clock output to SoC components.

12. The method of claim 11 in which the plurality of third divider circuits provide the third clock output to a SoC component corresponding to a controller for the content addressable memory.

13. The method of claim 11 in which the SoC components comprise a NAND controller, a MMC controller, a messaging network, a Flash interface, a compression engine, a GPU, data transfer engine, a RAID engine, an encryption engine, a security acceleration engine, a network acceleration engine, or a RSA/ECC engine.

14. The method of claim 11 in which an individual SoC component or component type corresponds to a dedicated divider circuit.

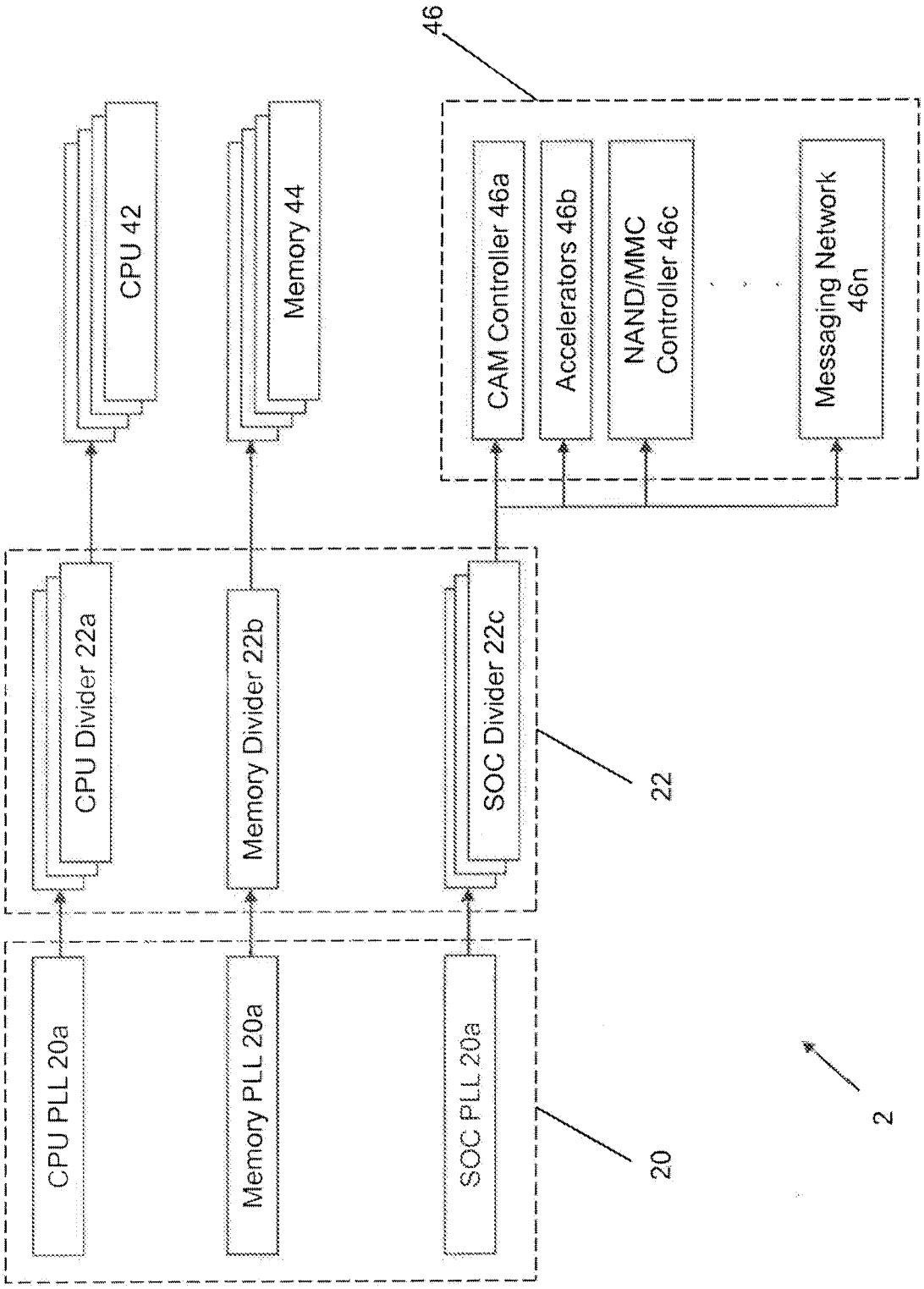
15. The method of claim 14 in which the first, second, or third divider circuits are implemented as dynamic frequency selection dividers.

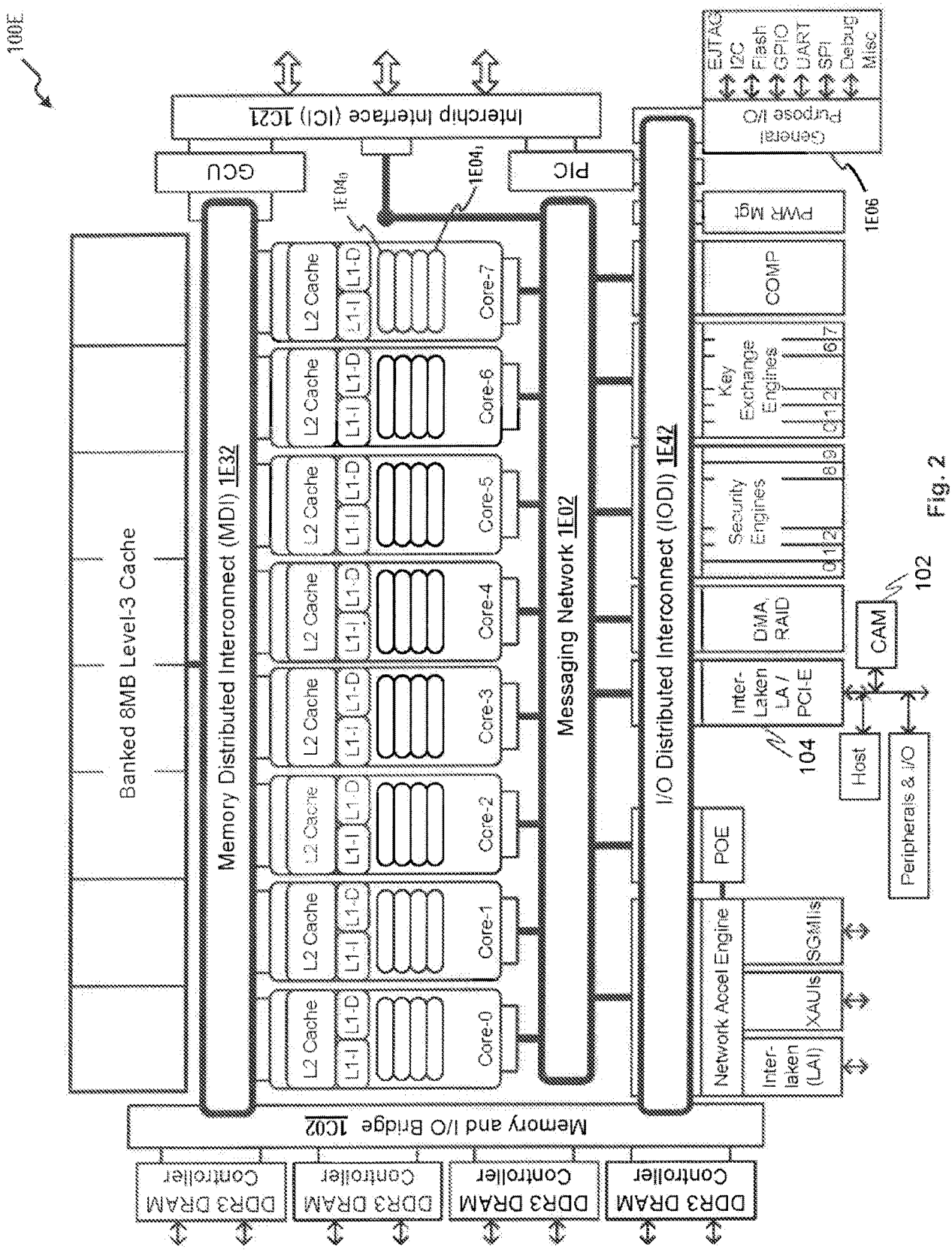
16. The method of claim 15 in which a counter is used to control the dynamic frequency selection divider.

17. The method of claim 16 in which the counter is a gray-code counter.

18. The method of claim 14 in which a phase delay is imposed for the plurality of first divider circuits.

Fig. 1


46
CPU 42
Memory 44
CAM Controller 46a
Accelerators 46b
NAND/MMC Controller 46c
Messaging Network 46n
CPU Divider 22a
Memory Divider 22b
SOC Divider 22c
22
CPU PLL 20a
Memory PLL 20a
SOC PLL 20a
20
2


100E
Interchip Interface (ICI) 1C21
GCU
PIC
1E04b
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Core-7
Core-6
Core-5
Core-4
Core-3
Core-2
Core-1
Core-0
L2 Cache
L1-I
L1-D
Banked 8MB Level-3 Cache
Memory Distributed Interconnect (MDI) 1E32
Messaging Network 1E02
I/O Distributed Interconnect (IODI) 1E42
Memory and I/O Bridge 1C02
DDR3 DRAM Controller
DDR3 DRAM Controller
DDR3 DRAM Controller
DDR3 DRAM Controller
Network Accel Engine
POE
Inter-laken (LAI)
XAUIs
SGMIIs
Inter-Laken LA / PCI-E
104
DMA RAID
Security Engines
Key Exchange Engines
COMP
PWR Mgt
General Purpose I/O
EJTAG
I2C
Flash
GPIO
UART
SPI
Debug
Misc
1E06
CAM
102
Host
Peripherals & I/O

Fig. 2

Fig. 3

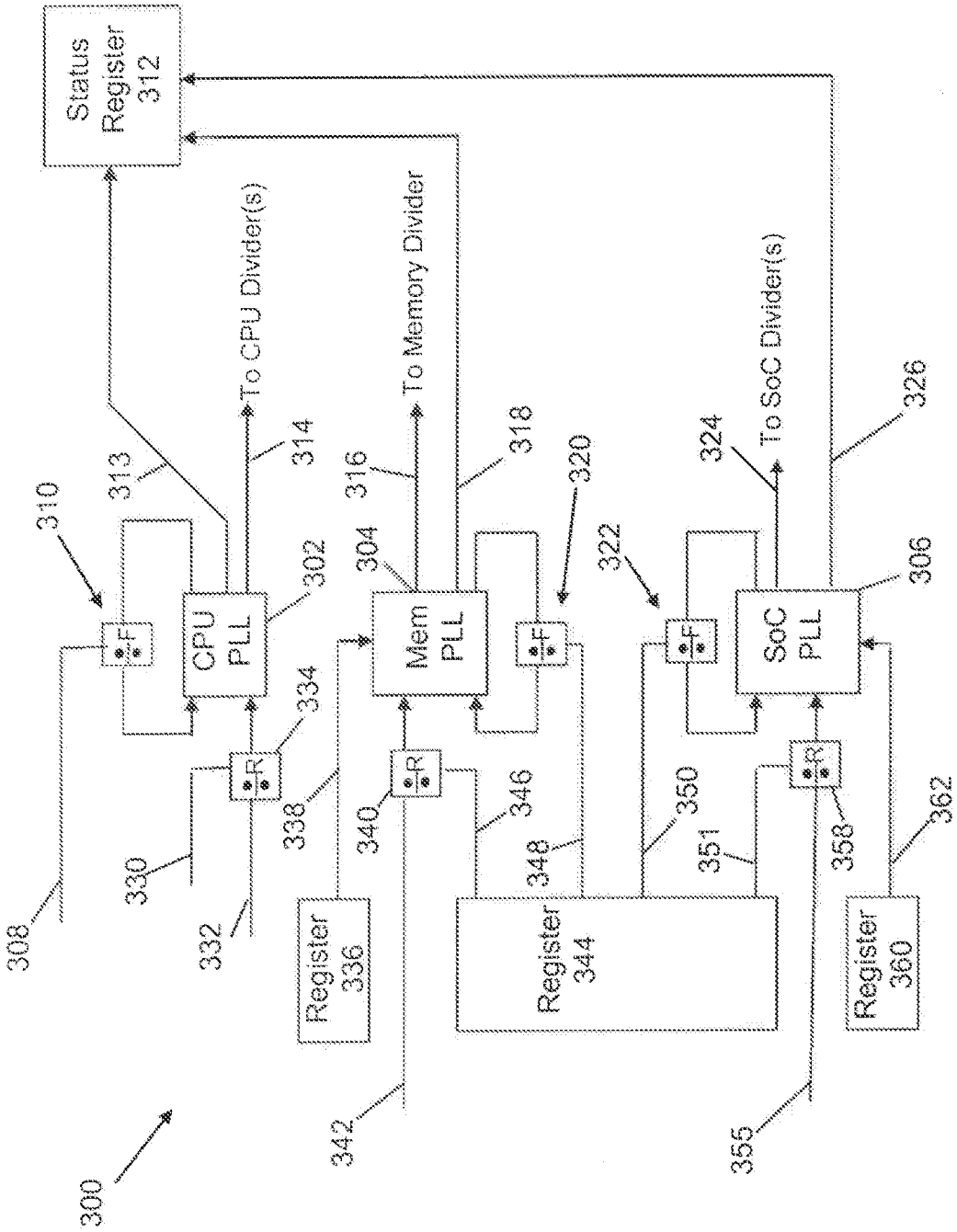

Status Register 312
To CPU Divider(s)
To Memory Divider
To SoC Divider(s)
CPU PLL
Mem PLL
SoC PLL
F
R
Register 336
Register 344
Register 360
300
302
304
306
308
310
313
314
316
318
320
322
324
326
330
332
334
338
340
342
346
348
350
351
355
358
362

Fig. 4

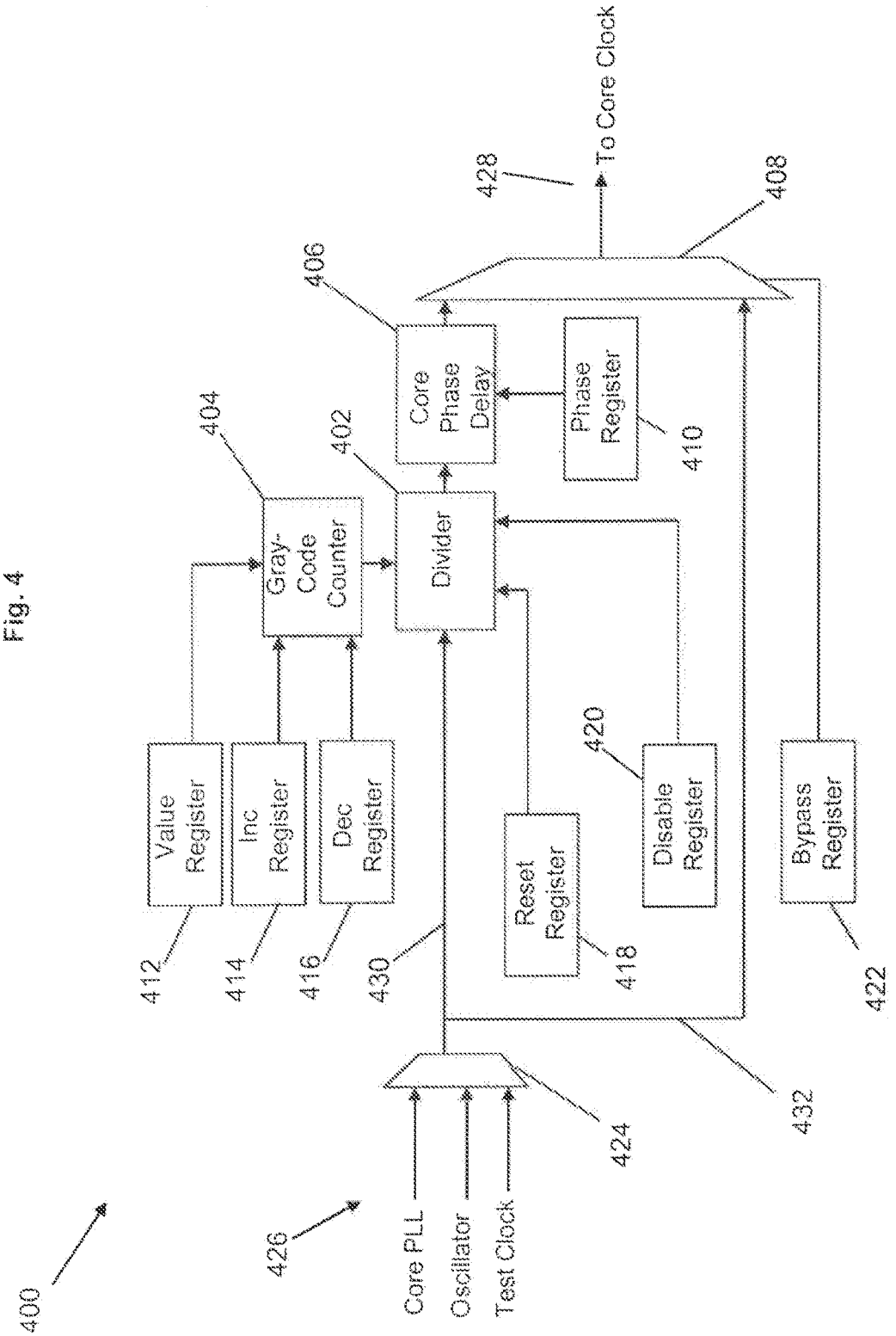
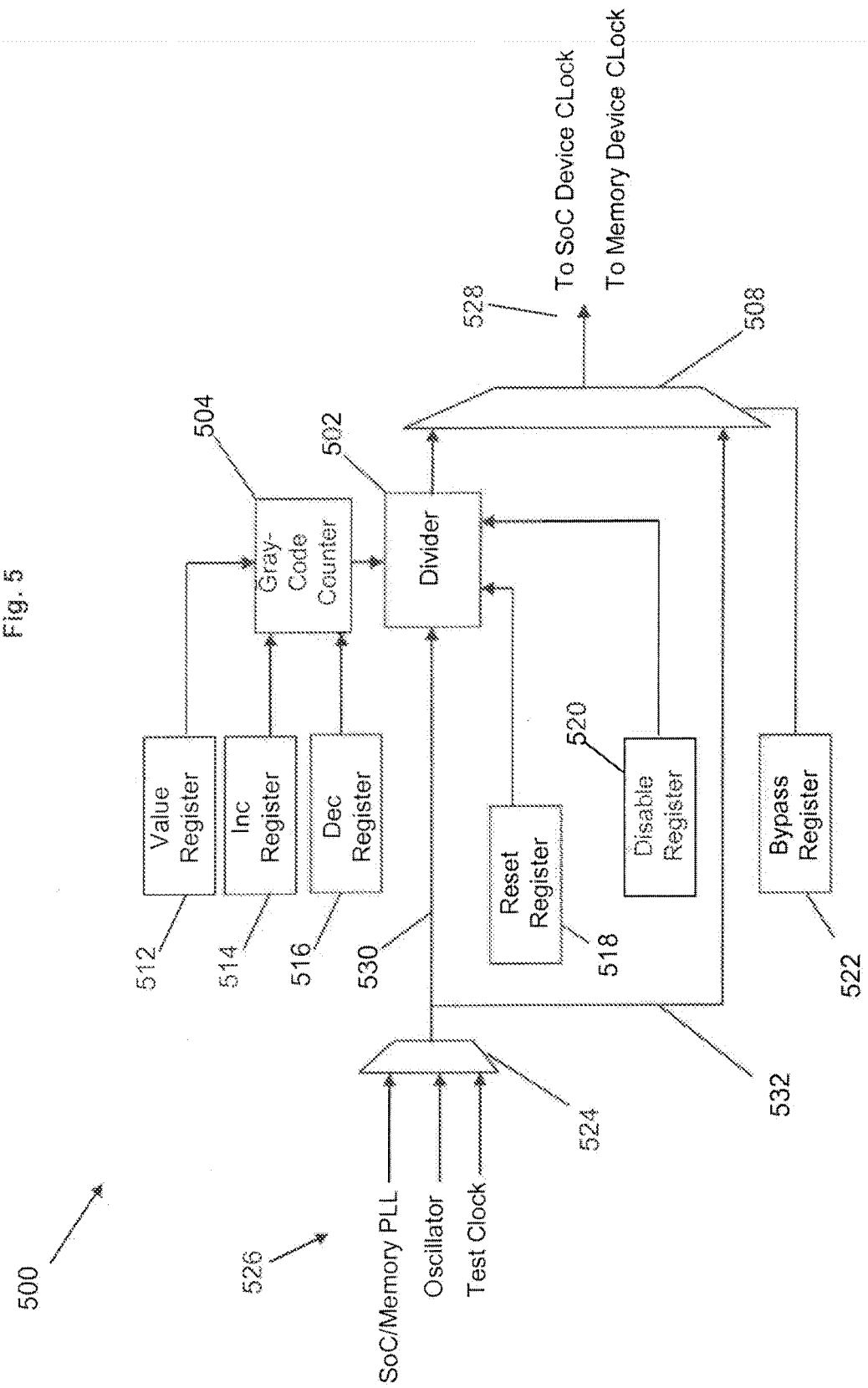

400
426
Core PLL
Oscillator
Test Clock
424
432
412
Value Register
414
Inc Register
416
Dec Register
430
Gray-Code Counter
404
Divider
402
Reset Register
418
420
Disable Register
422
Bypass Register
Core Phase Delay
406
Phase Register
410
408
428
To Core Clock

Fig. 5


500
526
SoC/Memory PLL
Oscillator
Test Clock
524
532
530
512
514
516
Value Register
Inc Register
Dec Register
Gray-Code Counter
504
502
Divider
528
To SoC Device CLock
To Memory Device CLock
508
Reset Register
518
520
Disable Register
Bypass Register
522

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 12/42697

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - H03D 3/24 (2012.01)
USPC - 375/376
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
USPC: 375/376

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
USPC: 375/354, 359, 376; 327/1, 12, 17, 18; 331/11 (keyword limited - see search terms below)

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
PubWEST (PGPB, USPT, USOC, EPAB, JPAB); GOOGLE; Google Scholar, Thomson Innovation
Terms: clock, phase, lock, loop, processor, cores, frequency, divide, content, addressable, memory, associative, storage, system, chip, scaling, multiple, dynamic, delay, count, gray, code.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2009/0085620 A1 (May et al.) 02 April 2009 (02.04.2009), entire document, especially abstract, Figs. 1, 2, para [0007], [0016], [0017], [0018], [0019], [0020], [0021], [0022].	1-18
Y	US 2011/0051486 A1 (Chang et al.) 03 March 2011 (03.03.2011), entire document, especially abstract, para [0007], [0042], [0044].	1-18
Y	US 2008/0028249 A1 (Agrawal) 01 January 2008 (01.01.2008), entire document, especially abstract, para [0010], [0011], [0014], [0032].	6-8, 15-17
A	US 2007/0208964 A1 (Sandon et al.) 06 September 2007 (06.09.2007), entire document, especially abstract, para [0003], [0005], [0016], [0017], [0025].	1-18
A	US 2011/0001571 A1 (Sutardja) 06 January 2011 (06.01.2011), entire document, especially abstract, para [0157], [0158], [0170].	1-18
A	US 2009/0115472 A1 (Pfaff et al.) 07 May 2009 (07.05.2009), entire document, especially abstract, para [0009], [0064], [0077], [0096], [0112].	1-18

☐ Further documents are listed in the continuation of Box C. ☐

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
21 August 2012 (21.08.2012)	07 SEP 2012
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	Authorized officer: Lee W. Young PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

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