

[72] Inventor Yasumasa Narukiyo
Nagoya, Japan
[21] Appl. No. 844,339
[22] Filed July 24, 1969
[45] Patented Sept. 7, 1971
[73] Assignee Okuma Machinery Works Ltd.
Nagoya, Japan
[32] Priority June 24, 1963
[33] Japan
[31] 38/33,318
Continuation-in-part of application Ser. No.
376,689, June 22, 1964, now Patent No.
3,478,346.

[51] Int. Cl. G08c 9/04
[50] Field of Search 340/347,
357, 358; 250/233

[56] References Cited
UNITED STATES PATENTS
3,478,346 11/1969 Yasumasa Narukiyo..... 340/347
Primary Examiner—Maynard R. Wilbur
Assistant Examiner—Charles D. Miller
Attorney—Waters, Roditi, Schwartz & Nissen

[54] NONE-AMBIGUOUS READING SYSTEMS FOR
ANALOG-TO-DIGITAL CONVERTERS
8 Claims, 19 Drawing Figs.

[52] U.S. Cl. 340/347 P

ABSTRACT: Reading system free from ambiguity of reading at the boundary of two digits in which two n -digits code disks representing higher order digits and lower order digits are employed and three successive signals from said higher order code disk which generate signals, adjacent two signals of which partially overlap each other, and two signals generated from said lower order disk respectively representing any digits in the higher half and lower half of n -digits are fed to a logical circuit performing a particular logical operation.

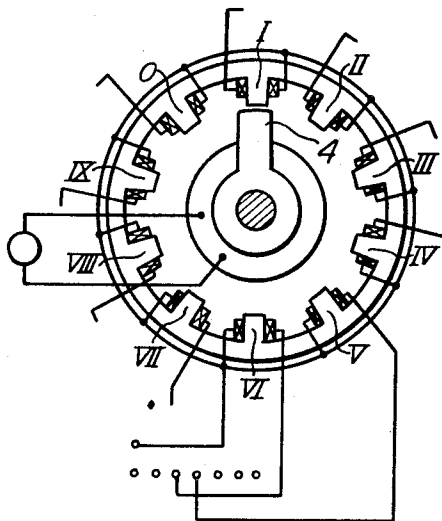


FIG. 1

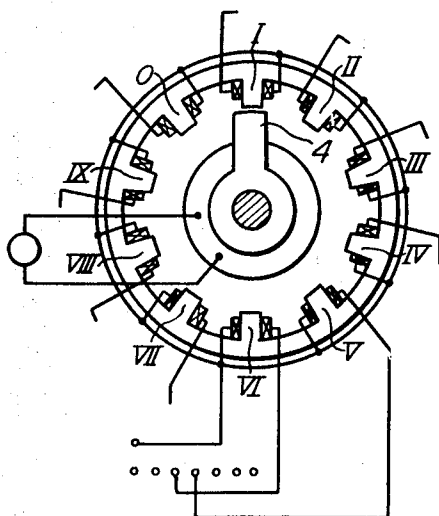


FIG. 2

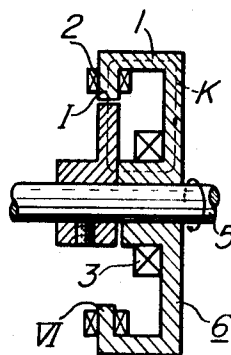
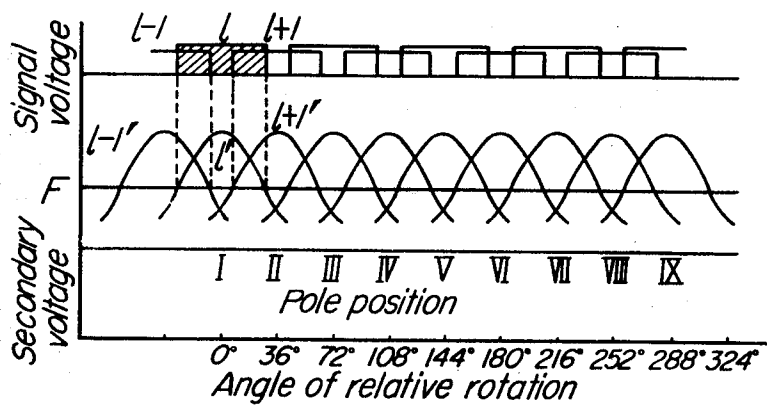


FIG. 3



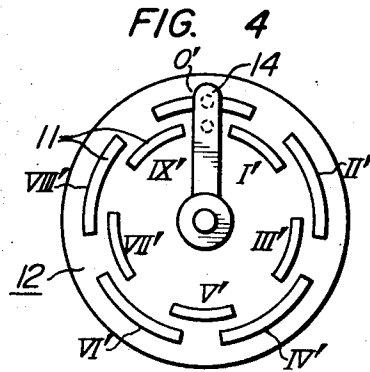
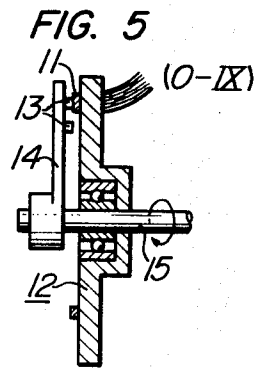
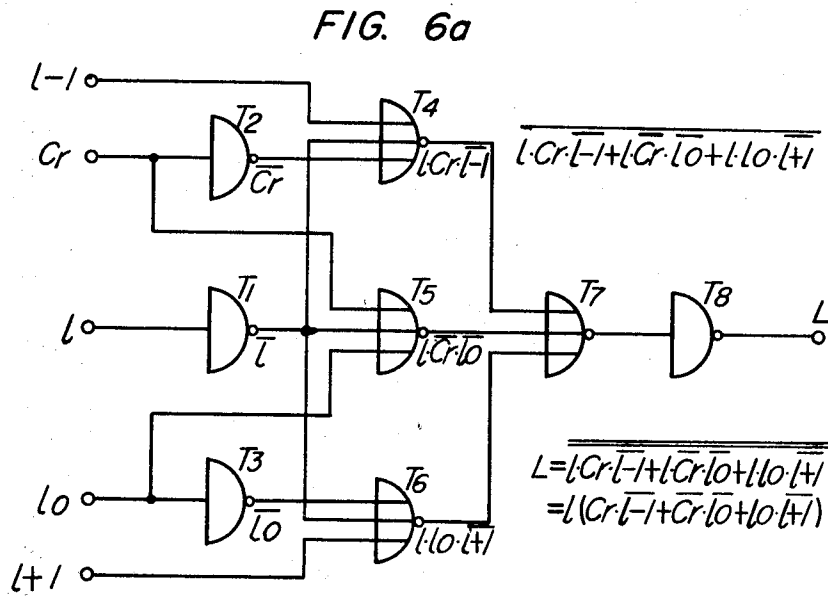


FIG. 6b

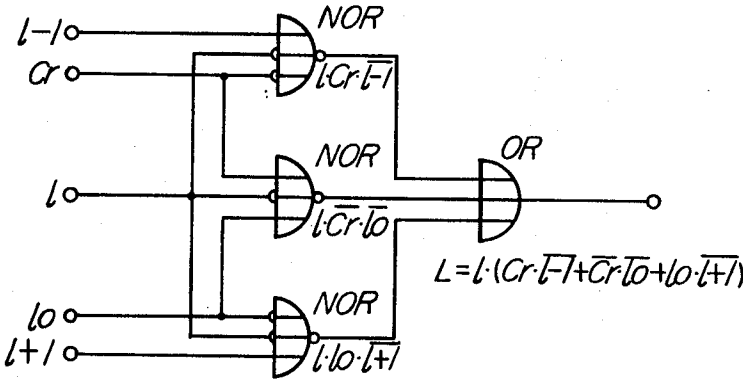


FIG. 6c

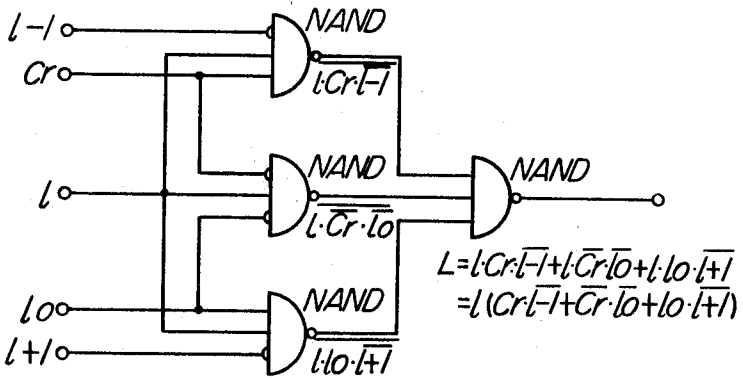


FIG. 6d

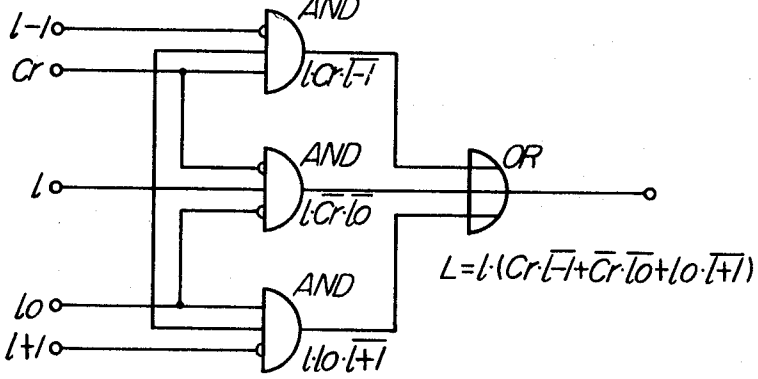


FIG. 7

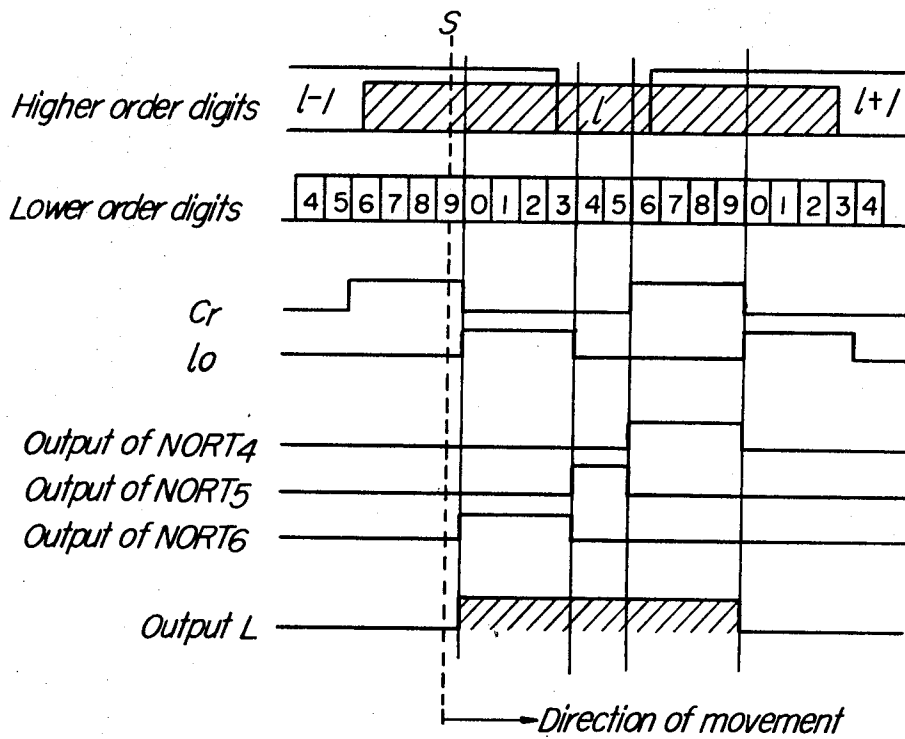


FIG. 8a

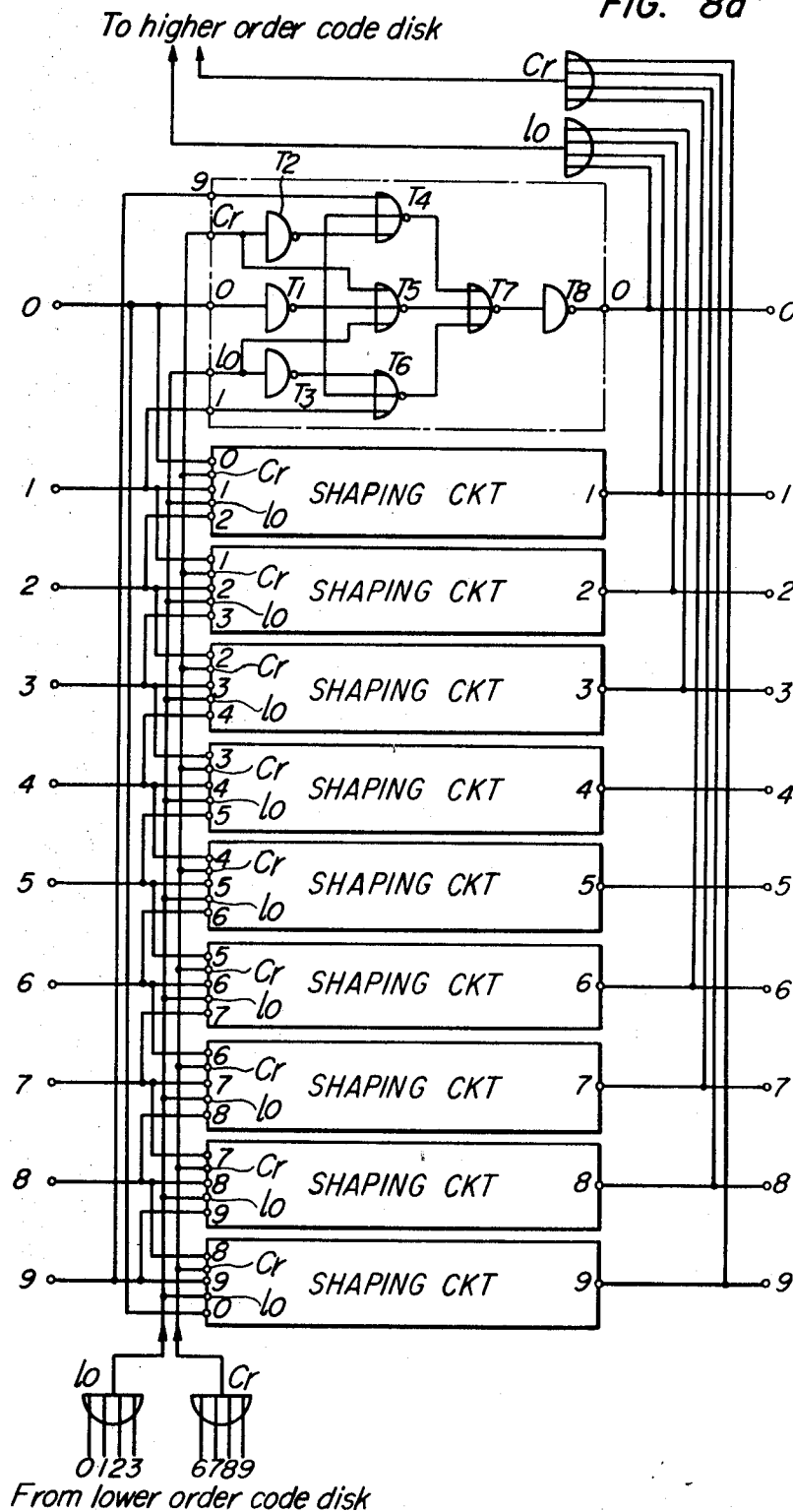


FIG. 8b

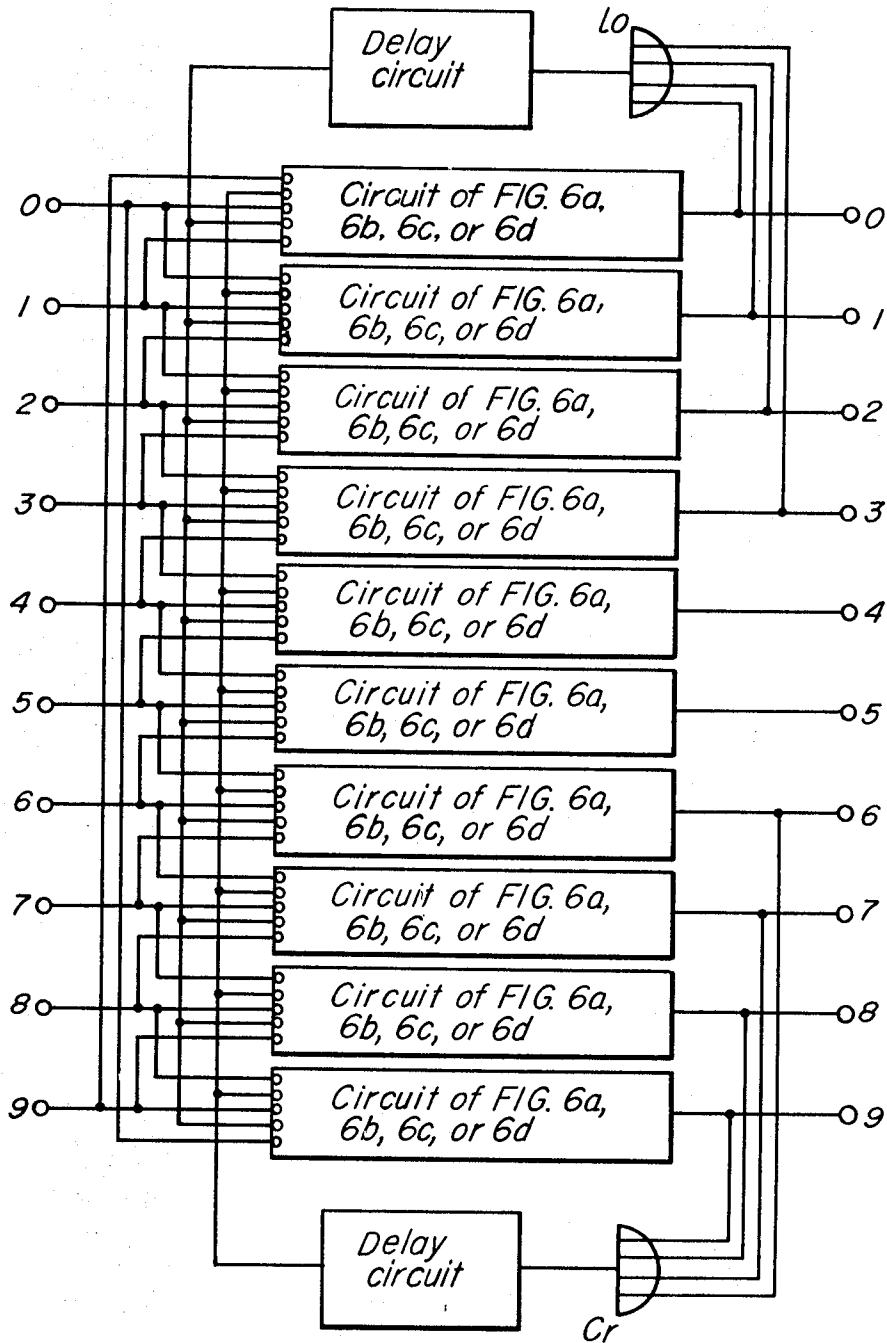


FIG. 9

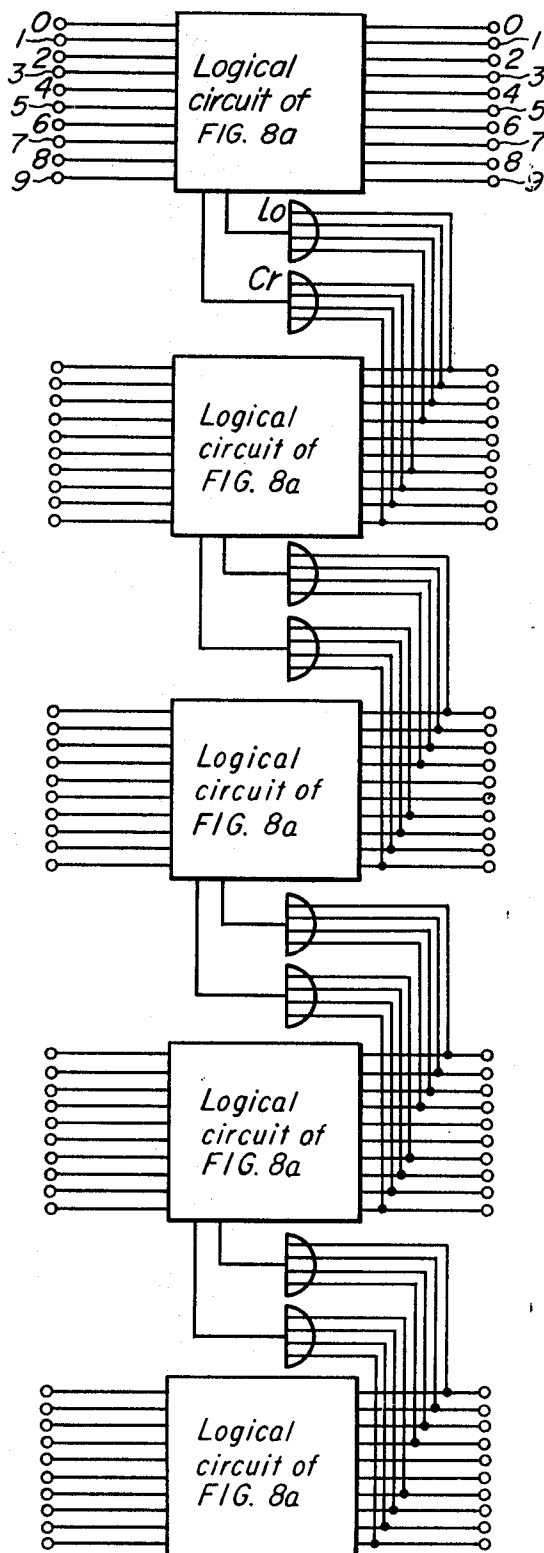
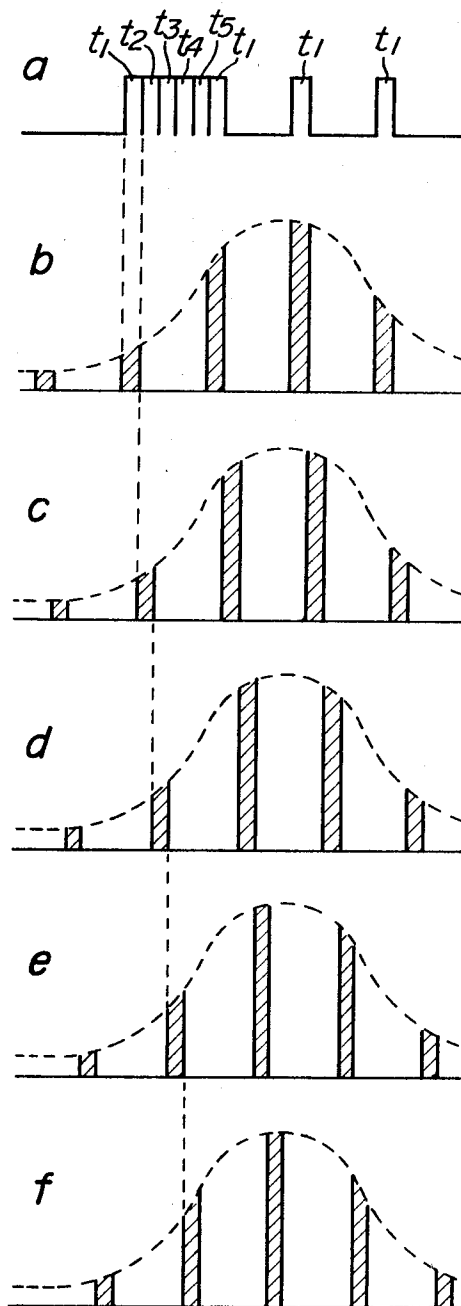


FIG. 10



NONE-AMBIGUOUS READING SYSTEMS FOR ANALOG-TO-DIGITAL CONVERTERS

CROSS-REFERENCES TO RELATED APPLICATIONS

This application is a continuation-in-part application of my earlier application Ser. No. 376,689, filed June 22, 1964, and now U. S. Pat. No. 3,478,346.

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to reading systems of analog-to-digital converters for converting analog quantities, such as angles of rotation and so on into digital quantities.

2. Description of the Prior Art

In general, a code disk, forming the main part of an analog-to-digital converter, is subject to being erroneously read at boundaries between adjacent digits on the code disk. Thus, due to inevitable minor errors, such as caused by unevenness of end conditions of the code disk and brushes and so on whether "9" is read or "0" is read is, for example, governed by chance, this resulting in numerous errors.

There have been various contrivances proposed for preventing errors, for example, greater than one digit. Particularly, there have been utilized a code disk of alternate or binary code, a Gray Code disk, a special reading brush arrangement such as a dual-brush system, V-brush system, and the like.

SUMMARY OF THE INVENTION

An object of the present invention is to provide a novel reading system of high precision, which is simple in construction and low in cost, preserving the advantages of noncontact point technique of the prior art.

According to the present invention, a code disk capable of supplying signals of a required number of digits is employed for providing signals successively overlapping in time, which are introduced into a logical circuit satisfying the logical equation, $L = (C_r l - 1 + C_r l_0 + l_0 l + 1)$, whereby the reading of an erroneous signal is prevented.

BRIEF DESCRIPTION OF THE DRAWING

FIG. 1 is an elevational view of a noncontact-type code plate or disk embodying the present invention;

FIG. 2 is a longitudinal sectional view of the disk shown in FIG. 1;

FIG. 3 is a graph showing the relation between an angle of relative rotation of the disk and a secondary voltage induced therein;

FIG. 4 is an elevational view of a contact-type code disk embodying the invention;

FIG. 5 is a longitudinal sectional view of the disk shown in FIG. 4;

FIGS. 6a to 6d are block diagrams of logical circuits according to the invention;

FIG. 7 is a graph showing wave forms at various parts of the logical circuit of FIG. 6;

FIGS. 8a and 8b are block diagrams of logical circuits according to the invention for a decimal code disk and disks, respectively;

FIG. 9 is a block diagram of a logical circuit according to the invention for five-decimal code disks; and

FIGS. 10a - 10f are graphs for illustrating time-sharing operation.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Let us consider a code disk for providing 10 decimal digits per rotation of the disk shaft by way of example. If two such disks are used, and the rotating shafts are coupled together with a great ratio of 10 : 1, the input shaft can provide 100 digits. In this case, when the lower order shaft is at the boundary between "9" and "0," the higher order shaft should be at

the boundary between adjacent digits, and the change of the higher order shaft by one digit and the change of the lower order shaft from "9" to "0" should be coincident in position with regard to time. However, it is generally impossible to accomplish this coincidence because of mechanical inaccuracy, and erroneous signals are apt occur. For example, an incorrect reading of "17", "18", "19", "10", "20", "21," can be effected on rotation of the input shaft.

The present invention prevents such an error from occurring. Thus, referring to FIGS. 1 and 2, the code disk shown comprises a stator 6 carrying uniformly spaced magnetic poles 1 along the outer periphery, the poles extending inwardly towards the center of disk.

Each pole 1 carries a secondary coil 2 wound thereon. The stator 6 also has a boss around which a primary coil 3 is wound. A rotating shaft 5 rotatably passes through the boss of stator 6 and carries a rotatable magnetic piece 4 fixed to the shaft, and having a circumferential width larger than that of each pole 0, I, II, III,

When the primary coil 3 is energized and the shaft 5 is rotated, with the magnetic piece 4 successively passing in front of poles 1 each carrying the secondary coil 2, with a magnetic circuit K (FIG. 2) completed and opened successively, voltages are successively induced in the secondary coils 2 as shown in FIG. 3 by $l-1$, l , $l+1$,, which overlap one another with respect to time. These voltages are introduced into a shaping circuit such as a Schmitt trigger circuit, to provide successively overlapping signals, $l-1$, l , $l+1$,, as shown in FIG. 3, with a line F as the operating point. These signals are introduced into the logical circuit shown in FIG. 6a, 6b, 6c or 6d.

The logical circuit of FIG. 6a, which performs the logical operation $L = (C_r l - 1 + C_r l_0 + l_0 l + 1)$, comprises NOR circuits T_1 , T_2 , T_3 , T_4 , T_5 , T_6 , T_7 and T_8 . The NOR circuit is a circuit in which, when a signal A is received as an input signal, the circuit delivers a signal $\bar{A}$ as an output signal, and when the input signal is A, B, and C, its output is $\overline{A+B+C}$, i.e. $\bar{A}\bar{B}\bar{C}$. In other words, the NOR circuit is the combination of a NOT circuit and an OR circuit. The symbols $l-1$, l , and $l+1$ represent any successive digital signals signals such as 0, 1, 2; 5, 6, 7; 9, 0, 1 and the like which are obtained by shaping the output of each pole of the higher order code disk as shown in FIG. 3, whereas the symbols $l-1$, l , and $l+1$ represent inverted signals thereof. C_r and l represent signals from the lower code disk which will hereinafter be referred to as carry signals for the sake of convenience. C_r can be a signal generated when the magnetic piece 4 passes a pole of the lower code disk according to any one of successive digits including 9 taken from 5 to 9, for example 6,789, and l_0 can be that of successive digits including 0 taken from 0 to 4, for example 0123. However, it is preferable to take 56,789 and 01,234 for C_r and l_0 signal generation, respectively, because this selection enables to make tolerance of the coupling error of the higher order digits and the lower order digits larger. $\bar{C}_r$ and $\bar{l}_0$ represent inverted signals of C_r and l_0 .

Now, referring to FIGS. 1 and 3, if the outputs of the poles 0, I and II of the higher order A-D converter are taken to be $l-1$, l , and $l+1$, respectively, and if the carry signals C_r and l_0 are arranged to be generated when the lower order A-D converter outputs are 6 to 9 and 0 to 3, respectively, the wave shape of each part of the logical circuit of FIG. 6a which is reading out the output signal of the pole I varies as shown in FIG. 7 when the movable piece 4 moves in the increasing number direction.

In FIG. 7, character S represents the position of the movable piece of 4 of the higher order A-D converter. It is assumed that the output of the lower order A-D converter is 9, the higher order converter is delivering both signals $l-1$ and l . The aforementioned logical equation $L = (C_r l - 1 + C_r l_0 + l_0 l + 1)$ is the logical equation for reading out the output l of the higher order converter. Since the signal C_r as well as the signal $l-1$ is being delivered at the position S, the equation L is not satisfied. When the movable piece 4 moves in the increasing

number direction and the lower order digit changes from 9 to 0, the signal C_r disappears, but instead the signal l_0 appears. Consequently $l_0 \cdot \overline{l+1}$ of the NOR circuit T_6 is satisfied resulting in the generation of the signal L. If the movable piece moves further and the lower order digit changes from 30 to 4, the signal l_0 disappears, and hence the term $l_0 \cdot \overline{l+1}$ is no longer satisfied. However, since $l \cdot \overline{C_r} \cdot \overline{l_0}$ of the NOR circuit T_3 is satisfied, the signal L is maintained. If the lower order digit changes from 5 to 6 as a result of a further movement of the movable piece, the term $l \cdot \overline{C_r} \cdot \overline{l_0}$ is no longer satisfied, but instead $l \cdot \overline{C_r} \cdot \overline{l+1}$ of the NOR circuit T_4 is satisfied, and hence the signal L is still maintained. However, if the lower digit changes from 9 to 0 with a further movement of the movable piece, all the terms of the logical equation are no longer satisfied, and hence the signal L disappears. Thus, the logical equation of the signal L is satisfied when the lower order digit is from 0 to 9 within the region of the higher order signal l , and hence the output signal L of the logical circuit of FIG. 6a exactly represents the position of the pole I of the higher order converter.

FIG. 6a shows the logical circuit for reading out the signal of the pole I of the higher order A-D converter. For decimalism, the position of each pole of the higher order A-D converter can be exactly read out by employing 10 such circuits as shown in FIG. 6a.

FIG. 8a shows such a logical circuit for a decimal converter disk. In FIG. 8a, lower left input terminals 0, ---, 3 and 6, ---, 9 are merely connected through respective shaping circuits to the corresponding poles of the lower (or the lowest when more than two code disks are employed) order code disk, respectively. Upper left output terminals C_r and l_0 are connected to input terminals C_r and l_0 , respectively, of the similar logical circuit for the next higher order code disk when more than two code disks are employed, at which time 1,000 or more digits are available. Input terminals 0, ---, 9 are connected to the poles of the higher order code disk corresponding to digits 0, ---, 9, respectively, through respective shaping circuits.

When the carry signals C_r and l_0 satisfy the condition $C_r = \overline{l_0}$, the above mentioned logical equation becomes $L = (C_r \cdot \overline{l+1} + \overline{C_r} \cdot l+1)$. Thus, by employing the carry signals C_r and l_0 , the tolerance of the coupling of the lower order and the higher order digits can be made great. This is one of the outstanding features of the invention.

In the above description, the logical operation has been explained with reference to the logical circuit of FIG. 6a. However, instead of the logical circuit of FIG. 6a, either one of the logical circuits shown in FIGS. 6b to 6d can similarly be employed. The circuit of FIG. 6b comprises three NOR circuits and one OR circuit. The circuit of FIG. 6c comprises four NAND circuits, and the circuit of FIG. 6d comprises three AND circuits and one OR circuit.

If digits are to be read from, for example, five code disks, five such circuits as shown in FIG. 8a are employed as shown in FIG. 9. Thus, if the number of code disks increases, the logical circuit for reading the digits becomes correspondingly complicated and expensive. However, if a time-sharing technique is employed, the reading can be effected with only one such logical circuit as shown in FIG. 8a.

If such logical circuit as shown in FIG. 8a is successively switched from a code disk to the next higher order code disk, ---, to the highest order code disk, to the lowest order code disk, and so on with a train of timing pulses with intervals of, for example, several microseconds, the outputs from the logical circuit for respective code disks will be as shown in FIG. 10 which illustrates the case of five code disks employed. In this case, although the signal for each digit is actually discrete, practically it can be regarded as a continuous one because each time duration of t_1 , t_2 , ---, t_5 is such a short duration as several microseconds.

When only one logical circuit is employed in a time-sharing manner as has just been described for reading digits from any number of code disks, there is the problem that a time dif-

ference by one time interval between adjacent timing pulses exists between the readings of one code disk and the next higher order code disk. However, this difficulty can easily be overcome by delaying the carry signals l_0 and C_r from each code disk by one time interval by employing a delay circuit as is shown in FIG. 8b. Thus, by connecting each input terminal of the logical circuit of FIG. 8b with all the code disks in common, the digits of all the code disks can be read with only one logical circuit as shown in FIG. 8b.

Referring to FIGS. 4 and 5, when a contact-type code disk 12 is shown as a decimal code disk, it may be such that the circle is divided circumferentially into 10 parts, with conductors 11 of 36° spacing for one digit overlapping one another by 18° , and insulated from one another by about a 54° width. The disk 12 carries a central shaft 15 rotatably, which in turn carries a movable piece 14 having contact brushes 13 fixed to the outer end thereof. When the movable piece 14 is rotated with brushes 13 engaging conductors 11 successively, the signals from respective are "on" and "off" signals, the same as shown in FIG. 3. These signals are applied to the logical circuit of FIG. 6a, 6b, 6c or 6d, and L signals are obtained from an output terminal just as in the first embodiment shown in FIGS. 1 and 2.

With the above-mentioned construction of the present invention, there is no danger of erroneous reading, and no limit to number of digits which can be employed. The invention is particularly useful for decimalism and is not limited to "on" and "off" types of signalling.

According to experiments, the width of each digit may vary by ± 20 percent, without affecting the operation. Particularly for noncontact types of reading, there are no sliding parts that would affect the useful life and, moreover, high-speed reading is possible.

I claim:

1. A system for reading digits from an analog-to-digital converter having at least two n -digits notation code disks, n being larger than two, said system comprising m sets of n logical circuits, m being the number of said n -digits notation code disks, the l -th circuit of said logical circuits performing the logical operation $L = (C_r \cdot \overline{l+1} + \overline{C_r} \cdot l_0 + l_0 \cdot \overline{l+1})$ where L is the signal corresponding to any digit signal l generated from the higher order code disk of successive two code disks of said at least two n -digits notation code disks, C_r is a carry signal generated when one signal included in the upper group of output signals from the lower order code disk of said two code disks appears and l_0 is a carry signal generated when one signal included in the lower group of outputs from said lower order code disk appears, said outputs of said lower code disk being divided into said upper and lower groups, said l -th logical circuit having C_r and l_0 input terminals for respectively receiving said carry signals C_r and l_0 from said lower code disk and $l-1$, l and $l+1$ input terminals for respectively receiving three successive digit signals $l-1$, l and $l+1$ from said higher order code disk and L output terminal for deriving therefrom said signal corresponding to said digit signal l , said C_r and l_0 input terminals of each of said n logical circuits of the set corresponding to said higher order code disk being supplied with said carry signals C_r and l_0 from the set of n logical circuits corresponding to said lower order code disk, each of said logical circuits comprising a first NOR circuit coupled to said l , C_r and $l-1$ input terminals, a second NOR circuit coupled to said l , C_r and l_0 input terminals, a third NOR circuit coupled to said l , l_0 and $l+1$ input terminals, and an OR circuit coupled to said first, second and third NOR circuits.

2. A system for reading digits from an analog-to-digital converter having at least two n -digits notation code disks, n being larger than two, said system comprising m sets of n logical circuits, m being the number of said n -digits notation code disks, the l -th circuit of said n logical circuits performing the logical operation $L = (C_r \cdot \overline{l+1} + \overline{C_r} \cdot l_0 + l_0 \cdot \overline{l+1})$ where L is the signal corresponding to any digit signal l generated from the higher order code disk of successive two code disks of said at least two n -digits notation code disks, C_r is a carry signal generated

when one signal included in the upper group of output signals from the lower order code disk of said two code disks appears, and l_0 is a carry signal generated when one signal included in the lower group of outputs from said lower order code disk appears, said outputs of said lower code disk being divided into said upper and lower groups, said l -th logical circuit having C_r and l_0 input terminals for respectively receiving said carry signals C_r and l_0 from said lower code disk and $l-1$, l and $l+1$ input terminals for respectively receiving three successive digit signals $l-1$, l and $l+1$ from said higher order code disk and L output terminal for deriving therefrom said signal corresponding to said digit signal l , said C_r and l_0 input terminals of each of said n logical circuits of the set corresponding to said higher order code disk being supplied with said carry signals C_r and l_0 from the set of n logical circuits corresponding to said lower order code disk, each of said logical circuits comprising a first NAND circuit coupled to said l , C_r and $l-1$ input terminals, a second NAND circuit coupled to said l , C_r and l_0 input terminals, a third NAND circuit coupled to said l , l_0 and $l+1$ input terminals, and a fourth NAND circuit coupled to said first, second and third NAND circuits.

3. A system for reading digits from an analog-to-digital converter having at least two n -digits notation code disks, n being larger than two, said system comprising m sets of n logical circuits, m being the number of said n -digits notation code disks, the l -th circuit of said n logical circuits performing the logical operation $L = l(C_r \cdot \overline{l-1} + \overline{C_r} \cdot l_0 + l_0 \cdot \overline{l+1})$ where L is the signal corresponding to any digit signal l generated from the higher order code disk of successive two code disks of said at least two n -digits notation code disks, C_r is a carry signal generated when one signal included in the upper group of output signals from the lower order code disk of said two code disks appears, and l_0 is a carry signal generated when one signal included in the lower group of outputs from said lower order code disk appears, said outputs of said lower code disk being divided into said upper and lower groups, said l -th logical circuit having C_r and l_0 input terminals for respectively receiving said carry signals C_r and l_0 from said lower code disk and $l-1$, l and $l+1$ input terminals for respectively receiving three successive digit signals $l-1$, l and $l+1$ from said higher order code disk and L output terminal for deriving therefrom said signal corresponding to said digit signal l , said C_r and l_0 input terminals of each of said n logical circuits of the set corresponding to said higher order code disk being supplied with said carry signals C_r and l_0 from the set of n logical circuits corresponding to said lower order code disk, each of said logical circuits comprising a first AND circuit coupled to said l , C_r and $l-1$ input terminals, a second AND circuit coupled to said l , C_r and l_0 input terminals, a third AND circuit coupled to said l , l_0 and $l+1$ input terminals, and an OR circuit coupled to said first, second and third AND circuits.

4. A system for reading digits from an analog-to-digital converter having at least two n -digits notation code disks, n being larger than two, said system comprising a set of n logical circuits, a delay circuit and a switching circuit, the l -th circuit of

said n logical circuits performing the logical operation $L = l(C_r \cdot \overline{l-1} + \overline{C_r} \cdot l_0 + l_0 \cdot \overline{l+1})$ where L is the signal corresponding to any digit signal l generated from the higher order code disk of successive two code disks of said at least two n -digits notation code disks, C_r is a carry signal generated when one signal included in the upper group of output signals from the lower order code disk of said two code disks appears, and l_0 is a carry signal generated when one signal included in the lower group of outputs from said lower order code disk appears, said outputs of said lower code disk being divided into said upper and lower groups, said l -th logical circuit having C_r and l_0 input terminals for respectively receiving said carry signals C_r and l_0 from said lower code disk and $l-1$, l and $l+1$ input terminals for respectively receiving three successive digit signals $l-1$, l and $l+1$ from said high order code disk and L output terminal for deriving therefrom said signal corresponding to said digit signal l , said C_r and l_0 input terminals of each of said n logical circuits being supplied with said carry signals C_r and l_0 from said L output terminal through said delay circuit, said switching circuit switching connections from said input terminals to said code disks from one code disk to another code disks with predetermined time intervals.

5. A system for reading digits from an analog-to-digital converter according to claim 4, wherein each of said logical circuits comprises first, second and third NOR circuits respectively coupled to said l , C_r and l_0 input terminals, a fourth NOR circuit coupled to said $l-1$ input terminal and to said first and second NOR circuits, a fifth NOR circuit coupled to said C_r and l_0 input terminals and to said first NOR circuit, a sixth NOR circuit coupled to said $l+1$ input terminal and to said first and third NOR circuits, a seventh NOR circuit coupled to said fourth, fifth and sixth NOR circuits, and an eighth NOR circuit coupled to said seventh NOR circuit.

6. A system for reading digits from an analog-to-digital converter according to claim 4, wherein each of said logical circuits comprises a first NOR circuit coupled to said l , C_r and $l-1$ input terminals, a second NOR circuit coupled to said l , C_r and l_0 input terminals, a third NOR circuit coupled to said l , l_0 and $l+1$ input terminals, and an OR circuit coupled to said first, second and third NOR circuits.

7. A system for reading digits from an analog-to-digital converter according to claim 4, wherein each of said logical circuits comprises a first NAND circuit coupled to said l , C_r and $l-1$ input terminals, a second NAND circuit coupled to said l , C_r and l_0 input terminals, a third NAND circuit coupled to said l , l_0 and $l+1$ input terminals, and a fourth NAND circuit coupled to said first, second and third NAND circuits.

8. A system for reading digits from an analog-to-digital converter according to claim 4, wherein each of said logical circuits comprises of first AND circuit coupled to said l , C_r and $l-1$ input terminals, a second AND circuit coupled to said l , C_r and l_0 input terminals, a third AND circuit coupled to said l , l_0 and $l+1$ input terminals, and an OR circuit coupled to said first, second and third AND circuits.