

- [54] **DISCOVERY IN A FLUIDIC COMPUTER**
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[52] U.S. Cl. **235/201 PF**, 137/804, 137/820, 137/821, 235/151.34
[51] Int. Cl. **G06d 1/10**
[58] Field of Search 137/804, 805, 814-821; 235/61 M, 151.34, 201

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[57] **ABSTRACT**

A device for calculating and displaying the total gasoline sale price at a gasoline pumping station. A unit price selecting and displaying mechanism controls three fluidic encoders which translate the unit price of gasoline into binary-coded decimal numbers representing tenths, hundredths, and thousandths of a cent respectively. Fluidic decade circuits representing tenths, hundreds and thousandths of a cent respectively are arranged to receive these outputs from the encoders, so that the appropriate cost amounts are added in each decimal digit position. The addition is performed in response to each one of a series of fluidic "add" pulses from a gasoline flowmeter. Each decade circuit includes a BCD adder receiving an addend input from its associated encoder, a BCD accumulator which receives the accumulator total as a return path which reinserts the accumulator total as an augend input into the BCD adder. In response to the flowmeter pulses, the adder adds the unit price digit available from the encoder to the previous total available from the accumulator, and thus generates a new total for the accumulator. Each decade circuit develops a carry output to the next more significant decade.

20 Claims, 6 Drawing Figures

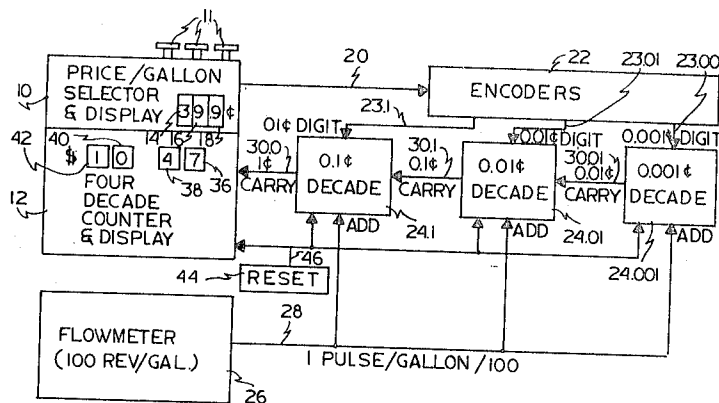


FIG. 1

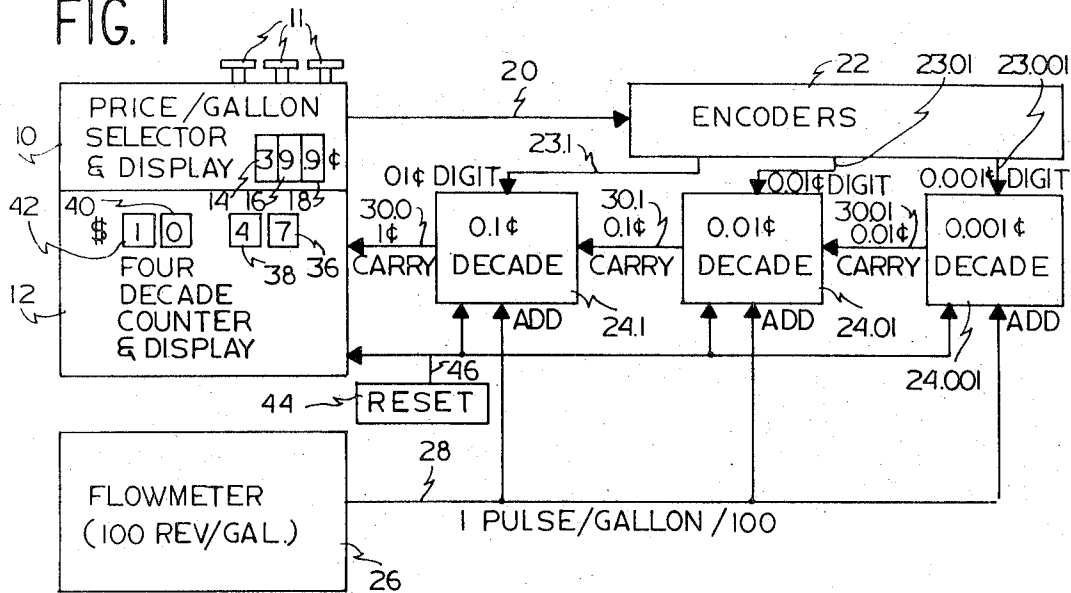


FIG. 3

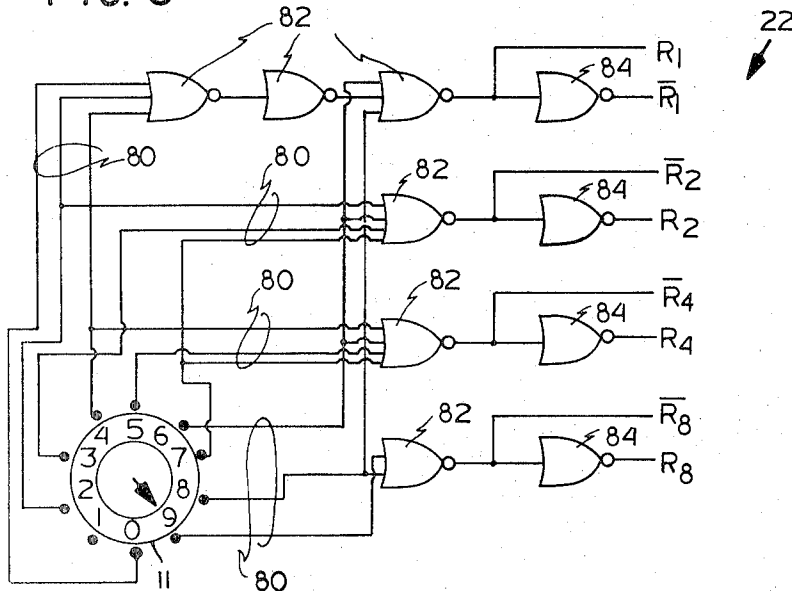
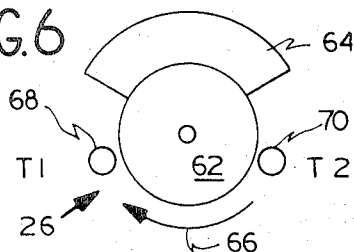
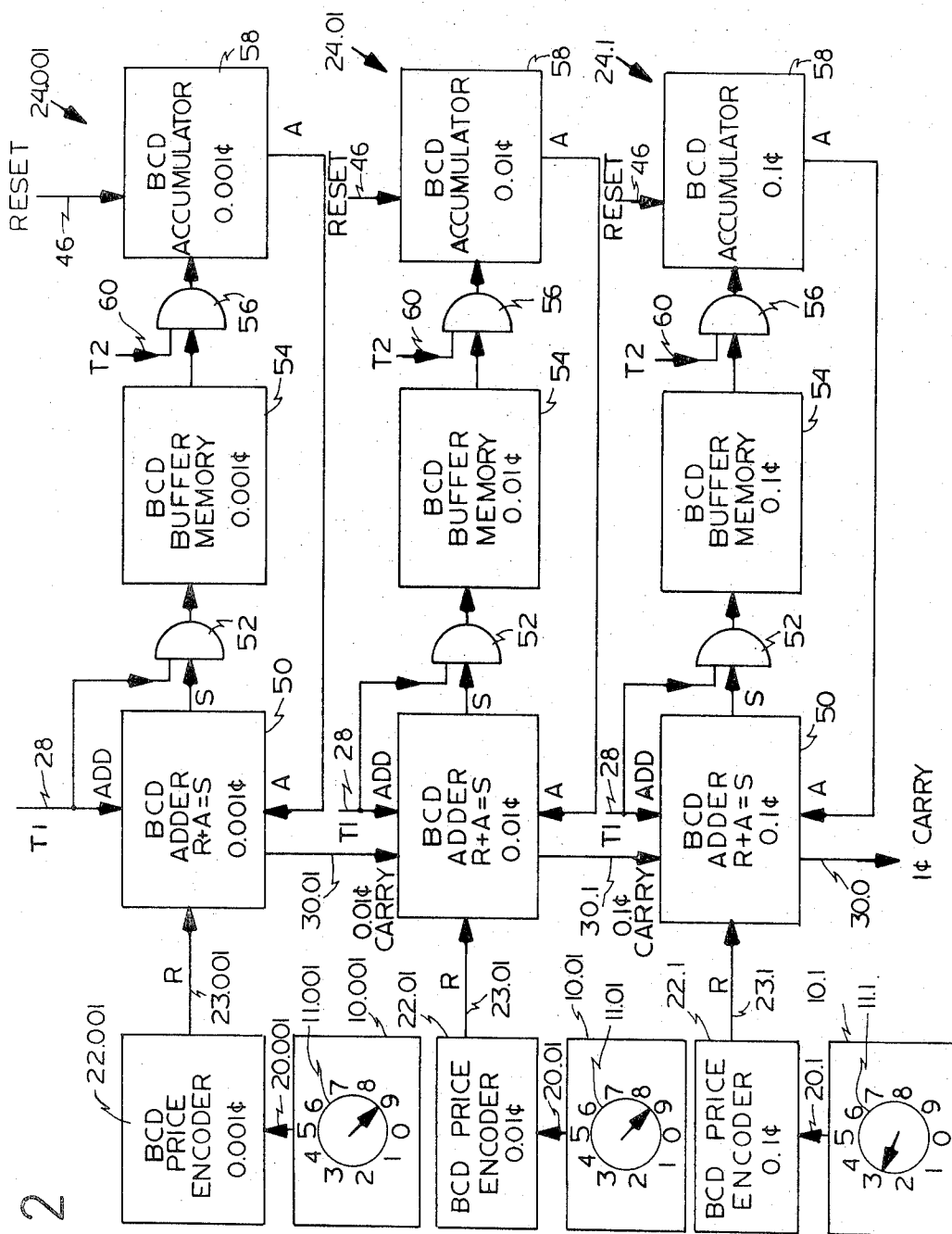
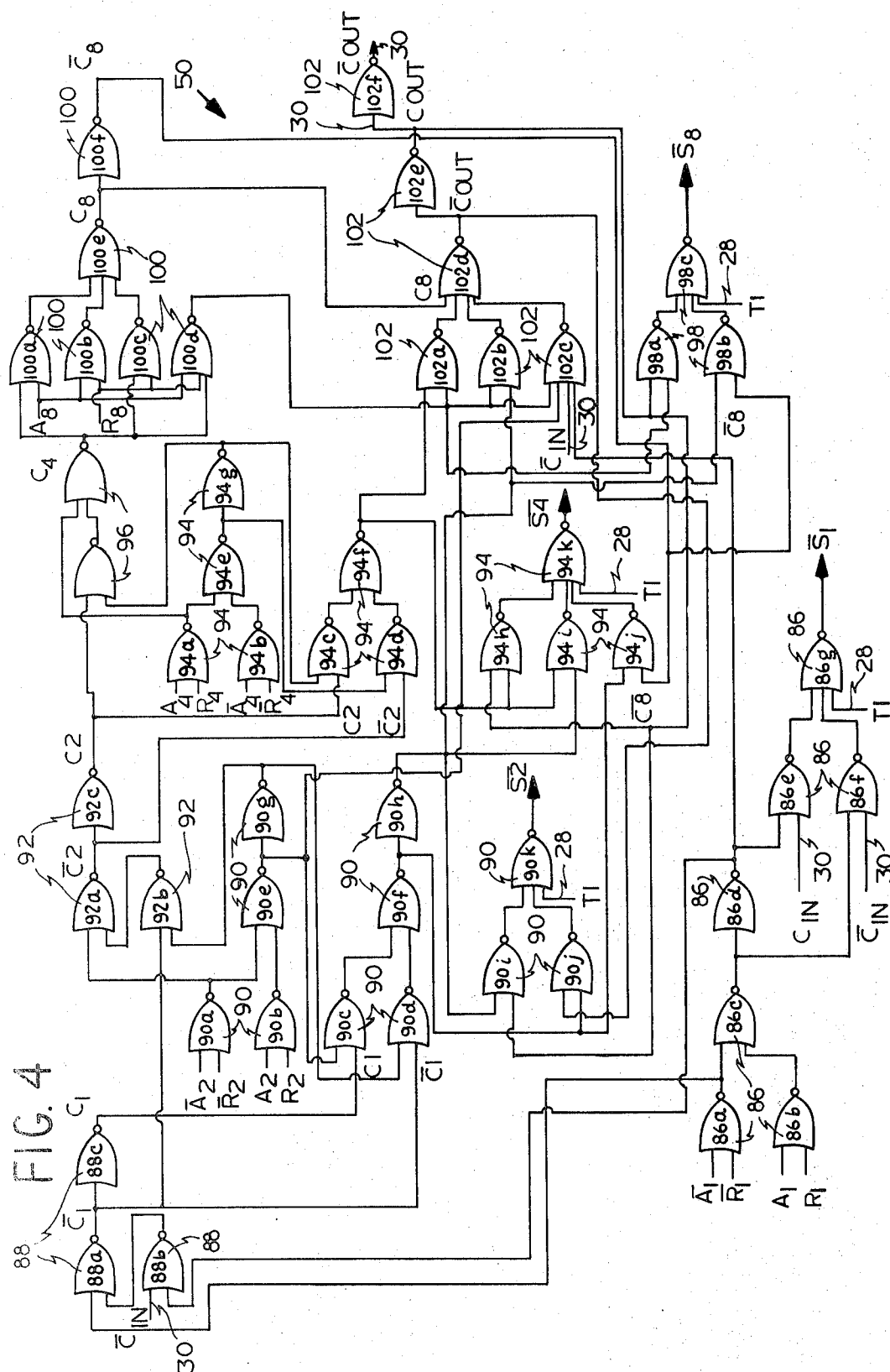


FIG. 6



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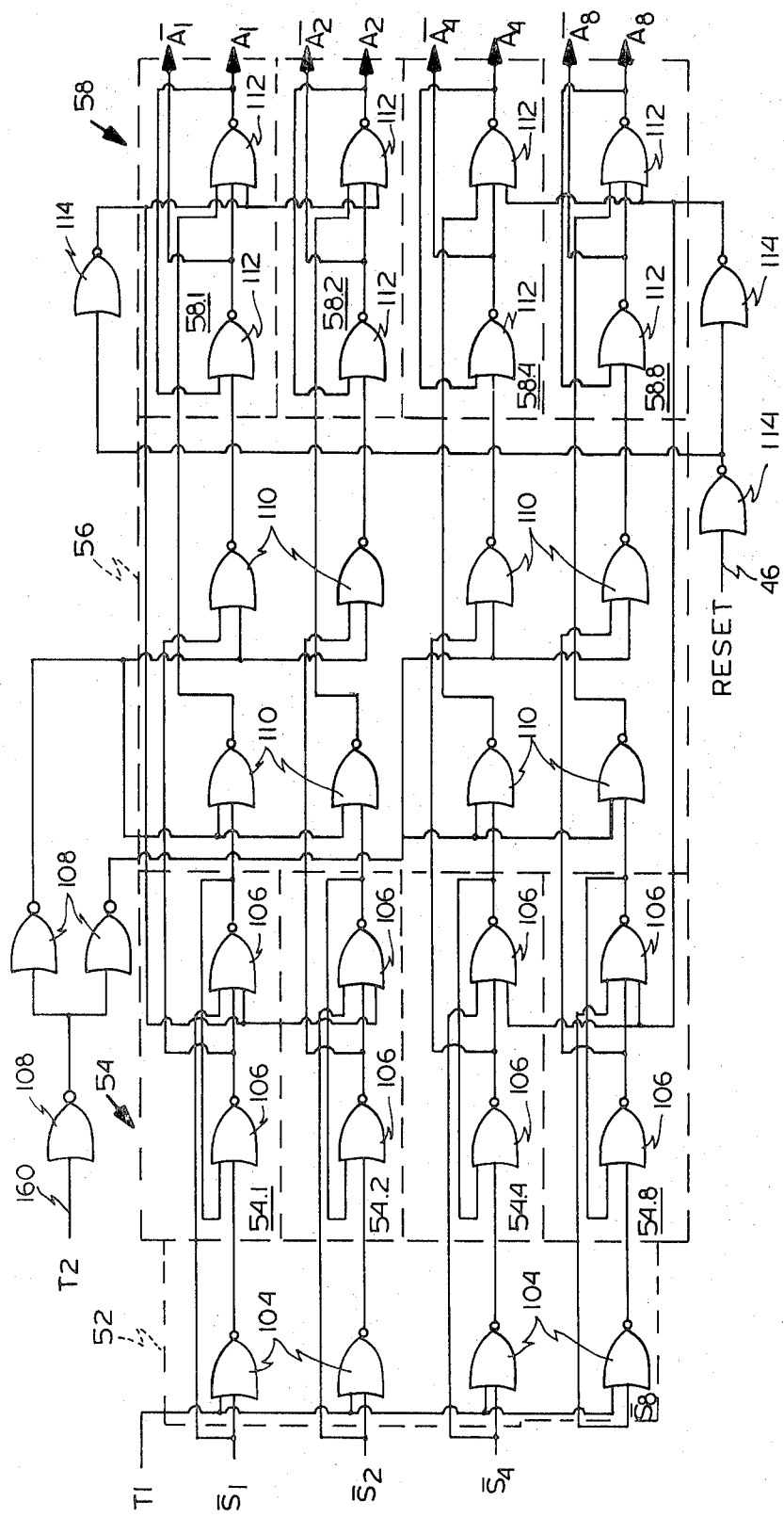


FIG. 5

DISCOVERY IN A FLUIDIC COMPUTER

REFERENCE TO RELATED APPLICATION

This application is a continuation application of applicant's copending application of the same title, Ser. No. 44,782, filed June 9, 1970, now abandoned.

FIELD OF THE INVENTION

This invention relates generally to fluidic computation, and is particularly concerned with a computer for calculating costs or other quantities in flammable environments, such as gasoline stations, where there is a need for high computation speeds without the dangers usually associated with electrical computing equipment.

THE PRIOR ART

This invention can be employed in any computing application where it is desirable to use fluidic circuitry, but necessary to operate reliably at speeds usually attained only by electronic equipment. The most pressing need for an invention of this kind, however, and the context in which it is described in detail below, is a pumping station for the sale of gasoline or other flammable materials; because such materials raise a risk of fire or explosion when electronic calculating equipment is used in their immediate vicinity. Thus, in describing the prior art, attention may be focused specifically on the familiar type of cost computing and displaying device which is incorporated in dispensing pumps installed at gasoline stations everywhere.

At the present time these gasoline cost computers are usually mechanical devices incorporating decade counter wheels driven by a gasoline flowmeter. They do not entail any fire hazard, but they have disadvantages usually associated with moving mechanical parts: i.e. frictional wear leading eventually to malfunction and consequent unreliability in the computation. Since the applicable government regulations require gasoline sales cost computations to be quite accurate, and since overhaul or replacement is expensive, it would be desirable to replace these mechanical counter wheel units with computing equipment employing no moving parts. Moreover, the information stored in these mechanical computers is not easily transmitted or otherwise manipulated as is presently desirable in point-of-sale equipment.

Electronic computation equipment meets these requirements, and certainly entails no difficulty so far as speed and accuracy are concerned. But electrical equipment should be avoided in an environment where gasoline or other dangerous materials are dispensed.

Pure fluidic devices also eliminate moving mechanical parts, and have been employed for computing applications in the past. But fluidic equipment operates at much slower speeds than electronic equipment, and presents a serious problem in meeting the operating requirements for gasoline cost computers. Specifically, in a particular gasoline sales application for which the preferred embodiment of this invention is designed, the amount of gasoline dispensed must be measured to an accuracy of 0.01 gallon, pumping rates as high as 20 gallons per minute may be encountered, and the unit cost of gasoline must be adjustable from 0.1 cent to 99.9 cents per gallon. These operating requirements can combine to exceed the maximum operating speed

of fluidic computing equipment when employed in any of the conventional digital counting circuit configurations.

This is readily apparent from a simple worst case analysis. In order to meet the gasoline volume accuracy requirements, the flowmeter must put out a minimum of one pulse per hundredth of a gallon of gasoline, and the computer must perform a counting operation in response to each such pulse. Thus, at the maximum pumping rate of 20 gallons per minute, the computer would have to perform as many as 2,000 counting operations per minute. This allows a cycle time per counting operation of slightly over 33 milliseconds, which would be acceptable only if relatively few pulses had to be counted per hundredth gallon. For example, if the computation were performed on a decimal basis, and the price per gallon were the minimum of 0.1 cent, then the price per hundredth of a gallon would be 0.001 cent. Therefore only a single fluidic pulse representing an incremental cost of 0.001 cent would need to be counted, plus any necessary carries, in each 33 millisecond interval; and this would be within the capabilities of fluidic devices. But when the price is the maximum of 99.9 cents per gallon, it takes at least 27 pulses to represent the cost (0.999 cents) of one hundredth of a gallon, and therefore 27 consecutive fluidic pulses have to be entered; nine in the thousandths, nine in the hundredths, and nine in the tenths of cents decades, plus carry pulses from the less significant decades to the more significant decades when required. Since all of this must take place within the space of a single 33 millisecond cycle time, and since present day fluidic circuits do not operate reliably at rates above 200 Hz, alternate computing techniques are required.

THE INVENTION

This invention provides a pure fluidic computer with no moving parts to wear out, and no electrical equipment to create a risk of fire or explosion in dangerous environments, which overcomes the speed limitations described by avoiding the pulse counting approach entirely, and employing instead an adding approach. It has one or more individual digit position computing circuits, each corresponding to a separate digit position of a unit price. Each time a gasoline flowmeter or other material detector senses a unit quantity of the material in question, it delivers an "add" signal to each of the digit position circuits, causing it to add to its previous total an additional quantity equal to the number which falls in that digit position of the unit price. All the digit position circuits perform their additions simultaneously, and the addition for each digit position preferably is carried out on a binary-coded, bit-parallel basis, so that it consumes the minimum number of pulse transfer times per arithmetic operation.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a simplified overall block diagram of a fluidic gasoline cost computer in accordance with this invention.

FIG. 2 is a more detailed block diagram of a portion of that computer.

FIG. 3 is a detailed fluidic circuit diagram of one of the price digit encoders of that computer.

FIG. 4 is a detailed fluidic circuit diagram of one of the adders of that computer.

FIG. 5 is a detailed fluidic circuit diagram of one of the feedback circuits, including transfer gates, a buffer memory and an accumulator, of that computer.

FIG. 6 is a schematic illustration of the flowmeter and fluidic "add" signal generator of that computer.

The same reference numerals designate the same elements throughout the several views of the drawing.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

This invention is applicable to any fluidic computer which must operate at higher than normal speeds. But since the natural choice for most high speed applications would be electronic equipment, it is particularly applicable to environments where the presence of any electrical devices would be hazardous, for example in the presence of flammable or explosive materials. Gasoline is one such material, but the invention is also applicable to other hazardous environments, for example in an operating room where anesthetic fumes are present, or in a factory where hazardous materials are handled.

The invention is described for the purpose of illustration, however, in connection with a particular application relating to the dispensation of gasoline; and the computation performed is one of cost, although it could relate to any other parameter which is a function of the quantity of material or any other variable. For example, if the computer receives information concerning the density of a material, it could calculate the total mass of a measured volume of that material.

In the specific application illustrated, the computer is used in conjunction with a conventional pump of the kind that is used in gasoline stations everywhere, and as in the past, the computer includes a device 10 mounted on the pump and used for selecting the unit price and displaying it to the customer. In the illustrated example the price currently selected and displayed is 39.9 cents per gallon; but in order to meet all operating requirements, the selector device 10 has to be adjustable from 1 cent to 99 cents per gallon. In addition, as in the past there is a counter device 12 mounted on the pump, which accumulates and displays the total sale price, up to 99.9. In accordance with the present invention, both the selector 10 and the counter 12 differ from their prior art counterparts in that they are fluidic devices, to avoid both the wear associated with mechanical devices, and the hazard that would be associated with electronic equipment in a gasoline environment.

The price selector 10 comprises three fluidic valves 11 designed to select the tens of cents, cents, and tenths of cents digits respectively for a price per gallon figure falling in the range from 0.1 cent to 99.9 cents. Individual display devices 14, 16 and 18 are responsive to respective valves 11 to display the tens, cents, and tenths digits.

Fluidic signals derived from the price selector valves 11 are applied (arrow 20) to pure fluidic encoder circuits 22 which convert the three digits of the selected price per gallon into binary-coded decimal form, and apply them (arrows 23) to three pure fluidic decade circuits 24.1, 24.01 and 24.001. A flowmeter 26 measures the amount of gasoline dispensed, and generates a fluidic "add" signal (arrows 28) for each unit volume of gasoline dispensed. Since the calculation must be accurate to a hundredth of a gallon, the flowmeter 26 is

designed to make 100 revolutions per gallon, and to generate one "add" pulse per revolution. Thus an arithmetic operation can take place to increment the accumulated cost figure for each hundredth of a gallon of gasoline dispensed.

The speed problem arises from the fact that an arithmetic operation must be performed for each hundredth of a gallon dispensed, coupled with the fact that at high pumping rates, these arithmetic operations may have to be performed as often as every 33 milliseconds. The required one hundredth of a gallon resolution dictates that for computation purposes the unit price of gasoline must be expressed in cost per hundredth gallon. At the maximum price level the cost per hundredth gallon is 0.999 cents, which has significant digits only in the tenths, hundredths and thousandths digit positions. It follows that the speed problem with which we are concerned here affects only those digit positions. Thus the technique of price calculation by repetitive adding of unit prices is carried out only in the thousandths through tenths of cents digit positions. So far as all higher order digit positions are concerned, it is permissible to use the prior art technique of a simple chain of decade counters in cascade relationship.

Thus the adding technique is carried out by decade 24.001 which receives encoded thousandths of cents decimal digit increments from encoders 22 in binary-coded bit-parallel form, decade 24.01 which receives hundredths of cents decimal digit increments in binary-coded bit-parallel form from encoders 22, and decade 24.1 which receives tenths of cents decimal digit increments in binary-coded bit-parallel form from encoders 22. There is a 0.01 cent carry from decade 24.001 to decade 24.01, a 0.1 cent carry from decade 24.01 to decade 24.1, and a one cent carry output from decade 24.1 (see arrows 30). The prior art technique of straight pulse counting is then used in the accumulating and cost displaying device 12, comprising four fluidic digital decade counter stages 36 through 42, which participate in the cost computation from the cents order through the tens of dollars order respectively. The one cent carry output represented by arrow 30.0 drives a pennies decade 36 of counter 12, which develops a carry output to a dimes decade stage 38. In like manner, stage 38 develops a carry output to a dollar decade stage 40, and that in turn develops a carry output to a tens of dollars decade counter stage 42. The technology required for making a chain of straight fluidic digital decade counters such as these is well known at the present time; see for example Robert O'Keefe, "Fluidic Decimal Counter For Digital Control Applications", paper 68-937 presented at the 1968 annual conference of the Instrument Society of America.

The technology required for visibly displaying the sale price by fluidic means is disclosed in the present inventor's U.S. Pat. No. 3,400,478 of Sept. 10, 1968, which is owned in common with the present application. By such means the contents of the four counter stages 36 to 42 are displayed on the face of the device 12, to read out the total sale price of gasoline. There is no point in displaying the contents of decade stages 24, since this country has no currency smaller than a penny. However, to display a cost accurate to the nearest penny, the one cent carry output (arrow 30.0) can be made to increment the penny counter stage 36 at 0.5 cents rather than 1.0 cents.

At the start of each sale, the station attendant manually operates a device 44 to reset all seven of the decade stages to zero, as indicated by arrow 46.

FIG. 2 shows the price selector 10, the encoders 22, and the decade circuits 24 in somewhat greater detail. Each decade 24 includes a binary-coded decimal adder 50, a first transfer gate 52, a BCD buffer memory 54, a second transfer gate 56, and a BCD accumulator 58. Each adder 50 received fluidic BCD addend and augend input quantities R and A respectively, and provides a fluidic BCD sum output S, after performing the computation $R + A = S$. The first transfer gate 52 receives the sum S from the associated adder 50, and transfers it into temporary storage in the associated buffer memory 54. The second transfer gate receives the contents of the associated buffer memory 54, and at the appropriate time adds it to a total accumulated in the associated accumulator 58. Finally, the total in the accumulator 58 is fed back as a new augend input A to the associated adder 50 for the next arithmetic operation cycle.

The R addend input to each adder 50 (arrows 23) represents a single digit of the gasoline price per hundredth gallon, and is derived from the associated one of three individual digit-position BCD price encoder circuits 22.1, 22.01 or 22.001, which together comprise the encoder 22 of FIG. 1. These individual price encoders, in turn, receive digital fluidic signals from respective price selector devices 10.1, 10.01 and 10.001 which together comprise the price per gallon selector and display device 10 of FIG. 1. These selectors respond (see arrows 20) to respective manually operable fluidic valves 11.1, 11.01 and 11.001 which determine which decimal digit will appear in each of the three price digit positions. In the specific example illustrated, where the price of gasoline is 39.9 cents per gallon, the three selector valves are set to 3, 9 and 9 respectively. In FIG. 1 the three unit price digit display devices 14, 16 and 18 correspond to 10 cents, 1 cent and 0.1 cent respectively, to display a price which is correct at the gallon level. But because the fluidic outputs of the valves 11, when applied to the price encoders 22.1, 22.01 and 22.001, control the tenths, hundredths and thousandths of cents decades 24.1, 24.01 and 24.001 respectively operationally the price digits they select correspond to tenths, hundredths, and thousandths of cents, i.e., the price per hundredth gallon.

The gasoline flowmeter 26 is designed to provide two distinct fluidic pulse outputs. A first pulse, labeled T1, is represented by arrows 28, and provides the "add" signal which is applied to each adder circuit 50 of the three decades 24. It also provides enabling inputs to the first transfer gates 52. The second pulse, labeled T2 and represented by arrows 60, provides enabling inputs to the second transfer gates 56. Both transfer gates 52 and 56 are logically representable as AND gates at the block diagram level.

Each R signal from one of the price encoders 22 represents the application of one fluidic binary-coded decimal digit of the price per hundredth gallon to the addend input of the adder 50. The A signal is a similar BCD fluidic augend input, and represents the total cost digit quantity accumulated up to that moment by the accumulator 58 for that particular decimal digit position. Each time the "add" signal is received from the flowmeter 26, these two quantities are added together to produce the sum S. As soon as the quantity S is cal-

culated, it is unloaded into the associated buffer memory circuit 54, since the T1 signal enables the first transfer gate 52 at the same time that it triggers the operation of the adder 50. Thus each successive quantity S generated in the adder 50 is immediately unloaded, leaving the adder empty for the next addition operation.

As seen in FIG. 6, the flowmeter 26 includes a disc 62 which rotates (arrow 66) as the gasoline flows through. This disc has a flange 64 which rotates therewith and momentarily blocks a pair of fluidic tubes 68 and 70 in succession to produce the spaced flowmeter fluidic output pulses T1 and T2 respectively. Thus, pulses T1 and T2 are generated in succession during each revolution of the flowmeter wheel 62, i.e. once for each hundredth of a gallon of gasoline dispensed. As previously noted, the first flowmeter signal T1 of each cycle triggers the adder 50 and enables the first transfer gate 52 to load the quantity S into the buffer memory 54. An instant later the second flowmeter pulse T2 of each cycle enables the second transfer gate 52 to load the quantity S into the accumulator 58, where it replaces the previous total accumulated therein, thus generating a new total A. Then, on the next cycle, the new accumulator total A is available at the augend input of the adder 50, while a repetition of the price digit R is presented to the addend input thereof.

At the start of each individual gasoline sale, the contents of each accumulator is zero, as a result of reset device 44 and the fluidic reset output (arrow 46) which is applied to each of the accumulators. Thus, for the first addition operation $A = 0$, and $S = R + A = R + 0 = R$; then for the second addition operation $A = R$, and the next adder sum output $S = R + A = R + R = 2R$; and so on. It follows that the total A in the accumulator 58 increases by successive increments of R for each hundredth of a gallon of gasoline dispensed. The individual decade circuits 24 operate independently of each other, except for the carry outputs represented by the arrows 30, which go from the adder 50 of a less significant decade to the adder 50 of the next more significant decade each time there is a decimal overflow. Thus, the 0.001 cent adder provides a 0.01 cent decimal carry output (arrow 30.01) to the 0.01 cent adder, and the latter provides a 0.1 cent decimal carry output (arrow 30.1) to the 0.1 cent adder. The 0.1 cent adder provides a 1 cent decimal carry output (arrow 30.0) which drives the penny counter stage 36 of the gasoline cost accumulator and display device.

Even at this stage of the description, it will be appreciated that this invention completely avoids the necessity for counting up to nine successive pulses for each hundredth of a gallon in each decimal digit position. Instead, in each decimal digit position a single bit-parallel addition operation is performed rather than a succession of any bit-serial counting operations. In addition, the additions for all three decimal digit positions are performed simultaneously in the three independent decade circuits 24.

To appreciate this more fully, the reader's attention is directed to FIGS. 3 through 5 which show the detailed fluidic circuitry of the valves 11, the price encoders 22, the adders 50, the transfer gates 52 and 56, the buffer memories 54, and the accumulators 58 respectively. These drawings specifically show that all decimal digits handled at each point in each of the decade circuits 24 are binary-coded, so that all arithmetic

operations can be performed in bit-parallel, permitting each phase of each arithmetic operation in each decimal digit position to be carried out within a minimum number of pulse transfer times.

Looking first at FIG. 3, each of the decimal digit selector valves 11 is connected to a group of nine fluidic lines 80. Each line 80 represents one of the decimal numbers 0 and 2 through 9 which can be selected at a given decimal digit position in the unit price, and is connected to its associated one of ten output ports (labeled 0 through 9) of the associated price selector valve 11. The encoding logic is such that no connector 80 is selected to encode a decimal digit 1; therefore no connector 80 is needed for the "one" output port of the valve 11. It is understood that the arrow in FIG. 3 is a diagrammatic representation of an angularly positionable fluid connector for coupling a fluid pressure source (not shown) to the input of a selected one of the fluidic lines 80.

In the specific embodiment illustrated, the encoder 22 employs a plurality of one-input to four-input fluidic NOR gates 82, which are preferably devices of the type shown in FIGS. 12-15 of the present inventor's U.S. Pat. No. 3,469,593 of Sept. 30, 1969, which is owned in common with the present application. The truth table for this type of gate is simply that the output is one only when all inputs are zero, and zero under all other input conditions. In addition, there is an inverting gate 84 of the same type at each of the bit output positions, so that gates 84 give the four binary bits R1, R2, R4 and R8 of a single binary-coded decimal digit R of the price per hundredth gallon; and the gates 82 give the complements thereof $\overline{R1} - \overline{R8}$; all in bit-parallel.

FIG. 4 shows the specific fluidic circuitry of each of the adders 50. This circuit, which employs the same type of NOR gates, accepts A, R and C inputs and calculates C and S outputs. The A (augend) inputs are respectively the four binary bits A1-A8 of a binary-coded decimal digit A of the "total" output of the associated accumulator 58, and their complements $\overline{A1} - \overline{A8}$ respectively, all generated as discussed below in connection with FIG. 5. The R (addend) inputs are R1-R8 and their complements $\overline{R1} - \overline{R8}$ respectively, all derived from the associated encoder 22 as discussed above in combination with FIG. 3. The C outputs are C1-C8 and their complements $\overline{C1} - \overline{C8}$ respectively, representing the adder's four internal binary carry bits from the 1, 2, 4 and 8 value binary bit positions; and C_{out} and its complement $\overline{C_{out}}$, appearing on output lines 30 and representing the external decimal carry output from an adder 50 of a less significant decade 24 to the adder 50 of the next more significant decade 24, or to the penny counter 36 in the case of the tenths decade 24.1. The C inputs are C_{in} and its complement $\overline{C_{in}}$, which appear on input lines 30 and represent the same decimal carry signals just discussed, but are derived from the adder 50 of the next less significant decade 24. (In the case of the least significant decade 24.001, these carry inputs are lacking.) The S outputs are the complements S1-S8 of the four binary bits S1-S8 of a single binary-coded decimal digit S, representing the sum calculated by the adder 50.

A first group of NOR gates 86 in FIG. 4 add the first bits A1, R1, $\overline{A1}$, $\overline{R1}$ of the augend and addend together with the decimal carry signals in C_{in} and $\overline{C_{in}}$ arriving from a less significant decade 24 on lines 30 to compute the partial binary sum $\overline{S1}$. Specifically, if the least

significant bits A1 and R1 are unequal (a 1 and a 0), the outputs of gates 86a and 86b are each zero, then the output of gate 86c goes to a one, which disables gate 86f and, via gate 86d, enables gate 86e. The partial binary sum $\overline{S1}$ is therefore determined by the binary significance of the decimal carry in signal C_{in} when gate 86g is enabled by a binary zero add pulse T1 arriving over line 28. On the other hand, if the least significant augend and addend bits A1 and R1 are equal (both 0s or both 1s), the output of gate 86c is a zero to enable gate 86f and disable gate 86e. The partial sum $\overline{S1}$ is then determined by the binary significance of the complement of the decimal carry in signal C_{in} from the less significant decade.

The group of gates 88 are controlled by the binary addition of the least significant bits A1 and R1 and the complement of the decimal carry in C_{in} to generate the appropriate internal carry C1 and its complement $\overline{C1}$. Specifically, if A1 and R1 are both 1s, the output of gate 86a is a one which is effective to force a carry C1 = 1 at the output of gate 88c via gate 88a. If A1 and R1 are both 0s, gate 88a is enabled from the output of gate 86a, while gate 88b is disabled by the binary one at the output of gate 86d. Gate 88a thus senses a coincidence of zeros to generate a carry complement $\overline{C1} = 1$. Finally, if A1 and R1 are unequal, gate 88a is still enabled and gate 88b is enabled from the output of gate 86d to permit the decimal carry in signal $\overline{C1}_{in}$ to determine the binary significance of the internal carry signals C1 and $\overline{C1}$.

A second group of NOR gates 90 respond to the second least significant bits A2, R2, $\overline{A2}$ and $\overline{R2}$ of the addend and augend, together with the internal carry signals C1 and $\overline{C1}$, to generate the partial sum $\overline{S2}$. These gates 90 also co-operate with a group of gates 92 to generate the appropriate internal carry signals C2 and $\overline{C2}$. It is seen that gate 90a forces an internal carry C2 = 1 via gates 92a and 92c when its inputs A2 and R2 are both 0s, meaning that the second least significant bits A2 and R2 are both 1s. If these second least significant bits are unequal, the outputs of gates 90a and 90b are both zero to produce a one output from gate 90e, which is inverted by gate 90g to enable gate 92b. As a consequence, the binary significance of the internal carry signals C2 and $\overline{C2}$ are determined in accordance with the binary significance of the internal carry signal $\overline{C1}$ supplied to the other input of gate 92b. Finally, if A2 and R2 are both 0s, the output of gate 90a is a zero, as is the output of gate 92b forced by the binary one output from gate 90g. The coincidence of zeros at the outputs of gate 92a forces a binary 1 signal for $\overline{C2}$.

Gate 90c is enabled from the output of gate 90e when the second least significant bits A2 and R2 are equal so as to respond to the internal carry signal C1. On the other hand, gate 90d is enabled from the output of gate 90g when the bits A2 and R2 are not equal so as to respond to the internal carry signal $\overline{C1}$. The outputs of gates 90c and 90d are gated together in a gate 90f so as to provide a binary zero output if the binary sum $R2 + A2 + C1 = 0$ and a binary one if the binary sum $R2 + A2 + C1 = 1$. These binary signals are inverted in gate 90h and applied to gate 90i together with the decimal carry out signal C_{out} appearing at the output of gate 102e in the group of NOR gates 102. The output of gate 90f is supplied to gate 90j together with the complement of the decimal carry out signal $\overline{C_{out}}$ appearing at the output of gate 102d. If, as the result of the binary

addition performed by particular adder decade 24, there is no decimal carry out ($C_{out} = 0$), gate 90i is enabled to permit the output of gate 90h to determine the binary significance of the partial sum S2 at the output of gate 90k when the add pulse T1 goes to a binary zero. On the other hand, if it is determined that the decimal carry out $C_{out} = 1$, then its complement $\bar{C}_{out}$ enables gate 90j to permit the complement of the signal at the output of gate 90h, appearing at the output of gate 90f, to determine the binary significance of the partial sum S2. It can be shown that in converting from straight binary addition to binary coded decimal (BCD) addition, the binary significance of the partial sum S2 achieved by straight binary addition is merely complemented when there is a decimal carry ($C_{out} = 1$).

Still referring to FIG. 4, the group of NOR gates 94 handles the second most significant bits A4, R4, A4 and R4 of the addend and augend together with the internal carry signals C2 and $\bar{C}_2$ pursuant to generating the partial sum S4. Bits A4 and R4 are gated together in gate 94a, while their complements are gated together in gate 94b. The outputs of these two gates are combined in a gate 94e to provide a binary one output if A4 and R4 are unequal. This output is complemented in gate 94g to enable gate 96a of the group 96, whose other input is C2 derived from the output of gate 92c. The output of gate 96a is gated with the output of gate 94a in gate 96b so as to provide the internal carry signal $C_4 = 1$ when A4 does not equal R4 and $C_2 = 1$ or when both A4 and R4 are 1s. The output of gate 94e is combined with the internal carry signal $\bar{C}_2$ in gate 94d, while the complement of this signal, at the output of gate 94g, is combined with the internal carry signal C2 in gate 94c. The outputs of 94c and 94d are combined in gate 94f so as to provide a binary one output if the binary sum of $A_4 + R_4 + C_2 = 0$ and a binary zero if this binary sum equals 1.

This output from gate 94f is supplied as one input to each of gates 94h and 94i. A third gate in this subgroup, gate 94j, combines the output of gate 90f and the internal carry signal $\bar{C}_8$ generated at the output of gate 100f in the NOR gate group 100. The second input to NOR gate 94h is the decimal carry signal C_{out} derived from the output of gate 102e, while the second input to NOR gate 94i is obtained from the output of gate 90h. The outputs of these three gates are combined with the add pulse T1 in gate 94k to generate the partial sum S4.

It will be noted that gate 94h is enabled in the absence of a decimal carry C_{out} , and the straight binary addition of $A_4 + R_4 + C_2$, appearing at the output of gate 94f, controls the partial sum S4 at the output of gate 94k during the occurrence of the add pulse T1.

For the decimal sums 10 through 19, the decimal carry out signal C_{out} disables gate 94h, and the generation of the partial sum S4 is handled by gates 94i and 94j. More specifically, for the decimal sums 10 through 15, gate 94i is solely responsible for effecting the conversion from straight binary addition to BCD addition, insofar as the partial S4 is concerned. As previously noted, this gate responds to the complement of the straight binary addition of $A_2 + R_2 + C_1$ at the output of gate 90h and the complement of the straight binary addition of $A_4 + R_4 + C_2$ at the output of gate 94f. It can be shown that if either of these straight binary sums is a one (sums 10 through 13), then the partial sum S4

in BCD is a zero. Under these circumstances, the output of gate 94i is a zero, rendering the output of gate 94k a one, which is the complement of $S_4 = 0$. For decimal sums 14 and 15, the second least significant bit and the second most significant bit are both binary ones in straight binary encoding, and consequently the output of gate 94i goes to a one, causing the output of gate 94k to go to a zero to generate the partial sum $S_4 = 1$ in BCD encoding. For decimal sums 15 through 19 gate 94j is enabled by the presence of the internal carry $C_8 = 1$. For straight binary 16 and 17, the second least significant bits is a zero, which appears at the output of gate 90f, and gate 94j is fully enabled. Its one output disables gate 94k so as to generate the partial sum $S_4 = 1$ in BCD. Finally, for the sums 18 and 19, all three gates 94h, 94i and 94j are disabled, thereby generating the partial sum $S_4 = 0$ in BCD.

It will be seen that the gates 100b and 100c of group 100 operate to generate an internal carry $C_8 = 1$ at the output of gate 100e if the most significant bits A8 and R8 of the addend and augend are both binary 1s or if the internal carry $C_4 = 1$ and either A8 or R8 is a 1. Gate 100d is effective to generate a zero output for enabling gates 102a, 102b and 102c of the group 102 if either A8 or R8 or C_4 equals a binary 1.

An internal carry signal $C_8 = 1$, meaning a total of at least 16, is used to force a decimal carry $C_{out} = 1$ via gates 102d and 102e. Gate 102a is responsible for generating the decimal carry $C_{out} = 1$ when the two most significant bits of the summation of the addend and augend in straight binary are both ones. Gate 102b is responsible for generating the decimal carry $C_{out} = 1$ if the most significant bit and the second least significant bit of the straight summation of the augend and addend are both ones. Finally, gate 102c is responsible for generating a decimal carry if the summation of the augend and addend equals 9 with a decimal carry in, i.e., $C_{out} = 1$. To distinguish between the situations of summations of 7 and 9 with a decimal carry in, gate 102c looks at the outputs of gates 86d and 90e. If the summation is 7 with a decimal in carry, gate 102c is disabled from the output of gate 90e, thereby holding off the decimal out carry, i.e., $C_{out} = 0$.

Turning to the group of NOR gates 98 devoted to generating the partial sum S8, it is seen that gate 98a is enabled in the absence of a decimal carry out ($C_{out} = 0$) so as to generate, via gate 98c, the partial sum $S_8 = 0$ when neither R8, A8 or C_4 is equal to a 1, and to force a partial sum of $S_8 = 1$ when either A8, R8 or $C_4 = 1$. Gates 98a and 98b are both disabled when the decimal carry out $C_{out} = 1$ and the internal carry signal $C_8 = 0$ to force the partial sum S8 to a zero to handle the BCD sums 10 through 15. Finally, gate 98b is enabled when the internal carry signal $C_8 = 1$ to force the partial sum S8 to a zero when the straight binary sum of $A_2 + R_2 + C_1$ at the output of gate 90h equals a 0 (to handle the sums 16 and 17) and to force a partial sum $S_8 = 1$, when the straight binary summation of $A_2 + R_2 + C_1 = 1$ (sums 18 and 19).

The circuitry of FIG. 5 in effect represents a digital feedback loop from the S output of the adder 50 through the associated first transfer gate 52, buffer memory 54, second transfer gate 56, accumulator 58 and back to the A (or augend) input of the same adder 50. This feedback circuit uses the same type of NOR gate as was described previously. Each first transfer gate 52 consists of a group of four two-input NOR gates

104 which accept the $\overline{S1}$, $\overline{S2}$, $\overline{S4}$ and $\overline{S8}$ outputs respectively from the associated adder circuit 50, and are enabled by the T1 flowmeter pulse on line 28 at the same time that the circuit 50 carries out its addition operation. Thus the adder S output is passed through the gate 52 to the buffer memory 54 as soon as it is available. The buffer memory comprises four flip-flop stages 54.1 through 54.8, one for each of the binary bits S1 - S8. Each flip-flop comprises a pair of NOR gates 106 connected in cross coupled relationship to obtain bistable operation. The S quantity is retained in the buffer memory 54 until the T2 flowmeter pulse, appearing on line 160 and twice amplified and inverted by gates 108, enables the second transfer gate 56, which comprises a group of eight NOR devices 110. The second transfer gate 56 passes the S quantity into the accumulator 58 where it replaces any previous total that may have been accumulated therein. The accumulator comprises four flip-flop stages 58.1 through 58.8 corresponding to the four binary bits S1 through S8, and each flip-flop includes a pair of NOR gates 112 connected in a cross coupled configuration for bistable operation. Thus, the previous total in the accumulator 58 is replaced by the quantity S, a single decimal digit of the price per hundredth gallon, for each flowmeter revolution. Then the new accumulator total (output signals A1 - A8 and $\overline{A1}$ - $\overline{A8}$ in FIG. 5) are fed back to provide the A inputs to the adder 50 in FIG. 4. Consequently the new accumulator total A provides the base for the next cycle of addition.

After each gasoline sale is completed, and before the next sale is started, a fluidic "reset" signal from device 44 arrives over line 46, is amplified and inverted by gates 114, and is then applied to clear the all four flip-flop stages of the accumulator 58. This restores the zero-total initial conditions required for the beginning of the next sale and cost computation.

It will now be fully appreciated that all operations in each of the decade computing circuits 24 are carried out on a binary-coded basis, i.e. each of the decimal quantities R, S and A is represented by a coded set of four binary bits; and that all arithmetic operations and data transfers performed thereon are done on a bit-parallel basis with respect to such binary bits. It follows that each arithmetic operation and each transfer of a BCD digit can take place in a minimum number of pulse cycle times. This is coupled with the fact that each of the three decimal price digits, representing tenths, hundredths or thousandths of a cent, is operated on simultaneously with the other two decimal price digits, in what one might call decade-parallel fashion. Together, these two features, even at the maximum price level, allow all operations to be completed easily within the 33 millisecond time allowed for a single cycle of arithmetic operations when operating at maximum pumping rates.

Since the foregoing description and drawings are merely illustrative, the scope of protection of the invention has been more broadly stated in the following claims; and these should be liberally interpreted so as to obtain the benefit of all equivalents to which the invention is fairly entitled.

The embodiment of the invention in which an exclusive property or privilege is claimed and defined as follows:

1. A high speed digital fluidic computer for use in a material handling device, the computer comprising:

means for generating a first signal comprising repetitive fluidic pulses, the cumulative quantity of which represents a first variable to be entered into a computation;

means for providing a second signal comprising a persistent fluidic representation of a second variable to be entered into said computation by repetitive addition, said second signal providing means including material quantity detecting means and operating to generate said second signal once for each predetermined unit quantity of material detected by said detecting means;

and fluidic calculating means arranged to retain a total and responsive to said first and second signals to increment said total by the amount of said second variable for each of said first signal pulses.

2. A high speed digital fluidic computer for use in a material handling device, the computer comprising:

means adjustable for selecting a number;

a digital fluidic calculating circuit having a plurality of digital fluidic signal inputs;

number-representing means responsive to said number selecting means to present a digital fluidic signal representing said number to a first one of said calculating circuit inputs;

and means for repetitively generating a fluidic "add" signal and applying it to a second one of said calculating circuit inputs, said "add" signal generating means including material quantity detecting means and operating to generate said "add" signal once for each predetermined unit quantity of material detected by said detecting means;

said calculating circuit being arranged to accumulate and retain a total, and being responsive to each "add" signal to add to its current total the number represented by the signal presented to said first input.

3. A computer as in claim 2 wherein:

said calculating circuit includes a digital fluidic adder and a fluidic feedback circuit;

said adder has a digital fluidic sum output, and a digital fluidic addend input constituting said first input of said calculating circuit;

said feedback circuit has an input connected to said adder sum output, and a return path;

and said adder has a digital fluidic augend input connected to said return path and is operative to perform addition in response to each "add" signal.

4. A computer as in claim 3 wherein:

said feedback circuit includes transfer means and a digital fluidic accumulator;

said accumulator has a digital fluidic input;

said transfer means is responsive to each "add" signal to connect said adder sum output to said accumulator input;

said accumulator is arranged to accumulate said calculating circuit total, and is responsive to said adder sum output to increment said total by the amount of said adder sum;

and said accumulator has a digital fluidic total output connected to said return path.

5. A computer as in claim 4 wherein said transfer means comprises a buffer memory arranged to store said adder sum output temporarily during transfer to said accumulator.

6. A fluidic computer as in claim 5 wherein said transfer means further comprises a first transfer gate

responsive to each "add" signal to transfer said adder sum output to said buffer memory, and a second transfer gate operable thereafter to transfer the contents of said buffer memory to said accumulator input.

7. A computer as in claim 1 wherein said number selector means is arranged to select a non-binary number and said number representing means includes a digital fluidic encoder arranged to present to said first calculating circuit input a digital fluidic signal comprising a binary-coded representation of said non-binary number.

8. A computer as in claim 1 wherein said material handling device is a fluid dispenser, said material quantity detecting means is a fluid flowmeter, and said generator is arranged to generate said "add" signal for each predetermined volume of fluid dispensed.

9. A computer as in claim 1 for calculating the cost of a variable quantity of said material wherein said number selected is the price for said unit quantity of material.

10. A computer as in claim 9 wherein said number selecting means further comprises means for displaying the selected number and indicating that it is the price per unit quantity of said material.

11. A cost computer as in claim 10 further comprising means responsive to said calculating circuit for displaying the total cost of the cumulative quantity of material detected.

12. A computer as in claim 1 wherein:

said number selecting means is arranged for selecting a plurality of numbers, each constituting one digit of a quantity having a plurality of digit positions when represented in a selected number system;

there are a plurality of independently operable ones of said calculating circuits, corresponding to respective ones of said digit positions;

means providing said digit position calculating circuits with respective digital fluidic external carry outputs;

and each more significant one of said digit position calculating circuits having a third one of said inputs connected to said external carry output of the next less significant digit position calculating circuit, and being arranged to increment its current total by the quantity one for each external carry signal received therefrom.

13. A computer as in claim 12 wherein:

said digit position circuits include respective digital fluidic adders, respective digital fluidic accumulators, respective transfer means, and respective return paths;

said adders have respective digital fluidic sum outputs, and respective digital fluidic addend inputs constituting said first input of their respective digit position calculating circuits;

said accumulators have respective digital fluidic inputs;

said transfer means are responsive to each "add" signal for intermittently connecting said adder sum outputs to their associated accumulator inputs;

said accumulators are arranged to accumulate said digit position calculating circuit totals, and are responsive to their associated adder sum outputs to increment their respective totals by the amount of said adder sum;

said accumulators have respective digital fluidic total outputs;

said return paths are connected to their associated accumulator total outputs;

and said adders have respective digital fluidic augend inputs connected to their associated return paths to receive said totals, are operative to perform addition in response to each "add" signal, and are responsive to said external carry outputs of their next less significant digit position calculating circuits to add the quantity one of said sum input.

14. A computer as in claim 1 wherein:

said digital fluidic calculating circuit operates on a binary-coded basis;

and said number representing means is a digital fluidic encoder responsive to said number selecting means to present a binary-coded digital fluidic signal, representing the selected number, to said first calculating circuit input.

15. A computer as in claim 14 wherein said number selector means includes means for displaying the selected number in nonbinary form.

16. A high speed digital fluidic computer for use in a material handling device, the computer comprising:

means adjustable for selecting each digit of a number having a plurality of digit positions when represented in a nonbinary number system;

a plurality of independently operable binary-coded digital fluidic calculating circuits corresponding to respective ones of said non-binary digit positions, and each having a plurality of binary-coded digital fluidic signal inputs;

means responsive to said number selecting means to present respective binary-coded digital fluidic signals, representing the respective non-binary digits assigned to said digit positions by said number selecting means, to respective first ones of said digit position calculating circuit inputs;

means for repetitively generating a fluidic "add" signal and applying it to respective second ones of said digit position calculating circuit inputs, said "add" signal generating means including material quantity detecting means and operating to generate said "add" signal once for each predetermined unit quantity of material detected by said detecting means;

said digit position calculating circuits being arranged to accumulate and retain respective totals, and being responsive to each "add" signal to add to their respective current totals the respective non-binary digits represented by the signals presented to their respective first inputs;

means providing said digit position calculating circuits with respective digital fluidic external carry outputs;

and each more significant one of said digit position calculating circuits having a third one of said inputs connected to said external carry output of the next less significant digit position calculating circuit, and being arranged to increment its current total by the quantity one for each external carry signal received.

17. In a device for transferring flammable material; a high speed digital fluidic cost computer for calculating the cost of material transferred, comprising:

means adjustable for selecting a number having a plurality of decimal digit positions, and representing

the cost of a predetermined unit quantity of said material;

a plurality of independently operable digital fluidic decade calculating circuits corresponding to respective decimal digits of said cost, and each having a plurality of digital fluidic signal inputs;

digital fluidic encoding means responsive to said cost selector to present respective binary-coded fluidic signals, representing respective decimal digits of said cost, to respective first ones of said decade circuit inputs;

a material quantity detector arranged to detect each unit quantity of said flammable material transferred;

means responsive to said detector to generate a fluidic "add" signal for each unit quantity of said flammable material transferred, and to apply said "add" signal to respective second ones of said decade circuit inputs;

said decade circuits being arranged to accumulate and retain respective totals, and being responsive to each "add" signal to add to their respective current totals the respective decimal digits represented by the fluidic signals presented to the respective first inputs thereof;

and means providing said decade circuits with respective fluidic decimal carry outputs;

each said more significant decade circuit having a third one of said inputs connected to said decimal carry output of the next less significant decade circuit, and being arranged to increment its current total by the quantity one for each decimal carry output received.

18. A cost computer as in claim 17, further comprising means responsive to said cost selector to display a unit cost corresponding to the number selected thereby.

19. A cost computer as in claim 17, further comprising a digital fluidic decimal counter for accumulating and displaying cost, said counter being responsive to fluidic carry pulses, and the most significant one of said decade circuits being arranged to supply its decimal carry outputs to drive said counter.

20. In combination with a device for dispensing flammable fluid, a high speed digital fluidic cost computer for calculating the cost of fluid dispensed, comprising:

means on said dispensing device adjustable for selecting a number having a plurality of decimal digit positions, and representing the cost of a predetermined unit quantity of said fluid;

a plurality of independently operable digital fluidic decade calculating circuits corresponding to respective decimal digits of said cost, and each having a plurality of digital fluidic signal inputs;

digital fluidic encoding means responsive to said cost selector to present respective binary-coded fluidic signals, representing respective decimal digits of said cost, to respective first ones of said decade circuit inputs;

a flowmeter arranged to detect each unit quantity of said flammable fluid dispensed by said device;

means responsive to said flowmeter to generate a fluidic "add" signal for each unit quantity of said flammable fluid dispensed and to apply said "add" signal to respective second ones of said decade circuit inputs;

said decade circuits being arranged to accumulate and retain respective totals, and being responsive to each "add" signal to add to their respective current totals the respective decimal digits represented by the fluidic signals presented to the respective first inputs thereof;

means providing said decade circuits with respective fluidic decimal carry outputs;

each said more significant decade circuit having a third one of said inputs connected to said decimal carry output of the next less significant decade circuit, and being arranged to increment its current total by the quantity one for each decimal carry output received;

means on said dispensing device responsive to said cost selector to display a unit cost corresponding to the number selected thereby;

and a digital fluidic decimal counter on said dispensing device for accumulating and displaying cost, said counter being responsive to fluidic carry pulses;

the most significant one of said decade circuits being arranged to supply its decimal carry outputs to drive said counter.

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